Vertically Integrated Circuits at Fermilab

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***Abstract*– The exploration of the vertically integrated circuits, also commonly known as 3D-IC technology, for applications in radiation detection started at Fermilab in 2006. This paper examines the opportunities that vertical integration offers by looking at various 3D designs that have been completed by Fermilab. The emphasis is on opportunities that are presented by through silicon vias (TSV), wafer and circuit thinning and finally fusion bonding techniques to replace conventional bump bonding. Early work by Fermilab has led to an international consortium for the development of 3D-IC circuits for High Energy Physics. The consortium has submitted over 25 different designs for the Fermilab organized MPW run organized for the first time.**

I. Introduction

THE discussion of vertically integrated circuits entails definitions of the subject and the methods used for its physical realization.

The first definition refers to a chip in a vertically integrated circuit technology, also commonly known as 3D-IC technology, as a structure composed of two or more layers of active electronic components, integrated both vertically and horizontally [1].

The second definition introduces a set of methods [2], which emergence in the industry, enabled the 3D-IC technology. Those are: advanced and ultra high precision wafer thinning, high aspect (depth/diameter) ratio through silicon vias (TSV) fabrication [3] [4] and oxide or metal compression bonding. The required steps for wafer processing, which were not common so far in the microelectronics industry, include patterning of a back side of wafers, back-side metallization in order to provide connectivity between bonded tiers and establishing of bonding pads on the last tiers in the stack. The connectivity, enabling flow of signals, biases and distribution of power supply between different layers, commonly called tiers, is provided by technological means falling in different categories of advancement and complexity. Large diameter TSVs, located at the pad areas, allow stacking of circuits with communication at the level of input/output (I/O) pads only. Small diameter TSVs that vertically interconnect individual blocks located on different strata lead to the most efficient use of the 3D-IC technology, shortening the interconnects, thus minimizing RCs and bringing effectively more transistors into the blocks not causing penalty of the increased net area occupied [5]. The functionality of processing units can be extended. The latter is of extreme importance for number of devices. Especially pixel detectors, targeting high spatial resolution, are in focus. The inter-strata connectivity may extend to individual transistors as TSVs placed on a pitch of a few micrometers are achievable in the most advanced 3D-IC processes.

The introduction of TSVs is tackled in diverse ways by different manufacturers. TSVs may be added as the last step after wafer bonding or may be an integral part of the foundry process. The first approach is referred to as via last and the second one as via first. The stacking of tiers can be achieved by bonding directly whole wafers together (wafer-to-wafer), bonding singulated chips to host wafers (chip-to-wafer) or bonding individual dice (chip-to-chip). The wafer-to-wafer bonding is the most common way resulting from the easiness of alignment thus yielding lowest costs. However, high fabrication yield of chips on wafers is assumed as selection of known good dice is unachievable in this method.

The wafers are typically fused in one of two ways, i.e. by face-to-face or face-to-back bonding. The face-to-face assembly uses bonding posts on one metal layer that is last in the process and wafers are bonded in such way that front sides of both wafers are brought in contact. The face-to-back bonding requires extraction of bonding posts to the back side of one of the wafers and bonding is achieved by adding next strata in such way that front sides are facing the same direction. The requirements on the quality of the surfaces, to be appropriate for bonding of tiers are generally satisfied with typical foundry criteria for nowadays planarized processes, including chemical-mechanical polishing and metal filled vias. The thinning of wafers leads to the reduction of their thickness from initial several hundreds micrometers to even less than 10 μm. The post-thinning planes must be planar to the same degree as top sides of bonded wafers. The criteria on the surface topography are more strict on bonding based on oxide adhesion only. The topography should typically be not worse than a few hundred of nanometers and the wafer bow should typically not exceed a few tens of micrometers to yield 3D bonding steps successful [6] [7].

A. Steps at Fermilab

The exploration of the technologies for 3D circuits began at Fermilab in 2006. Fermilab participated in two Multi-Project-Wafer (MPW) runs (3DM2 and 3DM3) organized by MIT-LL under the DARPA Advanced Microelectronics

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Technology Development Program. Two versions of a prototype pixel readout chip targeting the specification of the vertex detector at the ILC were submitted. The 3D-IC 3DM2 and 3DM3 MIT-LL runs included stacking of three 6" wafers, fabricated in a 0.18 μm fully depleted Silicon-on-Insulator (FDSOI) process. The 3D method used in the MIT-LL process is via last [8][9][10].

Following the experience with 3D stacking of circuits on SOI wafers, Fermilab gained an access to the via first 3D process based on a commercial 0.13 μm bulk CMOS run at Chartered Semiconductor. The 3D integration is performed by Tezzaron Semiconductor using wafer with TSVs added after completion of the front-end-of-line (FEOL) part of the process [11][12].

The agreement with Tezzaron led Fermilab to the organization of a own MPW run and formation of an international consortium oriented on exploration of 3D-IC technologies for applications in High Energy Physics (HEP) and related fields [13]. The reticule was divided into 12 units of 5.5×6.3 mm^2. Fermilab submitted 3 fully functional prototypes on the run that was submitted for fabrication in mid 2009.

B. Sketch of new frontiers for detectors with 3D-IC

The 3D-IC technology allows not only to increase the complexity of the circuitry that can be fitted on a single die by allowing bigger density of transistors per an unit area resulting for example in a decrease of access time to a cache memory in a computer system [14] but the 3D-IC methods can be perceived as opening of new frontiers for detectors' and imagers' architectures [15],[16].

The introduction of TSVs embedded in the fabrication stage of the wafers, wafer thinning, leading to exposing of buried TSVs and wafer bonding with vertical electrical connections offer unprecedented opportunities for highly segmented detectors with optimized signal and power routing. The area not sensitive to the radiation can virtually be eliminated. Typical peripheral pad-rings in chips not reaping the advantages of the 3D-IC technology, occupy a few hundred of micrometers. They are necessary at least on one side of the die [17][18]. The mechanical mounting of the detectors in the imaging frame may be complex as dead area that is grown by the clearance for wire bonding cannot be eliminated. By applying 3D-IC methods, all connections can be routed to the back-side of the stacked device and redistributed over the available surface. Coming back to the front side, a detector connected to a readout chip by means of one of the 3D-IC bonding techniques yields a structure that is indistinguishable from monolithic configurations. The operation can be referred to as fusion bonding and offers a replacement of typical bump bonds. One of the processes that can be cited in this place is an oxide-to-oxide fusion bonding, called Direct Bond Interconnect (DBI). Fermilab has gained experience with DBI working with Ziptronix [19][20].

The 3D-IC technology is an efficient tool in providing separation of low-noise analog circuitry from digital blocks. This task is crucial in detector readout systems. A designer typically struggles how to floor plan a 2-dimensional chip attempting minimization of cross talks, substrate currents and capacitive couplings. The analog and digital functions can be allocated to separate tiers using 3D stacking. Completing the allocation of analog and digital parts is the methodology for routing of all lines carrying swinging signals. The polluting lines can be moved to tiers that are farther from the detector.

The paper discusses these new opportunities using the designs submitted by Fermilab as examples for illustration of the developed claims. Section II reviews the guidelines of the 3D-IC processes used by Fermilab. The details of the designed circuits are presented in Section III with related perspectives and goals that are also outlined.

II. 3D-IC PROCESSES USED BY FERMILAB

The fabrication of the first 3D chip, called Vertically Integrated Pixel (VIP1) designed at Fermilab, was realized wit the 3D-IC MIT-LL process using the via last approach [21]. The VIP1 chip is a demonstrator serving as proof of the 3D-IC principle for HEP. The implemented functionality targeted the vertex detector at the International Linear Collider (ILC) [22]. The stacked wafers were manufactured in an SOI process, featuring 400 nm-thick buried oxide (BOX) layer. The stacking processing consists of a few steps that are performed in sequence for each tier added. A simplified list of steps can be presented as follows: oxide-to-oxide bonding of planarized surfaces, thinning to the BOX level of the added tier, etching cavities for TSVs in the designated points, filling the obtained cavities with tungsten and preparation of the surface for adding a new tier. The presence of BOX is used as a naturally available limit for etching in the wafer thinning process. Ubiquitous oxides lead to a significant simplification of the 3D stacking process by naturally isolating the inserted TSVs. The TSVs are making contacts to the routing metals by means of specially designed landing posts that serve also as etch stops in creation of the cavities for TSVs. The fabrication of a 3D-IC chip using the via last method and circuits manufactured on CMOS SOI type wafers is shown in Fig. 1. It can be noticed that the first two wafers are bonded face-to-face, and the most top wafer is added using back-to-face bonding. Each tier has 3 routing metal layers and two top tiers have additional back metals layers deposited on BOX after thinning. These back metals are used in establishing connectivity between tiers and are also available for additional signal routing. The total thickness of the structure after completion of the 3D assembly is about 700 μm, while the thickness of the 3 active tiers is only about 22 μm.

The actual area required for each TSV is about 5×5 μm^2. This number acounts for clearance from neighboring circuitry. A TSV can be a buried via, providing connectivity between internal tiers only or can be a fully stacked pillow, allowing direct connectivity from the top tier to the bottom one.

The tests of the VIP1 chip showed correct functional operation of the structure. On the other hand, the fabrication yield was very poor and it was concluded that FDSOI processes are not best suitable for mixed-mode circuitry that includes high precision and low noise parts. The performance of the analog circuitry is strongly compromised by number of

factors, like variation of temperatures in the structure due to poor heat flow being impeded by the existence of oxides, presence of inter-tier cross-talk paths that may be dominant over interferences between components on the same tier, varying carrier mobility due to the straining of transistor on the BOX, variation of transistors' threshold voltages due to flow of ions eased through oxides, etc. [23][24][25][26].

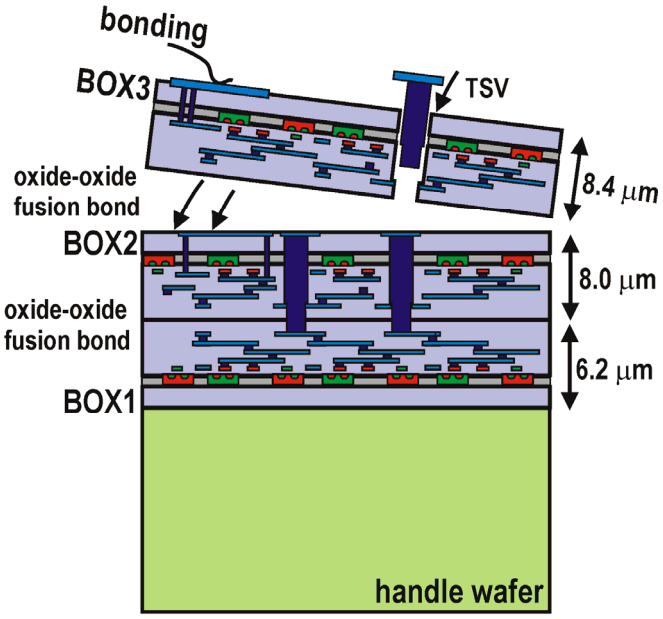

Fig. 1. Conceptual representation of the fabrication of a 3D-IC chip using the via last method and circuits manufactured on CMOS SOI type wafers.

The immediate successor, called VIP2a, of the first prototype was submitted in the FDSOI process to the next 3DM3 run opened by MIT-LL in 2008. The guidelines, aimed at the increase of yield and improvement in the operation of the circuitry were worked out and used in the design of the VIP2a chip. The power and ground routings were strengthened by linking them in a extensive mesh with connections between tiers in each pixel. The rules for trace routing were scaled by a factor equal to 1.2, resulting in wider paths and larger clearances. The process was virtually down-graded to a 0.5 μm feature size in respect to the rules for transistor sizes to decrease off-state leakages and to average structural effects. The delivery of the VIP2a chip is expected in early 2010.

More recent design work at Fermilab has focused on a 3D-IC process using bulk CMOS wafers with Cu-Cu thermo-compression bond interface. The processing of a commercial full CMOS 0.13 μm is supplemented by insertion of TSVs after completion of FEOL. The reactive ion etching (RIE) technique, as a first function meeting the installment of shallow trench isolations (STI), is applied for incising cavities for TSVs that are filleed with tungsten afterwards. The wafers are fabricated by Chartered Semiconductor and the stacking, as well as all processing steps required beforehand, is done by Tezzaron. Although as many as five stacked layers have been demonstrated by Tezzaron, the current Fermilab designs only use two layers and the face-to-face stacking method. The sketch how a 3D-IC chip using the Tezzaron via first method is obtained is shown in Fig. 2. The TSVs can be inserted either in one wafer only, as it is indicated in Fig. 2a, or in both wafer as it is followed in Fig. 2b. The presence of TSVs in both wafers is mentioned later in the article as fulfilling a crucial role for bonding of a detector to the readout chip on one side and protract all signals to the opposite side of the structure. The bonding interface, composed of uncovered metal bond-points, is highlighted in Fig. 2a. The bond-points are small 2 μm hexagons instantiated on the continuous hexagonal grid at a pitch equal to 4 μm. The bond-points are on the last metal layer. The sketch in Fig. 2b shows that one wafer, that will be called 'top tier' remains thick and another one, which will be called 'bottom tier', is thinned down to expose the tips of TSVs after bonding. Tezzaron delivers 3D structures in such arrangements of top and bottom wafers. It is worth mentioning, that the top tier can be in principle thinned down too. The whole structure may require interim attachment to a handle wafer to achieve this thinning goal.

The characteristics of the CMOS process used are: large, about 26×31 mm^2, reticule, single poly layer, 6 Cu metal layers, redistribution metal layer for pads, deep nwell, single mask metal-insulator-metal capacitors, low power 1.5V transistors (standard threshold voltage (SVT), low threshold voltage (LVT, zero threshold voltage (ZVT), IO 3.3V MOSFETs, high resistivity poly resistors. TSVs, intrinsic to the wafer processing, are 1.3 μm in diameter, 6 μm deep and 3.8 μm minimum spacing is required.

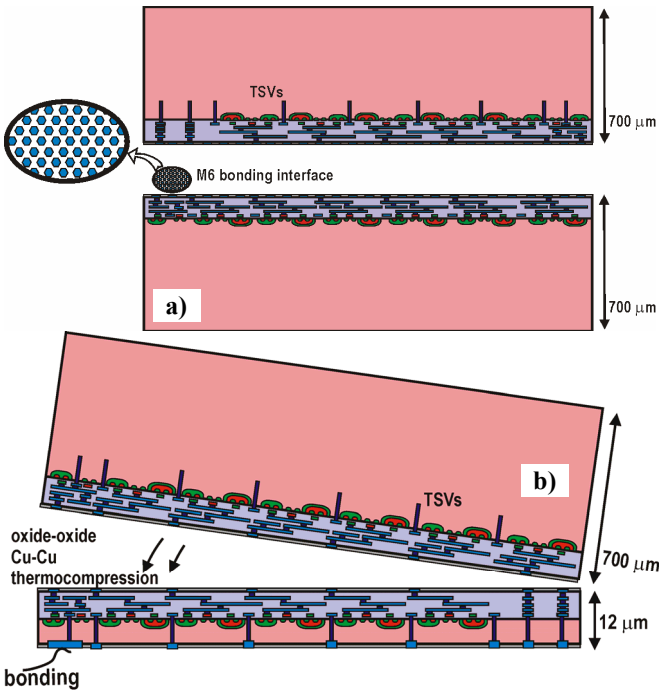

Fig. 2. Conceptual representation of the fabrication of a 3D-IC chip using the via first method and circuits manufactured on CMOS bulk type wafers, bonding interface a), bonding, thinning and I/O pads b).

To limit costs of the run, by using eventually only one set of masks, the reticule was divided symmetrically into two halves. So that the reticule hosts top-tier chips and bottom-tier

chips on its left and right side, respectively. The vertical symmetry about the center of the frame guaranteed matching of circuits for 3D assembly after flipping one wafer over another. The view of the whole frame fabricated is shown in Fig. 3. The Fermilab sub-reticules are H-H*, I-I* and J-J*, where the H-H* sub-reticule is occupied by the VICTR chip (Vertically Integrated CMS Tracker Readout), the I-I* sub-reticule is occupied the VIP2b chip (Vertically Integrated Pixel ver. 2b) and the J-J* sub-reticule is occupied by the VIPIC chip (Vertically Integrated Photon Imaging Chip).

Simple, planar, silicon detectors are under preparation for use with the 3D-chips submitted on the Tezzaron run. The detectors are in fabrication at the Instrumentation Division at Brookhaven National Laboratory (BNL). The design follows the rules for the DBI wafer bonding process. The DBI process begins with very small metal contacts imbedded in a smooth oxide surface. The wafer bond is achieved immediately after the two oxide surfaces are brought together. After the desired strength of the oxide bond is established, the heating is applied to expand the metal contacts to fuse compression bonds. The sub 10 μm bonding pitches are achievable, while the upper limit on the bonding metal density is around 10%. The DBI process is not limited to the wafer-to-wafer type bonding. Indeed, the assembly of the chips from the Tezzaron run to the detector will be done on the chip-to-wafer basis.

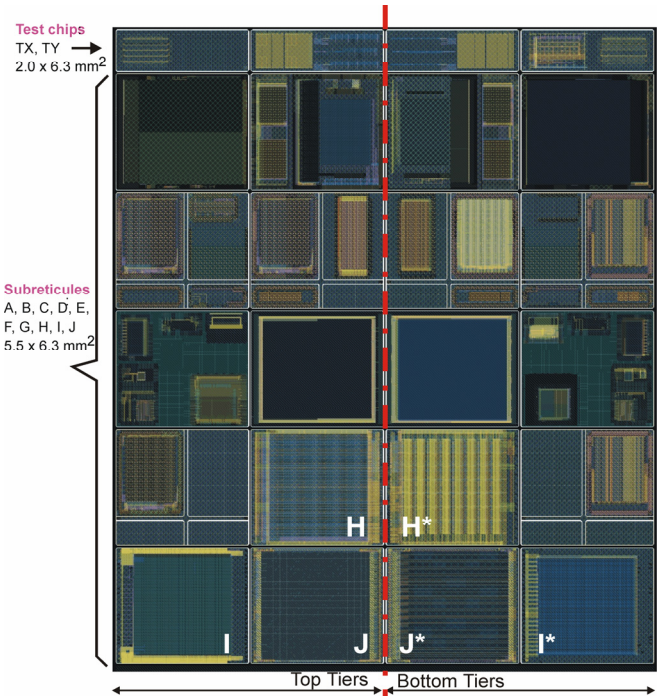

Fig. 3. View of the whole frame with Fermilab chips (H-H*, I-I*, J-J*).

III. 3D-IC DESIGNS BY FERMILAB

A. VIP2b

The VIP2b is a time stamping pixel readout chip for the vertex detector at the ILC. The chip is a re-design of the earlier VIP1/VIP2a device from the 3-tier designs submitted to the MIT-LL process to a two-tier circuit. The new circuit is an array of 192×192 pixels laid out in a square pitch of 24 μm^2. It has 8 bit digital time stamp allowing time bins equal to Δt=3.9 μs in the ILC time operation regime with readout between ILC bunch trains. The chip implements sparsification based on the token passing scheme that remains unchanged from the earlier prototypes. The front-end is a single stage integrating charge signal amplifier with discriminator and with 2 sample/hold (S/H) cells for analog signal output capability with in a correlated double sampling (CDS) mode. The front-end implements a polarity switch allowing accepting collecting of e^- or h^+. Each pixel features a separate test input allowing injection of test charges through a series capacitor. The addresses of hit pixels are output on a serial bus in parallel with the analog information on signal amplitudes that are available on the analog outputs.

The detector for the VIP2b chip has diode implant on the 24 μm pitch. The conceptual view of the mounting of a single VIP2b chip onto a detector is shown in Fig. 4. The detector wafers, fabricated at BNL, contain sensors for all Fermilab 3D-IC chips. The whole sensor wafers undergo necessary processing finished up with metal bonding posts. The image processing is performed on the wafers with chips. The chips with prepared bonding posts are singulated out from the 3D wafer. The individual chips are mounted on the corresponding sensors. The alignment targets integrated on both bonded components can be seen in infra-red light through the whole structure and allow precise alignment. All pads for power supplies, biases and analog and digital I/Os are routed to the pad-ring around the matrix of pixels on the VIP2b chip. The DBI bonding includes transferring of the VIP2b pads onto the sensor. The new pads are recreated on the sensor where the access is not obscured by the VIP2b chip and are reachable with a wedge or ball bonding head. There is a fan-out connection routed on the sensor. The traces are shielded from the sensor by a metal plane between the bonding positions and the pads on the sensor.

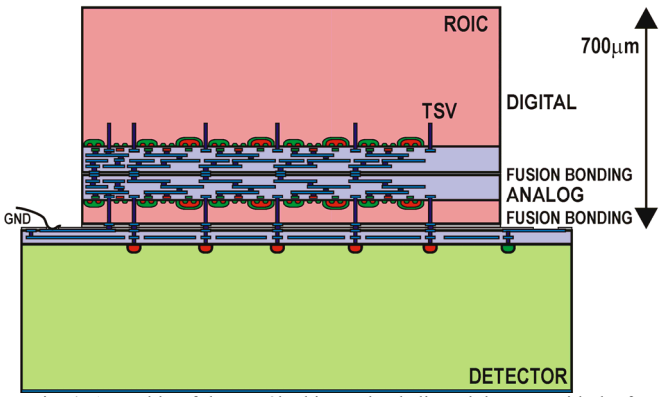

Fig. 4. Assembly of the VIP2b chip on the dedicated detector with the fan-out connection and pads for wire bonding on the detector.

The VIP2b chip and its assembly with the detector qualifies as the most moderate challenge in transition from conventional detector architectures to those that might be allowed exploiting the 3D-IC technologies that are addressed with the devices described in this paper.

B. VICTR

The next 3D chip, VICTR, embodies an initial step toward developing an intelligent tracker capable participating in production of Level 1 trigger at the upgrade of the CMS experiment at SLHC. It is expected that the tracker is able to identify hits associated with transversal momentum p_t>2 GeV for data transfer off the tracker and to participate in building tracks and identification those with p_t>15-25 GeV. The need for momentum cut automatically asks for hisgh spatial resolution the rϕ plane however, the tracker should provide good of about 1 mm resolution in the 'z' coordinate [27].

The p_t cut of the desired threshold can be achieved by processing hit coincidences from two layers of strips sensors. The sensors must be separated by a distance allowing enough track curvature that can be detected by observing offsets of hit positions from two layers providing the pitch of strips is tight enough.

The prototype system for the intelligent tracker is sketched in Fig. 5. The sensors for the VICTR chip are fabricated on the BNL sensor run too. There are two sensors used in the prototype as different strip arrangements are required. The top sensor, called ϕ strips, has 64 strips laid out on the pitch of 80 μm and its active part is 5 mm long. The bottom sensor, called 'z' strips, is a matrix of 64×5 short strips of 80 μm×1 mm. The VICTR chip is designed in such way that charge signals are transferred to the VICTR chip from two directions normal to the surface, i.e. form the bottom and top sensor. The required, for the momentum resolution, spacing between the sensors is achieved by insertion of a 1 mm thick interposer between the top sensor and the VICTR chip.

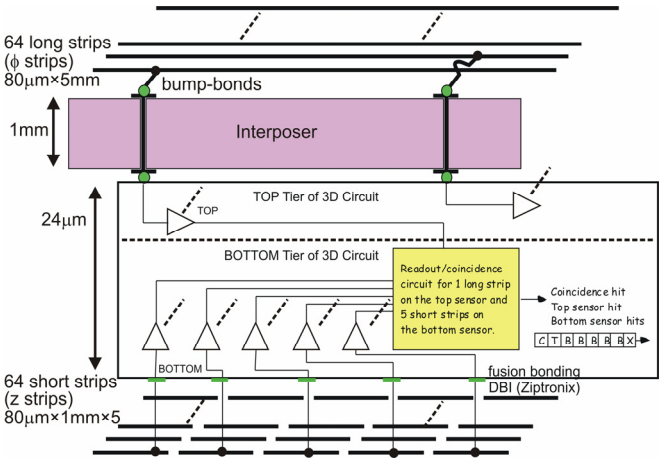

Fig. 5. Block diagram of the prototype unit implementing L1 trigger in the tracker upgrade of the CMS experiment at SLHC using the VICTR chip.

The candidate material for the interposer is silicon and charge signals are transferred through deep TSVs to the VICTR chip. The studies of the interposer are underway. The top tier of the VICTR chip looks at the ϕ strips, while the bottom one looks at the z strips. The coincidences are detected between each strip on the ϕ layer and each group of 5 short strips on the z layer. The processing electronics uses the FEI4 front-end design for the pixel detectors at the ATLAS experiment at LHC [28]. The design was graciously shared with Fermilab by the ATLAS pixel community.

The segmentation of the z layer provides the necessary spatial resolution but it is not used in the processing of coincidences. The VICTR chip processes signals with the typical LHC cadence of 25 ns. It provides serial readout of all top and bottom strips along with coincidence information. In the final circuit, the simple coincidence, circuit that is currently based on the AND logic, will take into account spread of signals onto the neighboring strips for improved spatial resolution.

The construction of the prototype unit for the implementation of the L1 trigger in the tracker upgrade of the CMS experiment at SLHC extends significantly exploitation of the 3D-IC methods comparing with the VIP2b chip. The VICTR chip must be thinned to about 24 μm so that the connections on the top and bottom of the chip could be used. Typically, silicon wafers cannot be handled if such aggressive thinning is applied. Thus, a handle wafer must be used in the fabrication of the final structure of the trigger module. The process starts with deposition of back metal, forming bases for the bump bonding pads on the top tier that is thinned by Tezzaron at the very first step. Then, the whole wafer is bonded to a handle dummy wafer. The bump bonding pads are buried between the wafer with readout chips and the handle wafer. The bond to the handle wafer is strong enough to thin the opposite side to expose TSV that will be contacted to the bottom sensor. The preparation of the bonding posts is performed on an exposed thinned surface and the 3D chips are singulated. The DBI mounting of each VICTR chip of the bottom sensors is done in the next step. The sensors wafer with VICTR chip is diced. The final processing step consists of dicing assemblies composed of the bottom sensors and the VICTR chip that are ready for connection using bump bonding to the top sensor.

C. VIPIC

The last 3D chip, VIPIC, was designed for X-ray photon correlation spectroscopy (XPCS) experiments on light sources. The XPCS is a technique that is used for studying of the dynamics in various processes on a nanometer scale lengths [29]. In these analyses, so called speckle patterns are generated. The photons are registered at different space positions with their arrival times. The results of the analysis are time correlation functions that are calculated for different sampling time intervals at different position. The detector must allow time resolved data acquisition. The targeted readout is continuous, registering of all data from the observed process. The time resolution set for the design was Δt=10 μs.

The VIPIC chip is a prototype matrix of 64×64 pixels. The pixel size is 80×80 μm^2. The fast data readout is achieved by using the data sparsification as the primary readout mode. The imaging mode is implemented as a second readout mode. Each pixel is able to count individual radiation events in both modes; however the imaging mode leads to reading out all pixels without sending out their addresses to the data acquisition system. The VIPIC chip functions dead-timelessly in both modes of operation. The main components of the pixel are: the charge sensitive amplifier followed by the 2-stage

shaping filer and the single threshold level discriminator; there are two DACs for tuning the decay time constant of the amplifier response and the threshold of the discriminator; there is the test charge injection circuitry; the hit holder circuitry; and there are two alternatively used 5-bit long event counters per pixel. The hit holder acquires new hits and feeds the hits to the sparsification circuitry in te time resolved manner. The hit holder integrates flexibility of managing acquisition of hits. It can be permanently set to ignore any hits or to always contain hit. It operates in a pipe-line. The toggling between pipe-line phases occurs with rising edges of the main time stamping clock. With a new rising edge of the clock the hit information is handed off from the cell waiting for hits to the cell connected to the readout. The time bins are defined by the time stamping clock. The period of the clock must be selected aiming at readout of all data within it each cycle. The analog part of the pixel was designed in collaboration with UST-AGH, Krakow, Poland.

The chip is divided in 16 group of 256 pixels read out in parallel through separate serial ports running on the LVDS standard. The data sparsification process is run simultaneously in each group. The block diagram of the VIPIC chip showing subdivision into the readout groups is presented in Fig. 6. The sparsification circuitry is common for each group of 256 pixels. The sparsification circuitry is a modified version of an old idea proposed for the MEPHISTO prototype [30]. It is primarily a multi-input logic OR gate integrated with priority encoder. The encoder selects pixels for readout and generates addresses of hit pixels automatically in the binary code. The layout of the sparsification circuit is distributed into all pixels.

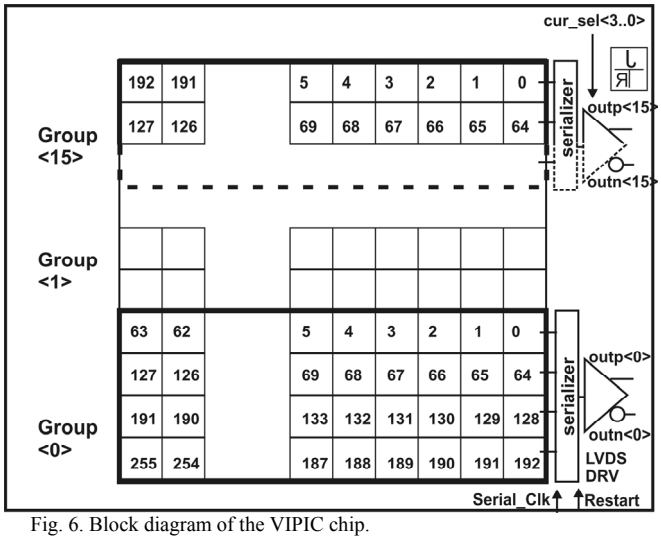

Fig. 6. Block diagram of the VIPIC chip.

The readout of the VIPIC chip is binary. Each hit is represented by a 16 bit-long word, where 3 bits are the start sign, 5 consecutive bits are the content of the in-pixel counter and the remaining 8 bits are the pixel address in the sparsification mode. The pixel addresses are not required in the imaging mode, thus the output word is shorter. The maximum number of hits that can be sent out within a 10 μs time period is 60 from one group of 256 pixels. This estimation assumes a moderate frequency of 100 MHz for the serial clock and occupation of separate pixels by 60 hits, i.e. each pixel is hit only once.

The imaging mode allows the rate of 50×10^3 frame/s. The length of the counter that is 5 bits guarantees dead-timeless and lossless operation in the imaging mode. This confidence stems from the fact that the time required to send out all data from all pixels in the group is shorter than the time to fill the working counter by new hits at the serializer operating at 100 MHz. The maximum speed at counting can occu is limited by the time at which the front-end returns to the baseline, otherwise signa; pile-ups are present.

The VIPIC main features are summarized in Table I

TABLE I. MAIN FEATURES OF THE VIPIC CHIP

Feature	Comments
X-ray detection (8 keV) with Si pixel detector	XPCS application
64×64 pixels, pixel area: 80×80 μm^2	5120×5120 μm^2
separate analog and digital tiers	
analog=280 transistors, digital=1400 transistors	
chip area 6.3×5.5 mm^2 (6.3×5.6 mm^2)	larger dicing for DBI
single threshold for discriminator,	
trim DAC/pixel for offset corrections	3 bits CSA feedback, 7 bits discriminator threshold
permanent set and permanent disable bit per pixel	
test charge injection circuitry	C_{inj}=1.7 fF
single ended or differential configuration of the front-end	
power consumption 25 μW/analog pixel	
CSA: noise ENC < 150 e$^-$, τ_p < 250 ns, gain 115 mV / 8 keV	C_{feed}=8fF
readout modes:	
- sparsified, binary readout (sparsified time slicing mode),	
- imaging binary readout mode (5 bit signal depth)	
dead-timeless and trigger-less operation in both readout modes	
sparsification: priority encoder based sparsification circuitry	
16 parallel serial LVDS output lines (16 groups of 4×64 pixels)	
two 5 bit counters per pixel for recording multiple hits per time slice (useable in the imaging mode)	
frame readout at 100 MHz serial readout clock	
- 160 ns / hit pixel in sparsified time slicing mode (up to 60 hit pixels / 10 μs)	
- 50×10^3 frame/s in imaging mode (5 bit counting)	

The design of the VIPIC chip uses the capacities of the3D-IC technology in the most complete way among all Fermilab's designs.

Achieved the first step is full separation of analog and digital circuits. The dividing line runs along the interface between tiers. The analog part of the pixel is connected to the digital part by 27 connections passing through the bonding interface for signals. Additional terminals, consisting of multiple bond-points, are used to transfer power supplies and grounds. The 27 signal connections include 10 pairs of complementary inputs of DACs, routed from the shadow latches of the configuration shift registers implemented on the digital level, 1 complementary global strobe signal for injection of test charges into the selected pixel, 1 complementary signal for selecting pixel for charge injection and one complementary signal for toggling between the single-ended and differential administration of the reference

level in a shaping filter. The last signal is an output of the discriminator feeding the hit holder circuitry located on the digital layer.

Achieved the second step is such preparation of the design that all pins of the chip are available on both side of the die. Such redundant configuration is a step bringing a detector structure without any connectivity on the sensor side into practical realization. Connections for diosed and I/Os on the same side are irrevocably introducing a significant dead area. Protraction of all signals and power supplies with no exception on the back of the chip and preserving the connectivity in a classical pad-ring on the front side is an opportunity of performing comparative testing. The VIPIC chip is prepared to test the mounting to the detector in the manner discussed for the VIPI2b chip. The front-side view of the chip, exposing bonding posts designed to connect front-ends to the diodes, and the signal fan-out traces routed on the detector, is shown in Fig. 7.

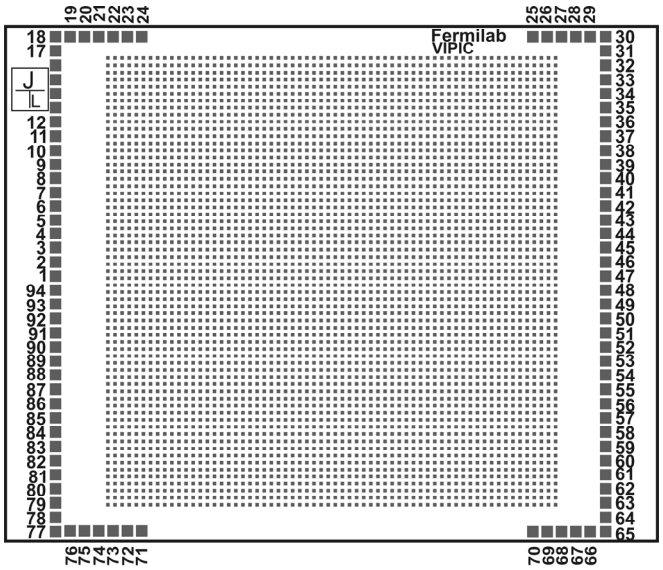

Fig. 7. Front-side view of the chip with bonding posts to the diodes and the signal fan-out routed on the detector.

The exploration of the mounting of the VIPIC in the manner not requiring any other connections on the side facing the detector than contacts to the diodes only is possible thank to the redistribution of all pins on the back side of the chip. The corresponding view of the back-side pins is shown in Fig. 8. A better distribution of the power supplies and grounds, that can be measured in the pursuit of the lowest impedance, is achieved by multiple, intertwined connection points spread over the whole area of the matrix of pixels. The distance between pins is 450 μm on the back side. Low pitch bump bonding, like Sn bump bonding, or gold stud bonding are proposed for mounting of the VIPIC chip on the dedicated host board. The embedding of TSVs in a single layer detector readout integrated circuit or more generally on both sides of the multi-layer structure allows venturing announcement of the feasibility of a full 4-side buttable pixel detector tile. The cross-section of the targeted detector architecture is shown in Fig. 9. The designs carried out at Fermilab gradually lead to the achievement of this objective. The VIPIC chip, being the most advanced prototype, is actually a demonstration of the possibility of achieving this technological dimension.

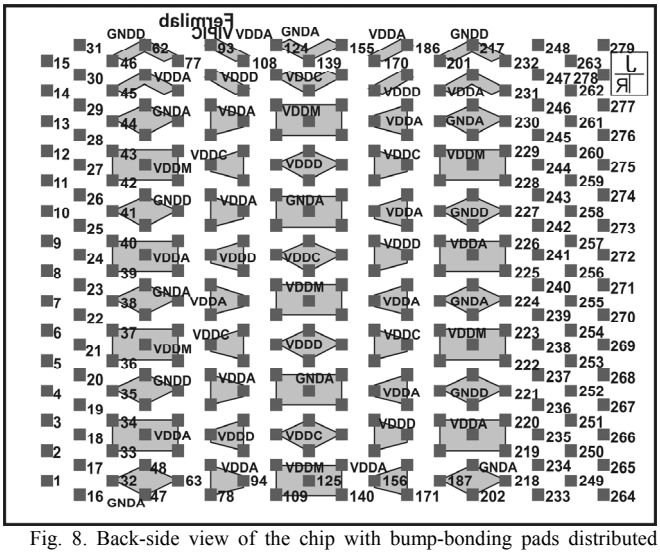

Fig. 8. Back-side view of the chip with bump-bonding pads distributed over the whole surface of the chip; the polygon shadowed shapes mark pins holding the same potential and the same use.

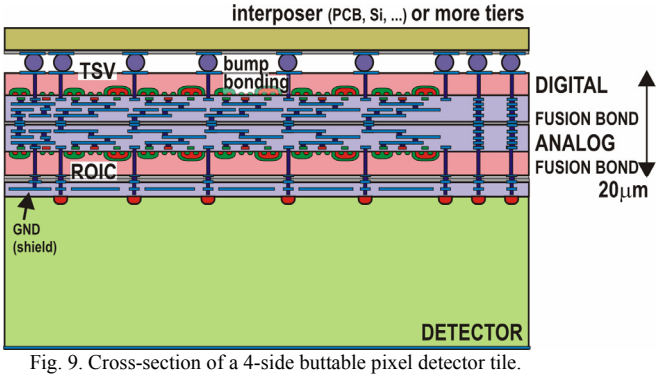

Fig. 9. Cross-section of a 4-side buttable pixel detector tile.

The detector can be fabricated as a homogeneous array of diodes using a whole area available on a wafer. Individual readout chips can be tailed on the detector wafer by fusion bonding. The low pitch connectivity on the back of the chips can be connected to the hosting substrate. The system can be built on an alumina or silicon interposer board, classical printed circuit board, etc.

D. Sensors and DBI bonding

The chips submitted on the Tezzaron/Chartered run require radiation sensors of characteristics that make them able to use fusion bonding technology. The fabrication of the dedicated sensors is underway with BNL. The sensors are p-on-n. The thickness and the resistivity of the wafer are 500 μm and 4 kΩcm, respectively. The pitch of the pixel devices is 24 μm and 80 μm for the VIP2 and VIPIC chip, respectively. The sensors for the VICTR chip are short strips laid out in the pitch of 80 μm. The cross-section of a single fusion bonding node of a 3D readout chip fabricated on the Tezzaron/Chartered 3D-IC run and the detector is shown in

Fig. 10. The bonding process is the Ziptronix's DBI technology. Seen no access to metal filled vias and planarization in the fabrication process of the detector, the thicknesses of the deposited layer must have been chosen carefully in order to provide surface topography sufficiently small for the DBI process . The thickness of oxide is 2000 Å, the thickness of sensor metal is 2000 Å and the thickness of oxide II is 2000 Å on the detector. The seed metal, DBI post and DBI oxide are deposited in the processing by Ziptronix. The size of the DBI post is 6 µm.

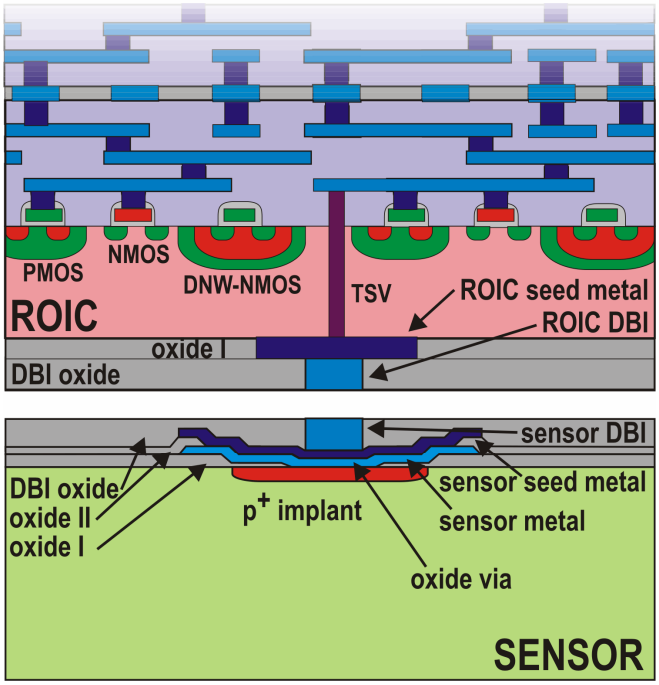

Fig. 10. Cross section of a single fusion bonding node of a 3D readout chip a detector using the Ziptronix's DBI technology.

IV. Conclusions

Fermilab has made first steps in introduction of the 3D-IC technology to the applications of particle tracking and imaging of ionizing radiation in HEP and domains that are closely linked by the same needs for detectors. Fermilab has had an opportunity to explore freshly emerging technologies, i.e. via last 0.18 µm FDSOI CMOS process available at MIT-LL, via first 0.13 µm bulk CMOS process available at Tezzaron/Chartered and the DBI fusion bonding process available at Ziptronix. The early Fermilab's experience was translated into the International Consortium of institutions that have come together to develop 3D integrated circuits for physics applications. The access to diverse technological approaches through the very early stages of the work allowed gaining valuable knowledge on usefulness of technological approaches in achieving reliable designs. The identification of the methods applied in the 3D-IC technology that, even when used alone without vertical stacking of the wafers with electronics, can solve many problems mounted up in the detector engineering, was another result. It can be summarized that 3D-IC offers new approaches to old problems in the detector development.

The five circuits designed by Fermilab target the wide spectrum of applications; four chips are still 'in fab'. The first earnest results are expected very soon. The paper attempted a review of the opportunities that are brought with the 3D-IC methods. The designs of chips, done at Fermilab, are employed as an illustration of the gradual progress and to expose the potential residing in the new tools. The feasibility of a 4-side buttable device, obtained by dragging and distributing of all connections on the side of the structure opposite to that bonded to the detector, has been demonstrated on the actual designs.

One may venture to say that another advantage of the 3D-IC technology is to slow down the pace at which designs of readout chips for radiation detectors need to reach out nano-scale processes, where challenges for example related to matching of active components need to be faced [31]. It is known that higher densities of electronic circuitry per unit area is needed to fit the functionalities requested in nowadays systems, but nano-scale processes exhibit extreme challenges in low-noise, precise analog design.

Further reflection on the 3D-IC technology is the use of heterogeneous wafers, i.e. wafers from different foundries or from different process families. This view may lead to the optimization of each tier in the 3D stack for the specific function, like detector, analog processing tier, digital communication tier, etc. [32]. The mixing of heterogeneous wafers because of technological or economical reasons may be unreachable directly at the foundry. The bonding of heterogeneous wafers can however can be achieved by using methods as DBI, offered by Ziptrornix, or similar approaches available elsewhere. An example of such heterogeneous wafer stacking is attachment of the detectors and it was presented in this paper too.

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