MIPP Plastic Ball Electronics Upgrade

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Abstract

An upgrade electronics design for Plastic Ball detector is described. The Plastic Ball detector was a part of several experiments in the past and its back portion (proposed to be used in MIPP) consists of 340 photomultipliers equipped with a sandwich scintillator. The scintillator sandwich has fast and slow signal component with decay times 10 ns and 1 μ s respectively. The upgraded MIPP experiment will collect up to 12,000 events during each 4 second spill and read them out in $\sim$ 50 seconds between spills. The MIPP data acquisition system will employ deadtime-less concept successfully implemented in Muon Electronics of Dzero experiment at Fermilab. An 8-channel prototype design of the Plastic Ball Front End (PBFEE) implementing these requirements is discussed. Details of the schematic design, simulation and prototype test results are discussed.

The backward hemisphere of the Plastic Ball detector proposed to be used in the Main Injector Particle Production (MIPP) experiment at Fermilab consists of 340 individual phoswich detectors. Each detector consists of a photomultiplier attached to a plastic scintillator 35.6 cm long. A 4 mm slice of $\text{CaF}_2(\text{Eu})$ crystal is mounted on the top of the plastic scintillator. The main component of the decay time of the plastic scintillator is $\sim$ 10 ns. The CaF_2 scintillator decay time is approximately 1 μ s. A 2-inch 10-stage 2202 phototube produced by Amperex is used.

The upgraded MIPP DAQ requires trigger rates up to 3 kHz with minimum interval between triggers of 16 μ s and trigger decision time of 2 μ s [1]. The extracted beam spill may be up to 6 seconds long. This requires for the front-ends to store up to 20000 events per spill. Stored events are to be read out during between spill intervals of 54 seconds.

The specified interval between triggers of 16 μ s allows implementing deadtime-less front-end electronics design similar to the D0 Muon Electronics readout [2]. Such an approach requires continuous digitization of the detector signal and allows using reliable

digital pipelines to compensate trigger decision time. A block-diagram of the Plastic Ball Front-End board is shown in Figure 1. The photomultiplier signal is split by a passive splitter with integration and differentiation times of ~ 20 ns. The differentiated signal is discriminated for time measurement and sent to one of the four TMC304 inputs [3]. The TMC chip allows high precision time measurement of rising and falling edges with ~ 100 ps resolution and has internal digital pipeline. The integrated portion of the signal is digitized at 26.55 MHz by Analog Devices AD9229 12-bit pipelined 4-channel ADC. The ADC output is de-serialized and delayed by an external digital pipeline. When the trigger signal arrives it generates a trigger gate which controls ADC and TMC data transfer to the external event memory.

A SPICE simulation of the passive signal splitter outputs with differentiation and integration time of 20 ns and 5 meters of RG-174 cable is shown in Figure 2. The photomultiplier signal was simulated by a current source with a rise time of 10 ns and fall times of 10 ns and 500 ns. The plots labeled dif and int show differentiated and integrated outputs of the splitter respectively. Additional study with the actual detector signal is necessary to finalize the value of the time constant of the splitter.

A detailed block diagram of four PBFE channels is shown in Figure 3.

The TMC chip has an internal pipeline of 128 cells which provides maximum delay of 4.8 μ s at clock frequency of 26.55 MHz. The pipeline for the ADC data is implemented in a FPGA. At the arrival of a trigger signal the digitized data from the TMC and ADC pipeline outputs is temporarily stored in FIFO memories. The duration of the trigger signal determines how many data words are written to the memory. Zero suppression is done during this process using hit bit for the TMC data and internally generated tag bit for the ADC data. The tag bit is generated individually for each channel by a programmable one-shot (see Figure 4). Using this procedure, only non-zero data words are stored in FIFOs. At the end of a trigger gate the event sequencer writes the

event data from FIFOs to the external RAMs. Writing event data to RAMs takes less than specified minimum interval between triggers, and the front-end is ready for the next trigger before it may arrive. This guarantees deadtime-less operations of the front-end. The PBFE has two read/write 16-bit registers to control delay and width of the trigger gate and ADC pipeline delay. The TMC read and write pointers are programmed via internal TMC registers [3].

At the end of the spill events are read out via serial DAQ interface. The interface uses transformer isolated LVDM receivers and transmitters on four twisted pairs of the standard networking cable CAT-5e. Two of the pairs are bussed and the other two are chained. The bussed pairs are terminated at the far end of the cable. The chains start at the far end and end at the readout controller. Each front-end board has two RJ-45 connectors to facilitate chain connectivity. One of the bussed pairs is used to transmit timing messages and a clock signal. The other pair is used to transmit command messages. The response of the front-end to a command and event data is received by the readout controller from two cable chains. The information is transmitted on all wire pairs in 20-bit frames. Each frame is FM encoded at 26.66 MHz and consists of a start bit, two control bits, 16 data bits and a parity bit [4]. When there is no data transmission undisturbed clock signal is sent instead. The PBFE also has an USB interface for debugging and test purposes. The FTDI UM245R daughter card can be installed in the board socket to facilitate this feature. The UM245R uses 8-bit wide data and mimics functionality of the standard serial interface. A different version of the control firmware is required for the UM245R interface.

An event is formed by the event sequencer upon readout request from the DAQ controller. The sequencer reads event length from each RAM and calculates total event length. The event then is transmitted via serial interface. The event format includes leading word count, event header, variable segments of ADC and TMC data for each channel that has a valid hit, and a global checksum. The event header includes 32-bit time stamp and status information. Each front-end has a time stamp counter which is sampled at the arrival of the trigger. The time stamp counter is reset at the beginning of the spill.

The PBFE board features programmable on-board test pulse generator with individual 12-bit DAC control and mask bit for each channel. Each channel has an individually programmable 8-bit threshold DAC.

Two prototype boards are assembled and tested using auxiliary USB interface. The DAQ software is in preparation for testing the board with Plastic Ball detectors in cosmic rays.

References:

- [1] Holger Meyer, "Specifications for MIPP readout electronics back end communication," MIPP-doc-186, April 2007, Unpublished
- [2] B.Baldin, et al. "D0 Muon Readout Electronics Design," IEEE Trans. on Nuclear Science, Vol.44, No.3, pp 363-369, June 1997
- [3] Y.Arai, "TMC304(TEG3) User's manual," KEK, v1.4, November 1996, Unpublished
- [4] B.Baldin, S.Hansen, "MIPP Data Cable Protocol," MIPP-doc-764, April 2008, Unpublished

- 1 List of captions:
- 2 **Figure 1 Block-diagram of the PBFE board.**
- 3 **Figure 2 SPICE simulation of the passive signal splitter.**
- 4 **Figure 3 Detailed block diagram of four channels.**
- 5 **Figure 4 Details of the trigger logic.**