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Power Conversion from Environmentally Scavenged Energy Sources

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Power Conversion from Environmentally Scavenged Energy Sources

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Abstract

As the power requirements for modern electronics continue to decrease, many devices which were once dependent on wired power are now being implemented as portable devices operating from self-contained power sources. The most prominent source of portable power is the electrochemical battery, which converts chemical energy into electricity. However, long lasting batteries require large amounts of space for chemical storage, and inevitably require replacement when the chemical reaction no longer takes place. There are many transducers and scavenging energy sources (SES) that are able to exploit their environment to generate low levels of electrical power over a long-term time period, including photovoltaic cells, thermoelectric generators, thermionic generators, and kinetic/piezoelectric power generators. This generated power is sustainable as long as specific environmental conditions exist and also does not require the large volume of a long lifetime battery. In addition to the required voltage generation, stable power conversion requires excess energy to be efficiently stored in an ultracapacitor or similar device and monitoring control algorithms to be implemented, while computer modeling and simulation can be used to complement experimental testing. However, building an efficient and stable power source scavenged from a varying input source is challenging.

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Nomenclature

SES	scavenging energy source
DC	direct current
DC-DC	direct current to direct current
COTS	commercial off-the-shelf
ESR	equivalent series resistance
ACT	Advanced Capacitor Technologies
MOSFET	metal-oxide-semiconductor field-effect transistor
CAD	computer-aided design
PCB	printed circuit board
TI	Texas Instruments
ADC	analog-to-digital converter
IC	integrated circuit
SPDT	single pole double throw
SPST	single pole single throw

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1. Introduction

A single scavenging energy source (SES) tends to produce a low and potentially intermittent voltage output, which is not suitable to provide uninterrupted power to load electronics. A method of storing any excess generated power is required to ensure continuous load operation in the event of transient environmental changes causing a loss of generated power. As an example, a solar-powered home relies on many photoelectric cells in combination to produce enough energy to power a home from only the sun. Capacitors, batteries, or another form of energy storage must be used so that power is available at night and on cloudy days when the photoelectric cells are not producing electricity. A step-up DC-DC converter must be used to increase the SES generated output voltage to a voltage that meets the minimum voltage requirements of the load. The output voltage from a DC-DC converter is designed to be stable over a range of current draws, while the voltage from a SES could decrease when supplying an increase of current. There are few DC-DC converters that operate at the low voltage levels generated from a scavenged energy source. Several commercial off-the-shelf (COTS) DC-DC converters meeting the low voltage input and output voltage requirements were compared to observe the most efficient operating setup.

A load device in its full operating power mode would require more continuous power than is available through scavenged energy source generation and deplete any previously stored energy. A creative duty cycle can lower the average power required by the load. Full power is used for a small fraction of the duty cycle, and the load device is turned off or placed in a low-power standby mode for the majority of the duty cycle. Using a duty cycle requires a controller to switch the load devices on and off as appropriate. Many microcontrollers are useful at this task, but they add an additional drain to the power supply.

This paper will deal with efficiently harnessing the output from a scavenged energy source to power load electronics for the longest time possible. A smart power supply would be useful in many applications. The methods described apply to any scavenged energy source thus specifics about scavenging energy from the environment will not be described. Energy storage, boosting a voltage to meet load requirements, and controlling the output power consumption must all be done as efficiently as possible to meet the goal of powering load electronics. Source and load devices will be generically modeled during experimental testing. Computational simulation can be used to increase the confidence in the experimental results as well as predict results that can not be easily tested in a lab.

2. Energy Storage

No matter how a working voltage for continuous device operation is produced, there must be a way to store the excess power for use in the event that transient environmental changes prevent the generator from operating. In the past this energy might have been stored through the use of rechargeable batteries. Batteries have several downsides that

eliminate their use as the primary power storage source. They recharge slowly, have a limited number of recharge cycles, require large volumes of space and weight, have a cold intolerance, and while batteries have a high energy density they also have a very low power density which means they are good for constant low power devices but cannot produce short bursts of high peak power due to their internal equivalent series resistance (ESR).¹

The ultracapacitor, also known as a supercapacitor, solves many of the limitations that arise with batteries. The biggest downside to ultracapacitors is that though they have a larger power density than batteries, they also have a smaller energy density than batteries. This means that for a capacitor and battery of equal volume, the battery can potentially store more energy than the capacitor, but the capacitor can output stored energy as power at a faster rate compared to the battery. Useful capacitor equations are described in Appendix A.

Many ultracapacitors use an electric double layer of activated carbon. Carbon is extremely porous with a large surface area approaching 2000 square-meters per gram. The charge separation of the carbon electrodes is less than 10 angstroms.² Both of these properties allow ultracapacitors to have capacitances ranging anywhere between several mF to kF. A larger capacitance allows for an increase in stored energy when compared to other capacitors. Ultracapacitors have a low ESR of several milliohms which allows for high peak output power. One downside is that ultracapacitors have a low working voltage which tends to be inversely related to the device capacitance. Devices with capacitances greater than 1 F tend to have a working voltage of less than 3 V. If ultracapacitors are used to power higher voltage devices such as at the output of a DC-DC converter, one can use ultracapacitors in the multiple farad range in series so that the voltage across any individual capacitor does not exceed its working voltage, or a single ultracapacitor in the hundreds of mF range with a higher working voltage.

A portable device that does not have access to renewable energy over long periods of time can increase its longevity by operating in a low power state; however energy storage devices have internal losses which can degrade the single charge operational time to less than its ideal value. An internal parallel equivalent resistance causes capacitor self discharging. Maxwell lists that their ultracapacitors have a self discharge rate of about 1.2% of its energy per day.³ This self discharge rate is dependent on temperature. Higher temperatures cause a faster decay than lower temperatures. Information about the computer modeling and self discharge rates of Maxwell ultracapacitors can be found in Appendix B

Next generation ultracapacitor technology is being researched in many places including Advanced Capacitor Technologies, Inc. (ACT) in Japan, and MIT's Laboratory for Electromagnetic and Electronic Systems (LEES). Both are studying nanotechnology in order to improve the effective surface area of the carbon electrodes. Activated carbon has a reduced efficiency because its pores have an irregular size and shape.⁴ MIT is using vertically aligned carbon nanotubes to improve this surface area and storage capacity. ACT refers to their technology as a "Nanogate" capacitor, which uses a form of

carbon with almost no pores that becomes porous when charge is first applied.⁵ While a large portion of ultracapacitor research is geared towards the improvement of battery life in hybrid cars, an individual ACT Nanogate Carbon® Capacitor cell would be useful for low power energy storage devices. The next ACT Premlis™ capacitor looks to raise the working voltage up to 4 V for 2000 F cells.⁶ The next generation of capacitor technology does not yet challenge the lithium battery in terms of energy density.

Ultracapacitors have a very low ESR, between several milliohms and several hundred milliohms, which allows them to be very good at providing peak power. Power generating devices, including batteries, are designed to operate under specific load conditions in order to maximize the power transferred into the load. A load that requires a burst of higher power will draw more current than a lower power requirement for a fixed voltage. However, this peak current could lower the operating efficiency of the power source or the source might not be able to provide this increase in power. The higher current causes a greater voltage drop across all parasitic resistances. It is important to have a low ESR to prevent the load voltage from dropping too low exactly when the load needs additional power and current. The ESR of a power source could be large enough to cause a voltage drop and prevent the load from receiving its necessary peak power. In such a situation, a low ESR ultracapacitor can be charged in parallel to the power source and then provide any additional current required by the load during the peak power phase. The voltage of any capacitor will decrease as its stored energy is used, but in a properly designed system this voltage drop will be smaller and slower than the drop in a system relying solely on the original power source. This will significantly improve the amount of time that peak power is available for the load.

3. DC-DC Converter

The DC-DC converter boosts the low output voltage from a scavenged energy source into a higher voltage that can power load electronics. Figure 1 represents an ideal DC-DC converter with a zero-resistance switch. In a physical DC-DC converter the switch is replaced by a MOSFET. The DC-DC voltage converter creates gain by rapidly switching current through an inductor to ground or to the load. When the switch closes, the current through the inductor increases which stores energy in magnetic fields. The energy stored in an inductor is:

$$Energy = \frac{1}{2} * L * I^2 \quad (1)$$

where L is the inductance and I is the current through the inductor. When the switch opens, stored magnetic energy opposes the now decreasing inductor current. This opposing force appears in the form of an induced voltage which adds to the original voltage source. The output capacitor charges to a constant output voltage when the inductor switches energy to the capacitor and load. An output capacitor also reduces voltage ripple, which could otherwise negatively impact the internal switching of the converter.

Figure 1. DC-DC Converter.

Power efficiency is the ratio of a device's output power to its input power. Power measured in Watts, equals the voltage times the current. Due to device parasitics, the output power of a system will always be less than its input power. Efficient power conversion requires minimizing losses in order to ensure that the load receives as much of the generated power as possible. The tested DC-DC converters have different power efficiencies due to their internal designs, as well as the selected inductive and capacitive components.

The input voltage seen by the converter is the output voltage from the SES. The output voltage from the converter is set by the choice of converter and specific setup. Input current to the converter is limited based on the properties of the SES. The output power from the SES is fixed and increasing the current from the source will cause its produced voltage to decrease. The output current from the converter is based on the load electronics. Given constant input and output voltages, the power efficiency for a specific converter varies based on its input and output current. A high current required by the load might require more power than a converter is able to produce. If the load draws more than a fixed threshold of current from the converter, the output voltage from the converter decreases to keep a constant output power. In turn the converter might draw additional current to its input, which lowers the voltage produced by the SES. The voltage produced by a SES is low and could be close to the converter's minimum operating input voltage. If the SES produced voltage decreases below the minimum converter input voltage threshold, the converter will not produce the proper output voltage for any output current.

4. Testing and Comparison of DC-DC converters

The manufacturer provides circuit schematics for each DC-DC converter in their datasheets. These schematics were developed into printed circuit board (PCB) designs using Eagle CAD software. Next the PCB designs were sent out for remote fabrication. Upon receiving the physical boards, each board was loaded with manufacturer recommended components, constructing completed circuits for testing. Figure 2, Figure 3, and Figure 4 display enlarged versions of the two-layer PCBs used to determine the efficiency of the Holtek, Seiko, and Texas Instruments (TI) low- input voltage DC-DC

converters. The circuit layouts include several jumpers to allow for easier measurements of the current and voltage.

Testing obtained the power efficiency of a given DC-DC converter over a range of output load currents given a fixed input voltage. The source generator and load electronics were simulated using typical lab devices. A variable power supply represents the low voltage output from a scavenged energy source. The output of the power supply connects to the input inductor of the DC-DC converter. A calibrated adjustable resistance representing the load electronics is connected to the output of the DC-DC converter. Higher load resistances draw less current than lower load resistances for a fixed output voltage, which can be calculated from:

$$I_{out} = V_{out}/R_{load}. \quad (2)$$

where I_{out} is the output current, V_{out} is the output voltage, and R_{load} is the load resistance. Care must be taken during testing to maintain a constant output voltage from the DC-DC converter to produce the desired output current. Experimental results show that the output voltage is generally maintained only for lower output currents. When the output current passes above a fixed threshold for a given input voltage, the output voltage will sag due to the conservation of energy. These power efficiency tests do not limit the input current from the power supply to the converter. This allows the required input current for a given output load and a fixed input voltage to be measured. If the input voltage to the DC-DC converter increases, the converter's output current threshold tends to increase to higher current thresholds.

Figure 2. Holtek test board.

Figure 3. Seiko test board.

Figure 4. TI test board.

The DC-DC converters were tested over a range of load resistances while other system constraints were kept constant for a given load range. Each load resistance required measurements of the input and output voltages and currents. Ohm's Law allows the output current to be calculated from the output voltage and load resistance, eliminating one measurement and source for error. Breaking into the circuit to measure current caused small but noticeable differences in the measured voltage and current, occasionally making the difference between being above or below an operational threshold. Incorporating very low resistance current monitoring resistors will improve future testing results. The power efficiency can be calculated after measuring the currents and voltages:

The DC-DC converters tested were the Holtek HT7737 and HT7750, the Seiko S8353D50, and the Texas Instruments TPS61200. These converters all produce a voltage above the 3.3 V minimum required by the load electronics. All of the fixed voltage and current values produced by the variable power supply are generic. They are not related to any specific SES, and are a small subset of low voltage and current outputs from a wide range of potentially generated values. Additional testing may be required to account for the actual source values.

4.1 Holtek

The HT7737 is designed to produce 3.7 V at its output up to a maximum output current of 100 mA.^{7,8} It has a listed minimum start-up input voltage of 0.7 V. Holtek provides input and output data using input voltages as low as 1.2 V. The majority of tests included in this paper were performed with an input voltage below 1.2 V. Figure 5 shows the influence of the input voltage and output current on the output voltage. At lower input voltages the converter is able to maintain a proper output voltage until the load draws more than 5 mA. This would satisfy the load requirements in a low power mode, but will not meet full power and current needs. At higher input voltage levels the converter maintains its expected output voltage of 3.7 V over a range of output currents. The testing and manufacturer data agree that output voltage will drop with higher output current and lower input voltage. Using a 1.5 V input, the manufacturer shows that 100 mA of output current can be generated while the output voltage only drops 0.1 V. A higher input voltage will have an even smaller output voltage drop at 100 mA. This intuitively makes sense as less work is required to boost a higher voltage to 3.7V compared to boosting a lower voltage which eliminates efficiency losses that cause device failure for lower input voltages. If a scavenged energy source provides 760 mV, the converter would not be as likely to meet high current load requirements as if the input could be doubled to 1.52 V. Holtek has recently developed the HT77XXA, which increases the internal switching frequency and is capable of producing up to 200 mA of output current, but other product details are not yet known.

Figure 5. Holtek, V_{out} vs. I_{out} .

4.1.1 Current measurements

Figure 6. Holtek, I_{in} vs. I_{out} .

The required input current given a fixed input voltage, seen in Figure 6, is approximately linear with respect to the output current drawn by the load. Lower input voltages display a local maximum before resuming a linear slope. This maximum occurs when a rapid change in output voltage occurs over a small change in output current. An upward linear slope resumes as the output voltage stabilizes. An ideal power converter would have a perfectly linear slope due to constant efficiency, with respect to fixed input and output voltages. It should also be noted that the slope decreases for higher input voltages. This is because less input current is required to produce a given output current when larger input voltages are used.

Measuring current requires an ammeter to be in series with the component that is being measured. A current meter is designed to have low resistance and a very small voltage drop across its terminals. Because of the low operating voltages, any non-negligible voltage drop across a current meter could move circuit elements away from their expected operating voltage levels. The observed input and output voltage readings were impacted when measuring the current into the DC-DC converter. When the current meter is in the circuit, the output current threshold where the output voltage starts to decrease is lower compared to when the input current is not monitored. The addition or reduction of a few hundred millivolts or several milliamps might not cause a problem in many circuits, but it is a problem when optimizing for device efficiency at ultra-low voltages. The test results will have little value if the circuit behaves differently while the current is monitored when compared to its true operating behavior.

The initial voltage and current measurements were taken using a Fluke multimeter. Several other multimeters were tested to see if they would cause less disruption to the circuit. HP and Keithly 4-port multimeters are designed to measure current as low as several nA, but they have 2 A fuses that break the circuit at lower current levels and have a higher resistance than the Fluke fuses. The circuit displayed the least disruption when the Fluke was operated using its 10 A fuse input compared to other testing methods. Unfortunately this setting forced the meter to use a scale with a resolution of 1mA and an accuracy of $\pm (0.2\% + 2 \text{ mA})$. Using this setup allows the circuit to operate more like its behavior without measurements, however at lower current levels the observations are on the order of the multimeter error.

Improved current monitoring will be necessary for the static efficiency results, as well as measuring currents that change due to a changing output load. As the present design moves forward, current monitoring should be implemented using a current sensing resistor. A current sensing resistor is very low resistance, and when current is applied it will have a small but detectable voltage drop across its terminals. The voltage drop across this resistor should be small so the circuit does not fail in the way that is described above. This voltage drop and current can be calculated after the voltage is put into a high gain, high input impedance op amp and observed using a voltage monitor. If future current monitoring is to be done internally, both the op amp and resistor should be chosen to minimize power loss.

4.1.2 Efficiency impact of components

The specific PCB layout and the inductors, capacitors, and diodes used in each DC-DC converter impact the power conversion efficiency. Initial tests were performed using readily available components. Further refinement of component values should be performed to ensure overall efficiency within an observed trend.

The inductor is a critical component for any boost converter. It is located between the output of the SES and the input of the converter. Figure 7 indicates that the input inductor impacts the efficiency of the DC-DC converter. Lower value inductors are less resistant to a changing current compared to larger value inductors. The power efficiency for smaller value inductors is low because they require a larger input current to store the same amount of energy as a larger value inductor with less input current. The 100 μH and 200 μH inductors have similar efficiencies at low currents, but the 200 μH inductor has a lower efficiency at higher currents. It is expected that increasing the inductance beyond a specific value will cause diminishing returns. This is because higher value inductors have a larger parasitic resistance which causes current saturation. A larger value inductor also has a slower reaction to the rapid current switching, such that internal switching could switch the current before the stored inductor energy reaches its peak. Holtek suggests choosing an inductor value anywhere between 47 μH and 100 μH . These inductor efficiency tradeoffs are unique to each DC-DC converter and need to be further studied to optimize this device.

Figure 7. Holtek, efficiency vs. I_{out} due to inductors.

The output capacitor stores the boosted output voltage in the form of electrical energy. At the time of initial testing, Holtek recommended a minimum of 22 μF at the output, but they now suggest using two parallel 22 μF capacitors. Adding a second capacitor decreases the output resistance and increases the output capacitance. A larger value of capacitor with less equivalent series resistance (ESR) is more resistant to load voltage fluctuations. The output capacitor filters high frequency oscillations at the output of the converter, decreasing internal feedback which would influence the voltage oscillations to be even stronger. The capacitor charges to the voltage produced by the DC-DC converter without impacting that voltage as long as it is within the working voltage of the capacitor and can filter out high frequency oscillations.

Figure 8 shows that different output capacitors do not have a strong impact on the steady-state power efficiency of the DC-DC converter. This is especially true for higher current loads where the converter is not producing the proper output voltage. The majority of power efficiency measurements fall between 75% and 85% for low output current. There is a wide range in the efficiency measurements at the lowest output current levels where the measured output current is on the same order as the accuracy of the meter. The output capacitor behaves as an open circuit at steady state output current and should not impact the power efficiency until transition timing is included in the tests. Testing did not involve comparisons due to the ESR of a capacitor.

Figure 8. Holtek, efficiency vs. I_{out} , $V_{in}=0.76\text{ V}$.

Figure 9 illustrates that the output voltage produced using a given output current depends on the components used. Multiple values of output capacitor tested with the same input inductor and input voltage cause the converter to end production of the proper output

voltage at the same output current. Lowering the inductance extends the output voltage drop off when compared to higher valued inductors with the same output capacitance. Like in the inductor efficiency tests, it requires more current to saturate a smaller value of inductor than a larger value and the internal switching may take place before the inductor has stored enough energy to maintain the output voltage at higher output currents. Significant testing using multiple component values was not performed for the Seiko and Texas Instruments converters.

Figure 9. Holtek, V_{out} vs. I_{out} , various capacitors and inductors.

4.1.3 PCB Design

The initial PCB design of the Holtek board was patterned to be similar to a design by Janson Wu. As my familiarity with the EAGLE layout software grew, the layout of the designed PCBs was adjusted to solve potential layout problems. When moving from a symbolic circuit to a physical PCB there is additional resistance due to the copper wiring between components. Decreasing the resistance of this wiring was done by connecting components using thick copper traces and polygons. Large polygons were used to create ground planes. Device components were moved closer together to decrease the resistance and length of copper traces. It was expected that these improvements could improve the efficiency towards the listed efficiency of 85% but the advanced layout techniques only improve efficiency by a few percent compared to the older boards, though the changes could show additional improvements when the load is not a static output.

The circuit pads had to be small to fit the components but designed so that hand soldering could take place. This required the pads on the PCB to have additional “heel” and “toe” space beyond the exact size of the component pad. At times the manufacturer measurements were not precise, and soldering was difficult even including the padded margins. Development continued by adding jumpers to allow for easier current and voltage measurements without having to disconnect all connections breaking into the circuit. When the load testing changed from steady state to pulsed tests, the board complexity required a 4-layer board that is approximately the same size as the originally designed Holtek board. These design principles are also applied in the Seiko and Texas Instruments two-layer boards.

4.2 Seiko

Seiko’s S-8353 DC-DC converter requires a minimum input voltage of 0.9 V^{9,10}. Meeting this higher input voltage requires an additional process between the source and the DC-DC converter. The new stage is an S-882Z charge pump that takes the low input voltage from the SES and outputs a boosted voltage of 2.2V to the input of the DC-DC converter. The charge pump increases the input voltage, but not enough to power the load electronics without an additional voltage gain. Then the DC-DC converter boosts the voltage from the charge pump to meet the load voltage requirements. The Seiko charge pump can operate from an input voltage as low as 0.3 V, and depending on the specific model can output a voltage between 1.8 V and 2.4 V. The various models of the converter offer a wide range of output voltages, but the model selected to meet the minimum load requirements produces a voltage of 5.0 V. Any voltage above the required load voltage will need to be down converted to prevent damage to the load, but will not be covered in this paper.

Seiko lists the peak efficiency of their DC-DC converter is as 85%. The overall efficiency of the tested system multiplies the efficiency of the charge pump with that of the DC-DC converter. If the efficiency of the charge pump is no better than that of the converter, the system efficiency would be at most 72%. Seiko does not list a specific efficiency for the charge pump, but it must be a very high efficiency device if the overall two-stage system is to have a good efficiency. The Seiko converter tests were originally designed to meet the low input voltage of the Holtek converter, with an input voltage greater than 0.7 V. Some of the tested input voltages meet the input voltage requirements of the Seiko DC-DC converter without using a charge pump, but for experimental simplicity, all tests involved use of the charge pump. In the event that a scavenged energy source will produce more than 0.9 V, the Seiko converter would deserve additional testing to find the efficiency without an intermediate charge pump.

Figure 10 shows that the Seiko device produces the expected output voltage for low output current levels. Just like with the Holtek converter, there is an output current threshold beyond which the output voltage cannot be maintained. The Seiko output voltage has a gradual decay compared to the sharp Holtek voltage drop off. The Seiko current threshold increases when the input voltage increases.

The charge pump does not appear to improve aspects of the circuit operation beyond enabling the system to work at lower voltages. The input voltage from the charge pump to the converter is 2.2 V, and Seiko lists that this input voltage should produce the expected output voltage until the output current is greater than 100 mA. Instead the observed output voltage curves are similar to the curves that Seiko lists as if the converter was operating with output a charge pump. The charge pump increases the system input voltage so that the converter can operate, but the overall output characteristics depend on the input system voltage and not the boosted voltage from the charge pump.

Figure 11 shows that the efficiencies obtained for the two-stage Seiko converter are generally less than the Holtek efficiencies tested using the same input voltage. This is expected due to the two-stage Seiko design. The efficiency curves peak around 2 mA of output current and then gradually decrease. This decrease is similar to what is seen in the Holtek tests at low input voltage.

Figure 10. Seiko, V_{out} vs. I_{out} .

Figure 11. Seiko, efficiency vs. I_{out} .

The relationship between input and output current can be seen in Figure 12. There is a linear relationship between the two currents when the output current is not causing the output voltage to decrease. When the input voltage is increased, the system requires less input current to produce the same output current as would be necessary when using a lower input voltage. The slope at 0.76 V input is approximately 8, and the slope at 1 V input is approximately 6. There might be slight improvements in the Seiko converter results if the input voltage source meets the minimum converter input voltage without the intermediary charge pump. Because the current requirements and efficiency of the Seiko setup are slightly worse than the results of the Holtek setup, additional optimization tests were not performed for the components in the Seiko design.

Figure 12. Seiko, I_{in} vs. I_{out} .

4.3 Texas Instruments

Texas Instruments produces three low input voltage boost converters¹¹. The TPS61201 and TPS61202 have respective output voltages of 3.3 V and 5 V while the TPS61200 is unique among all of the tested converters because it has an adjustable output voltage. All three converters are listed as having a minimum startup voltage of 0.5 V. The adjustable output converter voltage is fixed based on a resistive divider that feeds voltage back into the converter. The resistive divider is designed to take the desired output voltage and return 0.5 V to a secondary converter input. The resistive divider uses power, but keeps losses low by using a combined resistance typically greater than one megaohm. The resistance ratio depends on the available resistors. To produce an output voltage of 3.7 V, resistor values should be 1 M Ω and 155 k Ω . Due to component availability, a 135 k Ω resistance was used instead of 155 k Ω . This resulted in an output voltage of 4.2 V.

The TPS61200 was tested using its power save mode. The power save mode allows the converter to briefly turn off when low output currents are required and the present output voltage is at or above its set value. The manufacturer specified low output current efficiency increases from its regular value in the low tens, to around 50% simply by automatically turning off the converter when possible. The low efficiency means that the device is not well suited to provide output current of less than 10 mA unless the power efficiency mode is active. In this case the listed peak efficiency is achieved with a load from the high tens of milliamps to hundreds of milliamps. The manufacturer recommended inductance value is 1.5 μ H to 4.7 μ H, which makes the converter better suited for higher output current than the two previously tested converters. A 10 μ H

inductor was used because when the test was designed there were no available inductors in the recommended range.

The TI converter has one behavior that is very different from the other tested converters. The output voltage did not remain constant with output current. Figure 13 shows that the output voltage increased nonlinearly with respect to the output current from 4.2 V to 5 V. The output voltage could not be maintained using higher output currents, but the output current threshold increases for higher input voltages. TI provides similar charts for their two fixed output voltage DC-DC converters, but not for the TSP61200. They claim that their fixed output voltage converters maintain a stable output voltage until the output current reaches several hundred milliamps. For the purposes of this paper, testing was not performed on the two TI fixed output voltage converters. The test results from the Holtek and Seiko devices show that their output current was able to remain stable or increase slightly as the output voltage decreased, but the TI results show that there is a slight overlap between output currents that produce the proper output voltage and those that cannot sustain the proper output voltage. More analysis should be performed to better understand this hysteresis curve.

Figure 13. TI, V_{out} vs. I_{out} .

The tested efficiency of the converter using several input voltages and output currents can be seen in Figure 14. The efficiency increases when a higher input voltage is used. However the TI results were the lowest when compared to results of the Holtek and Seiko devices at low input voltage and output current. The tested efficiency results are similar to the chart provided by TI. The TI provided charts configure the TPS61200 to produce

1.8 V and show reasonable efficiency results all the way from 1 mA to 1 A. There are two differences between TI's testing and the testing performed for this paper. The most likely reason for the differences in tested results compared to TI's charts is that TI used an output voltage of less than half what the tested generic load requires. Boosting an input voltage to 1.8 V should be easier than boosting it to 3.7 V, which allows the output current range to be extended when a lower output voltage is used. Second, TI would have used an inductor within the specified range. The 10 μ H inductor used in this paper could have contributed in limiting the output current at low values, but this effect should not dominate until tested at higher output currents.

Figure 14. TI, Power Efficiency.

Figure 15. TI, Input Current.

Figure 15 shows the input current required by the TPS61200 to produce a given output current. The slope of input current to output current is greater than ten for an input voltage of 0.76 V. The slope decreases as the input voltage increases, and is closer to four for an input voltage of 2 V. The hysteresis observed in Figure 13 also shows up in the required input current. Due to the low power efficiency and high values of input current required to produce a low value of output current, the TPS612XX series of converters will not be investigated any further at this time.

5. Experimental Load Simulation

In present testing the actual load electronics are unavailable and can not be used. The output load of the DC-DC converter will be simulated as a black box that internally switches between two different resistive loads. The resistors represent the current profile of any potential load electronics. Additional internal loads could be used to simulate multiple current profiles but at this point the exact load profile remains unknown. The current and time values used during testing are unrelated to any specific load electronics. A low value current represents when the load electronics are in a low power sleep or standby mode. The main consumption of power during the low power mode is due to monitoring controls which are implemented in the next section. A higher value of current represents the load in its fully active mode. The lengths of time used during testing represent the load being active for a small percentage of its operating duty cycle. The first load is normally on and draws a low current of approximately 1 mA. This load is switched off when load two draws current. The second load is normally off but draws a

higher current of at least 30 mA over 150 ms. The period between current pulses is approximately 15 seconds. The current pulse can be observed at the output of the converter due to the switching between loads.

During transient tests, the power supply provides an input voltage of 760 mV with a maximum current of 12 mA. More realistic simulations of the scavenging energy source would not have a hard limit on the supplied current, but could instead use a resistor that will decrease the voltage into the converter as the current increases. The required peak load current is greater than the 5 mA that the Holtek converter can provide without dropping its output voltage. The output voltage needs to be reliable and not drop, especially during the active mode. A large capacitor can be used to store charge and source additional current to the load beyond the 5 mA limit of the DC-DC converter while maintaining the output voltage. A capacitor resists a fast change in output voltage but still experiences a voltage decrease in as its stored energy is used. Constant current drawn from a capacitor during a current pulse will cause a linear decrease in that capacitor's voltage. Because the test resistance is fixed, when the output voltage decreases, the current drawn by the load resistor will be less than what it would be if the output voltage remained fixed. This means that the observed voltage decrease will have an exponential voltage decay that is slower than the linear voltage decay caused by a constant current into the load electronics, but linear to first order.

A 400 mF supercapacitor is placed at the output of the DC-DC converter in parallel with the resistive loads. After a high current pulse, the DC-DC converter supplies the low current to the load while the remaining current is used to recharge the output capacitor. During the output current pulse and while the output capacitor recharges, the converter requires enough input current that it reaches the current limit of the power supply. This causes the power supply to decrease its produced voltage from 760 mV to 360 mV. After a 30 mA current pulse it takes upwards of 45 seconds to recharge the output capacitor to 3.7 V due to the very low voltage and limited current applied at the input to the converter, while the recharge time is on the order of 10 seconds if the input current limit is increased from 12 mA to 20 mA. Increasing the output capacitance would decrease the voltage decay during the current pulse, but existing higher capacitance supercapacitors have working voltage levels that are equal to or less than the converter's output voltage and cannot be used individually, but could be used if several capacitors in series divide this high output voltage to an appropriate working voltage for each capacitor. Using ultracapacitors in series at the output has not been tested, but would significantly increase the output capacitance.

Next, a large ultracapacitor was placed in parallel with the input of the DC-DC converter to see if the output voltage recharge time following a high current pulse would decrease. The charged input capacitor prevents the source voltage from dropping by providing additional input current into the DC-DC converter when the power supply is at its current limit. The extra current at the DC-DC converter's input and a less drastic voltage drop translates into additional current available at the output to recharge the output capacitor. Early tests used a 400 mF capacitor at both the input and output sides of the DC-DC converter. This setup was an improvement over no input capacitor, but the input voltage

still dropped a substantial portion of its voltage while the output voltage recharged. It was determined that a 350 F ultracapacitor would be better than the 400 mF ultracapacitor at sourcing enough current to quickly recharge the output side because it would have a smaller voltage drop for the same required current. After incorporating the 350 F capacitor, the input voltage briefly drops several mV during a pulse cycle, and quickly recovers once the output capacitor is finished recharging. The output capacitor recharges in approximately two seconds. The low input voltage and current combination of the power supply is able to recharge both the input and output capacitors in less than five seconds from the beginning of the high current pulse.

Early load models used a human activated single-poll double-throw switch to change between the low and high current loads. Because the pulse lengths are very short, human reaction time plays a difference in the time and current required for the capacitors to return to their charged initial state. Early tests were performed with the peak current value set as thirty times larger than the standby current. The load current can be adjusted by changing the resistance of the load resistors. Later tests will adjust both the peak current and timing.

Additional switching could be implemented if the SES is connected to several converters. Only one system would operate at a time while the other converters are switched off and isolated from the SES. If monitoring detects that one system does not appear to be properly recharging, the monitor could switch the SES and load over to a second DC-DC converter system. This switching could also be used where one system is used for a pulse, and after the high current pulse the SES and load are switched to the next system while the first system recharges.

5.1 Intelligent Control

As load testing continued, it became clear that observations on the scale of millivolts and milliseconds required more precision and accuracy than available via human control. In order to improve the accuracy of the timed current pulse, a microcontroller with a timer function was used to switch between different load resistance and current profiles. Three components now comprised the entire system, a board for the DC-DC converter, the microcontroller on a manufacturer test board, and a breadboard with multiple loads for switching the output current. The microcontroller controlled switches which enabled or disabled specific output loads. The microcontroller performed its task for two loads by producing a 'high' voltage output for 150 ms and a 'low' voltage output for the remainder of the 15 second duty cycle.

These tests involved load resistors and an International Rectifier IRL2203N MOSFET located on a breadboard, represented by Figure 16. The microcontroller is represented by the left-hand switch and when it outputs a low voltage the switch is open, the MOSFET gate is connected to ground and the MOSFET acts as an open circuit. This causes the low current level to pass through the 120 Ω and 3.6 k Ω resistors. When the microcontroller outputs a high voltage the switch closes, high voltage is applied to the MOSFET gate, and the MOSFET appears as a negligible resistance, essentially creating a

short from its drain to the ground. In this case the peak current flows from the positive terminal, through the 120 Ω resistor, and directly to ground. The two right-hand resistors can be adjusted to change the low and peak current values.

Figure 16. Early load switching schematic

Later tests were performed using a peak current up to 1000 times larger than the standby current, and the length of the high current pulse extended to several seconds. The high current load was chosen to deliver a 1 A current with a 3.7 V output for a period of up to two seconds. Increasing the load current or the length of the high current pulse causes the output capacitor voltage to drop even further than in previous tests. The output voltage was 2.67 V after a half-second current pulse. The output voltage took 1 minutes to recharge and the input voltage took 5.5 minutes to recharge. The output voltage after a two second current pulse was 1.3 V, which took 2 minutes to recharge while the input voltage took 13.5 minutes to recharge. When the output voltage significantly decreases, the desired load current is not achieved over the entire duty cycle, and the experiment results will show a smaller voltage drop than a constant current load would cause under actual operating conditions. Equation (A-8) is useful for calculating the ideal capacitor voltage drop that takes place using a fixed current and length of time.

Figure 17 shows the automated pulsing setup. Moving clockwise beginning in the lower left corner we have the 350 F input capacitor, the load switching on a breadboard, the low input voltage power supply, a multimeter displaying the output voltage, a TI designed test board for the microcontroller, the 400mF output capacitor, and the PCB with the Holtek DC-DC converter.

Figure 17. Complete circuit load testing.

When this proof of concept operated successfully, the converter, microcontroller, and switching loads were integrated into a single four-layer PCB with the layout shown in Figure 18. The top and bottom layers were used for components while the two inner planes were supply layers for ground and the output voltage from the DC-DC converter. Figure 19 contains the original Holtek converter PCB (upper) and the fully integrated 4-layer PCB (lower).

Figure 18. Integrated 4-layer board layout, PCB.

The microcontroller is powered by the DC-DC converter. Care must be taken to ensure that any design complexity added for the purpose of intelligent control does not consume excessive amounts of power and then prevent proper operation of the original load electronics. There are several microcontrollers that consume very low power. The microcontroller used in these experiments is the Texas Instruments MSP430.^{12,13} The MSP430 uses approximately half a milliamp in its active mode and less than five microamps in its low-power mode. The DC-DC converter is able to produce enough current to power the microcontroller in its active mode, but proper programming will allow the microcontroller to spend the majority of time in its low-power mode consuming very little power. Figure 20 represents the circuit for the DC-DC converter, which provides power to the microcontroller, switches, and load.

Figure 19. PCB revisions.
Top, original Holtek DC-DC converter. Bottom, complete 4-layer design.

Figure 20. Integrated design schematic, voltage conversion.

The microcontroller is intended to operate without human interaction, and it is straightforward to have a timer-based pulsing loop. This would be a poor method of control and could cause system failure. If the current levels are adjusted so that the high current pulse is no longer tens of milliamps but now draws anywhere from hundreds of milliamps to several amps, the output voltage could significantly sag and the system might not recharge before the timer initiates its next current pulse. An alternative method would use a time period between pulses that is very long and is guarantees system

recovery between pulses. This method would not be ideal, because when the system recovers quickly another pulse could be initiated but won't be until the set amount of time has passed. This time is wasted because a high current pulse into the load could have properly taken place. This poor control method would also cause output load failure in the event that the scavenging energy source is not producing any power to recharge the system. When a human controls the load switching they can observe the input and output capacitors to make sure that both have recharged to the initial voltage following one high current pulse prior to allowing a second high current pulse. Without a similarly "intelligent control" to prevent high current pulses from taking place until after the system returns to its fully charged state, pulses would occur too frequently and the capacitors would have a lower charge after each pulse cycle until the load could no longer be properly powered.

The microcontroller has a built in analog-to-digital converter (ADC). The ADC monitors the voltage of a given point or points, compares it to an internally fixed reference voltage, and records the external analog voltage in a digital format. The MSP430 is designed to have a resolution of 0.366 mV per digital count using a 1.5 V reference, and a resolution of 0.610 mV per digital count using a 2.5 V reference. External voltage division must be used to monitor the DC-DC converter's output or anything else with a voltage larger than the reference voltage. This voltage division is another power parasitic, but the power loss can be kept low by using large resistance values corresponding to low current use. Next the ADC monitors a point inside the voltage divider and is programmed to account for the true voltage outside of the voltage division. The microcontroller's timer can initiate the ADC monitor on a regular basis and then compare the recorded voltage from the ADC with the expected voltage of a fully recharged capacitor. When the microcontroller detects that the monitored voltage is properly recharged it can initiate a high current pulse. If the voltage has not completely recharged, the microcontroller will keep the low output current active and continue to regularly monitor the input and output voltages until both meet their cutoff levels to be considered fully recharged. This "intelligent control" will solve the above problems of either too many or too few pulses. In the event of a power failure from the source, the controller can operate on stored energy in the capacitors and can keep the load in low current mode until the source turns on and recharges the capacitors.

Figure 21 contains the schematic for the microcontroller circuit, including the connections necessary to program the microcontroller, the inputs to the ADCs, and the outputs to control the switches.

Figure 21. Integrated design schematic, microcontroller.

The integration of the microcontroller controlled load switching eliminated the breadboarded switches made from power MOSFETs, and introduced an integrated circuit (IC) packaged switch. The switch should have a very low ‘on’ resistance so that there is not a significant voltage drop from input to output, and a very high ‘off’ resistance so that power is not consumed in a portion of the circuit that is supposed to be switched off. The switch chosen to control the load resistances is a single pole double throw (SPDT) Intersil ISL84684. This chip has a listed ‘on’ resistance of $0.26 \, \Omega$, a listed isolation stronger than -110dB at low frequencies calculating as an ‘off’ resistance of $15.8 \, \text{M}\Omega$, and a switching time of less than $15 \, \text{ns}$. Intersil switches were also used to break the connection between the ADC monitoring points and the ADC inputs of the MSP430. The dual single pole single throw (SPST) ISL43L120 has a listed ‘on’ resistance of $0.16 \, \Omega$, low frequency isolation of -95dB calculating as an ‘off’ resistance of $3 \, \text{M}\Omega$, and a switching time of less than $15 \, \text{ns}$. There are two switches in each IC package. Both switches of the ISL43L120 were connected in series and their controls were tied together to increase the effective ‘off’ resistance. Figure 22 is the switching schematic. The two upper switches control the path between the ADC inputs and the monitored input and output voltages of the DC-DC converter. The lower switch controls whether the high or low value of resistance is used for the load.

Figure 22. Integrated design schematic, switches.

The microcontroller records the voltages at its ADC inputs. The result of this digital conversion is displaying jitter. For a fixed analog input, each digital conversion records a slightly different value. The jitter would not be a concern if it was only a few millivolts. However the recorded ADC voltages from the DC-DC converter are showing fluctuations between tens of millivolts to several hundred millivolts. There are only several hundred millivolts between the operating input voltage to the DC-DC converter and the minimum voltage where the device would fail. Such strong noise values could cause the microcontroller to initiate a high current pulse even if the capacitors have not fully recharged. It is possible that the noise is due to an active microcontroller clock and could be reduced by using a low power mode. The noise can be observed on an oscilloscope, which indicates that the noise is physical and not a software issue with the programming of the microcontroller. The noise could be induced in the circuit by the current switching action through the inductor of the DC-DC converter, or an artifact of the 60 Hz noise from the electrical grid via the power supply. The ADC even records jitter when supplied with a constant voltage from a power supply and the cause of this noise still needs to be resolved. It might be possible to eliminate this noise by adding a small value capacitor at the input of the ADC, a low pass filter, or another form of data averaging.

5.2 Increasing the output current

One recurring problem is that the DC-DC converters are designed to output a maximum ranging between 100 mA to several amperes of current, but due to the low input voltage supplied by the scavenged energy source they only achieve a small fraction of this current. The output capacitor exhibits voltage decay as its stored energy is consumed by supplying the additional load current. The recharge time of the output capacitor is limited by the low value of current that can be output from the converter. If the converter could output a higher value of current, less current would be required from the output

capacitor and the output voltage would experience a smaller voltage drop. Even if the output voltage drop stayed the same, the recharge time would decrease because less energy would be needed to recharge the capacitor and the converter could supply more current to charge the capacitor.

The steady-state tests show that for low input voltages the output current limit of a converter increases when the input voltage increases. It is unlikely that the scavenged energy source can be reconfigured to produce a higher voltage, but additional capacitors can be used to increase the input voltage. As seen in Figure 23a, when multiple capacitors are charged in parallel, an equal voltage is applied across all of the devices, and they appear as an equivalent capacitance with the sum of their individual capacitances. If two capacitors of equal capacitance, 'x' farads, are in parallel, the equivalent capacitance is '2*x' farads. After the capacitors are charged to the voltage source, they can be disconnected from the source, and placed in a series configuration where the voltages add so that the net voltage from the negative terminal of the first capacitor to the positive terminal of the second capacitor is double the voltage produced by the source as seen in Figure 23b. Reconfiguring the input capacitors should allow the output voltage to have a smaller voltage drop depending on how much additional current the converter is able to provide. Figure 5 shows that if the scavenged energy source produces 0.76 V which is then doubled to 1.52 V, the maximum output current at the proper voltage grows from 5 mA to at least 30 mA. The Holtek data sheet shows that 100 mA of output current can be produced from an input of 1.5 V, while dropping the output voltage by less than 0.1 V.

When multiple capacitors are in series, the effective capacitance would be the reciprocal of the sum of the reciprocals of the individual capacitances. If there are two equal value capacitors, the net series capacitance is '0.5x' farads. The decrease in capacitance means that the charged voltage will decrease faster for a series combination than one single capacitor. After the output capacitor has recharged following an output current pulse, the series capacitors should be reconfigured into their original parallel combination, and the input capacitors will recharge to the voltage source. As the capacitors are switched from parallel to series and again during the reverse process, the converter will briefly have no applied input voltage. During this brief switching the output load will be in a low current mode and the output capacitor can supply the necessary energy to the load.

One potential drawback to this design is that the input capacitance of the parallel configuration will double from its original value, and the recharge time for the input capacitors will double using the same fixed current from the source. These tests were done by physically disconnecting and rewiring the input capacitor connections and then returning them to the original state after the output recharged. The first qualitative tests were done using two 350 F capacitors where the series/parallel configuration was changed manually. The decay of the output voltage did improve, but when the input capacitors were placed in parallel following the current pulse, the effective 700 F capacitor was unable to recharge using the current limited source. The input capacitance was decreased to 20 F by using two 10 F ultracapacitors. This configuration will store substantially less energy than using 350 F capacitors, but manual switching shows that

the output voltage decay has decreased and the input capacitors are able to recharge when connected in parallel. If the load peak current increases from the tested 30 mA, more current will be drawn from the output capacitor and the output voltage drop will increase. Additional testing should be performed using the microcontroller and low 'on' resistance IC switches to control the series/parallel reconfiguration of the input capacitors.

Figure 23. Capacitor configuration.
(a. parallel charging. b, series voltage doubling).

6. Computer Modeling and Simulation

Computer modeling is a powerful circuit analysis tool. It can be used to test and verify a conceptual design prior to physical construction. Solving circuit equations with a computer uses complex device models and can lead to more accurate analysis that would not be available if calculations were done by hand. One caveat about computer modeling is that the simulation results will be valid only if the user includes all relevant information necessary for circuit analysis. Results might not be valid, or may only be valid for a small subset of what the simulation was intended to analyze if a physical parameter affects the circuit in a way that is not well understood and thus not included in the simulation.

Many electrical component designers do not provide computer models of their devices. Simple devices like diodes and transistors can be tested in a lab to determine the necessary modeling properties. Devices with more complexity may need to be behaviorally modeled. A behavioral model is designed to mimic the input and output characteristics of an experimentally tested device without relying on the physical first principles of engineering and physics. It may be impossible to test all possible combinations and create a comprehensive model when there are many influential properties. This means that a behavioral model will likely have restrictions as to when it can be used to obtain valid results.

The DC-DC converters used in previous sections did not have computer models available from the manufacturer. There are two main ways that people tend to model DC-DC. The first way delves inside the integrated circuit using a typical DC-DC converter design, including an inductor, diode, MOSFET, and internal switching. This creates a DC-DC converter model based on first principles, but it is difficult to match this model to the actual device characteristics under all possible scenarios. Another problem with this method is that the internal switching takes place at hundreds of kilohertz. The simulator must use a time step in the range of microseconds or smaller to accurately portray this rapid switching. This is suitable only when simulating the stable output of a DC-DC converter. If this model is used in a more complex circuit with the purpose of viewing a transient over a long time scale ranging from several seconds to minutes or hours, the computational time will be much too long for someone looking to quickly test and analyze multiple adjustments to the circuit.

The second way to model a DC-DC converter is behaviorally. The DC-DC converter experimental measurements provide a good starting point for developing a behavioral model. Both the input current and output voltage of the tested DC-DC converters display dependence on the output current at a fixed input voltage. For the purpose of this report, all computer modeling was done using OrCAD's Capture and PSpice®.^{14,15} In the model a 0-volt voltage source at the output of the DC-DC converter monitors the DC-DC converter output current. The model works by modeling both the output voltage and input current on the output current. The output voltage is based on the laboratory data using a table-based current-controlled voltage-source shown in Figure 24. The input current is modeled as a current-controlled current-source which is curve fit to the experimental data using a third-order polynomial and shown in Figure 25. The actual capture model is represented in Figure 26. The left portion of the model calculates the input current, and the right half contains the load switching and calculates the output voltage.

Figure 24. Table-based output voltage.

Figure 25. Simulated input current.

Figure 26. Capture model.

This model assumes that the input voltage is fixed at exactly 760 mV. In reality, every measurement was recorded at a desired input voltage plus or minus several millivolts due to adjustments between tests and the difficulty of tuning the power supply to an exact voltage. The error due to a few stray millivolts should not have a large impact on simulating the steady-state outputs for fixed output load resistances. The modeled efficiency results are similar to the experimental values. At this point the simulation is not describing anything that wasn't explicitly tested and programmed into the model. One problem is that the model does not include feedback where the input voltage level falls due to the output current pulse and a limited input current. Pulsing experiments used a current limited source to prevent the power supply from providing more than 12 mA of current. The power supply's voltage decreases when it reaches its predefined current limit. Devising a simulation with a changing input voltage would require knowing the output voltage and input current characteristics at every possible input voltage as well as the ability to smoothly transition between these curves when the input voltage changes.

Switching the output resistance during a simulation occurs just like during the experimental load pulsing. Both show that the output voltage sags during a high output current pulse. Experiments show that both the output and input voltages sag after a high current pulse and without any capacitors they might not return to their original values during the low current phase. As soon as the computer simulated output load is not drawing high current, the output voltage returns to its proper value. This does not account for the experimental observation that the input voltage falls and a physical DC-DC converter would not have the power to produce its normal output voltage. Including an output capacitor in the simulation decreases the output voltage drop during a high current pulse. When an output capacitor maintains the output voltage, the maximum output current from the converter can be observed as 5 mA, the remaining output current comes from the capacitor. Including an input capacitor in the simulation has no effect

because the input voltage is an ideal voltage source with no current limit. The voltage source supplies all the current required by the DC-DC converter, while experimentally an input capacitor would provide current to prevent the input voltage from drastically decreasing.

Several problems occur simultaneously with the model. The modeling software does not provide a straightforward method to non-linearly control a voltage source based on a current which is what takes place experimentally by current-limiting the power supply. It is possible to take steady state experimental measurements for several input voltages over a range of output currents. It could be possible to extrapolate the DC-DC converter's characteristics when operating in between the tested input voltages, but PSpice does not offer a method to combine these experiments into one seamless model. At this point the simulation is required to operate with a fixed input voltage during the entire simulation. Experimentally the input voltage varies due to the high current load and the modeling cannot be advanced until the simulated input voltage varies either based on a nonlinear current-limited voltage source or the source is modeled with an internal resistance to vary its output voltage with its produced current.

7. Conclusion

Several advances will allow this smart power supply to better meet its purpose of producing stable power for a long lifetime. The implementation of internally monitoring currents along with stable voltage ADC will allow for more accurate analysis and system-controlled responses. The application of input capacitor-based voltage doubling should improve the stability of the output voltage and decrease the time between peak current pulses. Improvements in computer modeling will enhance the understanding of the circuit under a variety of operating conditions. Future ultracapacitor and DC-DC converter technology currently under development should lead to additional improvements in this power supply system.

The construction of a long lasting, efficient, and stable power source operating from a scavenging energy source has many challenges. Energy storage, power transfer, and device control must be optimized for low working voltages and currents. Further development of this power conversion system will be continued in order to see improvements in how frequently power can be transferred to a load and how much power can be transferred to load electronics in every cycle. With proper calibration this design should allow for stable power generation from any environmentally scavenged source.

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Appendix A

Useful Capacitor Equations

The capacitance of a capacitor is the ratio of its stored electrical charge at a given voltage. A conventional capacitor stores energy in the form of an electric field between two conductors using a dielectric insulator between the conductors to increase the stored energy at a given voltage. Capacitance is defined as

$$C = Q/V \quad (A-1)$$

where C is measured in Farads, Q is the stored electrical charge, and V is the voltage between the conductors of the capacitor.

For a parallel plate capacitor

$$C = \varepsilon * A / d \quad (A-2)$$

where ε is the dielectric constant between the conducting plates, A is the area of the plates, and d is the distance between the plates. The capacitance of a physical device increases by increasing the dielectric constant, or conductor surface area, or decreasing the spacing between conductors.

The stored energy of a capacitor, measured in Joules, is

$$E = 1/2 * C * V^2 \quad (A-3)$$

Increasing the capacitance causes a linear increase in the possible stored energy.

Using Eq. (A-3) twice and subtracting the final energy from the initial energy results in the decrease of energy stored in a capacitor when the voltage of the capacitor decreases.

$$EnergyLoss = 1/2 * C * (V_{Initial}^2 - V_{Final}^2) \quad (A-4)$$

The relationship between a capacitor's current and voltage involves the time derivative of voltage

$$I = C * \frac{dV}{dt} \quad (A-5)$$

Working with a constant current load means that the voltage of a capacitor changes linearly with time

Instantaneous electrical power measured in Watts or Joules per second is

$$Power = I * V \quad (A-6)$$

Due to the linearity of the voltage with respect to current, electrical energy consumed is the time integral of the power

$$\begin{aligned} \text{Energy} &= I * V_{\text{Average}} * \text{Time} \\ &= 1 / 2 * I_{\text{Load}} * (V_{\text{Initial}} + V_{\text{Final}}) * \text{Time} \end{aligned} \quad (\text{A-7})$$

When a capacitor loses stored energy by providing a constant output current, the capacitor energy loss in Eq. (A-4) must equal the energy consumed in Eq. (A-7). After rearranging, the result is the minimum capacitance required to provide a constant I_{Load} of current for a fixed time and a fixed change in voltage across the capacitor.

$$C_{\text{Min}} = \frac{I_{\text{Load}} * \text{Time}}{V_{\text{Initial}} - V_{\text{Final}}} \quad (\text{A-8})$$

Any four out of the five terms in Eq. (A-8) can be used to determine a requirement for the remaining term.

Appendix B

Ultracapacitor Modeling and Self-discharge

Modeling

The Maxwell BCAP350 and PC10 ultracapacitors were modeled by Stanley Atcitty of Sandia/New Mexico using Electrochemical Impedance. The resulting models are five stage RC ladders as shown in Figure B-1. Table B-1 lists the parameters for each of the SPICE models. It should be noted that the first element in both capacitor models is an inductor. The inductance causes the modeled capacitors to have a different high frequency response when compared to an ideal capacitor of the same total capacitance. Sweeping the AC voltage frequency in Figure B-2 for both modeled ultracapacitors and their corresponding ideal capacitors with the same capacitance while observing the voltage across the capacitor shows that the modeled ultracapacitor has a low-pass band similar to an ideal capacitor, but the ultracapacitors differ from the ideal by passing high frequencies as well as low frequencies in a band-stop setup. Figure B-3 and Figure B-4 show the band-stop frequency response of the ultracapacitor models and the low-pass frequency response of the 350 F and 10 F capacitors respectively. As energy storage devices the ultracapacitors will be operating in the low frequency region.

Figure B-1. Ultracapacitor SPICE model.

Table B-1. Ultracapacitor model parameters.

	L	R1	C1	R2	C2	R3	C3	R4	C4	R5	C5
BCA P350	43.5 62n H	1.79 14m	2.65 96F	0.116 49m	23.6 899F	0.340 05m	26.3 271 F	0.302 06m	78.5 779 F	2.14 12m	131. 1757 F
PC1 0	43.2 26n H	61.5 08m	12.8 6mF	10.25 7m	472. 32m F	17.36 7m	1.65 49F	73.66 4m	3.73 94F	10.1 488	321. 16m F

Figure B-2. Model to simulate capacitor frequency response.

Figure B-3. Frequency response of 350 F ultracapacitor (upper curve) and ideal 350F capacitor (lower curve). Resistance = 0.1 Ohm.

Figure B-4 Frequency response of 10 F ultracapacitor (upper curve) and ideal 10F capacitor (lower curve). Resistance = 5 Ohms.

Capacitor Self-Discharge

Future modeling of these capacitors should include the parasitic leakage resistance, which Maxwell lists as 1.2% of energy per day, though varies based on environmental temperature. This parasitic may be available after further analysis of the self-discharge voltage data based on device temperature.

The self-discharge tests were performed in a closed Thermotron test chamber for approximately one day each and occurred over the range of (-25°C) to 60°C . This range was chosen to be overly broad compared to the temperatures where this device will operate, and also fall within Maxwell's stated operating range of (-40°C) to 65°C . The capacitors were charged and then left as an open circuit except when measuring their present voltage value. Energy drains from the capacitors when they are connected to the multimeter, but this additional leakage current is expected to be small due to the short period of time while a capacitor is connected to the multimeter. Figure B-5 and Figure B-6 illustrate the respective temperature trends for the PC10 and BCAP350 ultracapacitors. At higher temperatures the ultracapacitors exhibit faster discharge rates, while at lower temperatures the self discharge is much slower to almost nonexistent. Because the capacitors were not charged to exactly the same voltage at each tested temperature but plus or minus several millivolts, it is important to observe the slope or rate of decay between test points for a given temperature rather than the absolute voltage. The error bar for the PC10 shows 5% deviation from the ideal, while the error bar for the BCAP350 shows 1% deviation from the ideal. Further testing should be performed at the temperature extremes to account for tests at the hot end which experienced unusually fast decay rates, and occasional tests with the PC10 at the cold end where the observed voltage increased over time or showed voltage waveforms of extremely fast cycles of exponential decay followed by an abrupt recharge.

Additional self-discharge tests were performed on the BCAP350 at room temperature, where it was observed that the state of discharge prior to recharging for the next test influences the early discharge rate of that next test. Capacitors that were discharged only tens of millivolts due to the self-discharge of a previous test had a constant rate of voltage decay throughout the subsequent test. Capacitors that were discharged to 0 volts prior to recharging experienced a sharp rate of decay for the first few hours of the test which then slowed and became similar to the rate of discharge for the capacitors not discharged to 0 volts prior to recharging for the subsequent test. In Figure B-7, the red curves were discharged to 0 volts prior to charging for the next test, the blue curves were recharged immediately following the prior discharge test, and 2% error bars are displayed on the ideal 1.2% discharge rate. The two Maxwell ultracapacitors as well as an AVX ultracapacitor can be seen in Figure B-8.

Figure B-5. PC10 Self-discharge.

Figure B-6. BCAP350 Self-discharge.

Figure B-7. Room temperature discharge rates.

Figure B-8. Ultracapacitors.
(L-to-r. AVX 400 mF, Maxwell PC10, Maxwell BCAP350)

Distribution

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