FRONT-END ASIC FOR A SILICION COMPTON TELESCOPE

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Abstract — We describe a front-end application specific integrated circuit (ASIC) developed for a silicon Compton telescope. Composed of 32 channels, it reads out signals in both polarities from each side of a Silicon strip sensor, 2 mm thick 27 cm long, characterized by a strip capacitance of 30 pF. Each front-end channel provides low-noise charge amplification, shaping with a stabilized baseline, discrimination, and peak detection with an analog memory. The channels can process events simultaneously, and the read out is sparsified. The charge amplifier makes use of a dual-cascode configuration and dual-polarity adaptive reset. The low-hysteresis discriminator and the multi-phase peak detector process signals with a dynamic range in excess of four hundred. An equivalent noise charge (ENC) below 200 electrons was measured at 30 pF, with a slope of about 4.5 electrons/pF at a peaking time of 4 µs. With a total dissipated power of 5 mW the channel covers an energy range up to 3.2 MeV.

I. INTRODUCTION

A large field-of-view silicon Compton telescope was recently proposed for detecting Special Nuclear Materials (SNMs) [1-5]. Among other advantages, this instrument can operate at room temperature and achieve a high signal-to-noise ratio by reducing the background to the events that are reconstructed to the same location as the source of interest [6]. Other applications that can benefit from this development include nuclear astrophysics, high-energy solar observations, and nuclear medical imaging [2].

The Compton telescope, shown in Fig. 1, is composed of 24 layers of 3 x 3 sensor arrays. Each array contains nine double-sided 2-mm thick silicon sensors each of 9 x 9 cm², bearing orthogonal strips on the opposite sides. The strips are daisy-chained in both directions, realizing a total of 192 strips per side, each about 27 cm long (pitch ≈ 1.4 mm). A bias voltage is applied to deplete the sensors, and the charge generated by the ionizing event induces on the strips a positive or a negative charge, depending on the sensor’s side. The orthogonal arrangement allows the reconstruction of the position of the event in each layer.

To read out the signals from the 9216 strips (4608 for each polarity), a low-noise application specific integrated circuit (ASIC) is required. When connected to the strips that are characterized by a capacitance of about 30 pF, the ASIC must provide a resolution better than 3 keV FWHM (about 360 electrons rms), covering an energy range of 1.6 MeV without dissipating more than a few mW per channel.

The ASIC discussed here was developed for this purpose jointly by the Naval Research Laboratory (NRL) and Brookhaven National Laboratory (BNL). In this paper, we describe the ASIC’s architecture, and report our first experimental results.

II. ARCHITECTURE OF THE ASIC

Fig. 2 shows the architecture of the ASIC that comprises 32 front-end channels, 32:1 multiplexers, bias circuitry, a test-pulse generator, two 10-bit DACs for threshold and test pulse control, configuration registers, and logic to control the acquisition, readout, and configuration. Each channel implements a low-noise charge amplifier, a shaper with stabilized baseline, a discriminator with trimming, and a peak detector with analog memory. Details of some of these circuit blocks are given below.

![Fig. 2. Architecture of the 32-channel ASIC.](image)
negative input charge polarity (dotted lines in Fig. 3), and bypassed in the other case (dashed line in Fig. 3). To have each reset stage to properly operate with either the negative or the positive input charge, a combination of both classical and mirror configurations is simultaneously implemented and alternatively enabled (MOSFETs indicated either in red for negative input charge polarity, and in blue with dots for the other case) depending on the input charge’s polarity. The output of the last stage (the second or the third depending on the polarity), is connected to the virtual ground input of the shaping amplifier.

![Fig. 3. Multi-stage charge amplification with adaptive continuous reset for operating with both polarities of input charge. The output is connected to the virtual ground input of the shaping amplifier.](image)

To match the 30 pF strip capacitance, the input MOSFET $M_1$ has a relatively large gate size, which entails a small output resistance, $r_D = 9 \, \text{k}\Omega$, and a relatively large gate-to-drain capacitance, $C_{gd} = 1.1 \, \text{pF}$. To achieve a high voltage gain and wide bandwidth, the voltage amplifier typically implements a cascode, where the current is about one tenth of the drain current of $M_1$. In our case, due to the small $r_D$ and large $C_{gd}$, a single cascode (SCS) configuration, based on one MOSFET $M_C$, as shown in Fig. 4(a), would considerably limit the amplifier’s performance. With its relatively high input impedance, the SCS limits the dc gain and adds a pole at the drain of $M_1$ at relatively low frequency. In addition, it affects the pole-zero cancellation of the charge amplifier because of the contribution from $C_{gd}$ which, multiplied by the gate-to-drain voltage gain of $M_1$, integrates a non-negligible amount of the signal charge. The resulting effective increase in the overall feedback capacitance introduces an error in the pole-zero cancellation.

To improve the performance, the input impedance of the cascode must be reduced. We analyzed two solutions, both frequently adopted by designers: the amplified cascode (ACS) shown in Fig. 4(b), and the dual cascode (DCS) shown in Fig. 4(c).

![Fig. 4. Alternative cascode configurations: (a) single non-amplified SCS, (b) single amplified ACS, and (c) dual DCS.](image)

The ACS controls the gate voltage of $M_C$ through a feedback loop realized using the voltage amplifier $M_A$. The DCS has a second cascode $M_D$, located between $M_1$ and $M_C$, operating at the same current as $M_1$. We compare the three configurations in Fig. 4 analyzing them in terms of impedance at the drain of $M_1$, amplifier dc voltage gain, bandwidth, noise, voltage drop, and dissipated power.

In the following, $(g_{mC}, r_{OC}, C_{gsC}, C_{gdC})$, $(g_{mA}, r_{OA}, C_{gsA}, C_{gdA})$, and $(g_{mD}, r_{OD}, C_{gsD}, C_{gdD})$ are, respectively, the transconductance, output resistance, gate-to-source, and gate-to-drain capacitance of $M_C$, $M_A$, and $M_D$; while $r_O$ is the resistance of the current source, $I_C$. In all cases and for all MOSFETs we assume a dc gain $g_{ma}r_O >> 1$.

In terms of the impedance, $Z_{dd}$, at the drain of $M_1$, the comparison can be done at low frequency. It results in the corresponding resistances $r_{dd}$:

\[
\begin{align*}
  r_{dd} &= r_O \frac{r_C + r_{OC}}{r_C + r_{OC} + r_{OD}g_{mc}r_{OC}} \quad \text{SCS} \\
  r_{dd} &= r_O \frac{r_C + r_{OC} + r_{OA}g_{mA}r_{OA}g_{mC}r_{OA}}{r_C} \quad \text{ACS} \\
  r_{dd} &= r_O \frac{r_C + r_{OC} + r_{OD}g_{mc}r_{OC} + r_{OD}g_{mD}r_{OD}g_{mC}r_{OD}g_{mC}r_{OD}g_{mD}r_{OD}g_{mD}}{r_C} \quad \text{DCS}
\end{align*}
\]

and, within the typical cases of $r_O >> r_{OC}$ and $r_O >> r_{OD}g_{mc}r_{OC}$, both the ACS and DCS exhibit a similar $r_{dd}$ performance.

In terms of the amplifier’s dc voltage gain, $A_0$, the results are:

\[
\begin{align*}
  A_0 &= \frac{r_C g_{mC}r_{OC}g_{mC}r_{OC}}{r_C + r_{OC}g_{mC}r_{OC}} \quad \text{SCS} \\
  A_0 &= \frac{r_C g_{mA}r_{OA}g_{mA}r_{OA}g_{mC}r_{OA}}{r_C + r_{OA}g_{mA}r_{OA}g_{mC}r_{OA}} \quad \text{ACS} \\
  A_0 &= \frac{r_C g_{mD}r_{OD}g_{mD}r_{OD}g_{mC}r_{OD}g_{mC}r_{OD}g_{mD}r_{OD}g_{mD}}{r_C + r_{OD}g_{mD}r_{OD}g_{mC}r_{OD}g_{mD}r_{OD}g_{mD}} \quad \text{DCS}
\end{align*}
\]

So, again, within the typical cases, both the ACS and DCS exhibit comparable $A_0$ performance.

In terms of bandwidth, the SCS introduces in the amplifier’s voltage transfer function only one pole (time constant $\tau_1$), while the ACS and the DCS introduce two poles (time constants $\tau_1$ and $\tau_2$), but at higher frequency. For the case of the ACS the two poles can be complex conjugate, and consequently, the associated phase margin could make difficult for the designer to stabilize amplifier’s feedback loop. To guarantee real poles the ACS must be designed to satisfy the following condition:

\[
  g_{mA} > 4g_{mC} \frac{C_{gsC} + C_{gdC}}{C_{gsA} + C_{gdA}} \quad \text{ACS}
\]

and, assuming that (3) is satisfied, the three alternatives perform as follows:
to MD, the ACS and DCS deliver comparable performances.

We note that if MA operates with a size and current comparable to MD, the ACS and DCS deliver comparable performances.

In terms of noise, performing for simplicity the calculations at low frequency and assuming an infinite load resistance $r_C$, it follows

$$\tau_i = \frac{C_{g_{DC}} + C_{g_{MC}}}{g_{MC}} = \frac{C_{g_{MC}}}{g_{MC}} \quad \text{SCS}$$

$$\tau_i = \frac{C_{g_{DA}} + C_{g_{MC}}}{g_{MC}} = \frac{C_{g_{DA}}}{g_{DA}} \quad \text{ACS}$$

$$\tau_i = \frac{C_{g_{DB}} + C_{g_{MC}}}{g_{MC}} = \frac{C_{g_{DB}}}{g_{DB}} \quad \text{DCS}$$

where $v_{ac}$, $v_{na}$, and $v_{sd}$ are, respectively, the equivalent input noise voltages of $M_C$, $M_A$, and $M_D$, and $v_{ae}$ is the corresponding equivalent contribution at the input of the amplifier. If $M_A$ operates with a size and current comparable to $M_D$, the ACS and DCS offer similar performances.

In terms of additional voltage drop compared to the single cascode, for the ACS it depends on the gate-to-source voltage of $M_A$, while for the DCS it is controlled by the gate bias voltage of $M_D$. Considering that the source-to-drain voltage of $M_A$ and $M_C$ can be contained in most cases within very few hundreds of mV, the two solutions exhibit an equivalent drop.

In terms of power dissipation, the ACS requires the additional current associated with $M_A$ that, to contain the noise and satisfy (3), can be non-negligible.

Taking all these findings into consideration, we adopted the DCS configuration. The gate width of $M_D$ that maximizes the bandwidth can be calculated from (4), and it is about one third to one fourth of the gate width of $M_I$, depending on the gate width of $M_C$.

The charge amplifier in Fig. 3 is followed by a 5th order shaper [10] that provides charge to voltage conversion and filtering with a peaking time adjustable to 0.5-, 1-, 2-, and 4-µs. The output baseline is stabilized with a band-gap-referenced BLH circuit [11]. The overall channel gain can be set to nominal values of about 14-, 28- or 56-mV/fC, thus covering an energy range up to 3.2 MeV. A low-hysteresis comparator with multiple-firing suppressor [12] accommodates event discrimination with a threshold controlled through a 10-bit DAC common to all channels, and a 4-bit DAC per channel for equalization. Above-threshold events are processed by a multi-phase peak detector with analog memory [12, 13].

The acquisition is enabled by setting the external LVDS (Low Voltage Differential Signal) Enable at high; it can be automatically disabled either when a first channel crosses the threshold, or when a first channel finds the peak. An LVDS Flag, which can be released either at the first peak found or 200 ns later, indicates one or more successful acquisitions. Users can set the delay, during which other channels may be processing events, after which the read out of the measured amplitudes can start. The ChipSelect high sets the ASIC in the readout mode, and at each LVDS Clock, the peak amplitude and the address of those channels that processed the above-threshold events are made sequentially available at dedicated outputs (one analog output for the peak amplitudes, five digital outputs for the address), thus providing sparsification.

Each channel implements a 200 fF test capacitor connected to the input, with another terminal connected to an on-chip pulse generator. The pulse generator is triggered with the LVDS clock TestCk, and has an amplitude adjustable with a dedicated 10-bit DAC. Additional ASIC functions include per channel masking, channel shaper output monitor, and a DACs monitor.

Fabricated in CMOS 0.25 µm, the ASIC has 80 pads and measures about 5 mm × 5 mm. The channel itself is 4.2 mm × 120 µm and dissipates about 4 mW. The entire ASIC system dispels about 160 mW, yielding an effective power per channel of about 5 mW. Fig. 5 is a picture of the die.

Fig. 5. Picture of the 5 mm × 5 mm die.

III. FIRST EXPERIMENTAL RESULTS

The ASIC initially was characterized without sensor and then, in preliminary experiments, with a sensor; we report here the most relevant results.

Fig. 6 illustrates the response of the channel to a negative charge of about 25 fC for the four peaking times and three gain settings. The baseline is about 260 mV. We measured an integral linearity error below +/- 0.25 % (+/- 0.4 % at 0.5 µs peaking time) for amplitudes of output signal up to 2.25 V (including the • 260 mV baseline), corresponding to an input charge up to 140 fC at the lowest gain setting. A channel-to-channel dispersion of about 5 mV rms and 1.6 % rms (3.7 % rms at 0.5 µs peaking time) respectively characterized the baseline and gain.

The ENC versus external input capacitance is shown in Fig. 7 for the four peaking time settings, measured at each of the three gain settings. Fig. 7(a) shows the case of negative charge amplification, while Fig. 7(b) shows the positive. A noise slope from about 4.5 eV/pF at 4 µs to about 12 eV/pF at 0.5 µs was extracted for both.
In Fig. 6, we depict the gain versus external input capacitance for the same settings. We measured a drop in gain from 3%/100pF at 4 μs to 6%/100pF at 0.5 μs. The stronger dependence of the gain on the peaking time was apparent in the positive charge amplification. We are investigating this effect; it might be partially attributed to the edge of internal pulse generator, which is non symmetrical with respect to the polarity. A gain 9% larger than the nominal was measured at the maximum gain setting and at 4μs peaking time, but reduced for shorter peaking times.

In Fig. 9, we plot the measured peak amplitude, processed by the discriminator and peak detector circuits, as a function of the injected charge. The error in the peak detected amplitude, compared with the actual shaped pulse amplitude, also is shown. The circuits can discriminate and process for peak detection amplitudes from about 8 mV above baseline (about 0.22 e− at this gain setting), demonstrating a dynamic range of about 400. In this measurement the dynamic range still is limited by the hysteresis (about 10 mV) of the comparator in the discrimination circuit, as it can be evaluated considering the signal-to-noise ratio of about $1400\sigma/100 e^{-}=14$.

Fig. 10 shows a preliminary spectrum of $^{241}$Am and $^{57}$Co acquired at NRL using the ASIC connected to a silicon strip sensor of 1.7 cm $\times$ 1.4 mm $\times$ 500 μm. At a temperature of -40°C, we obtained a resolution of about 1.4 keV at 59.5 keV with a peaking time of 4 μs and at a temperature of -40°C. The $^{57}$Co peak at 122 keV, with a resolution of 1.5 keV, is also visible. The available linear range at this gain setting of 56 mV/μC (2.5 mV/keV) is about 800 keV.
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