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A New Inner Layer Silicon Micro-strip Detector for DØ

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Abstract

The DØ experiment at the Fermilab Tevatron is building a new inner layer detector (Layer-0) to be installed inside the existing DØ Silicon Micro-strip Tracker (SMT). The Layer-0 detector is based on R&D performed for the RunIIb silicon upgrade, which was cancelled in the fall of 2003. Layer-0 will be installed between the bean pipe and the the 2.2cm radius opening available in the SMT support structure. The radius of the first sampling will be reduced from 2.7cm to 1.6cm. Layer-0 will be radiation harder than the current SMT, thus ensuring that the silicon tracker remains viable through Tevatron RunII.

Key words:

1 Introduction

The DØ Silicon Micro-strip Tracker (SMT) has successfully been operated since the start of physics data taking in RunII. A new inner layer silicon micro-strip detector (Layer-0) has been built to mitigate tracking efficiency losses due to detector failures [1]. Layer-0 will also provide more robust tracking and pattern recognition capabilities for higher luminosities and improve the impact parameter resolution. Figure 1 illustrates the improved impact parameter resolution with the addition of Layer-0 as a function of the transverse momentum of the tracks. This will translate into a significant increase in the efficiency to tag jets originating from b quarks and improve the resolution for B_s meson flavor oscillations.

2 Design

Layer-0 is designed to fit inside the existing RunII detector [2]. It will utilize much of the existing infrastructure as well as the new electronics and readout chip designed for the cancelled RunIIb silicon replacement [3]. The current DØ silicon tracking detector consists of six 4-layer barrel structures intercept with discs. Figure 2 shows an end view of the current detector with the new Layer-0

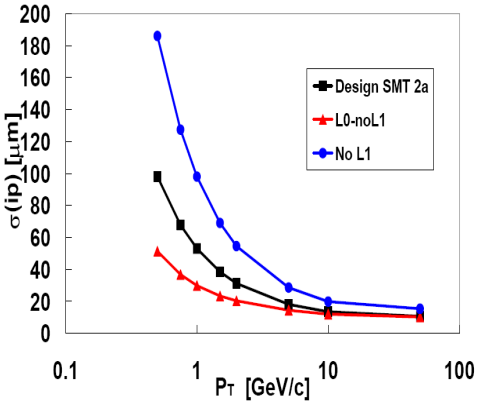

Fig. 1. The three lines show simulations of the impact parameter resolution as a function of the transverse momentum of the tracks. The squares show the performance of the current RunIIa detector. The other two lines correspond to simulations with total loss of the innermost layer-1 of current RunIIa detector: one with the addition of Layer-0 (triangles) and one without (circles).

superimposed in the center.

Layer-0 is designed to slide over a new beryllium beam pipe and associated mounting flanges that have a diameter of 30.5mm. The design includes a 1.0mm separation from the beam pipe to limit capacitive coupled noise. The new detector clears the inner most layer of the current detector through a 44.0mm diameter aperture. In addition to the tight mechanical constraints the detector is designed to maximize acceptance (98.5%) and readout segmentation. A 6-fold geometry was chosen with inner layer of sensors positioned at a radius of 16.0mm and an outer layer of sensors at a radius of 17.6mm. Figure 3 shows an enlarged view of Layer-0 illustrating sensor positions.

Hybrids are located on both sides in z outside of the active volume and are connected to the sensors with fine pitch analog cables. Segmentation in beam direction (Z) is limited to eight

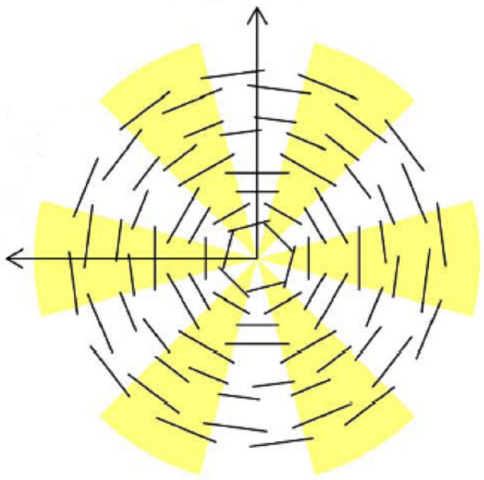

Fig. 2. South end view of the DØ silicon detector. The figure shows the radial and azimuthal location of the silicon sensors. The six Layer-0 sensors are show in the center. The current RunII sensors are distributed in four double-layers, each providing full azimuthal coveage. The inner two double-layers have 12 sensors, the outer have 24 sensors.

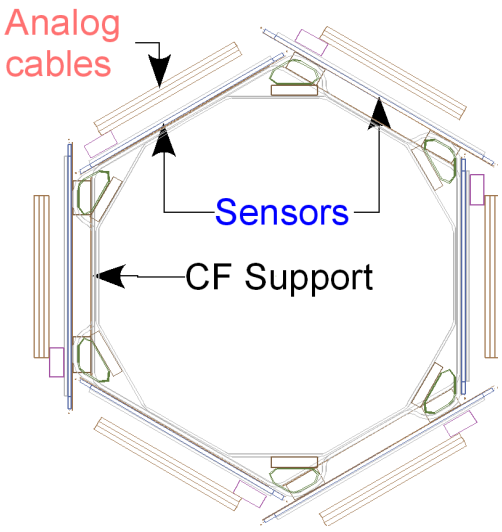

Fig. 3. Layer-0 end view with support structure, sensors and analog cables.

Table 1
Geometric parameters of the DØ Layer-0 detector and sensors.

Layer	Radius	Z segment	Readout Pitch	Length	Cable Lengths
0 inner	16.0mm	central	71μm	70mm	320mm, 346mm
0 inner	16.0mm	peripheral	71μm	120mm	167mm, 244mm
0 outer	17.6mm	central	81μm	70mm	320mm, 346mm
0 outer	17.6mm	peripheral	81μm	120mm	167mm, 244mm

sensors by the radial buildup of the cable bundles. The four central sensors have a length of 70mm, while the peripheral ones are 120mm long. This arrangement provides better segmentation near the center of the interaction region (Z=0) and equalizes the load capacitance by having lower sensor capacitance on the strings with longest analog cables. Table 2 summarizes the geometric dimensions of the Layer-0 components. Inner radius sensors have strips with 71μm pitch while 81μm pitch sensors are used at larger radius positions. All sensors are manufactured by Hamamatsu Photonics and have intermediate strips that are not read out.

A single cable pitch is accomplished by utilizing ceramic pitch adapters mounted on the sensors that also carry decoupling capacitors. Analog cables provide an interface between the pitch adapters and the hybrids. To minimize mass in the active region, 91 μm pitch kapton cables are used. The analog cables are flexible circuits manufactured by Dyconex. The cable lengths vary, with the longest at 34.6mm, and have a capacitance of 0.35 pF/cm. Careful design of these cables was required to minimize the capacitance presented to the readout chip pre-amplifier. The most outermost sensor is connected to the outermost hybrid and the cables are routed on top of the sensors, but below the hybrids. Kapton mesh spacers with 90% open area are used to separate analog cables thus minimizing capacitive coupling.

The Layer-0 readout is based on the SVX4 chip [4], which is a 0.25 μm technology silicon readout chip originally developed for the RunIIb upgrades. These chips provide analog pipeline, signal digitization and online zero suppression. The SVX4 uses a readout protocol similar to the currently installed SVX2 chips but operate with a single 2.5V supply rather than the 3.3V to 5V supplies needed for the SVX2 [5]. Each ceramic BeO hybrid holds two SVX4 chips. The SVX4 electrical ground is connected through hybrid vias to contacts on the co-cured flex circuit on the carbon fibre support.

Digital signals from the hybrid are carried to the end of the support structure using a kapton flex digital jumper cable. The jumper cable is then coupled to a twisted pair cable using a junction card located on the existing silicon support structure. An adapter card with active

circuitry, mounted on the wall of the DØ calorimeter, interfaces Layer-0 to the existing readout. The Layer-0 readout is designed to utilize the existing SVX2 data acquisition electronics hardware downstream of the adapter cards. The SVX4 channels are grouped to electronics modules that are configured with a SVX4 specific firmware.

Several RunIIb studies have established that low coherent noise can be achieved by good low inductance ground connections to the support structure [6]. This is accomplished by co-curing mesh ground planes onto the carbon fiber support structure and utilizing low inductance flex circuits which carry bias and ground from the bottom to the top of the sensors. Since Layer-0 is a longitudinally continuous conductor, the potential exists for a serious ground loop encircling the DØ calorimeter. The adapter card was designed to provide electrical isolation from the DØ detector ground. This card converts single ended SVX2 control signals, supplied by existing electronics, into differential signals needed by the SVX4. Ground isolation is achieved by the high impedance of the differential signal lines. A separate isolated 2.5V supply provides power to the SVX4 chips. The isolation requirement is greater than 10Ω.

3 Performance

The completed Layer-0 detector mechanical dimensions have been compared to aperture measurements of the RunIIa silicon detector taken during an access to the central detector area in 2004. The aperture measurements show that Layer-0, with an outer radius of 22.02mm will have a radial clearance to the existing structures by 0.86mm horizontally and 1.67mm vertically. The 1.0mm spacing requirement, to prevent capacitive noise coupling from the beam pipe, has also been insured.

Two noise issues arose while testing Layer-0. The isolated low voltage power supply for the SVX4 chips was found to require a filter to reduce pick-up noise on the readout. Ferrite core inductors used on the power cables have shown to reduce the noise to acceptable levels. The use of a specifically designed LC filter has also been investigated. The second issue involves the resistive temperature device (RTD) system, which is used to monitor the sensor temperature. The RTD system consists of a RTD soldered onto a flex circuit affixed longitudinally to Layer-0. The flex circuit is then adapted to cryogenic type wire. A braided shield around the cryogenic wire connected to the Layer-0 isolated ground eliminated the noise.

Maximizing the signal to noise response has been addressed throughout the design of Layer-0. The single Minimum Ionizing Particle (MIP) equivalent is about 30 ADC counts. Readout tests on the full system show a noise level of 2 ADC counts, thus resulting in a signal to noise ratio of 15:1. This was attained with a 200V sensor bias and a ferrite core on the isolated power supply leads.

The signal to noise ratio is uniform as a function of the Z location. This gives adequate signal available for tracks incident at the extreme edges of the detector and ensures reliable readout and track reconstruction.

4 Conclusion

A new inner layer silicon detector for the DØ experiment has been designed, built, and tested. Strict mechanical specifications, electrical isolation from the rest of the DØ detector, and a high signal to noise ratio have been demonstrated. Layer-0 will be installed during the next shutdown period scheduled for early 2006.

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