DØ Layer 0 - innermost layer of Silicon Microstrip Tracker

K. Hanagaki *
for the DØ Layer 0 group

Fermilab, P.O.Box 500, Batavia, IL, 60510

Abstract

A new inner layer silicon strip detector has been built and will be installed in the existing silicon microstrip tracker in DØ. We report on the motivation, design, and performance of this new detector.

Key words: Silicon Microstrip Tracker, DØ, Radiation damage

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1. Introduction

The DØ collaboration has built a single layer silicon strip detector, Layer 0 (L0). The construction was completed in August 2005. L0 will be installed inside the barrel part of the existing silicon microstrip tracker (SMT) [1]. The DØ SMT consists of six barrels, 12 central disk, and four forward disk detectors. Each barrel has four super-layers, and is 12 cm long.

There are three major motivations for L0. Due to its proximity to the interaction point adding L0 significantly improves impact parameter resolution, as shown in Fig. 1, resulting in better sensitivity for B_s mixing measurement and higher efficiency for b -jet tagging. The addition of another layer also provides better pattern recognition, especially in high luminosity operation. We therefore expect a reduction of the fake track rate. Finally, the innermost layer of the SMT was expected to start losing functionality after seeing a luminosity of $4\text{--}5\text{ fb}^{-1}$ or $11\text{--}15 \times 10^{12}/\text{cm}^2$ 1 MeV neutron equivalent, requiring replacement to maintain functionality of the tracker.

Figure 2 shows the depletion voltage as a function of fluence measured at the Fermilab 8 GeV

Fig. 1. The impact parameter resolution for a central track with and without L0 as a function of the momentum in Monte Carlo simulation. Data with the current detector are confirmed to be in agreement with the upper curve.

booster (proton beam) using spare sensors. Also shown are the recent in situ measurements for the sensors installed in the SMT. The SMT uses several types of silicon sensor technology. Most of the sensors behave as predicted by the Hamburg model [2]. However the Double Side Double Metal (DSDM) sensors used in the first layer show abnormally high depletion voltage sensitivity. This would shorten the expected lifetime, which is due to the onset of microdischarge at a bias voltage of 125-150 V.

It turns out, however, that the actual sensors used at DØ do not show such abnormal depletion

* Corresponding author. ph +1-630-840-2327
Email address: kazu@fnal.gov (K. Hanagaki).

Fig. 2. The depletion voltage for various silicon sensor types as a function of fluence. The open circles show the result for the DSDM sensor used in the first layer of SMT obtained by bias current scans in the actual detector. The line indicates the Hamburg model prediction.

voltage¹, as also shown in Fig. 2. The lifetime estimate of the innermost layer of the SMT has been updated to $5\text{--}7\text{ fb}^{-1}$ based on the new in situ measurement.

L0 uses the R&D effort and human resources invested in the Run 2b silicon upgrade project [3], which was canceled in 2003. For example, the read hard single sided sensor, SVX4 readout chip, and hybrid developed for Run 2b are all used in L0. These investments enabled us to design and completely build L0 within two years.

2. Design

As L0 must be installed within the existing detector, the space constraints are severe. The inner radius is determined by the beam pipe ($r=15\text{ mm}$), and the outer by the support of the existing detector ($r=23\text{ mm}$). These constraints do not allow us to place the readout chip on the sensor because of the lack of space as well as insufficient cooling. Our choice is to use a Kapton flex circuit as an analog cable to transmit the unamplified signal from the sensor directly mounted on the carbon fiber support structure to the readout chip mounted on a hybrid outside the fiducial region. This design is similar to the CDF L00 [4].

¹ The difference between the booster beam test and the measurement at DØ is the annealing time. We believe that there was not enough time for the sensors to release trapped charge during the beam test.

L0 has a six-fold geometry with the inner layer at $r=16.0\text{ mm}$ and the outer layer at $r=17.6\text{ mm}$, as shown in Fig. 3, having an acceptance of 98.5% for tracks traveling perpendicular to proton or anti-proton beam direction. The readout pitch is $71\text{ }\mu\text{m}$

Fig. 3. Cross section of L0. The six planes (dark grey) near the beam pipe indicate the sensors, and the other six narrow planes (light grey) indicate the analog cables.

for the inner and $81\text{ }\mu\text{m}$ for the outer sensors with intermediate strips. The number of readout strips are 256 for both types of sensors. For a given ϕ sector, there are four 7 cm long sensors covering the central part, and four 12 cm long sensors for forward parts (two for each end), resulting in 48 sensors or modules in total, where a module is a set of a sensor, a hybrid, and two analog cables connecting the sensor and the hybrid. All the sensors are single sided and AC coupled sensors fabricated by Hamamatsu.

Each hybrid is located at the same ϕ as the corresponding sensor. Therefore four hybrids are aligned at each end of the support. The resulting lengths of the analog cables are 20, 27, 34, and 36 cm, depending on the location of the module. The analog cable is fabricated by Dyconex. The cable pitch is $91\text{ }\mu\text{m}$. We use a pair of analog cables, stacked with a $45\text{ }\mu\text{m}$ offset, for each module. Because the analog cable is longer for the shorter sensor, the capacitive load is similar for all the types of modules with a typical value of 22 pF .

L0 uses SVX4 as the readout chip, which is a $0.25\text{ }\mu\text{m}$ technology silicon chip and the latest in the SVX series developed by Fermilab and LBNL [5]. The SVX4 has 128 input channels, and equivalent noise charge (ENC) = $300 + 41 \times C$ electrons, where C is the load capacitance at 69 ns preamp rise time², and is measured to be rad-hard up to 20 Mrad . SVX4 can suppress coherent noise by utilizing event by event dynamic pedestal subtraction. The hybrid is formed on a BeO substrate, and holds two SVX4 to accommodate the readout from a single sensor. The SVX4 uses 2.5 V power with differential output signals, while the SVX2 chip [6], which is used in SMT, needs 3.3 V and 5 V with single ended signals. Since the SVX4 must be read out through the existing DAQ system, an additional card downstream of the hybrid, the adapter card, is used to accommodate the differences.

The use of analog cable makes achieving a low noise system difficult [7]. It behaves as an antenna, while the signal provides ~ 23000 electrons. In addition, the impedance of carbon fiber for high frequency AC (53 MHz readout in our case) turns out to be very small. There is no difference among carbon fiber, stainless steel, and aluminum. Therefore, the support structure must be carefully grounded, and the grounding scheme is the most important electrical issue [8].

All our studies indicate that the low inductance grounding connection to the SVX4 on the hybrid is critical for noise reduction. For example, Fig. 4 shows noise for a module on the prototype support structure as a function of the number of wires (order cm long) connecting the ground of the hybrid to the support. To achieve low inductance grounding connections, the hybrid has ground pads on its backplane which are silver epoxied onto the copper rail on a Kapton flex ground mesh circuit which is cocured with the carbon fiber support structure.

² The rise time will be much slower in the actual L0 operation where the bunch spacing is 396 ns . Run 2b expected a bunch spacing of 132 ns .

Fig. 4. Noise as a function of the number of wires connecting the ground between the hybrid and the reference grounding plane. The vertical scale is arbitrary.

The sensor ground is similarly connected to the support structure using a Kapton flex circuit.

Another important variable is the proximity of the analog cable to the grounded support structure. To avoid coupling of noise generated by the finite impedance of the structure, the space under the analog cable has to be maintained and optimized. Layers of Kapton mesh spacers are used, providing to 0.36 mm separation under the analog cable.

3. Performance

With the various tricks discussed above, a single L0 module has no coherent pickup noise when the L0 grounds are tied to the common detector ground, as shown in Fig. 5. The total noise, defined

Fig. 5. The pedestal (black triangles), total noise $\times 10$ (dark grey circles), and differential noise $\times 10$ (light grey squares) of a module in units of ADC counts. There is no coherent pickup noise observed, leading to the same noise level for total and differential noise.

as RMS of the pedestal, is about 1.8 ADC counts . A MIP creates 29 ADC counts of signal. This has

Fig. 6. The pedestal (black), total noise $\times 10$ (dark grey), and differential noise $\times 10$ (light grey) of 23 modules on the support structure in units of ADC counts.

been verified with cosmic rays. The resulting signal to noise (S/N) ratio is 16.

Because L0 is read out from both ends of the detector, while the support structure is electrically uniform, a ground loop may exist in the DØ collision hall. In order to break such a loop, L0's ground can be isolated from the common detector ground. This grounding scheme increases the sensitivity to external noise, especially for the noise pickup from power lines of the SVX4. The total noise can be as large as 5 to 12 ADC counts, while the differential noise stays at 1.8 ADC counts, indicating the increased noise is completely coherent. A noise filter based on toroid coils has been built for the power lines, and reduces the total noise down to an average of 2.5 ADC counts. In addition, the dynamic pedestal subtraction by the SVX4 chip eliminates the coherent noise completely as indicated in Fig. 6 which shows the noise, as well as the pedestals, for 23 modules after installation onto the support structure with dynamic pedestal subtraction. This provides additional redundancy to reject noise pickup.

All the 96 chips in L0 have been verified to be working properly. The total number of dead channels is about 10, all due to wire bond failures. Bias voltage and bandwidth scans were conducted, verifying the expected noise behavior. Thermal cycling was performed between 15 and -5°C , finding no problems.

After the construction, extensive mechanical measurements were conducted. The deflection is about $27\ \mu\text{m}$ over the sensor region. The accuracy of installation alignment was measured to be $2\text{--}3\ \mu\text{m}$. The measured dimensions were compared to the aperture of the existing SMT measured during a shutdown in 2004. This comparison verifies that

L0 will fit into the desired space. The installation procedures have been tested successfully using a mockup.

4. Conclusions

L0 has been designed to satisfy the tight space constraints with the special grounding efforts to establish a low noise system. The mechanical specifications have been met. The system has been tested and has demonstrated low noise behavior.

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