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1. Identification and Significance of Innovation

Cost-effective, low power time-to-digital converters (TDCs) with a high level of integration and minimal latency suitable for an open system architecture play an important role in digitizing, triggering, and processing data in High Energy Physics (HEP) and Nuclear Energy Physics (NEP) experiments. TDCs are required for scientific applications including particle identification in Time-of-Flight (TOF) detectors and particle tracking in gas-based drift detectors, and commercial products such as laser range-finders and logic analyzers.

Future Large Hadron Collider (LHC) experiments such as ATLAS and CMS [1-4], as well as experiments at the Relativistic Heavy Ion Collider (RHIC) and GRETINA, will utilize more than eighty million parallel signal channels that are associated with different types of detectors (wire chambers, silicon detectors, calorimeters, etc.), each delivering a wide dynamic range of signals with different timing characteristics and different interfaces, making large-scale integration essential. Another important desire is to have data reduction at the earliest possible stage of processing in order to reduce interconnect bandwidth and the required buffering capacity of the final data processor.

Highly integrated, cost effective, and low power electronics is absolutely vital for handling the increasing number of channels in future particle physics experiments. The use of standardized electronic components could simplify the development, commissioning, and data taking period of an experiment. Bulky (2-3 cPCI slots), high-speed, power hungry, multi-sampling digitizers are manufactured by many different vendors such as Acqiris Inc, Applied Physica Laboratory, Tektronix, and others. At the same time, future DOE experiments will require higher time resolution, as well as smaller sized and easy upgradeable devices. In accordance with the available information, there are no state of the art (SOA) components that provide a power effective system-on-chip (less than 2W) solution that performs sub-picosecond TOF measurements and digitizing operations as well as provides a robust scalable serial network interface.

It is obvious that the requirements for the time-to-digital converters (TDCs) vary significantly according to the different kinds of applications. Some of the most challenging conditions are related to large particle detectors. The experiments being performed by DOE National Laboratories will require interval measurements with sub-picosecond resolution.

1.1. Technical Approach

In order to satisfy the discussed requirements, the Advanced Science and Novel Technology Company (ADSANTEC) in collaboration with the Physics Division of Oak Ridge National Laboratory has develop a concept of a novel, Multi-channel time Interval Digitizing system with digital Initial Calibration (MIDIC) that utilizes a proprietary combinational method of time measurements.

The proposed approach represents a modification of the well-known vernier delay line (VDL) methodology with parameter stabilization by means of a delay-locked loop (DLL). The high digitization accuracy at a reasonable level of complexity is achieved by utilization of a high-
speed internal clock derived from a stable low-speed external clock by means of multiplication within the on-chip phase-locked loop (PLL).

Based on the achieved promising results of computer simulations, ADSANTEC is ready to finalize MIDIC’s architecture and implement it as an ASIC during Phase II. The developed ASIC will be fabricated using the selected BiCMOS technology. Promex Industries Inc., our long term partner (see Agreement in Attachment) is willing to support ADSANTEC’s efforts and will perform the packaging and assembly of the developed ASIC using its proprietary high speed surface mount package.

2. Phase I Technical Objectives

The main goal of the Phase I project is to prove the feasibility of the proposed concept. Important issues to be addressed in this Phase I program include the architecture development and preliminary simulations of the MIDIC system.

In order to achieve this goal, the following objectives have been established:

Objective 1. Evaluate the existing technologies for high-performance IC fabrication and select the process most suitable for MIDIC’s implementation.

Objective 2. Define MIDIC’s external parameters and develop its architecture.

Objective 3. Develop TDC’s channel architecture and perform initial timing analysis.

Objective 4. Develop the main critical blocks of TDC and estimate their parameters.

In order to meet the objectives outlined above, the following questions will be answered in the course of this project:

1. Which technological process is suitable for MIDIC’s implementation?
2. What is the optimal architecture of the proposed system?
3. What are the achievable parameters of TDC?

3. Phase I Work Plan

The project objectives listed in Section 2 were accomplished through the following tasks:

3.1. Project Tasks

Task 1. **IC Fabrication Technology Selection (Objective 1).** Within this task, ADSANTEC investigated the available high-speed IC fabrication technologies in order to define the processes most suitable for the implementation of the proposed MIDIC.

Task 2. **MIDIC Architecture Development (Objective 2).** This task was devoted to the development of the system’s general architecture.

Task 3. **TIC Architecture Development (Objective 3).** Under this task, ADSANTEC developed the architecture of MIDIC’s main part.
Task 4. **Development of VDL-Based Interpolator (Objective 4).** This task was devoted to the design and optimization of the internal DLLs and delay lines in order to achieve the required digitization accuracy of 1\(\text{ps}\).

Task 5. **Development of CNT and Code Converter (Objective 4).** Though this task was initially intended for the FIFO design, ADSANTEC has replaced the development of this standard block by the preliminary design of more critical parts of TIC including the clock period counter (CNT) and code converter.

Task 6. **Preparation of the Final Report.** This task is devoted to the preparation of the final report that includes the Phase I activity results.

### 3.2. Phase I Performance Schedule

The tasks listed above were performed in accordance with the schedule shown in Table 1.

**Table 1. Project Schedule.**

<table>
<thead>
<tr>
<th>ID</th>
<th>Task Name</th>
<th>Month 1</th>
<th>Month 2</th>
<th>Month 3</th>
<th>Month 4</th>
<th>Month 5</th>
<th>Month 6</th>
<th>Month 7</th>
<th>Month 8</th>
<th>Month 9</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IC Fabrication Technology Selection (Objective 1).</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADSANTEC</td>
</tr>
<tr>
<td>2</td>
<td>MIDIC Architecture Development (Objective 2).</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>ADSANTEC, ORNL</td>
</tr>
<tr>
<td>3</td>
<td>TIC Architecture Development (Objective 3).</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADSANTEC, ORNL</td>
</tr>
<tr>
<td>4</td>
<td>Development of VDL-Based Interpolator (Objective 4).</td>
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<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADSANTEC</td>
</tr>
<tr>
<td>5</td>
<td>Development of CNT and Code Converter (Objective 4).</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>ADSANTEC</td>
</tr>
<tr>
<td>6</td>
<td>Preparation of the Final Report.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADSANTEC, ORNL</td>
</tr>
</tbody>
</table>
4. Phase I Work Results

During Phase I, ADSANTEC developed the architecture, major blocks, and performed computer simulations of the MIDIC system. The achieved results have proved the feasibility of the selected approach and demonstrated the possibility to achieve the time interval digitization accuracy of 1 ps.

All technical Objectives and Tasks have been accomplished. The results of Phase I are summarized below.

4.1. Technological Process Selection (Objective 1, Task 1)

The main project’s requirement of a 1 ps accuracy dictates the selection of the most advanced technological process for the ASIC design and fabrication. This kind of performance can be achieved with the SiGe BiCMOS technologies offered by several foundries including IBM, Jazz Semiconductor, Atmel, SG Thomson, and some others.

The SiGe BiCMOS technology, which achieved its first manufacturing qualification in 1996, is now in its fourth lithographic generation of development, as shown in Table 2.

<table>
<thead>
<tr>
<th>Generation</th>
<th>$f_T$, GHz</th>
<th>$L_G$, µm</th>
<th>Metal Type</th>
<th>Process</th>
<th>Foundry</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>35</td>
<td>0.5</td>
<td>Al</td>
<td>5S</td>
<td>IBM</td>
</tr>
<tr>
<td>2</td>
<td>50-60</td>
<td>0.35 / 0.5</td>
<td>Al</td>
<td>5HP</td>
<td>IBM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6HP</td>
<td>IBM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SiGe60</td>
<td>Jazz</td>
</tr>
<tr>
<td>3</td>
<td>90-120</td>
<td>0.18 / 0.35</td>
<td>Al / Cu</td>
<td>7HP</td>
<td>IBM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SiGe120</td>
<td>Jazz</td>
</tr>
<tr>
<td>4</td>
<td>200</td>
<td>0.13 / 0.25/ 0.35</td>
<td>Al / Cu</td>
<td>8HP</td>
<td>IBM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SBC13</td>
<td>Jazz</td>
</tr>
</tbody>
</table>

This class of technology integrates high-performance HBTs with a state-of-the-art CMOS technology. Key technology characteristics of the four generations have been reported by IBM [5-8]. All generations of the BiCMOS technologies are compatible with an associated CMOS technology in terms of devices, metallization (interconnects), and ASIC design flow [9].

The SiGe technology is evolving very rapidly and has of today reached a point where it is comparable with the best of the III-V technologies. With the recent announcement of SiGe HBTs having a peak cutoff frequency of $f_T>300$GHz [10], and complimentary (nnp and pnp) SiGe HBTs having peak $f_T$ values above 180GHz and 80GHz respectively [11], the application space for SiGe technologies now includes a wide variety of analog and RF mm-wave applications.

The most advanced SiGe technologies commercially available in the US are listed in Table 3. Both IBM and Jazz offer a comparable service and technology level, as well as similar lists of components.
Table 3. Parameters of SiGe Technologies.

<table>
<thead>
<tr>
<th>Foundry</th>
<th>IBM</th>
<th>IBM</th>
<th>Jazz</th>
<th>Jazz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>7HP</td>
<td>8HP</td>
<td>SiGe120</td>
<td>SiGe200</td>
</tr>
<tr>
<td>(f_T), GHz</td>
<td>120</td>
<td>205</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>(f_{\text{max}}), GHz</td>
<td>100</td>
<td>285</td>
<td>170</td>
<td>200</td>
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<tr>
<td>(BV_{\text{CEO}}), V</td>
<td>2.0</td>
<td>1.8</td>
<td>2.2</td>
<td>1.9</td>
</tr>
<tr>
<td>(BV_{\text{CEO}}), V</td>
<td>6.4</td>
<td>6.0</td>
<td>7.0</td>
<td>5.5</td>
</tr>
<tr>
<td>(W_{\text{E min.}}, \mu m)</td>
<td>0.2</td>
<td>0.12</td>
<td>0.2</td>
<td>0.15</td>
</tr>
<tr>
<td>(V_a), V</td>
<td>90</td>
<td>-</td>
<td>60</td>
<td>60</td>
</tr>
<tr>
<td>Gain</td>
<td>500</td>
<td>500</td>
<td>140</td>
<td>140</td>
</tr>
</tbody>
</table>

**MOSFET (NFET and PFET)**

<table>
<thead>
<tr>
<th>(L_G) min., (\mu m)</th>
<th>0.18</th>
<th>0.12</th>
<th>0.18</th>
<th>0.13</th>
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<tbody>
<tr>
<td>Other (L_G), (\mu m)</td>
<td>0.36</td>
<td>0.36</td>
<td>0.36</td>
<td>0.36</td>
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</tbody>
</table>

**Other Components**

<table>
<thead>
<tr>
<th>Resistor, (\Omega/\square)</th>
<th>8.1</th>
<th>8.8</th>
<th>5.5</th>
<th>8.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>72</td>
<td>58</td>
<td>21</td>
<td>-</td>
</tr>
<tr>
<td>-</td>
<td>105</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>-</td>
<td>142</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>-</td>
<td>260</td>
<td>340</td>
<td>205</td>
<td>310</td>
</tr>
<tr>
<td>-</td>
<td>1600</td>
<td>1700</td>
<td>1000</td>
<td>890</td>
</tr>
<tr>
<td>MIMCap, fF/(\mu m^2)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2.8/5.6</td>
</tr>
<tr>
<td>MOSCap, fF/(\mu m^2)</td>
<td>2.5</td>
<td>11.3</td>
<td>8</td>
<td>-</td>
</tr>
</tbody>
</table>

| Inductor | Spiral/Line | Spiral/Line | Spiral | Spiral |
| Varactor | Yes | Yes | Yes | Yes |
| Transmission Line | Micro-strip | Micro-strip | No | No |
| Schottky Diode | No | No | Yes | No |
| Metal | Cu / Al | Cu / Al | Al | Al |
| No. of levels | 7 | 7 | 6 | 6 |

The process of technology selection performed by ADSANTEC includes the technology performance evaluation, as well as cost considerations. Due to high attention paid by DOE to the price of the experimental systems, ADSANTEC considered only the processes of the 3rd generation as the candidates for the MIDIC design. The characteristics of NPN HBTs have been compared. Fig. 1 presents the dependence of the HBT’s main parameters on its emitter current in case of a 0.2x0.76\(\mu m^2\) emitter area and for different junction temperatures and process corners.
Fig. 1. $f_t$ and BETA of the 0.76µm Digital HBT in the SiGe120 Process.

Similar plots are shown in Fig. 2 for the similar transistors in the BiCMOS7HP processes.

The investigation of the plots leads to three main conclusions:

1. The worst-case maximum value of the BETA parameter for the 7HP process (~15) is lower than for the SiGe120 (~20) technology.
2. While this BETA value for the SiGe120 process corresponds to the emitter current that also provides the frequency $F_t$ close to its maximum, in case of the 7HP process the $F_t$ maximum is achieved at much higher emitter currents where the worst-case BETA is unacceptably low. The frequency achievable at the maximum BETA is about 60% of its maximum value.

3. The variation of the BETA value for the 8HP process (15-150) is higher than for the SiGe120 technology (20-120), which presents a challenge for the design of high-performance IC products.

Based on the above considerations, ADSANTEC has selected the SiGe120 technology for the MIDIC development. The correctness of this selection is also confirmed by investigations of ADSANTEC’s proprietary CML libraries of basic cells performed under separate SBIR contracts (No. DE-FG02-03ER83597, No. NNG05CA10C). The achievable speed exceeds 13GHz at 2.2mA/cell current level, which provides a reasonable margin compared to the required 10GHz speed of MIDIC [12].

4.2. MIDIC Architecture Development (Objective 2, Task 2)

4.2.1. General Description

A block diagram of the proposed MIDIC system is shown in Fig. 3. It consists of $k \leq 4$ TDC channels, the internal PLL, and an external processor interface (EPI).

![Fig. 3. MIDIC Block Diagram.](image)

PLL converts the low-speed reference clock (CRF) with frequency $F$ generated by an external ultra-stable oscillator into the system’s internal clock (CI) with frequency $M \times F$ and divided clock (CI/N) with frequency $M \times F/N$. 
The system’s operation cycle is initiated by the falling edge of an external reset signal (RES) or internal loss-of-lock (LOL) signal indicating the locking state of PLL. The working edge of the first following start pulse (SRTi) in a certain TDC channel (e.g. number “i”) indicates the beginning of the time interval to be digitized. The end of this time interval is set by the matching working edge of the next stop pulse (STPi). The type of working edge (rising or falling) can be selected by the corresponding edge-selecting (ESi) signals.

The time interval calculator (TIC) represents the specified interval as an output digital code with the bit length defined by the maximum required period of time and the accuracy of its digitization. Based on the interactions with the ORNL staff, ADSANTEC has selected a 16-bit representation of the time interval, which provides the characteristics shown in Table 4 depending on the structure of the system. The intermediate type of MIDIC’s implementation is ideally suitable for the needs of ORNL experimental systems.

<table>
<thead>
<tr>
<th>Type of the system</th>
<th>Accuracy, ps</th>
<th>Maximum interval length, ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>High accuracy</td>
<td>1</td>
<td>65.5</td>
</tr>
<tr>
<td>Intermediate</td>
<td>4</td>
<td>262</td>
</tr>
<tr>
<td>Long interval</td>
<td>10</td>
<td>655</td>
</tr>
</tbody>
</table>

The resulting 16-bit digital code is sent to the current measurements register (CMR) and then to the output interface EPI through the code calibration adder (CCA) and the optional FIFO. During the initial calibration period, the same start and stop signals are sent to all channels, the initial calibration registers in all channels (ICR) are reset to zero, and the output codes represent the same time interval with variations caused by mismatches of the input interconnects. The external processor identifies the required code correction by subtracting the minimum code value from the value for the particular channel, and writes it to the corresponding ICR. This correction is subtracted from the current measurements in CCA thus resulting in the accurate equalization of all channels.

EPI includes \( k \) input interfaces for writing the initial codes and \( k \) output interfaces for uploading the time measurements codes to the processor. The exact types of the interfaces will be finalized during Phase II of this project.

### 4.3. TIC Architecture Development (Objective 3, Task 3)

TIC is the main block of each TDC. The proposed TIC architecture is shown in Fig. 4. It includes the first delay-locked loop (DLL1) with delay step \( \tau_1 \) that controls the operation of the first signal delay line (SDL1), the second delay-locked loop (DLL2) with delay step \( \tau_2 = \tau_1 - \Delta \tau \) that controls the operation of the second delay line (SDL2), an input access control circuit (IAC), a retiming D-type flip-flop (DFF), a compensation delay block (del), two banks of code-locking DFFs, two time code registers (TR1 and TR2), a clock periods counter (CPC), and an output adder / code converter (ADD). DLLs and the associated SDLs incorporate the same internal delay cells with exactly the same loading, which guarantees a constant delay per cell defined by the DLL. The delay lines, the banks of flip-flops, and the code registers represent a fine interpolation block for measuring the clock-to-signal delays within one clock period, while the counter outputs the number of full clock periods corresponding to the measured time interval.
The differential input signals SRT and STP are first pre-processed by IAC that generates a pre-shaped pulse with its rising edge corresponding to SRT’s edge and its falling edge corresponding to STP’s edge. This pulse is further retimed with the internal CI clock to generate a sampled pulse whose length approximates the measured time interval with the closest number of full clock periods. The sampled pulse is sent to CPC to count the exact number of full clock periods in the time interval (T13), as well as to SDL2 that contains $K_{SDL2}$ delay stages. The 1-period uncertainty of the pulse retiming is of no concern because this period will be calculated either by the counter or by the fine interpolator.

The pre-shaped pulse is also delayed to compensate for the retiming process and sent to the input of SDL1 that contains $K_{SDL1}$ stages. The absolute amount of this delay is not important as long as it is not longer than the retiming delay.

The non-retimed edges of the pre-shaped pulse propagate through SDL1 and are latched to the code-locking DFFs by the chasing retimed edges of the same pulse propagating through SDL2. As a result, the first part of each DFF bank is set to logic “1”, while the second part is set to logic “0”. The position of the “1”-to-”0” boundary represents the clock-to-signal delay for the SRT and STP signals in a thermometer code (T11 and T12).

The output adder converts all three codes into a binary representation and calculates the final length of the time interval as TIF=T11+T13-T12. This information is sent to the external processor together with the EOI signal that indicates the availability of the measured data.

4.3.1. IAC block

The block IAC processes two input signals and is designed to perform the following operations:
1. Generate the output logic “0” during the hard reset period defined by the high value of the “RES” signal;
2. Switch to the output logic “1” at the edge of the first input signal (IN1);
3. Ignore possible following signals at the input “IN1” until soft or hard reset;
4. Switch to the output logic “0” at the edge of the second input “IN2” or “RES” signals;
5. Ignore possible following “IN2” signals until the arrival of the next “IN1” signal preceded by either soft or hard reset.
6. Perform soft reset at the edge of the end-of-interval (EOI) signal if the output (OUT) is preset to logic “0”;

The logic structure of the block is shown in Fig. 5. It includes two logic AND gates, four logic OR gates, and two set/reset flip-flops. The first flip-flop performs all operations related to the output signal (1, 2, 4), while the second flip-flop is responsible for the soft reset related operation (3, 6). Operation (5) is performed with the help of a feedback connection from the output to the input of the second AND gate.

4.3.2. Retiming and Delay of the Signal Pulse

The retiming operation is performed by two D-type flip-flops to avoid a non-linear clock-to-data delay representation by a single DFF shown in Fig. 6.

This strategy allows the first DFF an extra clock cycle to stabilize its output signal before the second DFF samples and delivers it to the adjacent circuit blocks. According to Fig. 6, as long as the C-to-Q delay of the first DFF for all clock/data input phase combinations falls under roughly 60% of the sampling clock period (about 60\(\text{ps}\) at 10\(\text{GHz}\)), the total C-to-Q delay is essentially constant. The complete schematic of the retiming circuitry (RET) is shown in Fig. 7. It includes a
set of preliminary buffers followed by two DFFs with set/reset functions (DFF_SR). The flip-flops are designed as two CML latches with ADSANTEC’s proprietary set/reset configuration [13].

**Fig. 7. Schematic of the Pulse Retiming Circuitry (RET).**

The delay of the non-retimed pulse is provided by the block DEL shown in Fig. 8. In order to mimic the delay imposed by the retiming process, DEL includes a similar set of buffers, one DFF and the delay cell “del140u” equivalent to the ones used in DLLs and SDLs. The cell is properly loaded and controlled by the appropriate DLL to match the extra clock cycle of delay introduced by the second retiming DFF.

**Fig. 8. DEL Block.**

To ensure the correct operation of the interpolator block, the delay in the DEL block should never exceed the delay introduced by RET. The simulation results presented in Fig. 9 prove the possibility to achieve the required performance at all possible operational conditions.

**Fig. 9. DLY-to-RET Delay at Nominal (a), Slow (b) and Fast (c) Operational Conditions.**

The plots demonstrate the relative position of signal edges at the output of the first flip-flop in the retiming block (left-side edge) and at the DEL output (right-side edge). The worst-case variation of the relative delay does not exceed 5ps with the DEL output preceding the RET output by 5-10ps.
4.4. Development of VDL-Based Interpolator Architecture (Objective 4, Task 4)

The interpolator is intended for the digital representation of the clock-to-signal delays for the SRT and STP signals. It includes two DLLs and three SDLs incorporating ADSANTEC’s proprietary voltage-controlled delay (VCD) cells and operating with the divided-by-$N$ internal clock $CN$ with a frequency of $F_{CN} = F \cdot M / N$. The first DLL consists of $K_{DLL1}$ VCD cells with a delay value of

$$
\tau_1 = \frac{T_{CN}}{K_{DLL1}} = \frac{1}{F_{CN} \cdot K_{DLL1}} = \frac{N}{F \cdot M \cdot K_{DLL1}}.
$$

The same value for the second DLL is

$$
\tau_2 = \frac{N}{F \cdot M \cdot K_{DLL2}}.
$$

Finally, the main equation for the DLL design looks like

$$
\frac{N}{F \cdot M} = K_{DLL1} \tau_1 = K_{DLL2} \tau_2.
$$

Each SDL incorporates $K_{SDL}$ number of VCD cells that can be calculated as

$$
K_{SDL} > \frac{1}{F \cdot M \cdot \Delta \tau} = \frac{1}{F \cdot M \cdot \Delta \tau}.
$$

This number is defined by the requirement to achieve the delay mismatch in two types of SDLs not less than one period of CI plus the setup time of the retiming DFF. Possible combinations of DLL and SDL parameters are shown in Table 5.

<table>
<thead>
<tr>
<th>$F_{CI}$, GHz</th>
<th>$\tau_1$, ps</th>
<th>$K_{DLL1}$</th>
<th>$N$</th>
<th>$F_{CN}$, GHz</th>
<th>$K_{DLL2}$</th>
<th>$\tau_2$, ps</th>
<th>$\Delta \tau$, ps</th>
<th>$K_{SDL}$</th>
<th>VCD cells</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.0</td>
<td>100</td>
<td>19</td>
<td>19</td>
<td>0.53</td>
<td>20</td>
<td>95</td>
<td>5.0</td>
<td>22</td>
<td>105</td>
<td>105x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>29</td>
<td>29</td>
<td>0.34</td>
<td>30</td>
<td>96.7</td>
<td>3.3</td>
<td>33</td>
<td>158</td>
<td>158x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>39</td>
<td>39</td>
<td>0.26</td>
<td>40</td>
<td>97.5</td>
<td>2.5</td>
<td>44</td>
<td>211</td>
<td>211x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>49</td>
<td>49</td>
<td>0.2</td>
<td>50</td>
<td>98</td>
<td>2.0</td>
<td>55</td>
<td>264</td>
<td>264x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>99</td>
<td>99</td>
<td>0.1</td>
<td>100</td>
<td>99</td>
<td>1.0</td>
<td>110</td>
<td>529</td>
<td>529x</td>
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<td>100</td>
<td>8</td>
<td>4</td>
<td>2.5</td>
<td>9</td>
<td>44.4</td>
<td>5.6</td>
<td>20</td>
<td>77</td>
<td>144x</td>
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<td>100</td>
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<td>8</td>
<td>1.25</td>
<td>17</td>
<td>47.1</td>
<td>2.9</td>
<td>38</td>
<td>147</td>
<td>294x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>24</td>
<td>12</td>
<td>0.83</td>
<td>25</td>
<td>48</td>
<td>2.1</td>
<td>53</td>
<td>208</td>
<td>416x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>48</td>
<td>24</td>
<td>0.42</td>
<td>49</td>
<td>49</td>
<td>1.0</td>
<td>110</td>
<td>427</td>
<td>854x</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>100</td>
<td>2</td>
<td>2.5</td>
<td>9</td>
<td>44.4</td>
<td>5.6</td>
<td>40</td>
<td>137</td>
<td>274x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>16</td>
<td>4</td>
<td>1.25</td>
<td>17</td>
<td>47.1</td>
<td>2.9</td>
<td>76</td>
<td>261</td>
<td>522x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>24</td>
<td>6</td>
<td>0.83</td>
<td>25</td>
<td>48</td>
<td>2.1</td>
<td>106</td>
<td>367</td>
<td>734x</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>48</td>
<td>12</td>
<td>0.42</td>
<td>49</td>
<td>49</td>
<td>1.0</td>
<td>220</td>
<td>757</td>
<td>1514x</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>12</td>
<td>3</td>
<td>3.3</td>
<td>13</td>
<td>23.1</td>
<td>1.9</td>
<td>58</td>
<td>199</td>
<td>796x</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>24</td>
<td>6</td>
<td>1.7</td>
<td>25</td>
<td>24</td>
<td>1.0</td>
<td>110</td>
<td>379</td>
<td>1516x</td>
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<tr>
<td></td>
<td>25</td>
<td>16</td>
<td>2</td>
<td>2.5</td>
<td>17</td>
<td>23.5</td>
<td>1.5</td>
<td>147</td>
<td>474</td>
<td>1896x</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>24</td>
<td>3</td>
<td>1.7</td>
<td>25</td>
<td>24</td>
<td>1.0</td>
<td>220</td>
<td>709</td>
<td>2836x</td>
</tr>
</tbody>
</table>

The optimal combinations for the achievable accuracy of 1ps and 4ps are marked with red and green respectively.
4.5. Development of DLL (Objective 4, Task 4)

Top-level schematics of the DLLs can be seen in Fig. 10.

Both DLLs utilize the low-speed CN clock signal as its working signal, incorporate a set of VCD cells with realistic loading, and employ a special early/late phase detector (PD). For simulation purposes, DLL1 employs 99 stages while DLL2 employs 100 stages. It is imperative that the delay stages in each DLL are loaded with dummy cells that mimic the loads of the delay cells in the corresponding SDLs. The dummy emitter follower stages in DLL2 need to be loaded by dummy DFF cells to exactly mirror the conditions seen by the delay cells in SDL2. Matching of the loads seen by the delay cells in SDL1 is accomplished by the dummy buffer cell in DLL1. Since the output load driven by the delay cells in SDL2 is larger than the load seen by the delay cells in SDL1, different versions of the delay cell are used in each block (i.e. “del140u” for SDL1 and DLL1 and “del140u_1” for SDL2 and DLL2).

The phase detector shown in Fig. 11 accommodates the delay variation within the range of 2 CN clock periods without locking to the double or half of the required delay.

It includes two DFFs that latch the half-delayed and fully delayed clock signals with falling edges of the input clock. The corresponding timing diagram is shown in Fig. 12.
The top signal (Line 1) represents DLL’s input clock signal. The rest of the plot is divided up into 4 different sections with each section containing the maximum (dotted line) and minimum (solid line) possible outcomes of the two delayed signals DDP,N<0> and DDP,N<1> within a certain clock period range. The four delay ranges (0.5-1.0, 1.0-1.5, 1.5-2.0, and 2.0-2.5 times the input clock period) result in latching of different output codes shown at the right-hand side of the plot. As an example, if the input clock signal is delayed within the range of 1.5 to 2.0 clock periods, then the sampled values of “DDP,N<0>” and “DDP,N<1>” produce the output code “00” as shown on Lines 6 and 7 of the timing diagram.

The resulting 2-bit code indicates the value of the total delay and dictates the required delay adjustment as shown in Table 6.

### Table 6. PD’s Output Codes.

<table>
<thead>
<tr>
<th>Code</th>
<th>Total delay value</th>
<th># of the half-period</th>
<th>Delay adjustment function</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>1.5 – 2.0 CN periods</td>
<td>0</td>
<td>Decrease</td>
</tr>
<tr>
<td>01</td>
<td>1.0 – 1.5 CN periods</td>
<td>2</td>
<td>Decrease</td>
</tr>
<tr>
<td>10</td>
<td>0.5 – 1.0 CN periods</td>
<td>1</td>
<td>Increase</td>
</tr>
<tr>
<td>11</td>
<td>0 – 0.5 or 2.0 – 2.5 CN periods</td>
<td>0 or 4</td>
<td>Increase or Decrease</td>
</tr>
</tbody>
</table>

As can be seen, the “11” code is not defined uniquely. The selection of the corresponding function depends on the delay variation range defined by the parameters of the VCD cell.

The schematic of the proprietary VCD cell “del140u” is shown in Fig. 13. The two-level CML cell consists of a main current switch (Q2 and Q4) loaded with a cross-coupled transistor pair (Q103 and Q104). About one half of the cell’s tail current is steered between the current switch...
(less delay) and the cross-coupled pair (more delay) through the bottom-level current switch (Q96 and Q97) by a differential control signal at the input pins “crp/crm”. The linear delay control function within the range of $400\text{mV}$ is achieved by insertion of emitter degeneration resistors R127 and R143.

![Fig. 13. Schematic of VDL Cell.](image)

Table 7 details the delay values of the VCD cells loaded with either CML buffers or emitter followers and DFFs for different process corner, temperatures, and control voltages.

<table>
<thead>
<tr>
<th>Process Corner</th>
<th>Operational temperature, °C</th>
<th>Delay of the cells “dell140u_1”, ps</th>
<th>Delay of the cells “dell140u”, ps</th>
<th>Delay range, CN periods</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow</td>
<td>125</td>
<td>Min. 96 Typ. 134 Max. 246</td>
<td>Min. 98 Typ. 138 Max. 270</td>
<td>0.8 – 2.7 (&lt; 4 halves)</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>Min. 90 Typ. 123 Max. 233</td>
<td>Min. 90 Typ. 128 Max. 260</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-25</td>
<td>Min. 84 Typ. 114 Max. 222</td>
<td>Min. 85 Typ. 119 Max. 254</td>
<td></td>
</tr>
<tr>
<td>Nominal</td>
<td>125</td>
<td>Min. 70 Typ. 98 Max. 181</td>
<td>Min. 72 Typ. 98 Max. 203</td>
<td>0.6 – 2.1 (&lt; 4 halves)</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>Min. 65 Typ. 90 Max. 171</td>
<td>Min. 66 Typ. 94 Max. 190</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-25</td>
<td>Min. 61 Typ. 83 Max. 163</td>
<td>Min. 62 Typ. 87 Max. 179</td>
<td></td>
</tr>
<tr>
<td>Fast</td>
<td>125</td>
<td>Min. 50 Typ. 69 Max. 130</td>
<td>Min. 51 Typ. 72 Max. 145</td>
<td>0.4 – 1.5 (&lt; 3 halves)</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>Min. 47 Typ. 63 Max. 121</td>
<td>Min. 48 Typ. 66 Max. 133</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-25</td>
<td>Min. 43 Typ. 59 Max. 115</td>
<td>Min. 44 Typ. 61 Max. 127</td>
<td></td>
</tr>
</tbody>
</table>

It can be seen that the variable delay can be both lower than 0.5 of the CI clock period (values marked in blue) and higher than 2.5 clock periods (values marked in red). At the same time, these extreme values appear at different process corners. The total delay variation range for each particular process corner never exceeds 4 halves of the CN clock period though the absolute values are slightly shifted to the higher end. The delay values will be centered during circuit optimization in Phase II of this project.

As can be understood, the “11” code should be associated with the half-period #4 at the Slow and Nominal process corners, but with the half-period #0 at the Fast process corner. The locked
codes are logically processed by the following AND gate or simple buffer depending on the “11” code association. The selection is performed by a standard selector cell available in ADSANTEC’s CML library and controlled by a special signal. Two different approaches can be employed to correctly choose the “11” code association and generate the corresponding control signal. Within the first approach, this can be achieved by an external control signal. The second method uses additional circuitry to measure the minimum delay in order to determine the identity of the process corner.

The locked codes are then applied to the inputs of a differential charge pump “chgpmp” with an on-chip low-pass filter. The charge pump’s current is kept low in order to minimize the size of the filter. The resulting integrated error signal is applied to the “crp/cm” inputs of the delay cells in the DLL, as well as in the associated SDLs.

The accuracy of the time interval digitization is directly related to the jitter generated by the DLLs that can be minimized through charge pump and filter optimization. During the Phase I period, ADSANTEC performed simulations of the DLL’s locking process. The simulated shapes of the DLL’s internal signals at nominal conditions are shown in Fig. 14. Fig. 15 demonstrates the output clock eye with a maximum jitter of 0.002UI.

![Fig. 14. DLL Simulated Internal Signals.](image1)

![Fig. 15. DLL’s Output Clock Eye.](image2)
The achievable alignment of the DLL’s input and output clock signals is shown in Fig. 16. It corresponds to less than 1\(\mu\)s error at the delay of 10\(\text{ns}\).

![Fig. 16. AC Simulation Results for DIB-AS.](image)

**4.6. Development of SDL (Objective 4, Task 4)**

The schematic of SDL1 is shown in Fig. 17. It consists of 10 blocks, each incorporating 10 delay cells. SDL2 is very similar in structure except that it only contains 99 slightly different delay cells. The number of cells in the SDLs have been selected equal to those in the DLLs for the simplification of the simulation. The actual required numbers are higher by approximately 10% as discussed in Section 4.4.

![Fig. 17. Schematic of SDL1.](image)

The outputs from the SDL1 blocks drive the data inputs of the two DFF blocks while the signals from SDL2 through emitter followers drive the DFFs’ clock inputs. The sampling results obtained in the DFF blocks are recorded in two registers (TR1 and TR2) for later time code processing. Since these registers only latch their input signals once every measurement cycle, they can be implemented utilizing low-speed DFFs to minimize the system’s power consumption.

**4.7. Development of the Code Converter (Objective 4, Task 5)**

The outputs of the DFF blocks represent the time measurements in thermometer code and need to be converted into their normal binary representations. Converting the raw thermometer codes from the register blocks into their appropriate binary representations decreases the amount of logic circuitry required in the following processing section. An example of a thermometer to
A binary encoder has been designed and simulated with the schematic and results shown in Fig. 18 and Fig. 19 respectively.

**Fig. 18. Schematic of Thermometer to Binary Encoder.**

**Fig. 19. Encoder Simulations: (a) Input Thermometer Code, (b) Output Binary Code.**
The 7-bit to 3-bit encoder block consists of an array of XOR logic gates with their inputs tied to the appropriate input signals. The architecture can easily be expanded to accommodate additional input lines. For every power of two increase in input line density, the number of logic layers in the circuit increases by one. In the example, the input line density is $2^3-1=7$, so the XOR layer depth is 3. The processing latency of the encoder depends on the number of input lines and sizing of the XOR gates. This latency should be kept under one measurement cycle of the TIC, which is possible even with minimum power consumption.

4.8. Development of CNT (Objective 4, Task 5)

A binary counter architecture that is suitable for this project is shown in Fig. 20. The example counter’s size is 8 bits, but can easily be increased in order to accommodate the project’s desired maximum measurement time interval. The simple counter structure includes 8 divide-by-two circuits connected in series by intermediate emitter follower stages. The initial divider is driven by the high-speed clock CI with a frequency of 10GHz. The counter is reset to all zeros before each measurement cycle through the universal input pin “r”. Counting begins when the input SRT pulse sample generated by RET is delivered to the counter’s input. A similar sample of the STP signal terminates the counting operation and freezes the final count code until the counter is reset to all logic zeros in preparation for the next measurement cycle.

![8-bit Binary Counter](image.png)

The counter’s contents can not be written to the adjacent register bank until the final divider in the counter has had sufficient time to produce its correct output value. This delay is an additive function of the individual delays of each divider in the counter. The designed 8-bit counter with a minimized power consumption has a system latency of only $178\text{ps}+1.75\text{ns}=1.93\text{ns}$ as recorded in Fig. 21. The delay of the final version of the counter should not be larger than the delay introduced by SDL1, which is approximately 10ns. The total delay of the counter can be minimized by utilizing higher power divider stages, if necessary.
The schematic of the 8-bit register that records the counter’s final output is displayed in Fig. 22.

Since the register samples only the final state of the counter’s outputs, which takes roughly 2\(\text{ns}\) to become available once counting stops, the DFFs included in the stage are all of minimum power. The input latching signal “storep/storen” is connected to the EOI signal. This signal’s
characteristics ensure that the input values to the register are stable and correct from the counter and that the register records only one counter code per measurement cycle. This same type of register architecture and latching signal can be used for the blocks TR1 and TR2.

Waveforms of the signaling encountered during the counter’s operation can be seen in Fig. 23. The first or top signal on the plot represents the sampled STR signal that starts the counter with a positive signal edge as reflected by the activity seen on the counter’s first output bit as shown on the third line of the plot. The counter continues to run until the arrival of the sampled STP signal edge (second line on the plot). Once the counter is deactivated, the register’s latching signal (last line) does not arrive until 3ns later to ensure that the counter’s delay margin has been satisfied.

4.9. CIT Top-Level Schematic and Simulations

The schematic implementation of TIC is shown in Fig. 24. The differential input signals “srtp/srtn” (SRT) and “stpp/stpn” (STP) drive the input IAC block. IAC’s output signal is sampled by the internal 10GHz clock “cp,cn” (CI) in the RET block and also delayed by the DEL block. The sampled results “cntp/cntn” are sent to both the counter (not included in the schematic) and to SDL2. The delayed version of the signal after the DEL block is sent to the delay line SDL1. The multiple delayed versions of the delayed and retimed signals generated by the stages of SDL1 and SDL2 are routed to two separate banks of DFFs that are both named “dff8u5x100”. The outputs of the DFF banks are sent to two timing registers TR1 and TR2 (not included in the schematic). Latching signals for TR1 and TR2 are provided by the differential output signal “qsdl1p/qsdln” that corresponds to the EOI signal in Fig. 4 and is used to reset IAC after the end of a measurement cycle. The delays of the delay cells in SDL1 and SDL2 are set by DLL1 and DLL2 activated by the low-speed clock “clp/cln”.

Current source reference lines for the CML cells are strategically routed to TIC’s different circuit blocks in such a way that each line is loaded with a similar amount of cells. This load balancing methodology mitigates potential current source differences throughout the system.
Fig. 24. Top-Level Schematic of TIC.

To simulate TIC’s functionality in a reasonable amount of time, DLLs were removed from the test version of the block. The delay control signals from the DLLs were replicated by ideal voltage sources during the simulations. The simulated input pre-shaped pulses are shown in Fig. 25.

Fig. 25. TIC Simulation Results.
A universal or hard reset for IAC was provided by a high logic level at the input “reset”. The measurement cycle was started with a positive edge on the “srtp/srtn” signal and stopped once the positive edge of the “stpp/stpn” signal propagates through the SDL1 block and becomes “qsdl1p/qsdl1n”. In simulations, the stop signal was delayed 1\text{ns} compared to the start pulse which constitutes 10 full periods of the input 10\text{GHz} clock. In this case the output codes for both SRT and STP signals should be equal. Due to the omission of the TR1 and TR2 registers, the timing codes of both the start and stop signals were obtained directly from the DFF banks. As can be seen from Fig. 26, the output codes for both banks are 1111000…0, which proves the required performance of the system.

![Fig. 26. Output Signals from the First (a) and Second (b) DFF Banks.](image)

### 4.10. Conclusions

During Phase I of this project, ADSANTEC has developed the architecture of the proposed multi-channel TDC with sub-picosecond accuracy in the form of a detailed block diagram. The possibility to achieve the required parameters is based on the utilization of the company’s proprietary techniques including:

1. Utilization of the same data path for both start and stop signals;
2. Utilization of the same signal for activation of the clock period counter and delay interpolator;
3. Utilization of a proprietary high-speed CML library in the advanced SiGe120 technology;
4. Utilization of a balanced dual-voltage reference structure and matching equivalent loads for all critical cells;
5. High-accuracy DLLs and SDLs based on the proprietary VCD cells.

All critical blocks of the developed system have been designed using the advanced SeGe120 BiCMOS process that helps to achieve the required high operational speed (up to 10GHz) at a low level of power consumption.

The detailed transistor-level simulations of the developed critical blocks performed over the worst-case operational conditions (process variation, temperature, supply variation) have proved the feasibility of the selected design approach. The accuracy of 1ps has been achieved in realistic computer simulations of DLLs and SDLs using the delay cells with a power consumption of less than 300µW/cell.

In general, the MIDIC system is ready for the final design and optimization, followed by the ASIC layout and fabrication.

5. Technical Activities

5.1. Recent Technical Activities

Recent technical activities have been focused on the finalization of MIDIC’s architecture and schematic implementation of its most critical blocks. Based on the detailed discussions with the ORNL representatives during the meeting held at Oak Ridge on February 26-27, 2007, as well as detailed computer simulations, ADSANTEC has introduced some principal improvements into MIDIC’s block diagram, which target the achievement of a maximum possible accuracy. Further simulations confirm the feasibility of a 1ps digitization accuracy for time intervals in access of 65ns.

5.2. Future Technical Activities

Based on the results of the Phase I investigations, ADSANTEC plans to finalize MIDIC’s architecture and the structures of its critical blocks at the beginning of Phase II. Following the request of ORNL, the final design will include up to 4 channels with the accuracy up to 1ps. The initial part of Phase II will be also used for the definition of the required output interface and data exchange protocol.

The complete system design will also include a phase-locked loop (PLL) for the reference clock multiplication. A version of the required PLL was developed during other SBIR programs and will be used for the final design on MIDIC during Phase II of this program.

The results of the architectural and schematic design will be used for the ASIC’s layout design. The required high operational frequency of the system dictates a multi-step approach to the chip implementation. The first step will include the initial flour planning of the chip and preliminary layout of all blocks. Parasitic components will be then extracted and included into MIDIC’s schematics for the final simulations. The next step will include layout corrections and
optimization based on the simulation results. The finalized layout will be submitted to Jazz Semiconductor for fabrication within an MPW program.

ADSANTEC plans to develop the system’s test plan and perform the required tests before the end of Phase II.

6. Commercialization Activities

The developed TDC with extremely high accuracy can find applications not only in Physics experiments performed by National Laboratories, but also in the commercial world. Its potential applications include radar systems, collision avoiding devices for military and commercial aircrafts, a variety of NASA scientific applications, including space ship landing and docking electronics and mini and nano satellites, missile defense agency programs for anti-missile defense, measurement instrumentation, and others. The compact size, high resolution, and low cost of the developed ASIC will be very attractive to the automotive and avionics (commercial jets) industry and will greatly improve traffic safety.

The novel TDC will be a key component for the next generation of Proton Imaging Medical Diagnostic equipment, including Proton Radiography and Proton Emission Tomography since it guarantees significant advantages in analog signal processing performed by the complex medical instruments. ADSANTEC strongly believes that both the developed ASIC and the complete system will be very useful for military and commercial applications. The company has a preliminary agreement with Gamma Medical Inc. at Northridge, CA about the IP integration into their medical diagnostic equipment.

The innovative MIDIC can be also integrated into the network test equipment. According to Frost & Sullivan, the ADC/TDC based measurement instrumentation market is currently estimated to be about $4.5B. Due to the present-day market conditions, ADSANTEC strongly believes that the proposed PSoC, PSiP, or PSoB approach will attract interest of outside investors.

The novel MIDIC concept will improve the accuracy, resolution, power consumption, and complexity of the future DOE detector systems. This technology will be a critical part for the next generation of NPEs, which will be performed by ORNL and other DOE research facilities, as it was stated at the joint ADSANTEC/ORNL meeting on February 26-28, 2007 at ORNL.

7. References


