17th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes

Workshop Proceedings

Proceedings

NREL/BK-520-42056

August 2007

Workshop Chairman/Editor: B.L. Soporì

Program Committee:

M. Al-Jassim, J. Gee, J. Kalejs, J. Rand,
T. Saitoh, R. Sinton, M. Stavola, R. Swanson,
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Vail Cascade Resort
Vail, Colorado
August 5–8, 2007

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TABLE OF CONTENTS

Title/Author(s):	Page
<i>Silicon Workshop: "Expanding Technology for a Future Powered by Si Photovoltaics</i> Bhushan Sopori	1
<i>Origin and Structure of Electrically Active Intra-Grain Defects in Multicrystalline Silicon for Solar Cells</i> Michio Tajima, Hiroki Sugimoto, and Kiyoto Araki	2
<i>Formation of Spherical Si by Seeding Crystallization Technique in High-Speed Dropping and Improvement of the Performances of Spherical Si Solar Cell</i> Zhengxin Liu, Koichi Asai, Takehiko Nagai, Atsushi Masuda, Mikio Murozono, and Michio Kondo	8
<i>Relationship of Intrinsic Luminescence to Recombination Lifetime in Single-Crystal Silicon Wafers</i> R. K. Ahrenkiel, S. W. Johnston, and P. Dippo	12
<i>Towards Zero Kerf Loss: Using Laser Induced Cleavage</i> Stephen C. Baer	20
<i>Analysis of Stresses During Handling and Transport</i> Xavier F. Brun and Shreyes N. Melkote	26
<i>In-Line Crack Detection in PV Silicon Wafers: Resonance Ultrasonic Vibrations Approach</i> W. Dallas, A. Monastyrskyi, O. Polupan, and S. Ostapenko	34
<i>Strength of PV Silicon Wafers – Fracture Mechanics Approach</i> P. Rupnowski and B. Sopori	44
<i>Electrical Characterization of n-type Crystalline Si/Amorphous Si:H Structures</i> Yutaka Hayashi	49
<i>Current Status and Future of Global Polysilicon Production</i> Richard Winegarner	53
<i>Laser-Processing for High-Efficiency Solar Cells</i> P. Engelhart, S. Hermann, T. Neubert, R. Grischke, N. P. Harder, and R. Brendel	57
<i>Understanding Shunting Mechanisms in Silicon Cells: A Review</i> O. Breitenstein	61

Advances in Thin Film Crystalline Silicon Solar Cells	71
Armin G. Aberle	
Thin Solar Cells: Issues and Processing for High-Efficiency	79
G. Agostinelli, P. Choulart, Y. Ma, and Guy Beaucarne	
Scanning Tunneling Luminescence of Large-Grained Polycrystalline Silicon Thin Films	87
Manuel J. Romero, Charles W. Teplin, Chun-Sheng Jiang, and Mowafak M. Al-Jassim	
Fundamental Mechanisms in Fire-Through Contact Metallization of Si Solar Cells: A Review	93
Bhushan Sopori, Vishal Mehta, Przemyslaw Rupnowski, Manuel Romero, Helio Moutinho, Didier Domine, Bobby To, Robert Reedy, Mowafak Al-Jassim, Aziz Shaikh, Nazarali Merchant, Chandra Khadilkar, Dave Carlson, and Murray Bennet	
Advanced Metallization for Crystalline Silicon Solar Cells	104
A. Mette, A. Filipovic, M. Hörteis, O. Schultz, D. Pysch, P. L. Richter, C. Schetter, and S. W. Glunz	
Department of Energy's Solar America Initiative (SAI) – Briefing for Crystalline Silicon Workshop	112
Jeffrey Mazer	
High-Efficiency Si Solar Cell Processing Requirement: Why $0.5 + 0.5 \neq 1$ (i.e., >3)	116
Bolko von Roedern	
Interaction of Hydrogen With Extended Defects in Si	121
Joerg Weber	
Introduction of H into Si from a SiN_x Coating: Role of the SiN_x Density and the Si/SiN_x Interface	122
S. Kleekajai, C. Peng, Michael Stavola, V. Yelundur, K. Nakayashiki, A. Rohtagi, and J. Kalejs	
Silicon Solar Cell Passivation Using Heterostructures	130
S. Olibet, E. Vallat-Sauvain, C. Ballif, L. Korte, and L. Fesquet	
Grid-Competitive Systems Technology A Systems Driven Approach To Cost Reduction	138
Terry Jester	
Accuracy in Solar Cell and Module Measurements and Approaches to Improve Them	145
Keith Emery	
Results of European “Performance” Project on PV Module Testing	151
W. Herrmann, S. Mau, F. Fabero, T. Betts, N. vander Borg, K. Kiefer, W. Zaaiman, and G. Friesen	
Valence-Mended Si(100) Wafers for Improved Cell Efficiency	157
M. Tao	
Structures and Properties of Defects in Cast-Grown Polycrystalline Silicon	161
Yoshio Ohshita, Koji Arafune, Hideaki Kawai, Atushi Ogura, and Masafumi Yamaguchi	
Characterization of Metal Precipitate Located on the Grain Boundary in as-grown Cast mc-Si	165
T. Asano, S. Wakamatsu, H. Ishida, and H. Oda	
Possible Reduction of Recombination Lifetime Due to Compensated Dopants	169
L. J. Geerligs, Daniel Macdonald, and G. Coletti	
An Optical Technique for Measuring Surface Recombination Velocity	174
R. K. Ahrenkiel and S. W. Johnston	

<i>Progress in the Determination of the Stress Optics Coefficient in Thin Polycrystalline Silicon Wafers</i>	179
F. Li, V. Garcia, and S. Danyluk	
<i>“Minicaster” – A Research-Scale Directional Solidification Furnace</i>	184
Vinodh Chandrasekaran, Chenlei Wang, Gregory J. Hildeman	
<i>Hydrogen Incorporation into Czochralski Silicon Wafer and Hydrogen Passivation of Grain Boundary in a Hybrid Orientation (110)/(100) Direct Silicon Bonded Wafer</i>	188
Yongkook Park, Jinggang Lu, and G. A. Rozgonyi	
<i>Intragrain Defect Characterization of Solar Grade Silicon Using Near-Field Optical Beam Induced Current</i>	192
J. K. L. Peters, M. C. Wagener, H. D. Hallen, and G.A. Rozgonyi	
<i>Correlation of Polycrystalline Silicon Wafer Mechanical Properties with Minority-Carrier Lifetime</i>	197
K. M. Youssef and G. A. Rozgonyi	
<i>Passivation of Ideal, High-Angle Grain-Boundaries</i>	201
Magnus Wagener, Mike Seacrist, and George Rozgonyi	
<i>FTIR Studies on Multicrystalline Cast Silicon Edge Slab</i>	205
Ian Witting, Magnus Wagener, Nathan Stoddard, and George Rozgonyi	
<i>Characterization of Polycrystalline Sheet Silicon With Improved Lifetimes</i>	209
Prashant Kulshreshtha, Magnus Wagener, Mason Reed, Oleg Sulima, Ralf Jonczyk, and George Rozgonyi	
<i>Determination of Surface Recombination Velocities for Thermal Oxide and Amorphous Silicon on Float Zone Silicon</i>	214
D. L. Meier, M. R. Page, E. Iwaniczko, Y. Xu, Q. Wang, and H. M. Branz	
<i>Reducing the Concentration of Interstitial Iron in Crystalline Silicon Solar Cells via Low ($\leq 500^\circ\text{C}$) Temperature Annealing</i>	218
Tonio Buonassisi, Matthew D. Pickett, and Robert Sweeney	
<i>Cross-Sectioning Si Solar Cells: Mechanics of Polishing</i>	222
Bhushan Sopori, Vishal Mehta, Nathan Fast, Helio Moutinho, Didier Domine, Bobby To, and Mowafak Al-Jassim	
<i>Surface Photovoltage Technique: Renewed Interest in Si-PV Measurements and Diagnostics</i>	228
Kamau Mbalia, Donovan Bradley, Jesse Appel, Peter Rupnowski, and Bhushan Sopori	
<i>Electrical Investigations On SiC Precipitates Found In Block-Cast Solar Silicon</i>	233
Jan Bauer, Otwin Breitenstein, Michael Becker, and Jörg Lenzner	
<i>Surface Passivation of Heterojunction Solar Cells Using PECV-Deposited Hydrogenated Amorphous Silicon Oxide Layers</i>	237
T. Mueller, S. Schwertheim, Y. Huang, M. Scherff, and W. R. Fahrner	
<i>Simulation of Interface States in α-Si:H/mC-Si Heterojunction Solar Cells</i>	243
Wolfgang R. Fahrner, Maximilian Scherff, Thomas Mueller, and Stefan Schwertheim	
<i>High-Speed Diagnosis of Multicrystalline Silicon Wafers by Photoluminescence Imaging with HF Immersion</i>	249
H. Sugimoto and M. Tajima	

<i>Effect of Surface Passivation on Si Heterojunction and Interdigitated Back Contact Solar Cells</i>	253
U. K. Das, S. Bowden, M. Burrows, M. Lu, and R. W. Birkmire	
<i>Progress In Diffusion-Free Back Contact Solar Cells Fabricated on S-Passivated p-type Si(100) Substrate</i>	258
G. Song, M. Y. Ali, and M. Tao	
<i>Measurement of Dislocation Distribution In Multicrystalline Silicon Ingots Using PVSCAN, a Fast Optical Scanning Method</i>	262
Ning Duanmu, Chandra P. Khattak, Morten Jensen, Rita Glenne, Bhushan Sopori and Peter Rupnowski	
<i>Evaluation on Uniformity of Polycrystalline Silicon Substrates for Solar Cells</i>	267
K. Imai, S. Tanaka, A. Ogura, Y. Ohshita, K. Arafune, F. Kusuoka, H. Kawai, M. Tajima, and M. Inoue	
<i>Large Area EFG (100-cm²) Ribbon Silicon Solar Cells With Screen-Printed Contacts</i>	271
A. Ebong, K. Nakayashiki, V. Upadhyaya and A. Rohatgi	
<i>Impact of Intrinsic Buffer Layer Thickness on the Open-Circuit Voltage in aSi/p-cSi Heterojunction Solar Cells</i>	275
Arnab Das, Dong Seop Kim, and Ajeet Rohatgi	
<i>Fabrication and Analysis of High Efficiency Textured String Ribbon Silicon Solar Cells</i>	281
Saptharishi Ramanathan, Kenta Nakayashiki, Vijay Yelundur, Ajeet Rohatgi, Chris Dube, and Jack I. Hanoka	
<i>a-Si/c-Si Heterojunction for Interdigitated Back Contact Solar Cell</i>	286
Meijun Lu, Stuart Bowden, Ujjwal Das, and Robert Birkmire	
<i>Deep Level Transient Spectroscopy Study of Dislocations in SiGe/Si Heterostructures: The Impact of Fe Contamination and Phosphorous Gettering</i>	290
Jinggang Lu, Yongkook Park, and George Rozgonyi	
<i>Photovoltaic Manufacturing Initiative at Georgia Tech – An Update</i>	294
S. Danyluk, S. N. Melkote, A. Dugenske, F. Li, V. Garcia, X. Brun, and D. Furbush	
<i>Response of n-type mc-Si to Large Variations of Gettering and Hydrogenation</i>	298
Simona De Iuliis and Bart Geerligs	
<i>Role of the Damage Layer in Bulk and Surface Passivation of Silicon Solar Cells by SiN:H</i>	303
Chuan Li, Bhushan Sopori, Rene Rivero, P. Rupnowski, Anthony T. Fiory, N. M. Ravindra	
<i>Application of PV Optics to Si Solar Cell Design</i>	309
Gilda Jimenez and Bhushan Sopori	

Workshop Theme: Expanding Technology for a Future Powered by Si Photovoltaics

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Manufacturing and sales of photovoltaic (PV) cells and modules have been growing at rates exceeding 30% for the last several years. In 2006, PV production reached beyond 1 GW and it is expected to surpass 2 GW in 2007. Currently, silicon is the dominant material for solar cells, but, cells based on other material systems such as a-Si, CdTe, and CIGS are gaining ground rapidly. The recent shortage of polysilicon feedstock has helped to further expedite the commercialization of non-silicon technologies. However, this may be viewed as a positive feature for silicon technologies because the maturing of thin-film PV has filled the slack that could otherwise have dampened the growth because of a lack of available products. The important outcome is that the increased demand for PV will benefit *all* PV technologies.

In the wrap-up sessions of many previous workshops, we have often polled the attendees for their opinions on how long they think Si PV will maintain its dominant role. And the (somewhat biased) response has been that it is expected to remain the main technology for at least 10 more years. As the Si PV industry continues to expand and seeks to maintain its market dominance, it will experience new challenges and growing pains. It will require continued R&D, increasing manufacturing capabilities, market development, and an infrastructure—that is, a pool of scientists and technologists, equipment manufacturers, and services providers. New approaches are also needed to increase cell/module efficiencies, develop energy-efficient processing techniques, develop low-cost sources of feedstock, and minimize encapsulation costs. R&D efforts need to be extended into module technology to lower the module costs.

It is important to keep in mind that expansion of the PV market into new areas and applications will offer specific advantages to different PV technologies. Special features such as radiation resistance, favorable temperature coefficients, aesthetic appearance, and adaptability for building integration can create niche markets for some technologies. Likewise, the impact of concentrator technologies can vary from technology to technology. The terrestrial market will primarily be driven by cost considerations.

This workshop has a number of sessions that will address many of the issues relevant to the continued strength of Si PV in the future. These sessions include crystal growth, impurity defect control, cell processing, and thin-film Si solar cells, module design, and measurements. We have planned discussion sessions to cover major tasks pertinent to the growth of Si PV. In addition, a rump session will explore views on how to meet the cost challenges for grid parity.

This is a very exciting time for PV. A host of new companies are coming on board. Some of these companies are also getting R&D funding from NREL/DOE to explore new designs, processes, and production approaches. My hope is that this workshop will help each one of you sort out the best approaches for successfully moving forward—with your research, your production, or both.

Origin and Structure of Electrically Active Intra-Grain Defects in Multicrystalline Silicon for Solar Cells

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Abstract

Origin and structure of electrically active intra-grain defects in multicrystalline silicon for solar cells were identified by photoluminescence (PL) mapping tomography combined with electron backscatter diffraction pattern measurement and etching/optical microscopy. PL dark patterns were observed in short minority carrier diffusion length regions, and we confirmed that the patterns came from the intra-grain defects. The tomography revealed that the defects have columnar structures extending towards the crystal growth direction. One-to-one correspondences among the PL, crystallographic-misorientation and etch-pit patterns lead us to conclude that the defects are metal-contaminated dislocation clusters which form subgrain boundaries.

1. Introduction

The reduction of electrically active defects is essential to improve the conversion efficiency of solar cells. The intra-grain defects in multicrystalline silicon (mc-Si) crystals for most prevailing solar cells have been successfully detected by the photoluminescence (PL) technique thanks to its great advantages of high sensitivity, high spatial resolution, high speed, noncontact and nondestructiveness [1-4]. Dark PL patterns were observed in the low minority carrier diffusion length region by PL mapping and imaging, and the defects responsible for these patterns are regarded as a serious obstacle to attaining high conversion efficiency. The purpose of the present paper is to identify the origin and structure of the defects. We analyzed the defects by PL spectroscopy and mapping combined with electron backscatter diffraction pattern (EBSP) measurement and etching/optical microscopy.

2. Experimental Technique

The mc-Si wafers used in this study were boron-doped p-type with a resistivity ranging from 1.0 to 1.5 $\Omega\cdot\text{cm}$, a size of 180 x 130 mm² and a thickness of 2.8 mm. They were sliced parallel to the crystal growth direction from an ingot fabricated by a unidirectional solidification technique with slow solidification [5]. Any sawing damage was etched off by HNO₃/HF solution, and then the samples were rinsed in pure water following 5% HF etching. Before the PL measurement, distributions of minority carrier diffusion length were measured by the surface photovoltage technique. We focus on slowly solidified crystals in this paper, and results on rapidly solidified crystals will be reported in a forthcoming paper [6].

The samples were excited by the 532 nm line of a Nd: YVO₄ laser for the PL measurement. We performed PL spectroscopy at room and liquid-He temperatures and macroscopic and microscopic PL mappings at room temperature. Details of the measurement apparatus were described previously [3,4]. We performed PL mapping tomography to investigate the three-dimensional structure of the intra-grain defects. This technique was a repetition of PL mapping and thinning the samples with the HNO₃/HF etching. The repetition was performed four times, and both sides of the samples were characterized by the PL mapping followed by an

Fig. 1. PL spectra from slowly solidified crystal at (a)(b) room and (c)(d) liquid-He temperatures in the (a)(c) long and (b)(d) short minority carrier diffusion length regions.

etching of about 100 μm /side each time. For the tomography, we used blocks of 30 x 30 mm^2 cut from the short diffusion length regions of the wafers. Not only the vertical surfaces of samples parallel to the growth direction, but also the horizontal surfaces perpendicular to it with an area of 30 x 2.8 mm^2 were characterized by the PL mapping.

We performed the EBSD measurement to understand crystallographic orientations and types of grain boundaries. The EBSD image was obtained from the intra-grain defect regions of the horizontal surfaces. An area of 2 x 2 mm^2 was scanned with the pitch of 10 μm , and the maximum resolution of misorientation was about 2 degrees. To assess the distribution of dislocations, the etch-pits of the same area were observed as of the EBSD measurement. Samples were etched with Dash-etching solution for 90 min, and then we observed the etch-pits with a Nomarski-contrast optical microscope.

3. Results and Discussion

3.1 Electrical activity of intra-grain defects

PL spectra from the slowly solidified crystal are shown in Fig. 1: They were measured at (a)(b) room and (c)(d) liquid-He temperatures in the (a)(c) long and (b)(d) short minority carrier diffusion length regions. Only near band-edge emission was observed in the long diffusion length region, while deep-level emission appeared in the short diffusion length region. We plot the intensity of the band-edge emission at room temperature on the wafer together with the diffusion length in Fig. 2. The sample was the latest mc-Si wafers and had a considerably long diffusion length of more than 500 μm [5]; however, there were also regions with quite a short diffusion length. We zoom into the short diffusion length region in Fig. 2(c). Due to the highly spatial resolution of PL mapping, we are able to recognize dark-line patterns [3,4]. Grains can be distinguished by the contrast of background in the PL mappings, and we learned that the dark PL patterns existed in the intra-grain areas. This means that these patterns were ascribable to the intra-grain defects. We found that these defects became the intensively active

Fig. 2. Comparison between (a) distribution of minority carrier diffusion length and (b) macroscopic PL mapping ($185 \times 140 \text{ cm}^2$) of slowly solidified crystal. (c) Microscopic PL mapping on the region marked with a square in (b).

recombination centers and greatly degraded the diffusion length, while the grain boundaries were electrically less active. Strong correlation between the PL mapping and the diffusion length (or lifetime) mapping has been well established [1-4].

3.2 Structures of intra-grain defects

PL mapping tomography was performed to determine the three-dimensional structures of the intra-grain defects. Figure 3 shows part of the results of this mapping tomography on the intra-grain defect region marked with a square in Fig. 2(c): (a), (b), (c) are the microscopic PL mappings on front side of the wafer before the etching, and after the first and second etching, respectively. Gradational dark patterns were observed on the sample before the etching, the gradational direction being along the growth direction. Positions of the patterns changed successively after the etching, shifting to the growth direction each time. Backsides of the sample were also characterized, and the opposite behaviors of the patterns were observed; the gradational direction was opposite to the growth direction and the patterns also shifted to the opposite direction. We found that the direction of the shift corresponded to the gradational direction of the patterns on the same surfaces. From this fact, we believe that the defects had plane-like structures as shown schematically in Fig. 4. If the defects had the plane-like structure,

Fig. 3. PL mapping tomography of intra-grain defect region marked with a square in Fig. 2(c): Microscopic PL mappings on front side of the wafer (a) before etching, and after (b) first and (c) second etching. The wafer was thinned by about $100 \mu\text{m/side}$ each time.

Fig. 4. Schematic illustration of plane-like defects which were observed as gradational dark patterns in PL mapping.

the patterns would shift successively. The depth of defect would also change successively, which created the gradational patterns; shallower defects caused greater degradation of the PL intensity because most of the excited carriers were produced nearby surface of the sample. For these reasons then, the shift directions corresponded to the gradational directions on the same surfaces.

In addition to the PL mapping tomography, the comparison of PL mappings was made between the horizontal and vertical surfaces with respect to the growth direction. The microscopic PL mappings on the vertical and horizontal surfaces of the wafer are depicted in Fig. 5(a). Dark-line patterns were

observed on the horizontal surface; however, there were no gradational patterns. The gradational patterns on the vertical surfaces corresponded well to the dark PL patterns on the horizontal surfaces. From the results of the PL mapping tomography and the PL mappings on the vertical and horizontal surfaces, we synthesized the three-dimensional structures of the intra-grain defects responsible for the dark PL patterns, as shown in Fig. 5(b). We confirmed that the growth conditions affected the size and density of the defects: rapider solidification led to intermittent plane structures with smaller sizes and higher densities [6]. These findings show that the defect structures can be controlled by regulating the growth conditions.

3.3 Origin of intra-grain defects

The origins of the intra-grain defects were analyzed by the EBSD measurement and the etch-pit observation in addition to the microscopic PL mapping, as shown in Fig. 6. Comparison between the microscopic PL and the EBSD crystallographic orientation mappings on the

Fig. 5. (a) PL mappings on vertical and horizontal surfaces of the wafer. (b) Three-dimensional structure of the intra-grain defects responsible for the dark PL patterns synthesized from PL mapping tomography and PL mappings on vertical and horizontal surfaces.

Fig. 6. Comparison between (a) microscopic PL and (b) EBSD crystallographic orientation mappings on horizontal surface of the wafer. Difference of background darkness in the EBSD mapping indicates different orientation, and gray lines show subgrain and $\Sigma 3$ grain boundaries, where the two boundaries were hardly distinguishable in the figure because of the quality the black and white printing. (c) Optical micrograph of etch-pits on identical area marked with a square in (a).

horizontal surface of the wafer is shown in Figs. 6(a) and (b). Difference of background darkness in the EBSD mapping indicates different orientation, and gray lines show subgrain boundaries and $\Sigma 3$ grain boundaries, where the two boundaries were hardly distinguishable in the figure because of the quality the black and white printing. Dot patterns originating from the roughness of sample surfaces were deleted in the figure. We confirmed that the patterns of the $\Sigma 3$ boundaries did not correspond to the dark-line patterns in the PL mapping, but that the subgrain boundaries corresponded well to them. Note that not all subgrain boundaries were observed because of the shortage of angle resolution for the present EBSD measurement. In Fig. 6(b), we believe there were subgrain boundaries with smaller misorientation than 2 degrees at the dark PL pattern regions where the subgrain boundaries were not detected by EBSD. Several researchers have reported the strong recombination activity of the subgrain boundaries by electron beam induced current (EBIC) measurement [7,8]. From these facts, we conclude that the intra-grain defects were ascribable to the subgrain boundaries.

Optical micrograph of the etch-pits on the identical area marked with a square in Fig. 6(a) is shown in Fig. 6(c). At the dislocation clusters, the etch-pits were piled up and looked like sharp lines. PL dark-line patterns corresponded to the sharp lines, which clearly shows that dislocation clusters existed at the dark PL patterns.

We performed low-temperature PL spectroscopy and found that dislocation-related D1-D4 lines [9] appeared in the region where the dark PL pattern was observed, as shown in Fig. 1(d). The D lines were below our detection limit in the region including the $\Sigma 3$ boundaries but not subgrain boundaries and in the region without the $\Sigma 3$ or subgrain boundaries, as shown in Fig. 1(c). The appearance of the D lines in the defect region was reported previously, and its relationship with the metal contamination was discussed [10,11]. The EBIC results have also shown that the metal contamination turns subgrain boundaries into strong recombination centers [7,8]. These findings confirmed for us that the intra-grain defects responsible for the PL dark patterns were the metal-contaminated subgrain boundaries which consist of dislocation clusters.

4. Conclusions

The intra-grain defects responsible for the dark PL patterns in mc-Si crystals reduced the minority carrier diffusion length. The three-dimensional structures of the defects were synthesized from PL mapping tomography, which revealed that they have columnar structures

extending towards the growth direction. Origins of the defects were analyzed by low-temperature PL spectroscopy, EBSD measurement and etch-pit observation, and from the results we concluded that the defects are metal-contaminated dislocation clusters which form subgrain boundaries.

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Formation of spherical Si by seeding crystallization technique in high-speed dropping and improvement of the performances of spherical Si solar cell

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[Abstract] Spherical Si with a diameter of approximately 1 mm was fabricated with the dropping method for solar cell applications. This paper introduces a seeding crystallization technique for the solidification of molten Si droplets. Si, SiC, SiO, SiO₂, Si₃N₄, and boron nitride were used as seeding source materials. They were ejected to molten Si droplets by Ar carrier gas at a specific region in the free-fall tube below the nozzle of the crucible. It was found that the seeding powder ejection caused the solidification to occur at low undercooling. The seeding effect was both determined by the affinity, that is the contact angle, to Si melt and impurity incorporations from the seeding powder. As a result, SiO₂ powder was the best candidate. The approaches for the improvements of spherical Si solar cell performances are also introduced. The highest conversion efficiencies of 12.5% and 11.0% were successfully achieved from single sphere cell and a 19-spheres module under AM1.5, 100 mW/cm² illumination.

1. Introduction

Spherical Si solar cells, in which polycrystalline Si spheres with a diameter of approximately 1 mm are used as emitters, is expected as a promising candidate for saving the Si feedstock and lowering the production cost. This is due to the fact that Si spheres are directly produced from molten Si by dropping through a nozzle in a free-fall tube, namely, the dropping method. Since this method does not contain the expensive processes, such as slicing and polishing, the crystalline Si spheres are ideal for low-cost PV module. However, since the molten Si droplets solidify at a high cooling rate without nucleation sites after being dropped from the nozzle, they rapidly fall into deep undercooling, and the solidification randomly occurs on the surfaces toward the inside. Because the volume of Si increases about 8% upon solidification, Si spheres formed by this method have poor crystallinity, containing high-density grain boundaries, point defects, and dislocations [1].

In this paper, we describe a seeding crystallization technique for the solidification of

molten Si droplets. This method significantly increased the crystallinity and production yield [2,3]. Then, we introduce approaches for the improvements of the performances of spherical Si solar cell.

2. Experimental

Figure 1 shows the schematic of the experimental apparatus used for the dropping method. It consists of a quartz crucible with a nozzle at the bottom, a furnace, a free-fall tube (12.5 m in height and 0.2 m in diameter), a seeding powder supply system and a receiving box. The entire apparatus was evacuated by a rotary pump to 1 Pa, and was backfilled to 1 atm pressure with 5 N pure Ar gas. Scrapped tops of Czochralski ingots of electronic industry were crushed into small bulks to use as source material. It was doped by boron with a resistivity of about 1 Ωcm. The source material was filled in the quartz crucible and melted at 1500°C. After the Si was completely melted, the temperature was decreased to the dropping temperature, typically 1480°C, and pressure was applied upon the Si melt by

inletting pure Ar gas into the crucible, then the Si melt was dropped from the nozzle. To form 1.0-mm diameter Si spheres, the nozzle size was 0.3 mm in diameter and 5 mm in length and the pressure in the crucible was 0.02 MPa. The Si droplets were cooled by the ambient Ar gas and finally collected in the receiving box. Highly heat-resistant Si oil was used as the receiving medium. The dropping rate was about 500 spheres per second. The Si spheres formed under these conditions had a broad size distribution from 0.5 to 1.8 mm and the distribution center was around 1.0 mm. The weight yield of the Si spheres with size from 1.0 to 1.4 mm, which can be used for our solar cell module, was about 50%.

Si, SiC, SiO, SiO₂, Si₃N₄, and boron nitride (BN) were used as seeding source materials. They were ejected to the Si droplets at a selected part using argon carrier gas with a supply system that was set in the free-fall tube. It was located 70 cm below the nozzle of the crucible. To investigate the seeding effect, a 2-wavelengths (730 and 1064 nm) high speed thermometer was used to measure the temperature of the droplets. It was set 15 cm below the center of seeding powder distribution area. For this measurement, we first recorded the temperature without powder ejection, and then start the ejection without stop the dropping. The

Fig. 1. Schematic of the experimental setup for the formation of Si spheres by the dropping method

temperature rise induced by the latent heat release could be observed by this measurement.

3. Results and Discussion

We first used Si powder (1~75 μm) as seeding source material. Fig. 1 shows SEM micrographs of Si spheres formed with and without seeding. They were cross-sectionally polished and etched with Secco etchant. The sphere formed without the seeding has an almost perfect spherical body with a small horn (denoted as horn type), which was caused by solidification from the surrounding surface toward the inside and the extrusion caused by the volume expansion upon the solidification. The horn type has poor crystallinity, containing high-density grain boundaries, point defects, and dislocations [Fig. 2(a)]. In contrast, when the seeding Si powder was ejected to the molten Si droplet, spheres changed into tear-drop-like shape (denoted as tear type). The tear type shows good crystallinity without noticeable grain boundaries and less etch-pits [Fig. 2(b)]. This is due to the effect of seeding powder ejection. The attached powders on the droplet work as nuclei and stimulate the solidification to occur from shallow undercooling, which was practically confirmed by the temperature measurement of the droplets with the thermometer. Fig. 3 shows photoluminescence (PL) spectra of a horn- and a tea-type Si spheres. The PL spectra of the horn type are dominated by the dislocation-related D₃ and D₄ bands. Whereas, for the tear type, these D bands are unclear, only B band and Si intrinsic bands are observed [4]. Lifetime measurements revealed that the lifetime of the tear type was $>2.0 \mu\text{s}$, which was 4 times

Fig. 2. SEM images of Si spheres formed (a) without and (b) with seeding technique after cross-sectionally polished and Secco etch.

Fig. 3. Photoluminescence spectra of Si spheres formed (a) without and (b) with the seeding technique.

higher than that of the horn type ($<0.5 \mu\text{s}$)

However, there were two problems in the seeding with Si powder. One was impurities involved into Si sphere through the powders [3]. Another was that the crystallinity decreased with the increase of the production yield: the number of the grains contained in a sphere increased and the grain size became small, which was caused by multiple attachments of the seeding powder on one droplet [3]. Therefore, it was difficult to improve the yield by seeding with Si powder.

Next, we used SiC, SiO, SiO₂, Si₃N₄, and BN powder as seeding materials. These materials have different contact angle, which means different affinity, to Si melt. As a result, all these powder showed seeding effect, and almost the same yields were obtained under the same conditions [Fig. 4(a)]. However, SiC and SiO powders, which have small contact angle and large affinity to Si melt, showed the same seeding effects as Si powder. In the cases of these powders, the temperature rise of the droplets caused by the latent heat release was not confirmed at low undercooling ($<-50^\circ\text{C}$), implying that Si droplets solidified directly without further fall into a deep undercooling after seeding powder attachment. On the contrary, in the cases of SiO₂, Si₃N₄ and BN powders, the temperature rise of the droplets was always confirmed even at low undercooling. These powders always generated Si spheres with good crystallinity even at high production yield. Considering the purity of seeding powder and the solubility in Si melt, SiO₂ powder was confirmed as the best candidate [Fig. 4(b)].

Fig. 5 shows the yield dependences on the

Fig. 4. Yields (a) and average carrier lifetime (b) of Si spheres formed by seeding with different powders under the same conditions. The upper layer shows the values of contact angle of seeding source materials to Si melt.

size and the density of SiO₂ powder. The density was adjusted by changing the flow rate of Ar carrier gas. It is evident that the yield is not affected by the size of SiO₂ powder. This indicates that seeding effect is mainly determined by the affinity, that is the interfacial energy between the seeding powder and Si droplet. On the other hand, the yield increases with the increase of the flow rate of Ar carrier gas. The maximum of nearly 70% is obtained at high SiO₂ powder density. It was also confirmed that the impurity concentrations and carrier lifetime did not change by seeding with SiO₂ powder.

Next, we introduce approaches for the improvements of solar cell performances. First, we think that a shallow p-n junction should be very important for high efficiency because carrier lifetime of Si spheres is as low as about $2 \mu\text{s}$. However, we found out that only P diffusion at low temperature near 800°C is essential to form a perfect emitter. Fig. 6 shows typical SEM micrographs of the surfaces of Si spheres after P

Fig. 5. The dependences of the yield on (a) size and (b) density of SiO₂ seeding powder.

Fig. 6. SEM micrographs of the surfaces of Si spheres after p-n junction formation by P diffusion at different temperatures. The surface before P diffusion is similar to that of 800°C.

diffusion at temperatures of 860 and 800°C. At temperature higher than 850°C, restructure on the surface occurs. The shape of the restructure changes on the P diffusion temperature. PL measurement also confirmed that defects generated near the surface. We consider this is caused by excess Si atoms generated during P diffusion. These Si atoms are easily trapped by high density kink or step sites on the spherical surface to form localized uniform structures to low the free energy, thus induce vacancies near the surface. A shallow p-n junction formed at 800°C increased the efficiency of solar cell by 2% in contrast to that formed at high temperature of 930°C.

Second, we carried out phosphorus gettering. The process contained P diffusion to form a high concentration P-diffused surface layer and a long time anneal at 600~700°C. It was testified that P gettering was effective to increase carrier lifetime and photo-response of the solar cell at long wavelength region. However, because the P diffusion at temperature higher than 850°C caused restructure on the surface and defects near the surface, it was prefer to limit the P diffusion temperature at near 800°C.

Third, hydrogenation. Prior to the hydrogenation, p-n junction was formed and the surface was etched with dilute HF to remove oxide layer. Then a Si_3N_4 layer was deposited on the surface of Si spheres. This Si_3N_4 layer was removed by etching with H_3PO_4 at temperature 150~160°C after annealed at 700°C for 10 s. This technique also expanded the photo-response of the cell to long wavelength region.

For the solar cell, a semi-concentration reflection module was applied. An F-doped SnO_2 layer was deposited as conductive antireflection layer. The highest efficiencies of 12.5% and 11.0% were achieved from single sphere cell and 19-spheres module under AM1.5, 100 mW/cm^2 illumination (Fig. 7).

Fig. 7. I-V curves of a single-sphere cell and a 19-spheres module under AM1.5, 100 mW/cm^2 illumination. The picture on the left is the schematic of the semi-concentration reflection module.

4. Conclusions

We described a seeding technique for the formation of Si spheres in the dropping method and the approaches for the improvements of spherical Si solar cells. The seeding with SiO_2 powder was effective to form high-quality Si spheres. P diffusion at low temperature near 800°C, P gettering and hydrogenation were essential to increase the efficiency of the solar cell and photo-response at long wavelength region.

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Relationship of Intrinsic Luminescence to Recombination Lifetime in Single-Crystal Silicon Wafers

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ABSTRACT

Intrinsic luminescence is suggested as a method to characterize the minority-carrier lifetime of crystalline silicon. The method is based on the theory that the steady-state intrinsic photoluminescence at 1.09 eV (1.134 μm) is proportional to the minority-carrier lifetime [1,2,3]. We reexamined the basic theory and included the effects of surface recombination and doping. In addition, we measured the band-edge photoluminescence (PL) intensities of a number of single-crystal wafers. The resistivity in the wafer set varied from 1 to 11,000 ohm-cm. We then measured the PL spectra using constant excitation intensity and recombination lifetimes of these wafer at low injection. The lifetimes were measured using resonant-coupled photoconductive decay (RCPCD) [4,5,6] in both air ambient and an iodine/methanol solution. The same procedure was used for the PL spectra. Plots of the measured lifetime versus the PL intensity showed weak correlation between the two quantities in air ambient. This variation is attributed to surface recombination effects. However, there is a positive relationship between the near-bandgap PL intensity and the recombination lifetime for surface-passivated wafers. However, there is considerable scatter in the relationship because of underlying, impurity-activated near-bandgap transitions. Some fundamental physical reasons will be used to explain these results.

INTRODUCTION

Carrier lifetime is critically important in photovoltaic and other electronic technologies. Improved methods of lifetime characterization are an area of intense research activity. Because silicon is the primary material used in current, commercial photovoltaic technology, improved lifetime characterization is an ongoing activity. The standard methods for measuring recombination lifetime in silicon involve several experimental configurations that measure the photoconductive decay rate. These include transient microwave reflection [7] and the quasi-static technique [8]. Several research groups [9,10,11,12] have recently used photoluminescence (PL) spectra as a diagnostic lifetime mapping technique in multicrystalline silicon. Here, we will examine the intrinsic photoluminescence on single-crystal materials that have a wide range of doping densities and will assess the technique as an indicator of carrier lifetime.

Because silicon is an indirect-bandgap semiconductor, the internal quantum efficiencies are extremely small by comparison with direct-bandgap materials such as GaAs. The intrinsic radiative recombination or B-coefficient in silicon is $2 \times 10^{-15} \text{ cm}^3 \text{ s}$ [13], which is about 10^{-5} times less than that of GaAs [14]. Consequently, measurements have produced absolute quantum efficiencies for silicon that vary from 10^{-6} to 10^{-4} . Radiative recombination at defects is accentuated because of the localized absence of translational symmetry and the small band-edge PL intensity. For example, significantly larger (5%) quantum efficiencies have been observed due to PL generated at very deep sulfur and selenium defects [15]. The majority of the defect-produced PL, which arises

from the common shallow donor/acceptor species such as phosphorous and boron, occurs near the band-to-band luminescence. At low temperature, PL spectroscopy is used as a means of defect identification [16]. At room temperature, these PL emissions broaden and the individual components overlap the intrinsic band-to-band process.

THEORETICAL ANALYSIS

The bulk quantum efficiency of any semiconductor can be written as:

$$\eta = \frac{R_r}{R_r + R_{nr}} = \frac{\tau_{nr}}{\tau_{nr} + \tau_r} \quad (1)$$

Here, R_r and R_{nr} are the radiative and nonradiative recombination rates, and τ_r and τ_{nr} are the radiative and nonradiative lifetimes, respectively. In low-injection conditions, the radiative lifetime is given by:

$$\tau_r = \frac{1}{BN} \quad (2)$$

where B is the intrinsic radiative recombination coefficient, which is about $2 \times 10^{-15} \text{ cm}^3 \text{ s}^{-1}$ for silicon. N is the doping or majority-carrier density. Therefore, at a doping density of $1 \times 10^{17} \text{ cm}^{-3}$, the radiative lifetime is about 50 ns and is orders of magnitude larger than the typical Shockley-Read-Hall [17,18] lifetime in solar-grade materials. Therefore, the bulk quantum efficiency can be approximated as:

$$\eta = BN\tau_{nr} \quad (3)$$

Equation 3 shows that the bulk PL intensity is a product of the doping density and the nonradiative lifetime. Therefore, PL map intensity is a product of the doping level and the nonradiative lifetime.

Effect of Surfaces

In most silicon wafers of standard thickness (i.e., 300 μm), the unpassivated surface is a strong component of the nonradiative recombination. To determine the effects of surface recombination on the PL intensity, one must solve the drift-diffusion equations with both bulk and surface components being present. The solution to this problem for an infinitely thick crystal has been developed in the literature [19]:

$$\eta = \frac{BN\tau_{nr}}{1 + SL/D} \left(1 + \frac{SL/D}{1 + \alpha L} \right) \quad (4)$$

Here, S is the front-surface recombination velocity; L and D are the minority-carrier diffusion length and diffusivity, respectively; and α is the absorption coefficient of the incident monochromatic light. At $S = 0$, Eq. 4 reduces to the product of bulk lifetime and doping concentration. Equation 3 is also valid when the thickness of the wafer is much larger than the diffusion length L . When photocarriers interact with both surfaces through diffusion, one can use an approximate expression [20] for the surface lifetime component:

$$\tau_s = \frac{d}{2S} + \frac{d^2}{\pi^2 D} \quad (5)$$

Here, d is the sample thickness and τ_s is the surface contribution to the nonradiative lifetime. The total nonradiative lifetime becomes:

$$\frac{1}{\tau_{nr}} = \frac{1}{\tau_s} + \frac{1}{\tau_b}. \quad 6)$$

This expression can be combined with Eqs. 5 and 3 to give the total quantum efficiency,

$$\eta = \frac{BN}{\frac{1}{\tau_b} + \frac{1}{\frac{d}{2S} + \frac{d^2}{\pi^2 D}}}. \quad 7)$$

In summary, the drift-diffusion equations indicate that the quantum efficiency, or PL intensity, is only proportional to the product of the bulk lifetime and the carrier concentration (Eq. 3) when the surface is passivated.

EXPERIMENTAL RESULTS

The wafers in these studies were obtained from a number of commercial sources. These included both wafer manufacturing companies and electronic companies that use similar wafers in their products. They were grown by both the Czochralski (CZ) and float-zone (FZ) methods. These wafers were chosen to provide a cross section of materials used in the microelectronics and photovoltaic industries.

PL Spectra

The PL data were obtained from a system with an optical multi-channel analyzer (OMA) and two different detector arrays. The first is a silicon-based charge-coupled device (CCD), and the second is an InGaAs array that extends the sensitivity into the infrared region. Several different cw lasers are available as excitation sources, and the chosen laser beam is modulated with a mechanical chopper. The latter allows the subtraction of dark current from the photocurrent by the associated electronics. The measurements reported here were primarily made using a HeNe 632.8-nm cw laser, with an unattenuated power of 18 mW. The wavelength chosen minimized the stray light pickup by the detection system in the near-bandgap wavelength region. A variable-temperature optical cryostat was used to cool the sample to as low as 4.2 K. We also added a sample holder that allowed room-temperature PL measurements in a passivating liquid.

Low-Temperature PL Spectra

The data of Fig. 1 were obtained by cooling three silicon wafers to 4.2 K and measuring the emission spectra with the InGaAs array detector. Sample 23 is a CZ-grown *p*-type wafer that is boron-doped to a level of $1.6 \times 10^{16} \text{ cm}^{-3}$. The room-temperature, low-injection lifetime in iodine/methanol solution is 3.2 μs . Sample 33 is a CZ-grown wafer doped *p*-type to a level of $4 \times 10^{15} \text{ cm}^{-3}$, and sample 36 is a FZ-grown wafer doped *p*-type to a level of $3.6 \times 10^{15} \text{ cm}^{-3}$. The dominant feature in all three spectra is the boron-bound exciton (TO phonons) transition at about 1.09 eV. Because of the limited wavelength resolution of the OMA, we are likely seeing both TO, $m=1$ and TO, $m=2$ modes (1.0930 and 1.0909 eV, respectively) merged into one peak. The second peak at 1.13 eV is the free exciton peak, activated by the TA phonon. Finally, the free exciton peak at ~ 1.16 eV is only observed in very high-purity material; here, it is apparent only in the FZ sample # 36. Although the lifetime varies by more than an order of magnitude in these three

samples, we see very little evidence of lifetime effects in the low-temperature spectral intensity. Plotting the $N \cdot \tau$ product of these samples versus the amplitude of the boron-bound exciton produces no observable correlation. The free exciton band is only observable in the longer-lifetime, FZ-grown sample and is the best correlation between high lifetime and low-temperature spectral properties.

Room-Temperature PL Spectra

The remainder of the work here will focus on room-temperature PL spectra. These data were all obtained using the silicon CCD array detector. This detector has been the basis for most of the current PL-lifetime correlation work.

Figure 2 shows the room-temperature PL spectra of six samples from a variety of sources. The spectra were obtained using a constant excitation-intensity setting for the HeNe (632.8-nm) laser, and there is a large variation in PL intensity. The boron doping levels varied from 3.6×10^{15} to $7.5 \times 10^{16} \text{ cm}^{-3}$ in this sample set. There is structure in the PL spectra, especially on the high-energy side of the silicon bandgap (1.11 eV). These PL data were not normalized to the background doping. The low-injection minority-carrier lifetimes were measured by RCPCD in a passivating, iodine-methanol solution and are shown in the bullets. The weakest PL signal is found in sample 33, which has a lifetime of 33.7 μs . The doping level of this sample is $4.0 \times 10^{15} \text{ cm}^{-3}$. The strongest PL signal is found in sample 35, which has a lifetime of 24.0 μs and a doping level of $7.5 \times 10^{16} \text{ cm}^{-3}$. We see from these data that the PL intensity, without carrier concentration normalization, is not a reliable indicator of bulk lifetime.

Figure 3 shows a bar graph in which the unpassivated lifetime is plotted alongside the integrated PL intensity divided by the doping concentration. There is a correlation between the two parameters, but a considerable amount of scatter. Figure 4 is a plot with the passivated lifetime plotted versus the integrated PL intensity divided by the doping density. The correlation is improved, but there is still a considerable amount of scatter.

We see in Fig. 2 that there is considerable structure in the PL spectra, and several underlying transitions are present. These bands are believed to be impurity-related transitions that overlap the intrinsic band-to-band transition. These transitions are the primary source of scatter seen in the data. Surface recombination effects also contribute to the scatter. Variations in the surface-recombination velocity from sample to sample influence the strength of the PL signal and add to the distortion of the relationship between integrated PL and lifetime.

Summarizing this section, we see that there is a correlation between the PL intensity and carrier-concentration and the minority-carrier lifetime product. The correlation shows a positive trend, but the scatter is too large for accurate determination of carrier lifetime.

PL in Iodine-Methanol Solution

We have measured a larger set of samples in a horizontal sample holder that allows PL measurement in a passivating iodine-methanol solution. The same excitation intensity was used as for the samples measured in air. However, there were two additional loss mechanisms introduced here. One is attenuation of the incident laser beam, and the second is the attenuation of PL signal by the solution. The PL collection efficiency is lowered because of losses at additional optics required to divert the beam into the horizontal sample chamber.

The spectra of three samples are shown in Fig. 5. Sample 36 is a FZ sample that is boron-doped to a level of $3.63 \times 10^{15} \text{ cm}^{-3}$. The passivated lifetime, as measured by RCPCD, is 47.9 μs , and the unpassivated lifetime is 8.9 μs . Curve A is the spectra in solution and curve B is the spectra in air. The ratio of the area of spectra A/B is 1.33, whereas the ratio of the respective lifetimes is 5.4. The difference is likely due, in part, to the optical loss in the solution. Sample 25 is an undoped FZ sample with a passivated lifetime of 455 μs . The background carrier concentration is about $1 \times 10^{12} \text{ cm}^{-3}$ as measured by a four-point probe. The PL spectra of the passivated and unpassivated samples are shown in curves C and D, respectively. The integrated PL ratio is 12 and is again less than the respective lifetime ratios. Sample 23 is a CZ-grown sample boron-doped to $1.8 \times 10^{16} \text{ cm}^{-3}$ and has a passivated lifetime of 3.2 μs . The lifetime is unchanged in air ambient, indicating that the bulk defects completely dominated the lifetime. Curve E is measured in solution and curve F is measured in air. The integrated PL of the latter is about 2.4 times that of the former.

Eight samples were subjected to a similar analysis, and the data are summarized in Fig. 9. The doping ranged from 2×10^{12} to $8 \times 10^{16} \text{ cm}^{-3}$. The carrier concentration in each sample was measured by both a mercury probe and a four-point probe. The PL spectra were measured in the horizontal holder in iodine-methanol solution. The lifetimes were measured by RCPCD in iodine-methanol solution after a cleaning sequence, starting with an HF etch.

The lifetime versus integrated PL divided by carrier concentration are shown in Fig. 6. We show a power law fit of the τ vs. PL/N data. The high-resistivity samples were excluded from the fit because calculations indicated that high-injection conditions were generated by the excitation source. The fit shows that PL/N increases with $\tau^{0.88}$, but there is a significant scatter about the fitting curve. The data show that PL/N is a qualitative indicator of carrier lifetime when the sample surfaces are passivated. The scatter is such as to make unreliable the quantitative determination of lifetime from PL intensity.

DISCUSSION OF RESULTS

Our data show that PL intensity is not a reliable indicator of carrier lifetime unless the samples are passivated. This situation parallels that found for the common techniques that measure lifetime by photoconductive decay. However, in this work, there is a considerable amount of scatter in the data even when the sample is passivated during the PL measurement.

We see from the spectral data that the near-bandgap region contains overlapping peaks in addition to the intrinsic PL. These additional peaks are attributed to impurity transitions. These effects are more pronounced in silicon because of the weak transition probability of the indirect band-to-band process, which requires phonon assistance. Impurities also disrupt local translational symmetry and relax the radiative selection rules. Therefore, the relative influence of impurity transitions is larger in silicon than in direct-bandgap materials. The overlap of impurity-activated transitions with the intrinsic band-to-band transition is the primary source of the scatter seen here. In the case of unpassivated surfaces, the near-bandgap impurity-activated transitions may become stronger than the intrinsic recombination band. Because the radiating impurity is a competitive pathway to electron-hole recombination, the PL intensity will be inversely

proportional to recombination lifetime in this process. Hence, there is a great deal of scatter in the PL-lifetime data in this case.

The surface recombination influences the PL measurement, as it does the photoconductive measurements. Thus, one must perform surface passivation to obtain reliable correlation between lifetime and PL intensity.

CONCLUSIONS

Room-temperature silicon PL luminescence is a useful tool for qualitative analysis in silicon characterization, but it is a limited measurement tool for minority-carrier lifetime. Surface passivation is required for meaningful correlation to be produced. In the case of passivated surfaces, there is considerable scatter in the lifetime-PL correlation. However, there is sufficient correlation for PL mapping to be a useful mapping diagnostic.

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FIGURES

Fig. 1. Sample 23 is CZ-grown *p*-type wafer doped at $1.6 \times 10^{16} \text{ cm}^{-3}$. Sample 33 is a CZ-grown *p*-type wafer doped to $4 \times 10^{15} \text{ cm}^{-3}$. Sample 36 is a FZ-grown, *p*-type wafer doped to $3.6 \times 10^{15} \text{ cm}^{-3}$. The measurements were made at 4.2 K.

Fig. 2. The room-temperature PL spectra of six single-crystal wafers using the 632.8-nm excitation wavelength. The RCPCD lifetimes measured in passivating iodine-methanol solution are also indicated.

Fig. 3. Comparison of the recombination lifetime of unpassivated single-crystal wafers and the integrated PL intensity divided by the doping density. There were six samples used in this study and the complete spectra are shown in Fig. 5.

Fig. 4. Comparison of the recombination lifetime of passivated single-crystal wafers and the integrated PL intensity divided by the doping density. There were six samples used in this study and the complete spectra are shown in Fig. 5.

Fig. 5. The PL spectra of three samples measured in air and in a passivating iodine-methanol solution. Curves A and B are data from a FZ-grown sample that is boron-doped to a level of $3.63 \times 10^{15} \text{ cm}^{-3}$. Curves C and D are data from a FZ sample that is undoped and with a background doping of $2 \times 10^{12} \text{ cm}^{-3}$.

Fig. 6. The integrated band-edge PL of eight single-crystal wafers in iodine-methanol solution versus the passivated lifetime. The integrated PL intensity is divided by the doping density. The two outlying points A and B come from undoped and very high-resistivity FZ wafers and are not included in the data fit. The PL increase is caused by high injection. There is a near-linear dependence of PL/N on the carrier lifetime; however, scatter is still a significant problem.

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Figure 1

Figure 4.

Figure 2

Figure 5.

Figure 3

Figure 6

Towards Zero Kerf Loss: Using Laser Induced Cleavage

Stephen C. Baer

We discuss the proposal that laser induced cleavage of single crystal silicon can produce very thin and large area single crystal silicon wafers, without kerf loss or the need for polishing. The laser causes transient heating of an elongated volume in the interior of the crystal, close and parallel to the end of the growing cleavage crack, generating tensile stresses at that crack end which are always perpendicular to the cleavage plane, and of a magnitude only slightly higher than the threshold for cleavage propagation. Furthermore the cleavage crack end is oriented in a direction that is not in any cleavage plane other than the desired one. In that way, cleavage in undesired cleavage planes is avoided so cleavage is exclusively in the desired plane. To heat the crystal in its interior without heating more superficial or deeper regions, a short-pulsed laser produces light of a wavelength such as 1.25 or 2.4 μm , to which silicon is relatively transparent at low intensities but absorbs at the high intensity beam focus by 2- or 3-photon absorption respectively.

Fig. 1. A side view (left) and perspective view (right) of a silicon ingot in the laser cleaving apparatus described in the text.

Single crystal silicon is difficult to cleave cleanly. According to Suwito et al. (1), the problem is that although the (111) is the primary cleavage plane, the (110) plane is “nearly as good.” For this reason, unless the tensile stress at the growing cleavage end is constantly maintained perpendicular to the desired plane as the cleavage propagates across the plane, the stress may trigger a new cleavage direction in one of the other (111) planes or in a (110) plane. However, by mounting a silicon crystal in a frame that ensured that the stress maintained this

perpendicular alignment throughout the course of the cleavage, and by avoiding any bending of the crystal, Hauch et al. (2) produced featureless cleaved surfaces. Yamada et al. (3) produced clean cleavage perpendicular to the surface of a silicon wafer by focusing a scanned laser-heated spot on the wafer surface near the cleavage crack end, producing tensile stresses that advanced the cleavage.

The Cleaving Setup:

Fig. 1 shows an arrangement intended to use laser-induced heating to produce the stresses required for wafer production. The output beam of a laser is first expanded by an anamorphic beam expander and the expanded beam is then focused by a cylindrical lens to illuminate and thereby heat an elongated volume of the crystal, with an axis near and parallel to the vertex of a notch on the side of the ingot. The vertex of the notch and the axis of the illuminated volume are both in the chosen (111) cleavage plane. The ingot begins as a cylindrical (111) ingot, machined to have a rectangular cross section, oriented so that the notch is 15° relative to the line of intersection between the chosen (111) plane and one of the other (111) planes, ensuring that no competing (111) or (110) plane passes through the advancing crack end. (An alternative process, cleaving on a (110) plane, could begin with a cylindrical (100) ingot machined to have flat (110) sides, and could produce very long wafers.)

Fig. 2. A detail showing the relationship between the notch, the cleavage plane and the illuminated/heated volume, when that volume is in the location for initiating the cleavage. The schematic diagram on the right shows the compressive stress by dotted radial arrows and the tensile stress by solid curved arrows.

Fig. 2 shows how as the illuminated volume in the crystal heats up, the thermal expansion creates radial compressive stress, and tangential tensile stress. The figure shows the

initiation of cleavage at the notch vertex, and one can see that by precisely focusing the beam in relationship to the notch, it should be possible to make the tensile stress almost exactly perpendicular to the desired cleavage plane. The figure also shows that once initiated, the cleavage crack is self-limited, since the tensile stresses weaken closer to the illuminated volume, but maintain the strict perpendicularity. For extending the cleavage, the illuminated volume is moved so maximal tensile stress is always at the new crack end. After the cleavage has advanced far enough, the illuminated volume can be moved to the already cleaved side of the crack end, and scanning is continued until cleavage is complete.

Although the notch is shown on a side of a rectangular ingot, the best place for the notch would on a corner of the ingot, since a shorter length would be required for the cleavage initiation step, which is expected to require greater stresses than cleavage extension, and also the expanding the cleavage end from a very small region will help ensure that it is all in the same plane.

Fig. 3. The slotted objective lens travels down a corner of the ingot on a V-groove, forming initial cleavage cracks at a regular spacing.

The objective lens in Fig. 3, fabricated from silicon, has a 90° V-groove that allows it to slide down a corner of the ingot, perhaps with an immersion fluid to improve imaging. The beam from a laser (not shown) is focused by a cylindrical lens (not shown) into a line, which is imaged by the objective into an illuminated volume in the interior of the crystal, as shown by the top right diagram in Fig. 3. A slot in the objective lets a sharp diamond blade

just nick the corner, while the silicon is under tensile stress from the expansion of the illuminated volume, triggering the formation of a short cleavage crack at that nick, and the crack may be extended a short distance from the corner by a few additional laser pulses, focused at successively greater depths from the corner. A specialized workstation may prepare the ingots with many such starting cracks, and then these prepared ingots may be transported to other workstations for the final cleaving.

Optimal wavelength and pulse parameters:

Silicon is transparent to 1.25 μm light, but when the light is extremely intense, as at the focus of a powerful, ultrashort pulse, the silicon absorbs at this wavelength by a two-photon process (Xu and Denk (4), Ramsay et al. (5)). Thus it is possible, in principle, to choose the pulse width and intensity that will lead to efficient absorption at the beam focus but little or no absorption above and below the focus. An additional constraint in the pulse parameters is that the energy of the pulse must be delivered to the heated volume quickly enough that it does not have chance to diffuse away, destroying the thermal gradients before the resulting stresses can lead to the cleavage, and this appears to mean less than a few tens of nanoseconds for a heated volume a few microns in diameter. With that limitation on the time available to deliver the pulse, the intensity must be sufficient to raise the temperature to an amount able to produce sufficient stresses at the growing crack end.

When a beam is focused to a spot, the total two-photon absorption at an axial distance r from the focal spot decreases approximately with $1/r^2$, leading to very selective absorption in the focal plane. In contrast, when the beam is focused to a line, the total absorption decreases with $1/r$, leading to much less selective absorption at the focal plane. One way of regaining selectivity is to generate the line with many spots presented asynchronously (6). Another solution is to employ three-photon absorption, which with a line focus decreases with $1/r^2$.

Nejadmalayeri, et al. (7) have attempted to inscribe waveguides deep in silicon crystals by using intense pulses at 2.4 μm , which is too long a wavelength to be absorbed by a two-photon process, but can be absorbed by a three-photon process. In their initial experiments, regardless of how deeply in the crystal these authors focused their 2.4 μm beam, waveguides formed near the surface, possibly because at the extremely short pulse durations, even when the beam was spread out at its site of entering the crystal, the intensity was still great enough to lead to three-photon absorption at that entry site. Hopefully, as pulse widths are stretched, reducing the peak intensities, it will be possible to use such three-photon absorption to deliver sufficient heating to the illuminated volume, without significant trapping of the energy in more superficial layers.

Peeling:

If successful, this proposed laser technique would produce a thin wafer with a perfectly flat surface in direct apposition to the matching perfect surface of the parent ingot. Between van der Waals forces pulling the wafer and the ingot together, and atmospheric pressure pushing the wafer against the vacuum of the interface, peeling the new wafer from the ingot may be a challenge. The following methods might promote peeling: 1) Reducing

atmospheric pressure or doing the peeling in an atmosphere of low viscosity gas. 2) Using the depth selectivity of the laser to specifically heat the deeper surface of the wafer near

Fig. 4. Processing thin wafers. a. A piece of adhesive tape able to survive the processing environment is attached to one edge of the wafer. b. The tape connects the wafer to a frame that surrounds the wafer. c. A cross section of the wafer, frame and the taped connections between them. d. A perspective view of the wafer and frame in c. e. The frames with their wafers are inserted into slots in superframes like panes in a window, and the superframes are connected into a fan-fold chain for processing.

an edge, causing curling upwards to generate a gap between the wafer and the ingot, towards which a heated gas jet could be directed, while cooling the wafer surface to maintain the upward curl as peeling continued. 3) Applying ultrasonic energy, which might specifically produce heating in the interface plane. 4) Applying a strip of adhesive tape to an edge of the wafer to pull on the wafer.

Dealing with inclusions:

A large precipitate particle in the desired cleavage plane might prevent completion of a cleavage, and require resurfacing of the ingot to remove the aborted wafer. To minimize the chances of this happening, it would be best to use FZ or MCZ silicon with a minimum of inclusions, in spite of the increased cost, which should be more than made up for by the wafer yield per kg silicon. It is also possible that while cleaving the top layer, the next deeper prospective cleavage plane could be imaged by reflected light confocal microscopy (in the infrared) to visualize any inclusions large enough to be expected to interfere with cleaving. If one were found, then the next layer below the first examined layer would be visualized to see if it was suitable (Baer (5)).

Processing thin wafers:

Current single crystal silicon solar cell processing is based on wafers that are stiff enough to be self-supporting through processing. The much thinner wafers that the present technique should make possible would require additional support, for example by vacuum holders that would travel thorough the production line along with the wafer. Another approach, shown in Fig. 4, is to tape the wafers in frames, which would be transported through a production line, perhaps in a fan-fold arrangement of “superframes,” so the production line could enjoy the economies of roll-to-roll processing. The cross-sectional view c in Fig. 4 shows that both sides of the wafer would be accessible for processes like ink-jet printing.

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Analysis of Stresses During Handling and Transport

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Abstract

A significant challenge in using thinner and larger crystalline silicon wafers for solar cell manufacture is the reduced yield due to increased wafer breakage. At a given process step, wafer/cell breakage depends on the nature and distribution of stresses produced in the wafer/cell due to processing, handling and/or transport and on the presence of defects such as cracks. This paper presents an analysis of the mechanical deformation and stresses generated in thin crystalline silicon wafers due to automated handling and transport using Bernoulli grippers. The total in-plane stress state in the wafer, due to Bernoulli gripping and pre-existing residual stresses, is evaluated using wafer deformation measurements and non-linear finite element analysis. The influence of the maximum in-plane principal tensile stress on the critical crack length necessary for breakage is analyzed using linear elastic fracture mechanics.

1. Introduction

Shortage of silicon (Si) combined with the need to lower the cost of crystalline silicon based solar cells has contributed to the growing use of thinner and larger wafers. However, studies have shown that the use of thinner wafers can lead to unacceptable yields arising from wafer breakage during handling, transport and/or processing [1]. Consequently, it is critical to understand the causes of wafer breakage [2]. Fundamentally, breakage of Si wafers is due to the propagation of cracks present in the wafer during a processing or handling step in solar cell manufacture. Knowledge of crack locations and sizes is therefore required to predict wafer breakage accurately. Several techniques have been developed to detect and quantify cracks in wafers [3-5]. A crack will propagate if a sufficiently large in-plane tensile stress is applied orthogonal to it (assuming Mode I fracture). Thus, it is necessary to evaluate the nature, magnitude and distribution of stresses produced in the wafer/cell during manufacture. This includes residual stresses generated in a prior process step and stresses applied to the wafer/cell by the current processing, handling and/or transport method used in manufacture.

The focus of this paper is on the analysis of mechanical stresses produced in silicon wafers during automated handling and their relationship to breakage. Specifically, the paper analyzes the handling stresses produced in Cz, Cast and EFG wafers of different thickness by a commonly-used automated wafer/cell handling device in the PV industry, namely the Bernoulli gripper. A non-linear finite element analysis is used to evaluate the total distribution of in-plane stress produced in the wafer due to Bernoulli gripping, including any residual stress already present in the wafer, using measured wafer deformation profiles as input. The relationship between the maximum in-plane tensile stress, the corresponding critical crack length and the likelihood of wafer breakage is also discussed.

2. Wafer Breakage

As mentioned earlier, the breakage of crystalline silicon wafers during solar cell/panel manufacture is a function of the stresses applied to the wafer during processing, the residual stresses generated in the wafer due to prior processing, and any structural defects such as cracks/micro-cracks. Wafer handling and transport is a process step that induces mechanical stresses in the wafer. By assuming the principle of linear-elastic superposition of stresses, the total stress in the wafer can be expressed as:

$$\sigma_{total} = \sigma_{applied} + \sigma_{residual} \quad (1)$$

The applied stress depends on the process itself and can be thermal or mechanical while the residual stresses are elastic stresses present in the wafer after the removal of loads applied during a prior process step (e.g. crystal growth, wire-sawing, grinding, etc.).

From the theory of linear elastic fracture mechanics, if a crack is located in an area of tensile stress, its propagation will depend on the following factors:

- magnitude of the tensile stress perpendicular to the crack plane,
- crack geometry (size and shape), and
- fracture toughness K_{IC} of the material (assuming mode I fracture is predominant).

For single crystal silicon (sc-Si) wafers and multi-crystalline silicon (mc-Si) EFG wafers, inherent material anisotropy will lead to different values of K_{IC} depending on the crystal orientation. For mc-Si cast wafers, anisotropy at the wafer level is absent and K_{IC} does not depend on orientation. Table 1 shows the fracture toughness of silicon for different wafers types and orientations as reported in the literature.

Table 1. Critical stress intensity factor [6]

Material	Cleavage Plane	K_{IC} (MPa $\sqrt{m}$)
sc-Si	{100}	0.95
sc-Si	{110}	0.90
sc-Si	{111}	0.82
mc-Si	N/A	0.75±0.06

The stress intensity factor for an internal crack in an infinite specimen is given by:

$$K_I = \sigma \sqrt{\pi l} \quad (2)$$

where σ is the stress and l is the crack length.

The crack will propagate when the stress intensity factor K_I reaches a critical value K_{IC} (also known as the Griffith criterion). The critical tensile stress is then:

$$\sigma_c = K_{IC} (\pi l)^{-0.5} \quad (3)$$

For a given tensile stress level, the maximum critical crack length that is acceptable in the wafer is:

$$l_c = \left(\frac{K_{IC}}{\pi^{0.5} \sigma_c} \right)^2 \quad (4)$$

To minimize wafer breakage and improve yield, it is important to know both the residual and applied stresses in the wafer. From a wafer handling standpoint, for a given residual stress state, the handling control variables must be optimized to lower the applied stresses and minimize breakage.

3. Handling Stresses

In a handling operation, the applied stress is a function of the handling control variables. Mechanical, vacuum and Bernoulli based wafer handling methods are used in the PV industry. While the Bernoulli gripper is one of the more commonly used devices, its capability of handling thin wafers have not been investigated thoroughly. Published scientific research on Bernoulli grippers is limited. Fundamental work reported to date is limited to handling of rigid semiconductor disks used in the IC industry [7, 8].

A schematic diagram of a typical Bernoulli gripper, which basically consists of an air nozzle, is shown in Fig. 1. In this device, a suction force is created between the gripper and the wafer by a radially diverging decelerating air flow. Generally, Bernoulli grippers are used as non-contact end effectors for “gentle handling” and the stand-off distance from the gripper to the handled object is fixed by equilibrium. In the PV industry, the Bernoulli gripper design often consists of soft rubber pads that determine the stand-off distance. Friction between the wafer and pads and the capability to vary the airflow and therefore the

suction pressures on the fly enables faster transport speeds for wafers of varying thicknesses. When handling thin wafers ($\leq 200 \mu\text{m}$), the low pressure created by the radially diverging air flow tends to deform the thin wafer and generate stresses. Neglecting the dynamic effects of the robot motion, the applied stresses are a function of the volumetric air flow rate and the stand-off distance imposed by the pads. It is important to be able to determine the applied stresses in order to adjust the handling control variables to lower the tensile stress levels in the vicinity of cracks and thereby reduce wafer breakage.

Figure 1. Schematic of a Bernoulli gripper

At Georgia Tech, we are currently working on developing models to predict the applied stresses using a combination of a fluid flow model of the Bernoulli gripper and a finite element model of the wafer. A preliminary version of this modeling approach has been presented elsewhere [9]. The model was found to yield reasonably accurate wafer deformation results in most cases, except for the thinnest wafers at large volumetric air flow rates. This was attributed to the lack of consideration of the influence of wafer elastic deformation on the air flow. Improvement and experimental validation of the fluid flow model is currently underway.

As far as residual stresses are concerned, in-plane residual stress measurements on Cz, EFG and cast mc-Si wafers have been performed using a near-infra red polariscope-based system developed at Georgia Tech [10, 11]. At present, these measurements give only the residual in-plane shear stress and not the full state of in-plane stress in the wafer. Thus, it is not yet possible to superpose the stresses as defined by Eq. (1) and evaluate the significance of the residual stress relative to the applied handling stresses.

In the absence of an accurate fluid flow model for the Bernoulli gripper and knowledge of the full state of residual stress in the wafer, experimentally measured wafer elastic deformation profiles are used in this paper to determine the total handling stress via a two step procedure. The first step involves fitting an analytical surface to the measured wafer deformation profiles in order to reduce the measurement noise. The second step involves calculating the handling stress distribution by solving a finite element model of the wafer with the fitted analytical surface imposed as a displacement boundary condition. Since the influence of residual stress is embedded in the measured deformation profiles, its effect on the total stress in the wafer is implicitly included in the calculation. Preliminary results from this two step procedure applied to EFG wafers were presented earlier [12]. In the present work, the material properties and finite element model have been improved and extended to account for different wafer types, thickness and size.

Experimental Setup

The experimental setup used to measure wafer deformation consists of a 4-axis Adept SCARA robot equipped with a Bernoulli gripper for wafer pick up and transport using high-precision and controlled gripping forces (see Figure 2). Sensors used in the setup include an air flow controller to measure and control the volumetric air flow rate in the gripper and a laser-based wafer deformation measurement system (Micro-Epsilon OptoNCDT 1700). This setup is part of an experimental PV cell manufacturing testbed recently established at Georgia Tech [13].

(a) (b)
Figure 2. a) Experimental set-up, b) Bernoulli gripper

The following steps define the wafer deformation scanning procedure using the laser-based sensor. The robot moves the wafer that is being handled to specific locations defining a grid with specified spacing while the laser sensor measures the wafer deformation. The volumetric air flow rate is kept constant during the scanning procedure. Once scanning is complete, the height between the laser and each of the four rubber pads on the Bernoulli gripper is measured. The data is then collected and, utilizing MATLAB, a least-squares reference plane is calculated using the heights measured at the pads. Thereafter, the deformed wafer profile is generated.

Table 2. Wafer characteristics and scan grid spacing specification

Wafer Type	Size	Average Thickness (μm)	# Samples	Grid Spacing (mm)
Cz wafer <100>	125 mm x 125 mm	219 ± 1.2	7	1
Cast wafer	125 mm x 125 mm	256 ± 1.1	10	1
Cast wafer	156 mm x 156 mm	166 ± 6.2	10	1.5
EFG wafer	100 mm x 100 mm	161 ± 5.4	10	1

Experiments were carried out on several silicon wafers as given in Table 1. The average wafer thickness was estimated through weight measurements. Wafers were used as provided by suppliers including some etching to remove surface damage from sawing/laser cutting operations. In each experiment with a given wafer type, the volumetric air flow rate was varied from 30 to 40 liters/min. The stand-off distance between the gripper and wafer was fixed at 3 mm. The measured response was the maximum deformation obtained from the laser scanning procedure.

The influence of volumetric air flow rate on the maximum wafer deformation is shown in Figure 3. It is clear that the maximum deformation increases with air flow rate and, for a given flow rate, is greatest in the thin EFG wafer and smallest in the thick 125 mm cast mc-Si wafer. It can also be seen that an upper limit of wafer deformation exists for the thin EFG wafers as the flow rate is increased. This is a result of the wafer deformation approaching the maximum displacement permitted by gripper and is a function of the particular gripper geometry used in the experiments.

The influence of volumetric air flow rate and wafer type on the wafer deformation contours is shown in Figure 4. Identical conclusions to Figure 3 can be drawn from these plots. In addition, one can see that for all wafer types there is a preferred orientation of the deformation as the volumetric flow rate is increased. Material anisotropy cannot explain this preferred orientation since it appears to be the more or less the same for all wafer types. It is likely that this effect is due to the compliance and imperfections of the rubber pads in the gripper. Further work is needed to clarify this observation.

Figure 3. Influence of air flow rate on maximum wafer deformation

Figure 4. Wafer deformation (in mm) pattern as a function of wafer type and air flow rate.

Modeling Work

Wafer deformation profile

A polynomial regression model was used to fit a surface to the measured wafer deformation profiles in order to represent the wafer deformation by a smooth, continuous and well-defined surface. A good surface fit was obtained using a fourth order regression model with two predictor variables. The regression function for this regression model was:

$$E\{Z_i\} = \beta_0 + \beta_1 x + \beta_2 y + \beta_{12} xy + \dots + \beta_{1111} x^4 + \beta_{2222} y^4 + \beta_{1122} x^2 y^2 + \beta_{1112} x^3 y + \beta_{1222} xy^3 \quad (5)$$

where x and y are the coordinates in the reference plane of the wafer and Z is the out-of-plane deformation. The coefficients β_i were determined using Excel Analysis ToolPak. For all cases the R-squared value was close to 1.

Finite element modeling of wafer stresses

The total distribution of stress produced in the silicon wafer due to handling forces exerted by the Bernoulli gripper and the residual stress present in the wafer were obtained by solving finite element models created using the ABAQUS software. For each wafer type, the silicon wafer was modeled as a thin plate of uniform thickness using thin shell elements (S4, 4-node general purpose shell element for finite strains). A non-linear analysis was used to capture the effects of geometric nonlinearity arising from the large deformation experienced by the wafer during handling. The material properties used for each wafer type are listed in Table 3.

Table 3. Material properties used in the finite element models

Wafer Type	Material Properties	Young Modulus (GPa)	Poisson Ratio	Elastic Stiffnesses (GPa)	Reference
Cz wafer <100>	Orthotropic	N/A	N/A	$C_{11}=165.7$ $C_{12}=63.9$ $C_{44}=79.6$	[14]
Cast wafer	Isotropic	162.5	0.223	N/A	[15]
EFG wafer	Isotropic	168.9	0.279	N/A	[16]

A Fortran subroutine (DISP) was used to define the magnitudes of the out-of-plane displacement (U_z) boundary conditions at all nodes. These displacements are obtained from the surface fitting procedure discussed earlier. In-plane wafer displacements were not restrained except for the center node of the wafer that was pinned to avoid rigid body motion of the wafer ($U_x=U_y=0$).

The results for the different wafer types are summarized in Table 4 where $\sigma_{\max}$ is the maximum in-plane principal tensile stress on the wafer top surface. Note that the stresses tend to switch from tensile to compressive and vice-versa when looking at the bottom surface instead of the top surface of the wafer. The location refers to the location of the maximum in-plane principal tensile stress in the wafer. The critical crack length is calculated using Eq. 4 assuming that a crack is present at the location of the maximum tensile stress. It is important to note that, in the current analysis, the crack is assumed to be perpendicular to the principal stress orientation. As expected, irrespective of the wafer type, an increase in volumetric air flow rate leads to an increase in the tensile stress and a smaller critical crack length for wafer breakage. At the highest air flow rate the principal tensile stress levels are quite high for all wafer types, with the thinnest wafer (EFG) yielding the highest value.

Table 4. Max. in-plane principal tensile stress and critical crack length results

	V (L/min)	K_{IC} Mpa.m ^{0.5}	$\sigma_{\max}$ (Mpa)	Location	l_c (mm)
Cz wafers	30	0.95	5.4	Center	10.037
	35		17.1	Edge	0.984
	40		133.2	Edge	0.016
EFG wafers	30	0.9	42.0	Center	0.146
	35		128.9	Edge	0.016
	40		226.9	Edge	0.005
Cast wafers 125 mm x 125 mm	30	0.75	4.5	Center	8.961
	35		11.1	Center	1.456
	40		118.6	Edge	0.013
Cast wafers 156 mm x 156 mm	30	0.75	8.0	Center	2.784
	35		49.6	Edge	0.073
	40		131.8	Edge	0.010

Figure 5 shows the typical Cz wafer deformation profiles for the lowest and highest volumetric air flow rates tested. The deformation profile and the corresponding maximum in-plane principal stress distribution are seen to change significantly with increase in the air flow rate. Specifically, the location of maximum tensile principal stress shifts from the center of the wafer to the edge. Although the precise reason for this shift is not entirely clear at present, it is thought to be related to the compliance and imperfections of the rubber pads in the gripper.

The implication of the results shown in Table 4 and Fig. 5 is that, for a given wafer type, breakage may initiate either in the center or at the edges depending on the presence, orientation and size of cracks equal to or greater than the critical crack length at the site of the maximum tensile stress. Similarly, if one could guarantee that all cracks present in the wafer are smaller than the critical crack length regardless of their location and orientation, wafer breakage would be avoided.

Figure 5. Typical Cz wafer deformation profile (mm) and maximum in-plane principal stress distribution (Pa) at two volumetric flow rates.

Conclusions

This paper presented an analysis of the mechanical deformation and stresses produced in sc-Si and mc-Si wafers by Bernoulli gripping and the relationship between the handling stresses and possible wafer breakage. The experimental work showed that the air flow rate, wafer type and thickness have a significant effect on the wafer deformation and stresses. For all wafer types, results showed a transition in the maximum in-plane principal tensile stress location from the center to the edges as the air flow rate was increased. The relation between the total stress and breakage was analyzed by calculating the critical crack length. In order to predict breakage, the location and orientation of the crack need to be known in addition to the total stress state (applied stress + residual stresses) in the wafer.

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In-Line Crack Detection in PV Silicon Wafers: Resonance Ultrasonic Vibrations Approach

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ABSTRACT. Resonance Ultrasonic Vibrations (RUV) methodology shows high potential to be adopted for in-line non-destructive crack detection in full-size Si wafers for solar cells as a production tool. In this paper we report recent results and outline technical barriers for RUV system to reject wafers with peripheral cracks with throughput rate matching solar cell production lines of 2.0 seconds per wafer. Finite Element Analyses was used to accurately predict various vibration modes in commercial grade Si wafers and support experimental data.

1. INTRODUCTION

To improve the economics of cell manufacturing, the PV industry requires that a special inspection and quality control tool be developed for integration into the production process. This in-line tool will allow (1) rejection of mechanically unstable Si wafers after ingot cutting before they are introduced into further cell processing, (2) identify wafers with mechanical defects (such as cracks) during production to avoid their in-line breakage, (3) find cracked cells before they will be laminated into modules to avoid panel efficiency reduction and product return from the field. The testing tool must possess the following features at a minimum: (i) high speed data acquisition and analysis, matching the approximately 2 seconds per wafer throughput rate of typical cell lines; (ii) high stability of the hardware performance including wafer loading/unloading and parts movement; (iii) easy integration into a belt conveyor configuration or cell testing station; and (iv) user-friendly algorithm for wafer/cell rejection with a minimum number of false positives.

Various research groups have presented laboratory results of experimental methods for non-destructive crack detection in Si wafers. The most interesting of them are optical and ultrasonic methods such as, optical transmission [1], photoluminescence [2] and electro-luminescence imaging [3], infrared lock-in ultrasound thermography [4], and scanning acoustic microscopy [5]. To our knowledge, none of these techniques completely satisfies all of the specifications listed above for in-line testing and mechanical quality control of Si wafers and solar cells. The optical crack detection system utilizes the transmission of a high intensity flashlight through the wafer and captures the image through optical filters with a CCD camera [1]. Processed wafers with the Al backside coating and final solar cells practically inhibit this form of crack detection, unless the crack penetrates the backside contact. This event has a low probability in practice. Additionally, the cracks in Cz-Si wafers can be closed having a width below the optical diffraction limit of ~ 1 micron. This makes them undetectable in the transmission test. The luminescence imaging employs the fact that under laser excitation or using forward bias, the Si wafer or solar cell emits infrared light due to band-to-band electron-hole recombination [2, 3]. These methods rely on cooled CCD cameras to detect the near-infrared part of the emission. Cracks or defects are expected to reduce minority carrier lifetime therefore reducing luminescence efficiency that can be viewed in the images. Though luminescence methods are fast and non-destructive, other types of defects such as surface scratches and dislocations may interfere and mislead crack identification. Additionally, optical detection methods rely on graphic detection and automation that requires fast image recognition software. In reference [4], the authors proposed using ultrasound vibrations to activate a local heating of the wafers in areas with cracks and image cracks using a near-infrared digital camera. Though this hybrid opto-acoustic approach offers high sensitivity with temperature gradients of tens of degrees, the data acquisition requires minutes due to high lock-in integration time to improve signal-to-noise ratio. Acoustic analysis using the scanning acoustic microscope (SAM) allows ultrasonic mapping of wafers with accurate identification of cracks in a micron's scale [5]. In SAM, the wafers are placed in a tank with deionized water to couple short nano-second ultrasound pulses with the material. Maps are taken in a raster scan method over a period of minutes and above. The cracks are visualized through material discontinuity resulting from the acoustic impedance mismatch due to cracks and sharp variation of the reflected acoustic beam intensity and map contrast. The SAM technique is employed in the current paper to support vibration methodology.

Other types of wafer breakage tests rely on mechanical stressing of the wafer. The wafers are tested by stressing them either using an opposing pin support mechanism as in reference [1] or by passing through rollers [6]. These breakage type tests rely on the fact that micro cracks have been shown to reduce the critical external stress applied to a wafer to cause fracture. Wafers that do not break are considered good and allowed to continue for further processing. These bending or twist tests physically load the wafer to a critical breakage point for undamaged wafers. Another approach uses an optical method which induces stress/strain at predetermined areas of the wafer through concentrated local heating [7]. These types of crack control have evident disadvantages because a critical load is a complicated function of the wafer geometry and crystal type (single versus polycrystalline structure) and have low sensitivity to short mm-length cracks. Solar processing steps (sawing, etching, P-diffusion, antireflection layer coating, contact fringes, and back contact deposition) induce numerous manufacturing flaws that can contribute to a lowering or increasing of the critical load. Additionally, loading the wafer can initiate its breakage in areas with high thermo-elastic stress, which is not acceptable.

We reported on an alternative approach for crack detection in solar grade Si wafers and cells using the resonance ultrasonic vibrations (RUV) system [8, 9]. The RUV method enables fast and accurate crack detection with simple criteria for wafer rejection from solar cell production lines. The RUV system relies on variation of modal vibration characteristics due to physical variations in the wafers caused by cracks. In Cz-Si wafers it has been shown that increased crack length leads to a decrease in peak frequency and an increase in peak bandwidth [8]. Minimum crack length sensitivity is related to the uniformity of the RUV parameters from wafer to wafer within a batch. Typically the RUV system is capable of detecting sub-millimeter length cracks. In this paper we further develop the fundamental aspects of the RUV technique and correlated experimental results on wafers with periphery cracks with Finite Element Analysis (FEA) modeling. Experiments with high-throughput RUV system matching production rate are demonstrated.

2. EXPERIMENTAL SET-UP

Ultrasonic vibrations are induced into an as-cut or processed silicon wafer of symmetrical geometry through a vacuum coupled high frequency piezoelectric transducer beneath the wafer as illustrated in Figure 1. Transducer frequency can be swept in the ultrasonic range from 20 kHz to 100 kHz. Standing longitudinal waves are set up at resonance frequencies with peak positions controlled primarily by the wafer's geometry, size, and material's elastic characteristics. The differing physical attributes of each Si wafer lead to altered resonance mode shapes including peak position, peak bandwidth and peak amplitude. The vibrations are detected using a broadband ultrasonic probe attached with a sensor-controlled force to the edge of the wafer. Stepper motors allow synchronized movement and precise positioning of the wafer and probe for RUV measurements. The entire system is computer controlled and programming devices are operated by Windows-based original software. The RUV unit may be integrated into an automatic belt-type solar cell production line or used as a stand-alone testing system for mechanical quality control.

Figure 1. (a) A schematic of the experimental RUV system;
(b) mutual layout of the transducer, wafer and probe in the RUV setup

The transducer beneath the wafer serves as both a holding stage via the vacuum coupling with the wafer as well as serving its primary purpose of inducing resonance vibrations in the form of standing waves into the wafer. The

acoustic probe transmits the electrical signal to a computer controlled lock-in amplifier allowing detection of mV scale ultrasonic signals with sufficient signal-to-noise ratio. In our experiments, the wafer was excited with longitudinal vibrations and a peak resonance of vibrations was detected at specific frequencies controlled primarily by the wafer's size and material's elastic properties.

When performing RUV experiments with wafers of new sizes or geometries, full spectrum measurements are conducted to locate the exact position of suitable resonance peaks. By exciting the wafers over a wide range of frequencies we can define the natural resonance frequencies. These peaks are characterized by narrow bandwidth, large amplitude, and peak separation. Once the resonance peaks are located further crack analysis is possible on a set of similar wafers. By comparing resonance peak properties, including frequency position, bandwidth, and amplitude, of wafers with similar geometries, crystal defects such as cracks or chips can be quickly detected. The RUV method is capable of fast, precise measurements within seconds. The interval includes wafer loading, data acquisition, analyses and wafer unloading. This high speed of measurement makes the RUV system a potential candidate for in-line crack detection matching the throughput rate of the production line. Scanning Acoustic Microscopy (SAM) was used as a supporting method to visualize cracks with highest resolution of 10 microns.

3. RESULTS

3.1 RUV mode identification

Specific resonance vibration modes were found by first measuring a full spectrum frequency scan on the representative cast and Cz-Si wafers with an illustrative example presented in Figure 2 for a 156 mm x 156 mm cast Si wafer. RUV in square-shaped wafers of different accepted photovoltaic industry standard sizes were measured and their peak positions are summarized in Table 1. Each experimental peak represents a particular vibration mode that is compared with FEA results. FEA parameters for analysis include a size specific mesh with square-shaped 1 mm or 2 mm individual elements. The silicon wafer is modeled as an isotropic thin plate with a Young's modulus of 167 GPa, a Poisson ratio of 0.3, and a density of $2.3 \times 10^3 \text{ kg/m}^3$. Free vibrations of the plate were calculated neglecting the effect of the transducer coupling and acoustic probe contact.

Figure 2. Broad range frequency scan of 156 mm x 156 mm cast Si wafer. Four individual RUV modes are shown. Insert zooms on the #1 mode at ~30 kHz (points) with Lorentzian fit (solid line).

Figure 3 Variation of the resonance peak position of four vibration modes presented in Figure 2 versus edge length of the square shaped wafer. Dotted lines – FEA calculations, dots – experimental data on Si wafers.

Even in this simplified model, we found a close match of the experimental and calculated frequencies (Table 1) in wafers of different sizes. As expected the resonance frequency of a specific mode (f_{res}) shifts upwards with reducing the wafer size (a). It practically obeys a simple relation, such as $f_{\text{res}} \sim a^{-1}$ which is illustrated in Figure 3 in the case of the four vibration modes numbered in Figure 2.

Table 1 Resonance peak frequencies for four vibration modes in Si wafers of different sizes: (a) experimental data, (b) FEA calculations. Calculated frequencies are rounded to the last digit.

Mode #	1		2		3		4	
	Peak Frequency (kHz)							
Wafer Size (mm)	(a)	(b)	(a)	(b)	(a)	(b)	(a)	(b)
103 x 103	42.5	47.6	69.8	69.6	-	103.1	-	135.3
125 x 125	37.3	39.3	57.4	57.4	83.8	84.9	-	111.5
156 x 156	29.7	31.5	45.7	45.9	68.2	68.1	87.4	89.3

To further verify this mode identification and in order to assure that FEA modeling matches the experimental data and provide correct representation of the vibration modes we conducted an experiment to determine the mode shape from a series of amplitude measurements along a wafer's edge. Once the peak vibration frequency of a specific mode was found, the mode shape was analyzed by conducting a single peak scan along one edge of the symmetrical wafer noting the amplitude change from point to point that is consistent with peaks and nodes in the modal standing waveform. The resonance peaks were measured with a step size between 3 and 5 mm to construct a representative mode shape. The change in peak amplitude along the edge of the vibrating wafer was found to be similar to the mode shapes at the respective frequency as predicted by FEA. Some asymmetry of the experimental data can be attributed to angular distribution of the transducer's vibrations.

Two unique resonant modes were analyzed at approximately 30 kHz and 45.6 kHz, that correspond to peaks #1 and #2 respectively (Figure 2) for a 156 mm x 156 mm square shaped cast silicon wafer. Figure 4 demonstrates the correlation between the amplitudes of the experimental data and theoretical FEA results. Experimental edge scans on other two vibration modes, #3 and #4, also show close relevance to calculated edge scans. The number of vibration nodes matches for both of the modes. However, an accurate fit of the experimental data is complicated due to a larger number of vibration periods for these high-frequency modes and limited spatial resolution of the probe. Good correlation between the experiment and the FEA modeling will serve as a guideline for crack influenced frequency-shifting behavior.

Figure 4 Amplitude variation of the RUV mode along the wafer edge representing Peak 1 at 30 kHz (left) and peak 2 at 45.6 KHz (right). (a) FEA modeling, (b) experimental data.

3.2 Crack elongation

In Figure 5 we show a variation of the RUV f-scan of the resonance vibration peak at 41.4 kHz (non-cracked wafer) caused by the 16 mm crack located on the wafer's corner and the same wafer with the crack elongated up to 34 mm. The data are presented for 125 mm x 125 mm Cz-Si wafer (#27a) with 220 microns thickness. This is very first experimental justification on a gradual variation of the RUV peak parameters with crack length performed on the same Si wafer. For this experiment we used specially designed experimental apparatus which allowed the wafer with initial "seed" crack to be bended with constant computer controlled bending speed and bending amplitude. The wafer was positioned in a clamping device with a single corner exposed. The device was clamped along a 45 degree

angle relating to a crystallographic $\langle 110 \rangle$ direction. The alignment was achieved using a previously cleaved Cz-Si “dummy” wafer. With the wafer clamped in the machine along its edge a stepper motor controlled rod exerted downward pressure at the exposed corner of the wafer. Slow stepping speeds of approximately 40 microns per second were used with maximum amplitude of wafer’s exposed corner deflection varied from 1 to 3 mm. In Figure 6 we present Scanning Acoustic Microscope (SAM) images of the wafer part subjected to initial crack (a) and elongated crack (b). The effect of a crack elongation is quite substantial. It can be specified as a gradual downward peak shift, increase of the peak bandwidth and a strong reduction of the peak amplitude.

3.3 Cast Wafers

Elongation experiments documented that crack length controls RUV peak parameters and validated high sensitivity of the RUV method with respect to minimum length of the detected crack. At the same time, we established that in a solar cell production environment other effects may control and affect the RUV method

Figure 7: Statistics of the bandwidth distribution on a set of identical 125 mm x 125 mm cast wafers. Red curve is an approximation of the histogram with normal distribution with parameters: mean value $M_{BW} = 90.4$ Hz, standard deviation, $\sigma_{BW} = 33$ Hz. Wafers with cracks are rejected using 3σ criterion.

statistical variation. According to data in Figure 7 most of measured cast wafers (95.4%) fall into the 3σ range of the normal distribution curve. The outliers (totally 13 wafers of 282, i.e. 4.6%) were rejected based on high bandwidth values. These wafers were analyzed also using SAM technique. Most of the rejected wafers had periphery cracks in

Figure 8: RUV measurements performed on a set of 156 mm cast wafers two of which had “smiling face” cracks as seen on SAM image (insert). Notice that this type of crack usually is not visualized with any type of optical equipment.

Figure 9: RUV data on a set of cast wafers (156 mm x 156 mm) illustrating the effect of “smiling face” crack on f-scan parameters: (a) peak position, (b) peak amplitude, and (c) bandwidth. Wafers # 14 and #28 have cracks while others are crack-free as confirmed by SAM study.

the range form 2 to 10 mm length. This statistical experiment illustrates that real sensitivity of the method is strongly affected by distribution of RUV parameters between regular non-cracked wafers.

In Figures 8 and 9 we show a special case of cracks observed in cast Si wafers, known as a “smiling face” type. It is a hypothesis that high local stress is created during ingot sawing which is released as a periphery crack in the sliced wafers and leading ultimately to almost 100% wafer’s breakage along the crack. RUV measurements were performed on a set of 24 wafers: 22 of them had no cracks while two others (#14 and #28) had cracks of this type. In Figure 8 (insert) the smiling face crack is easily observed using low-resolution SAM imaging (see bottom part of the wafer image). Frequency scans show high consistency of the RUV peak with maximum at approximately 57 kHz for wafers without crack. Cracked wafers clearly identified from non-cracked by having shifted peak position (~ 1000 Hz), reduced peak amplitude by a factor of two and increased peak bandwidth. This data are presented in Figure 9.

Table 2: RUV statistics in as-cut Cz-Si wafers			
	Mean Value	Std.Dev	% Std.Dev.
Amplitude	0.47	0.09	19.1
Bandwidth	122.0	14.7	12.0
Peak	58616	71	0.12

3.4 Cz-Si Wafers

To justify applicability of the RUV method on processed silicon wafers and identify potential problems we performed a statistical experiment. In this study we used a set of 100 as-cut Cz-Si wafers (125 mm x 125 mm, nominal thickness 220 microns) which was initially measured with RUV technique. This set then passed through consecutive solar cell production steps, which included surface texturing, centrifuge drying, diffusion, plasma and HF etching, anti-reflecting (AR) coating with SiN layer, metallization with front and back contacts, contact stripes

soldering. The processing was performed in commercial facilities of a solar cell producer. After each step the entire set was returned and remeasured with RUV technique. The objective of this study was to justify usage of the RUV system at different solar cell production steps. In the Table 2 we present data of the RUV statistics in as-cut wafers. It is clear that compared to cast wafers the standard deviation of all parameters is much smaller confirming high level of identity of Cz wafers. Specifically we observed the bandwidth S.D. only 14.7 Hz compared to 33 Hz in cast and 171 Hz in EFG wafers. As a result crack detection sensitivity is highest in Cz-Si wafers, followed by cast and then by EFG. In Figure 10 we show variation of the RUV parameters in processed Cz-Si wafers. According to the trend in BW and peak position values we found that these parameters are not changed from as-cut up to AR coating step, they exhibit a noticeable shift after the metallization step and another one after contact soldering.

These data along with variation of the standard deviation (not shown) document that RUV method sensitivity with respect to crack length is highest at the initial processing steps due to narrow statistical distribution and is lowest after contact stripe soldering.

3.5 RUV system stability and accuracy: fast mode.

To explore stability and performance of the RUV system we performed experiments by using RUV metrology with different cycling time by reducing measurement time down to targeted 2.0 seconds per cycle. Entire RUV measurement cycle consisted of the consecutive steps: wafer loading from a home position on the transducer by vacuum coupling the wafer and transducer, lifting the transducer with the wafer to a measuring position using computer controlled Z-stage, contacting the wafer's edge by ultrasonic probe using computer controlled X-stage, data acquisition by measuring f-scan, Lorentzian fit of the experimental data, wafer unloading to the home position. The duration of the measuring cycle can be varied by changing number of data points per f-scan or lock-in amplifier integration time. In figure 11 we show frequency sweeps performed with different data points per f-scan (from 100 to 10) and cycling time from 12.4 seconds down to 2.0 seconds per cycle. We documented in this type of measurements that 2.0 seconds per wafer is achievable throughput rate of the RUV system. Reduction of the data points per scan provides only small variation of the f-scan parameters. Specifically, peak amplitude is reduced by 16%, peak bandwidth is reduced by 7 Hz (5%), and peak position is changed by 14 Hz. These variations are much smaller compared to typical standard deviations of corresponding distributions for any type of silicon wafer technology. Therefore, fast 2.0 seconds cycle time is documented in these experiments.

Figure 11: Variation of the RUV peak with reduction of data points measured per f-scan and cycling time. The shortest time of 2.0 seconds per wafer is demonstrated in this experiment.

Figure 12: Variation of the RUV measurement cycle time by changing integration time for a single data point. Best result was achieved with lock-in amplifier #2, which allowed reducing total cycle time down to 1.8 seconds per wafer.

Other practical aspect explored in this project is how minimum cycle time of 2.0 seconds depends on specific hardware parameters used in the RUV system. In Figure 12 we show a dependence of the cycle time versus integration time constant of different lock-in amplifiers used in this study. It is obvious that reduction of the acquisition time with the lock-in time constant provides speeding up of the entire process but lead to deterioration of signal/noise ratio. We noticed that various hardware systems respond differently to this parameter. According to the data in Figure 12 the lock-in #2 shows a superior performance reducing a cycling time below 2.0 seconds. This is very encouraging result proving that further acceleration of the RUV technique is possible with optimizing regime of the hardware and software.

Table 3: Statistical parameters of two multiple runs

	Amplitude [mV]		Bandwidth [Hz]		Peak [Hz]	
	Mean	S.D.	Mean	S.D.	Mean	S.D.
1 st Run	0.45	0.06	156	11	67647	16
2 nd Run	0.43	0.06	146	9	67632	14

In Figure 13 we show a special experimental setting which essentially models a practical utilization of the RUV system in a solar cell production line. In this experiment the same Si wafer was multiple measured by the RUV system in the same manner through entire measuring cycle and data of individual measurements were compared and

plotted after Lorentzian fit of the f -curve. Two runs each of 582 cycles were performed with the same cast Si wafer. Though generally we found a consistency between these two runs (Table 3), a slow variation of the RUV parameters is recorded. For instance peak position is shifted upward by approximately 60 Hz, peak amplitude is reduced from 0.5 to 0.4 mV (20%) and bandwidth is essentially not changed. One technical problem was identified as a gradual variation of a vacuum coupling between the transducer and wafer. This effect has to be eliminated to assure higher stability of the RUV system as a production-grade in-line testing system. We documented that statistical variations of the data during each run are relatively small showing a standard deviation of 0.06 mV for peak amplitude, 9-11 Hz for peak bandwidth and 14 – 16 Hz for peak position. These values are substantially lower than similar parameter of wafer's statistical variations as presented in previous sections.

4. CONCLUSIONS

- (a) RUV methodology is applicable to all major Si wafer technologies used in solar cell production, such as single crystal (Cz), cast and ribbon (EFG). RUV method sensitivity is different for each type of Si materials due to statistical distribution of the wafer's characteristics. It is highest in Cz-Si followed by cast and EFG.
- (b) RUV method is applicable to as-cut and processed Si wafers including final solar cells. Its sensitivity depends on a processing step: the highest in as-cut wafers and lowest in cells with contact stripes.
- (c) Experimental RUV system (hardware and software) is capable to match 2.0 seconds per wafer throughput rate in state-of-art solar cell production lines. This time can be further shortened by optimizing system hardware and programming options.

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Strength of PV Silicon Wafers — Fracture Mechanics Approach

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Introduction

For the photovoltaic (PV) industry, breakage of silicon wafers from cracking is a major problem that limits the production yield, causes additional material loss, and increases the final cost of PV modules. In a typical manufacturing facility, the loss resulting from cracking can be as high as 5%. When silicon prices are high, PV companies try to reduce material usage by decreasing the wafer thickness. Such an approach, however, can significantly lower the mechanical strength of wafers and consequently negatively impact the production yield. Furthermore, the problem of fracture strength becomes important not only when the wafer is reduced in thickness, but also when its area increases. To successfully achieve the goal of reducing silicon usage and maintaining high yield, one needs to understand the fracture behavior of silicon wafers. This paper presents our general strength model for silicon wafers with sub-surface damage. The model is capable of predicting the distribution of maximum load (strength) of PV wafers for any load configuration and wafer size and shape. With this model, one can optimize production processes and develop wafer treatment techniques that will be suitable for thinner and larger wafers.

Strength of PV wafer and the scaling law

The characteristic feature of brittle materials such as silicon at room temperature is that their strength is limited by structural imperfections. Bulk-crystal defects such as micro-cracks, voids, grain boundaries, dislocation networks, and precipitated impurities can serve as stress concentrators and crack nucleation spots. In the vicinity of such defects, the stresses can be much higher than the nominal macroscopic load applied to a sample. A majority of silicon substrates for PV applications are manufactured by a multi-crystalline silicon (mc-Si) ingot casting followed by wafer sawing using multi-wire sawing systems. The surface of a post-sawn wafer is not only rough, but it contains a sub-surface damage as well [1, 2]. The maximum depth of observed micro-cracks was reported in the range of 10–70 μm . It is also known that due to different sawing conditions, the micro-cracks are larger in the vicinity of wafer edge [3]. It should also be noted here that in a typical manufacturing process, the post-sawn sub-surface damage is at least partially etched off.

In reference [3], a classical approach, which relates the strength of a specimen to its volume, has been used. According to this approach, a probability $F_V(\sigma)$ that a wafer survives load σ is given by:

$$F_V(\sigma) = \exp\left(-\int_V \left(\frac{\sigma - \gamma_V}{\alpha_V}\right)^{\omega_V} dV\right), \quad (1)$$

where γ_V , α_V , and ω_V are the three parameters of Weibull distribution. In the case of the multi-axial stress state, we need to regard σ as a position-dependent effective stress [4]. To fully describe the strength of a PV wafer, the model needs to be extended so that the surface and edge

effects are taken into account. For a wafer in which only the surface or edge damage are present, the probabilities of survival can be defined, respectively, as:

$$F_A(\sigma) = \exp\left(-\int_A \left(\frac{\sigma - \gamma_A}{\alpha_A}\right)^{\omega_A} dA\right) \quad F_L(\sigma) = \exp\left(-\int_L \left(\frac{\sigma - \gamma_L}{\alpha_L}\right)^{\omega_L} dL\right), \quad (2)$$

In the above two expressions, A represents the surface area, L stands for the edge length, and γ_A , γ_L , α_A , α_L , ω_A , ω_L are Weibull parameters, which are different from the parameters in expression (1). Formulas (1) and (2) describe the three failure modes of a PV wafer that represent the volume (bulk), area, and edge components. Based on the weakest-link property they can be combined to yield the effective probability of survival for the entire wafer: $F(\sigma) = F_V(\sigma) \cdot F_A(\sigma) \cdot F_L(\sigma)$. Plugging (1) and (2) into this expression gives:

$$F(\sigma) = \exp\left(-\int_V \left(\frac{\sigma - \gamma_V}{\alpha_V}\right)^{\omega_V} dV - \int_A \left(\frac{\sigma - \gamma_A}{\alpha_A}\right)^{\omega_A} dA - \int_L \left(\frac{\sigma - \gamma_L}{\alpha_L}\right)^{\omega_L} dL\right), \quad (3)$$

This is a general formula that fully and accurately describes the strength of an unpolished PV silicon wafer with rough surfaces. Equation (3) depends on nine constants. Contrary to the previous models, these parameters are the properties of a wafer itself and do not depend on the mechanical fixture used in the experimental setup.

Let's consider two specimens of surface areas A_I and A_{II} . Assuming that the specimens are subjected to the uni-axial tension (respectively σ_I and σ_{II}) and that the fracture is controlled by the surface damage, it can be shown based on equation (3) that:

$$\left(\frac{\sigma_I - \gamma_A}{\sigma_{II} - \gamma_A}\right)^{\omega_A} = \frac{A_{II}}{A_I} \quad (4)$$

This simple formula representing the scaling law differs significantly from previous approaches from literature [3], because it relates the wafer strength to the specimen area rather than to its volume.

Monte Carlo simulations

The main objective of Monte Carlo (MC) simulations developed in this study is to predict the strength distribution of PV silicon wafers. The presented technique is very general and allows for modeling of wafer of various sizes and shapes that are subjected to any type of loading. As an example, simulation results for a 5" x 5" wafer subjected to uni-axial tension will be presented., Bulk, surface, and edge flaws can be modeled theoretically using the proposed MC technique, however, this study focuses on the surface damage. As was mentioned before, PV silicon wafers contain sub-surface micro-cracks. It is reasonable to assume that due to the large surface area and relatively small volume, the strength of such wafers is determined mainly by the sub-surface and near-edge damage. The edge damage has not been well quantified yet, and the appropriate characterization data are not available in the literature. Therefore, in this study, it is assumed that the edge component is negligible. In other words, the results presented here show the effect of the surface damage on the wafer strength.

To perform MC simulations, we virtually generate a set of 100 wafers. Each wafer contains 100 surface cracks (50 on each side), which are randomly distributed and oriented. Figure 1 depicts an example of one 5" x 5" wafer with surface micro-cracks used in the MC simulation. For the

sake of legibility, the cracks are magnified 20 times in the figure. The maximum load for each wafer is calculated subsequently using the fracture-mechanics method combined with the weakest-link principle. The next step includes statistical analyses of the results for all 100 wafers to obtain the strength distribution. Finally, we determine if Weibull distribution can accurately fit the obtained results, and we find the corresponding Weibull parameters. The computations performed in this study were based on the following assumptions. a) The surface energy of silicon, γ_0 , is equal to 2.475 J/m^2 , and density of subsurface micro-cracks is $0.32/\text{cm}^2$. b) The cracks are semi-elliptical in shape, and the crack plane is perpendicular to the wafer surface. c) The size of the cracks varies randomly within the specified ranges: the length, L , from 0 to $20 \text{ }\mu\text{m}$; and the depth, D , from 0 to $200 \text{ }\mu\text{m}$. d) We also assume that the entire wafer fractures once a single crack starts to propagate. e) The entire system is linearly elastic. f) The cracks interact neither with the wafer edge nor with each other. This last assumption implies that the strength of a wafer is controlled by one critical sub-surface crack for which the energy-release rate is the highest. We are positive that the above assumptions are valid for the case of an unpolished PV silicon wafer with rough surfaces subjected to typical processing or handling loads at room temperature.

Figure 1. Example of wafer with randomly distributed surface cracks used in Monte Carlo simulation. For legibility, the cracks are magnified 20 times.

Fracture-mechanics modeling

The interaction between cracks is neglected in our model, so the stability of each crack can be analyzed separately. To predict the ultimate load for a wafer with one crack, we apply the fracture-mechanical computations based on gamma integrals [5] and the finite-element method. Empirical relationships for surface cracks are available only some for special cases. We need to use the finite-element method, because the orientation of the crack is arbitrary and the model should be able to handle any type of external load.

A geometrical representation of a semi-elliptical surface crack in a PV wafer is shown in Figure 2. In the figure, the length and depth of the crack are denoted as L and D . On the crack front, we also define point P that lays on the crack front; its position is fully defined by angle θ . After the model is built, stresses, σ_{ij} , strains, ε_{ij} , and displacements, u_i , in a wafer with a crack are obtained using a finite-element method. Next, the energy-release-rate vector, $\Gamma_k(\theta)$, is computed as a function of angle θ for an external load equal to 1 MPa :

$$\Gamma_k = \lim_{\text{length of } C \rightarrow 0} \oint_C (En_k - \sigma_{ij} n_j u_{i,k}) ds \quad \text{as length of } C \rightarrow 0, \quad k = 1, 2$$

The description of the parameters in the above expression can be found in Ref. [5]. According to the energy theory for the curved cracks, the propagation initiates when $\max(|\Gamma_k(\theta)|)$ as $\theta \in \{0^\circ, 180^\circ\} = 2\gamma_0$, where γ_0 is the surface energy, and $|\Gamma_k|$ denotes the length of vector Γ_k . Finally, the strength of a wafer can be determined using fact that Γ_k is proportional to the square of the external load.

Figure 2. A small part of a wafer containing a semi-elliptical surface crack

Results and discussion

Figure 3 and Figure 4 depict, respectively, the predicted strength distribution and the Weibull fitting results for a statistical sample of 100 wafers (each containing 100 cracks). It can be observed that the strength of wafers varied from 100 to 125 MPa, whereas the most probable value was 106 MPa. The graph in Figure 4 clearly shows that the strength data follow the Weibull distribution very well. The fitting procedure yielded the following values for the three Weibull parameters: $\alpha_A = 0.205 \text{ MPa } m^{2/\omega_A}$, $\omega_A = 2.49$, and $\gamma_A = 109 \text{ MPa}$. The obtained strength distribution can be compared with the available experimental results in literature. References [1, 6] present experimental data for statistical samples of PV wafers tested in the as-sawn state, as well as after etching off a 5-, 10-, and 20- μm layer of the surface. By comparing, one can find that the strength distribution predicted in this study fits between experimental distributions for the as-sawn and 5- μm etched wafers. Considering the fact that the experimental load conditions (bi-axial fixture) differed from the modeled one (uni-axial tension), we can conclude that the obtained agreement is very good. We are confident that if more accurate information about the experimental fixture and the actual surface damage is plugged into our model, then distribution of wafer strength yielded by the simulation will be almost exact.

The model developed in this study can be used to correlate the results from various experiments. Consequently, it makes it possible to compare the strength results obtained using various fixtures that apply the load differently. The important advantage of the model is that it requires only the information about the bulk, surface, and edge damage, which are the properties of the wafer itself. Based on the data, we are able to predict the strength of PV wafers for practically any load condition.

Figure 3. Predicted wafer strength distribution for a statistical sample of 100 wafers

Figure 4. Fitting the wafer strength results to Weibull distribution

Conclusions

A new expression, based on the multi-modal Weibull distribution, that takes into account the fracture properties of a wafer surface and edge has been proposed in this paper to describe strength of silicon wafers. The corresponding scaling law is also derived. In the second part, we present a general fracture-mechanics model that can successfully predict the strength of silicon wafers used by PV industry. The model combines Monte Carlo simulations with finite-element fracture computations. It has been shown that even with very limited surface damage data, the predicted wafer strength distribution agrees well with the available experimental results. The presented fracture model can be applied in the future to various practical applications, which can be grouped into the following two categories. First, it can simulate specific wafer processing steps in terms of mechanical stability of the wafers. As a result, a production yield loss due to fracture can be predicted. The second category is related to the optimization of wafer surface and edge-damage removal to achieve wafers of higher strength. In particular, the model can be applied to examine the effect of various sawing and etching conditions on the ultimate strength of a silicon wafer.

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Electrical Characterization of n-type crystalline Si/ amorphous Si:H structures

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[Abstract]

To extract the TCO/n-i-aSi:H/n-cSi junction resistance, resistances between the back-side Ag electrodes on a TCO/i-n-aSi:H/n-cSi structure, with TCO cut between the electrodes, was measured. The extracted junction resistance was in fairly good agreement with the previous reported value by “the potential probe method”.

A surface conductive layer was electrically observed in the surface of n-cSi under p-i-aSi:H/n-cSi structure. By analyzing back bias dependence of the conductance of the surface layer, it is concluded to be an inversion layer induced in the surface of n-cSi by p-i-aSi:H.

[Introduction]

It had not been clearly shown whether the back side crystalline silicon (cSi)/hydrogenated amorphous silicon (aSi:H) hetero-junction of a HIT cell^{[1],[2]} is a photo-voltage generating junction or an ohmic junction which ohmically interconnects cSi and the back conductive electrode of TCO/metal. As is shown in Fig.1, each of the electrical characteristics of the front junction and the back-side junction of a HIT cell could be extracted from one IV measurement of the solar cell with the newly proposed potential probe method.^[3] Where, the back-side hetero-junction (n-cSi/i-n-aSi:H/ conductive electrode) was characterized and shown as an ohmic junction and electron accumulation was confirmed by scanning probe Kelvin force microscope measurement near the back surface of the n-cSi at the n-cSi/ i-n-aSi:H interface.

In this paper, the junction resistance value of the back-side junction is estimated by analyzing the resistance between back-side Ag electrodes and a possible inversion layer in the front surface of the n-cSi at the p-i-aSi:H/ n-cSi interface is reported.

[Experiments]

To extract the electrical resistance of back-side junction, a set of back-side Ag electrode to Ag electrode resistances were measured. To eliminate a shunt current path of TCO on n-i-aSi:H between the back side Ag electrodes, TCO films at the both side of each Ag electrode were cut through to the n-cSi substrate to the depth of 40 micro-meter as shown in Fig. 2. Current-voltage

Fig.1 IV characteristics, #6 dark and illuminated

characteristics between the back side Ag electrodes with a fixed bias (0 volt) to the front electrodes were measured before and after the TCO cut.

On the other hand, to confirm possible existence of an inversion layer in the surface of n-cSi at the p-i-aSi:H/ n-cSi interface, current voltage characteristics between front Ag electrodes were measured with biases to the back-side electrodes as a parameter after etching of TCO on the aSi:H film as shown in Fig. 3. The etching of TCO is necessary to eliminate low resistance of TCO in parallel with the inversion layer.

For the IV measurement, the Agilent Technology semiconductor parameter analyzer 4156C and a multi-probe system were used.

Fig.2 structure with "TCO cut" to extract TCO/n-i-aSi:H/n-cSi junction resistance

Fig.3 structure with "TCO etched" to measure conductance of an surface inversion layer

[Results]

Fig. 4 shows obtained results on the resistances between the back-side Ag electrodes.

A lateral resistance between the Ag electrodes is 44 ohm and resistance between Ag/TCO and n-cSi via n-cSi/ i-n-aSi:H junction (junction resistance) is 167 ohm. Considering an effective electrode area (0.21mm x 2.1mm), [junction resistance] x [junction area] results 0.74 ohm-cm². This value is in fairly good agreement with the previously reported value 0.63 ohm-cm² obtained by the potential probe method.^[3] Without the TCO cut, the lateral current through TCO film connecting the Ag electrodes prevents extracting the actual junction resistance as shown data labeled as "w/o TCO cut" in Fig. 4.

Fig.4 resistance between back-side Ag electrodes

Fig. 5 shows measured conductance values between the front Ag electrodes with TCO films among the Ag electrodes etched away. G_{ba} denotes the conductance between Ag electrodes A and B, and G_{ca} denotes that between A and C. G_{dep} denotes theoretical conductance values with some fitting parameters which will be discussed later. Even after TCO is etched away (TCO under and near-by the Ag electrodes was left un-etched), conduction between Ag electrodes was observed and these conductances decreased as the reverse bias to the solar cell increased. This decrease can be theoretically explained by increase in electric charge of a surface depletion layer due to the reverse bias. These observation suggests that an inversion layer is induced in the front surface of n-cSi by p-i-aSi:H on n-cSi as is shown in Fig. 3.

[Discussion]

In the present analysis on the back-side junction resistance, it was assumed that a current path between electrodes A and C is not disturbed by the electrode B, because a calculated lateral resistance of n-cSi under the electrode B is small enough (7.5 ohm) than the junction resistance (167 ohm). Thus a resistance value (335 ohm) extrapolated (line for TCO cut) to vertical axis in Fig. 4 can be sum of the junction resistances under Ag electrode A and C. The resistance value denoted as “pp” in Fig. 4 was calculated using a voltage measured by contacting a potential probe on electrode B while measuring current voltage characteristics between the electrodes A and C. The resistance value “pp” was calculated from the potential of the electrode B divided by the current through the electrodes A and C. The resistance value “pp” contains a lateral resistance between the electrodes A and B and a junction resistance under the electrode A. By subtracting the resistance value “pp” from the resistance between the electrode A and B, we can know the junction resistance under the electrode B, which results 167 ohm. That is just a half of the above resistance value extrapolated to the vertical axis of Fig.4 and if the value of the junction resistance is supposed to be equal between the junctions under the electrode A and C, the value results also 167 ohm ($\sim 335/2$). The obtained unit area junction resistance is 0.74 ohm-cm² and it should be noted that this value also fairly good agreement with the previously reported value 0.63 ohm-cm² obtained by a different approach, “the potential probe method”^[3]. These coincidences show that the electrical model and material parameter applied to the present structure are valid.

In the calculation of G_{dep} , an impurity concentration of n-cSi and hole mobility in the inversion

layer are used as the fitting parameters. The impurity concentration of n-cSi was adopted from the result in the previous report. The hole mobility was fitted as $140 \text{ cm}^2/\text{v}/\text{sec}$. The value of the fitted mobility is about 1/3 of that of bulk Si but it is far larger than that known in aSi:H. Thus the lateral conduction between the Ag electrode occurs in the inversion channel in the front surface of n-cSi. The surface of the n-cSi is chemically textured and the textured surface is mainly of (111) face, thus surface mobility in the inversion channel is smaller than that of (100) face where MOS transistors have been fabricated. Furthermore, holes are forced to travel non-planar surface in the textured surface and their pass length is longer than a planar projection between the electrodes, thus again a smaller effective mobility results.

In the etching of TCO, the surface of the very thin (less than 10nm) p-aSi:H may be damaged or contaminated, thus the absolute value of conductance of the inversion layer may not exactly reflect that of the cell with TCO. However, possible existence of the inversion layer will give a new step for analyzing and designing the front junction of aSi:H/cSi hetero-junction solar cells.

[Conclusion]

Resistances between the back-side Ag electrodes on a TCO/n-i-aSi:H/n-cSi structure, with TCO cut between the electrodes, was measured. The unit area TCO/n-i-aSi:H/n-cSi junction resistance was extracted to be 0.74 ohm-cm^2 which was in fairly good agreement with the previous reported value by “the potential prove method”.

A surface inversion layer was electrically observed in the surface of n-cSi under p-i-aSi:H/n-cSi structure. This may give a new step for analyzing and designing the front junction of aSi:H/cSi hetero-junction solar cells.

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CURRENT AND FUTURE STATUS OF GLOBAL POLYSILICON PRODUCTION

17TH NREL SILICON WORKSHOP

by
Richard Winegarner

History of Polysilicon Production

- ✦ All polysilicon manufacturing facilities to date were built to manufacture semiconductor grade polysilicon
- ✦ The capacity of these facilities is stated in nameplate metric tons (that is the number of tons of semiconductor grade material that can be produced on an annual basis)
- ✦ Some of the material produced at these plants does not meet semiconductor specifications and is labeled as fallout
- ✦ This fallout material is typically sold to discrete and photovoltaic customers
- ✦ By volume fallout is about 9% of the total

AUGUST 2007

SAGE CONCEPTS

PAGE - 2

SEMICONDUCTOR POLYSILICON GROWTH

AUGUST 2007

SAGE CONCEPTS

PAGE - 3

TRADITIONAL POLYSILICON MANUFACTURERS

- WACKER
- HEMLOCK
- MEMC
- REC SILICON
- TOKUYAMA
- MITSUBISHI MATERIALS
- SUMITOMO TITANIUM

AUGUST 2007

SAGE CONCEPTS

PAGE - 4

POLYSILICON PLANT NAME PLATE CAPACITIES

COMPANY	CITY	LOCATION	2005	2006	2007	2008	2009	2010
HEMLOCK	HEMLOCK, OR	OREGON	7,700	10,000	10,000	12,500	14,500	15,000
WACKER	SÜDBURGEN	GERMANY	5,600	6,000	6,500	6,800	6,800	14,500
TOKUYAMA	YOKOHAMA, JPN	JAPAN	5,000	5,000	5,000	5,000	5,000	7,200
REC SILICON	CHINA	CHINA	3,000	3,500	3,600	3,600	3,600	3,600
MITSUBISHI	YAMAGUCHI	JAPAN	1,800	1,800	1,800	1,800	1,800	1,800
MEMC	PHOENIX	ARIZONA	2,300	2,300	3,000	4,000	4,000	8,000
SUMITOMO	YAMAGUCHI	JAPAN	1,250	1,450	1,350	1,850	1,850	1,850
OTHERS	VARIOUS	VARIOUS	1,300	1,200	1,200	1,100	1,300	1,300
TOTAL			31,400	35,250	37,750	46,650	60,250	62,100

AUGUST 2007

SAGE CONCEPTS

PAGE - 5

2006 COMBINED POLYSILICON SUPPLY

AUGUST 2007

SAGE CONCEPTS

PAGE - 6

HOW DID HEMLOCK SELL 11,621 TONS, WHEN THEIR CAPACITY IS ONLY 10,000 TONS?

- Nameplate capacity states a plant's capacity to produce semiconductor polysilicon
- Semiconductor polysilicon equipment can increase output by 30% when making PV polysilicon
- To determine a plant's actual output
 - First subtract their semiconductor sales from the name plate capacity
 - Multiply the remainder by 1.3
 - Add 10% to the semiconductor production as fall out
- For Hemlock $10,000 - 6860 = 3140 \times 1.3 = 4082$
 - Add $6860 + 686 + 4082 = 11,628$ metric tons

AUGUST 2007

SAGE CONCEPTS

PAGE - 7

HOW SHOULD POLY BE PRICED?

- POLY PRODUCTION BY SIEMENS PROCESS
 - SEMICONDUCTOR CZ POLY = INDEX 100
 - SOLAR POLY FROM SAME EQUIPMENT = 130%
 - FZ POLY OUT OF SAME EQUIPMENT = 50%
- NORMALIZED POLY PRICING
 - SOLAR POLY SOLD AT \$70 PER KILOGRAM
 - EQUIVALENT SEMI CZ PRICE = \$91
 - EQUIVALENT SEMI FZ PRICE = \$182

AUGUST 2007

SAGE CONCEPTS

PAGE - 8

2006 POLYSILICON PRICING

- SOLAR POLY PRICE = \$80 PER KILOGRAM
- SEMICONDUCTOR CZ PRICE = \$60/KG
- SEMICONDUCTOR FZ PRICE = \$200/KG
- SPOT MARKET PRICE = \$300/KG

WHY THE DIFFERENCE ?

AUGUST 2007

SAGE CONCEPTS

PAGE - 9

EXISTING SUPPLIER / CUSTOMER RELATIONSHIPS

- HEMLOCK > 25% OWNED BY SEH AND 12.5% OWNED BY MITSUBISHI MATERIALS
- WACKER > POLY & SILTRONIC (WAFERS) OWNED BY WACKER CHEMIE
- TOKUYAMA > CLOSELY TIED TO SHIN ETSU
- MEMC > POLY AND WAFERS OWNED BY MEMC
- MITSUBISHI POLY > OWNED BY MITSUBISHI MATERIALS WHICH OWNS 50% OF SUMCO
- SUMITOMO TITANIUM POLY > OWNED BY SUMITOMO METALS WHICH OWNS 50% OF SUMCO
- REC > 25% OF BUTTE PLANT OWNED BY KOMATSU

AUGUST 2007

SAGE CONCEPTS

PAGE - 10

HISTORICAL POLYSILICON PRICING

AUGUST 2007

SAGE CONCEPTS

PAGE - 11

MAKE OR BUY?

- When the price is within a few percent of manufacturing cost - buy
- When the price is much higher than manufacturing cost - make
- How difficult is it to manufacture polysilicon
 - ▶ The most pure material in volume manufacture
 - ▶ Very capital and energy intensive
 - ▶ Competitors have 50 years experience
- Many newcomers have decided to dive in
- How many will be successful in near term?

AUGUST 2007

SAGE CONCEPTS

PAGE - 12

NEWCOMERS

COMPANY NAME	COUNTRY	FEEDSTOCK	REACTOR TYPE	CAPACITY MT	SUCCESS PROBABLY
1 DC CHEMICAL	KOREA	TCS	SIEMENS	3000	
2 HOKU MATERIALS	DAWA	TCS	SIEMENS	1500	
3 SILICO EBERGIA	SPAIN	TCS	SIEMENS	2000	
4 SERPS	FRANCE	TCS	SIEMENS	3000	
5 CRYSTAL	KYRGISTAN	TCS	SIEMENS	40	
6 SOLARIS PROJECT	KRAVNOYORSK	TCS	SIEMENS	4000	
7 NITOL - U SBERGAN SI	IRKUSK	TCS	SIEMENS	1000	
8 POLYSL	BALIC RUSSIA	TCS	SIEMENS	1000	
9 M SILEX	JAPAN	STC	SIEMENS	1500	
10 JESI	GERMANY	STC	TUBE	850	
11 EUME	CHINA	TCS	SIEMENS	500	
12 LESHAN PHOSPHOR	CHINA	TCS	SIEMENS	1000	
13 SOJAN KIRGAND	CHINA	TCS	SIEMENS	1250	
14 LOYANG MONOCRYSTAL	CHINA	TCS	SIEMENS	60	
15 LOYANG SHONGGULI	CHINA	TCS	SIEMENS	1000	
16 SHANGHAI TELCOM	CHINA	TCS	SIEMENS	1000	
17 SHENZHEN	CHINA	TCS	SIEMENS	1000	
18 BRYTEL	CHINA	TCS	SIEMENS	1000	
19 CHINA SOUTH GLASS	CHINA	TCS	SIEMENS	1000	
20 JIANGLIANG IND DEV CO	CHINA	TCS	SIEMENS	1000	
21 SOLAR VALLEY AG	SLOVENIA	MgSi Upgrade		100	
22 DOW CORNING	BRAZIL	MgSi Upgrade		3000	
23 MANHARTH SOLAR	INDIA	BROWNE	SIEMENS	500	
24 AE POLYSILICON	USA	MONOSILANE	PBR	1200	
25 PTV SOLAR SILICON	JAPAN	ZSC		1500	
26 NIPPON STEEL	JAPAN			200	
27 JFE	JAPAN	MgSi Upgrade		400	
28 EUCOR	NORWAY	MgSi Upgrade		5000	
29 SILICON BEACONHUR	CANADA	MgSi Upgrade		300	
30 ARISE	CANADA	MgSi Upgrade		100	
31 SCHEUTEN SOLAR	GERMANY	MgSi Upgrade		1250	
32 GLOBAL PV SPECIALTIES	USA	NEW		100	
33 GRASOLAR	NETHERLANDS	NEW		100	
34 SOLAR ENERTECH	MONGOLIA	?		1000	
35 NAWAN TEE	TAIWAN	TCS	SIEMENS	1000	
				43,340	15,321

AUGUST 2007

SAGE CONCEPTS

PAGE - 13

WHO WILL GET NEW CAPACITY? SEMICONDUCTOR VS PV

- Investment Issue - A photovoltaic poly plant is 99% as expensive as a semiconductor poly plant
- It would seem obvious that the best business decision would be to build a plant capable of addressing both markets
- The problem is the proprietary knowledge needed. This may only come with experience.
- Many new plants will be PV only

AUGUST 2007

SAGE CONCEPTS

PAGE - 14

TOTAL POLYSILICON SUPPLY AND DEMAND

AUGUST 2007

SAGE CONCEPTS

PAGE - 15

Laser-Processing for High-Efficiency Solar Cells

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Abstract

We apply laser technology to create local contact openings in thermally grown passivating SiO₂ layers for high-efficiency Si solar cells. We use ultra-short laser pulses (pulse duration $t_{\text{pulse}} \approx 10$ ps) to ablate SiO₂-layers on P-diffused ($R_{\text{sheet}} \approx 100 \text{ } \Omega/\text{sq}$) emitters. The specific contact resistance that we reach with evaporated aluminium on such a locally opened emitter is in the range of 0.3 to 1 m Ωcm^2 . Ultra-short pulse laser ablation is sufficiently damage free to abandon wet chemical etching after ablation. We measure an emitter saturation current density of $J_{0e} = (6.2 \pm 1.6) \times 10^{-13} \text{ A/cm}^2$ on the laser treated areas after a selective emitter diffusion with $R_{\text{sheet}} \approx 20 \text{ } \Omega/\text{sq}$ into the ablated area; a value that is as low as that of reference samples that have the SiO₂ layer removed by HF etching.

1. Introduction

Low surface recombination losses in silicon solar cells can be achieved by passivating the surfaces with SiO₂, SiN_x or a-Si and by limiting the metal-semiconductor contacts to a small fraction of the total cell area. For such cells, a method for producing local openings in the passivating layer is required. Direct laser ablation of SiO₂ is an elegant method to realise such openings since no masks and wet chemical etching steps are required. However, laser-processing of optically transparent materials is particularly challenging due to their low absorption. SiO₂ has a bandgap energy of ≈ 9.3 eV, equivalent to 133 nm wavelength. For most laser sources this implies weak absorption and insufficient process control. We use ultra-short laser pulses with pulse durations in the picosecond range for the local direct ablation of SiO₂-layers from Si [1,2]. Such lasers became recently available for applications in industrial production.

We investigate the quality of SiO₂-ablation by means of contact resistance measurements and by charge carrier lifetime measurements on laser-processed silicon wafers. For this study we use a frequency-doubled Nd:YVO₄ laser ($\lambda = 532$ nm) with a pulse duration of $\tau_{\text{pulse}} \approx 10$ ps (ps-laser) and a frequency-tripled Nd:YVO₄ laser ($\lambda = 355$ nm) with $\tau_{\text{pulse}} \approx 30$ ns (ns-laser), respectively.

2 Experimental

A P-diffusion of B-doped float zone wafers with a resistance of $(5.0 \pm 0.5) \text{ } \Omega \text{ cm}$ yields a sheet resistance of $(100 \pm 5) \text{ } \Omega/\text{sq}$ or $(300 \pm 20) \text{ } \Omega/\text{sq}$ respectively. A subsequent wet oxidation yields an oxide of $(200 \pm 10) \text{ nm}$ thickness. For both lasers we optimise the laser fluence Φ_0 for a small contact resistance and little laser induced crystal damage. The laser fluence Φ_0 (in units of J/cm^2) is defined as the pulse energy density at the peak position of the Gaussian beam profile. The fluence Φ_0 and the $1/e^2$ beam diameter d in the focal plane describe the spatial energy profile irradiated per pulse onto the sample and thus fully characterise the laser pulse. With both lasers only a single laser shot per area is applied to ablate the SiO₂ layer.

Fig. 1 shows optical microscope images of the laser treated samples. The shape of the oxide openings created by using the ns-laser (Fig. 1a) is much less controlled than those

Fig. 1. Optical microscope image of a thermally oxidised Si wafer with locally ablated SiO₂ by laser irradiation: a) using a frequency-tripled Nd:YVO₄ laser with $\tau_{\text{pulse}} \sim 30$ ns; b) using a frequency-doubled ultra-short pulse Nd:YVO₄ laser with $\tau_{\text{pulse}} \sim 10$ ps. A clear advantage in the quality of the openings and the process stability can be observed for the ultra-short pulse laser.

made with the ps-laser (Fig. 1b). The ns-laser treated sample sometimes shows surface structures of molten Si. These structures are not observed at the ps-laser treated samples. Thus the process stability is better with the ps-laser.

Parallel to the laser-ablated samples we process and measure

reference samples for which the oxide layer is removed by wet HF-etching. This well established process reliably removes the oxide layer and is not expected to cause any crystal damage.

2.1 Contact Resistance Measurements

To test the removal of the SiO₂ by laser ablation we prepare contact resistance samples of P-diffused *p*-type FZ-Si wafers (2.5 x 2.5 cm²). The phosphorus diffused n⁺-region has a sheet resistance of (100 ± 5) Ω/sq and is covered by a thermally grown, 200 nm thick SiO₂ layer. We create lines of circular openings by laser ablation as shown in Fig. 1. Aluminium contact fingers are then evaporated through a shadow mask onto the openings in the oxide. The specific contact resistance ρ_{cont} is extracted by means of the transfer length method [3].

Fig. 2 shows the results of the contact resistance ρ_{cont} measurement for various applied laser fluences Φ_0 . Each symbol represents the average of five samples. The standard deviations of the measured values are shown as error bars. Using the ps-laser (open symbols in Fig. 2) we achieve specific contact resistances that are all well below 1.0 mΩ cm² for a laser fluence Φ_0 above 1 J/cm². The SiO₂ is not ablated with fluences of less than 1 J/cm². An increase of the laser fluence tends to result in a slight decrease of ρ_{cont} . At $\Phi_0 = 1.75$ J/cm² the contact resistance is about 0.4 mΩ cm²; a

Fig. 2. The specific contact resistance ρ_{cont} is plotted versus the laser fluence Φ_0 . The open symbols are for the ps-laser and the filled symbols for the ns-laser. The value for the reference sample is plotted at $\Phi_0 = 0$.

value as low as for the HF-etched reference samples (star plotted at $\Phi_0 = 0$). Thus, the laser process completely removes the SiO_2 with one laser shot per area and without an extra subsequent etching step.

In case of the ns-laser the threshold fluence for ablating SiO_2 is $\Phi_0 \approx 2 \text{ J/cm}^2$. At samples processed with a laser fluence $\Phi_0 \approx 2.2 \text{ J/cm}^2$, we measure a specific contact resistance of more than $100 \text{ m}\Omega \text{ cm}^2$ that is not of interest for high efficiency cells. Similar as for the ps-laser, the contact resistance decreases with increasing fluence. The smallest specific contact resistance ρ_{cont} that we measure is $8 \text{ m}\Omega \text{ cm}^2$ for a fluence of 3.4 J/cm^2 . A further increase in fluence does not further decrease ρ_{cont} , but causes an increased damage of the underlying Si and consequently destroys the emitter.

2.2 Local Emitter Saturation Current Density

In order to quantitatively investigate the effect of laser ablation on the local emitter saturation current J_{0e} in the ablated area, we perform effective lifetime measurements on phosphorus-diffused p -type (5.0 ± 0.5) $\Omega \text{ cm}$ FZ-Si wafers. From the lifetime measurements we extract the local diode saturation current in the ablated region [4].

Fig. 3 shows the local saturation current density J_{0e} of the ablated region for $100 \Omega/\text{sq}$ P-diffused samples. We reach a J_{0e} of $(3.0 \pm 0.9) \times 10^{-12} \text{ A/cm}^2$ on the laser treated areas using the ps-laser (open symbols) which is only about twice as high as the HF-reference value of $(1.4 \pm 0.1) \times 10^{-12} \text{ A/cm}^2$. It is important to mention that for the ultra-short pulse laser we achieve both low emitter saturation current densities *and* low contact resistances for a wide range of laser parameters. The broad process window ensures high process stability, whereas for the ns-laser a compromise has to be found balancing recombinative and resistive losses.

The emitter saturation current density increases with increasing sheet resistance on non-passivated emitters and decreases with increasing sheet resistance on well passivated surfaces [5]. For minimum recombination it is thus necessary to have a lighter emitter diffusion in the passivated area than in the contact area which is poorly passivated after metallisation.

We perform such a selective emitter diffusion resulting in a sheet resistance of $(20 \pm 3) \Omega/\text{sq}$ in the openings after laser ablating the SiO_2 . The SiO_2 layer acts as diffusion barrier in the non laser-treated area. Subsequently we determine the local emitter saturation current density $J_{0e,\text{sel}}$ of the samples again by means of lifetime measurements. Fig. 4 shows the emitter saturation current densities on P-diffused samples ($R_{\text{sheet}} \sim 300 \Omega/\text{sq}$) before (J_{0e}) and after ($J_{0e,\text{sel}}$) the second (selective emitter) diffusion ($R_{\text{sheet}} \sim 20 \Omega/\text{sq}$). The values for the ps-laser-treated samples are identical to

Fig. 3. Local saturation current densities of the ablated region for $100 \Omega/\text{sq}$ P-diffused samples. Using the ps-laser a value for J_{0e} is achieved (open symbols) which is only about twice as high as the HF-reference value (star).

Fig. 4. Emitter saturation current densities on P-diffused samples ($R_{\text{sheet}} \approx 300 \, \Omega/\text{sq}$) before (J_{0e}) and after ($J_{0e,\text{sel}}$) the second (selective emitter) diffusion ($R_{\text{sheet}} \approx 20 \, \Omega/\text{sq}$).

3. Summary

Laser processing is capable of replacing masking steps for local contact openings. The *direct* laser ablation of thermally grown SiO_2 layers using an ultra-short pulse laser permits a complete removal of the dielectric layer with a single laser shot. Diode saturation currents of the ablated regions as deduced from effective lifetime measurements confirm that direct laser ablation with a ps-laser induces less recombination centres than a ns-laser. For the ps-laser the level of damage is sufficiently small, so that there is no need to etch any damaged Si after laser processing. This simplifies the cell process. After a selective emitter diffusion, the diode saturation currents achieved with the ps-laser are identical to HF-etched reference samples.

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those of the HF-reference samples and decrease to a level of 600 to 700 fA/cm². Thus, any laser induced damage is sufficiently small to be irrelevant for the recombination losses in the region of the selective P-diffusion.

For comparison, after laser ablation the ns-laser treated samples (filled symbols) show J_{0e} -values of about one order of magnitude higher than the ps-laser treated samples. After the second diffusion these $J_{0e,\text{sel}}$ -values decrease to $(1.9 \pm 0.8) \times 10^{-12} \, \text{A/cm}^2$ and are about three times higher than the corresponding picosecond values.

Understanding Shunting Mechanisms in Silicon Cells: A Review

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Lock-in thermography (LIT) is until now the most successful technique for imaging local inhomogeneities of the dark forward and reverse current in solar cells and thus for investigating shunts in solar cells. By combining LIT and other microscopic investigations, meanwhile many different shunt mechanisms have been identified in silicon solar cells, which may show either a linear (ohmic) or a non-linear (diode-like) I-V characteristic. In addition, there is a third type of "shunts" having a great importance for the reliability of modules, which are pre-breakdown sites. While pre-breakdown sites are only little investigated yet, the physical nature of the most common linear and non-linear shunts in silicon cells is quite well understood now. Ohmic shunting may be due to (1) incomplete opening of the edge, (2) alloyed-in Al-particles or other metals at the surface, (3) cracks before processing, and (4) highly n-conducting silicon carbide filaments crossing the cell (only in multicrystalline cells). Non-linear (diode-like) shunts are (1) due to a direct contact of the grid metal to the base (Schottky-type) or (2) due to highly recombinative locally extended defects crossing the pn-junction (recombination-type). These defects may be material-induced (grain boundaries, dislocations, precipitates) or process-induced, like, e.g., a non-passivated edge region of the cell or scratches or fresh cracks. These local recombination shunts, rather than the material properties, are dominating the recombination of most solar cells. For a high local density of states in these defects, the recombination current shows an ideality factor larger than 2. Here the recombination occurs no longer via isolated point defect states but via multi-level recombination, which may show intrinsic saturation effects.

1. Introduction

Traditionally the name "shunts" was used only for ohmic connections between n- and p-side of pn junctions, like an incompletely opened emitter at the edge. Generally, shunts are leading to leakage currents in solar cells, thereby reducing their fill factor (FF) and the open circuit voltage (V_{oc}) in operation, but not the short circuit current I_{sc} . However, already early shunt investigations have shown that there are both shunts showing a linear (ohmic) I-V characteristic and showing a non-linear (diode-like) characteristic [1]. Therefore, in the following we will use an extended definition of "shunts" as all local sites in solar cells where the local current significantly exceeds the homogeneously flowing current. With other words, our definition of "shunts" includes all sites of the cell which cannot be described by a 1-dimensional (e.g. PC1D) model, which assumes a homogeneous cell made from homogeneous semiconductor material. We will see that, besides obvious ohmic shunts like an incompletely opened edge, all kinds of shunts are connected with extended crystal defects, which are not included in a 1-dimensional solar cell model. This definition includes, besides ohmic shunts, also non-linear shunts including edge currents and pre-breakdown sites.

At the beginning of solar cell technology, only the measured parallel resistance (R_p) was an indication about the presence of shunts. Later on steady-state infrared thermography was used to image shunts [2]. However, the sensitivity of even modern thermocameras is not sufficient to image

weaker shunts under forward bias close to the maximum power point, which is in the order of 0.5 V. Instead, a reverse bias of -5 to -10 V had to be applied to the cells to image the shunts thermally [2]. Another problem of direct thermography was the high heat conductivity of silicon, which leads to a very blurred appearance of the thermograms, thereby reducing the effective spatial resolution. The same limitations hold for liquid crystal sheet shunt detection [3]. The understanding of shunts in solar cells has very much improved after the introduction of lock-in thermography (LIT) techniques [4], which, due to their dramatically improved sensitivity, for the first time allowed for imaging shunts also under forward bias of the cell, corresponding to normal operating conditions. Moreover, due to the dynamic nature of this measurement technique, lateral heat diffusion is suppressed, leading to a considerably improved effective spatial resolution. Recently, also electroluminescence (EL) and photoluminescence (PL) techniques have been found to be effective in shunt detection [5, 6].

Localizing shunts is only the first step in understanding them, the next step must be to identify their nature in order to avoid them. This has been done extensively by microscopic and microanalytical techniques, including visible light microscopy, near infrared transmission light microscopy, transmission electron microscopy (TEM), and scanning electron microscopy (SEM) in secondary electron (SE), electron beam-induced current (EBIC), and energy-dispersive X-ray analysis (EDX) mode. In the following, after a brief summary over existing shunt detection techniques, an overview is given about the most important shunt mechanisms in silicon cells, which have been identified hitherto. Finally, the recombination mechanism of non-linear recombination-induced shunts is discussed in more detail. It is found that recombination via extended defects showing a high local density of recombination states may lead to inherent saturation effects, which is the key for understanding the commonly measured large ideality factors of the recombination current of solar cells.

2. Shunt detection techniques

The most simple and cheapest technique for shunt detection, which is also widely used now in research and industry, is the liquid crystal (LC) sheet technique [3, 7]. About 160 μm thick plastic sheets, which are containing a thermochromic LC layer film, are available e.g. from EdmundOptics. The most appropriate type is No. 72-374 being sensitive between 25 and 30°C (77 - 86°F). Such a sheet is sucked to or simply laid on top of the cell to be investigated, and a reverse bias of several Volts is applied to the cell. In the position of ohmic shunts or pre-breakdown sites, the temperature rises and the color of the sheet changes from black via brown and green to blue. The limitations of this technique are the following: (1) Due to the thickness of the sheets and due to the lateral heat diffusion in silicon, the accuracy of localization is only in the order of 1 mm. (2) The sensitivity of this technique is so low that it can be used only under reverse bias, which may be as large as many Volts. Hence, non-linear shunts, which are active only under low forward bias, cannot be detected by the LC sheet technique if they are not also pre-breakdown sites. The blurring influence of the lateral heat conduction in the silicon can be reduced by sucking the cells to a massive copper chuck. Then the heat diffuses mainly vertically from the cell into the heat sink, and lateral heat diffusion is suppressed on cost of a reduced sensitivity.

Steady-state thermography is only rarely used for shunt detection in silicon cells, since it shows the same limitations as LC sheet imaging. The breakthrough in shunt analysis came with the application of lock-in thermography (LIT) techniques. LIT means that the power dissipation in a device is periodically modulated (usually on/off square-pulsed with a frequency between 1 and 100 Hz), and the measured surface temperature data are evaluated and summed up over many periods to yield an image of the local temperature modulation amplitude and of the local phase shift between heat dissipation and temperature modulation [4]. LIT by using an infrared (IR) thermocamera and

on-line data processing was introduced in 1988 for failure analysis in electronic components [8]. In the 1990s this technique became popular for non-destructive evaluation (NDE) of materials, hence for detecting sub-surface defects in solid bodies, and for local stress analysis [9]. The first LIT application to solar cells was made in 1994 by using "Dynamic Precision Contact Thermography" (DPCT) [1]. This technique, which used an x-y-z table to sequentially scan a miniature thermistor across the surface in contact mode, delivered the first meaningful shunt images under forward bias. However, it was too slow for general use. In 2000, LIT based on an IR camera and on-line data processing was used for the first time for shunt imaging in solar cells [10]. While LIT systems dedicated to NDE and stress analysis are available since many years (e.g. by Cedip, Stress Photonics, e/de/vis), meanwhile also systems dedicated to solar cell analysis are commercially available (e.g. by Thermosensorik, Aescusoft, InfraTec).

The original operation mode of LIT, which is still the most successful one for shunt investigation, is LIT performed in the dark by applying a pulsed bias to the device (Dark Lock-in Thermography, DLIT) [4]. Here the cell must be electrically contacted, hence only readily processed cells can be investigated. The advantage of this technique is that the thermal signal is caused only by the currents flowing in the dark. Hence, with DLIT shunt currents can easily be quantified [11]. Recently several new LIT techniques have been introduced, which are using pulsed light irradiation instead of a pulsed bias [12, 13]. The advantage of these "illuminated Lock-in Thermography" (ILIT) techniques is that, in simplest case, they don't need an electrical contact to the cell, hence they can image shunts already in an early technological state of processing. If there is a contact to the cells, depending on the electric load of the cell, different ILIT operation modes are possible, which are leading to different physical meanings of the obtained images (V_{oc} -ILIT, J_{sc} -ILIT, mpp-ILIT) [14]. A special technique called R_s -ILIT is able to image local inhomogeneities of the series resistance [15]. The limitation of all ILIT techniques (except R_s -ILIT) is that here the heat generation includes also carrier thermalization heat, both in the base and at the pn-junction, which leads to a homogeneous background signal and complicates the quantitative evaluation of the results [16].

Recently also electroluminescence (EL) and photoluminescence (PL) techniques have been proposed for shunt imaging [5, 6]. The resulting images are looking very similar to Light Beam-Induced Current (LBIC) images, but here the shunt imaging effect relies on the local reduction of the intrinsic bias around the shunts. A recent comparison between PL, EL, and DLIT has shown that stronger ohmic shunts and also some pre-breakdown sites can be imaged reliably by luminescence techniques, but weaker ohmic and non-linear shunts can not [17].

3. Shunt types

3.1. Pre-breakdown sites

Pure pre-breakdown sites show a low conductivity under low forward and reverse bias, but an exponentially increasing one at higher reverse bias. Hence, they do not decrease the parallel resistance R_p . Since they may create hot spots in a module by shading some cells, whereby the shaded cell may come under higher reverse bias, they may be dangerous for the reliability of solar modules [18]. Regarding a base doping concentration of 10^{16} cm^{-3} , solar cells should stand a reverse bias of nearly -100 V. In reality, especially multicrystalline (MC) cells often start to break down already between -5 and -15 V. Very little is known until now about the nature of pre-breakdown sites. Several authors have observed visible and IR light emission at pre-breakdown sites and have concluded that this is due to some avalanche effect [19]. So the reason for the pre-breakdown sites should be a local increase of the electric field in the junction region due to a non-planar shape of the junction. Indeed, we have found pre-breakdown sites in a region containing voids in the material, which should lead to high local fields. Similar effects are expected in positions where the pn-junction is spiking, e.g. at certain grain boundaries with preferential P diffusion. Fig. 1 shows a reverse bias

DLIT image of a pre-breakdown site (a) and a SEM image of a polished surface (b) of the shunt region where the voids are visible. This has been a pure pre-breakdown site, hence at low forward and reverse voltage there was no shunt in this region. Another example of pre-breakdown sites is shown in Fig. 2 [17]. Here the left image (a) shows DLIT results and the right image a luminescence image, both measured at -5 to -6 V reverse bias. The insets show that here the breakdown sites are below grid lines. Maybe in these sites there is a direct contact between grid lines and base material, yielding a kind of Schottky contact, which breaks down at relatively low reverse bias. Another explanation is that here some metallic impurities have diffused from the grid material to the pn-junction, leading to an increased generation current there, which is avalanche-multiplied under reverse bias. This interpretation is supported by the fact that in many cases pre-breakdown sites have been seen in positions of non-linear shunts (see section 3.3). Obviously, if there is a recombination-active defect crossing the pn-junction, which leads to a recombination current under low forward bias, this defect also leads to a generation current under low reverse bias. Under low reverse bias this generation current is so low that it remains undetectable by DLIT, but at higher reverse bias this generation current is amplified by avalanche multiplication, then leading to the typical pre-breakdown sites. This hypothesis, however, still has to be proven. To summarize, until now there is evidence for three mechanisms for pre-breakdown sites: (1) High field strengths due to a non-planar pn-junction, (2) breakdown of a Schottky-type shunt, and probably (3) avalanche amplification of the generation current of an extended defect crossing the pn junction.

Fig. 1: DLIT image of a MC cell taken at -12 V reverse bias (a), and SEM (SE) image of a void in a pre-breakdown position after polishing the surface

Fig. 2: DLIT image taken at -6 V (a) and electroluminescence (EL) image taken at -5 V (b) of a MC cell. The arrows at the right are pointing to some point-like pre-breakdown sites, which are only partly visible in EL [17]

3.2. Linear (ohmic) shunts

Only this type of shunts is significantly reducing the parallel resistance R_p of the cell. Linear shunts can easily be recognized by the fact that in the DLIT amplitude image they show the same brightness (= temperature modulation amplitude) at + 0.5 V forward bias and -0.5 V reverse bias. Since the dissipated power increases for linear shunts with the square of the applied bias, they can easily be detected under higher reverse bias by LC sheet imaging. The most trivial case of a linear

shunt is an incompletely opened edge of a cell, which shows up in DLIT as a bright spot or line at the edge [1]. The residual emitter at the edge can nicely be imaged by SEM (EBIC) [20]. A similar mechanism holds if a cracked wafer is processed. Also then the emitter may go through the crack up to the back contact, thereby creating a linear shunt. During screen printing of contacts even metal paste may be squeezed through a crack, after firing creating a very strong ohmic shunt [20]. Another important linear shunt type is created by Al particles at the surface, which may come e.g. from stacking solar cells after drying and before firing the metal pastes. If such an Al particle is lying on top of a solar cell, during a subsequent firing step it alloys into the surface, creating a p^+ -region around. This p^+ -region is in direct (ohmic) contact to the p-base, and it yields a tunnel-junction to the surrounding n^+ -emitter, thereby producing an ohmic connection between emitter and base [20]. Fig. 3 shows a SEM (SE) image of an Al particle on the surface of a monocrystalline solar cell together with an EDX spectrum showing the Al lines. Not only Al creates ohmic shunts if it is alloyed into the emitter. Fig. 4 shows a region in a solar cell where the surface was cut by a Nd:YAG laser [21]. Where the grid lines were cut by the laser, (nearly) ohmic shunts appear. Obviously the grid line material contains certain impurities (Al, B?), which are creating ohmic shunts if they are alloyed into the emitter, either due to p^+ doping or due to the introduction of a very high density of gap states. Outside of the grid line positions, the Nd:YAG laser generates only non-linear shunts (see section 3.4.). The laser parameters can be selected in such a way that the creation of ohmic shunts can be avoided [21].

Fig. 3: SEM (SE) image (a) and EDX spectrum of an Al particle on top of a solar cell, which created an ohmic shunt

Fig. 4: Forward bias (a) and reverse bias (b) DLIT image of a region cut with a Nd:YAG laser [21]

Another important ohmic shunt type exists only in multicrystalline (MC) material. Especially in the uppermost part of the silicon block there may be a supersaturation of dissolved carbon (C) in the Si melt. This C tends to precipitate during the cooling phase in the block in form of SiC filaments, which are growing preferentially in large-angle grain boundaries. By performing microscopic 4-probe measurements including conductivity type detection on single SiC filaments, we have found

that they are highly n-conducting [22]. The doping is most probably due to N, which also exists in the melt, since the crucibles are covered by a Si_3N_4 layer. By performing EBIC on the polished backside of a solar cell containing such shunts, we have proven that these shunts are yielding n-conducting channels crossing the whole bulk of the cell [20, 22]. These channels are directly electrically connected to the emitter, and they may also be electrically connected to the base contact, either by direct contact to the base contact metal (Al) or by yielding a tunnel junction to the p^+ BSF layer. However, we have found that not all SiC filaments crossing the cell are making ohmic shunts. Until now it is not clear under which conditions the SiC filaments are making ohmic shunts. Fig. 5 shows an EBIC image of the backside of a cell, showing the n-conducting channels along a grain boundary, and the corresponding SE image of a lightly etched backside of a shunt region in a MC cell. The bright spots in the EBIC image are the n-conducting channels crossing the whole cell.

Fig. 5: EBIC image (a) and SE image (b) of a linear shunt region, taken from the lightly etched backside of the cell

To summarize, altogether 5 mechanisms creating linear (ohmic) shunts were found: (1) Incompletely opened emitter at the edge, (2) crack, containing an emitter layer or metal paste, (3) Al particle at the surface, (4) laser cut through a grid line, and (5) SiC filaments in MC material.

3.3. Schottky-type shunts

It had already been mentioned in section 3.1. that, due to an unusually thin emitter layer or to inappropriate grid firing conditions, the grid metal of the emitter may come in contact with the base material. Another mechanism for Schottky-type shunts has been described in [20], which are texturization tips, which are mechanically truncated after emitter formation, thereby exposing the bare base material to the surface. There may be also other reasons leading to a "hole" in the emitter layer, e.g. dust particles at the surface during emitter formation or scratches after emitter diffusion. If the emitter grid crosses such a site, the grid metal comes in direct contact to the base. It can be expected that such a "Schottky junction" is everything else but an ideal Schottky diode. Only for ideal Schottky diodes we expect an ideality factor of 1 of the I-V characteristic. Note that forming ideal Schottky diodes requires extremely pure metallization conditions, which are definitely not given here. Instead, we expect the formation of a "dirty" Schottky diode implying certain interface layers, which govern its electric properties. It is well-known that "dirty" Schottky diodes may show a recombination factor larger than 1 and even larger than 2 [23]. Nevertheless, they show a certain rectifying characteristic and also pre-breakdown behavior. Hence, their I-V characteristic is non-linear (diode-like) with preferred conduction under forward bias of the cell. Indeed, Huster et al. [24] have shown that intentionally made Schottky shunts show a combination of rectifying and ohmic behavior. This makes Schottky-type shunts electrically similar to recombination-induced non-linear shunts, which are described in the following section. In fact, if a non-linear shunt or a pre-breakdown site is in the position of a grid line (see Fig. 2), it can only be suspected that this is a Schottky-type shunt. An alternative explanation of such a shunt would be that the underlying Si

material is "poisoned" by certain impurities coming from the grid metal paste. A clear distinction between Schottky-type and recombination-induced shunts could only be made e.g. by high-resolution EBIC imaging of the underlying n^+ -layer and its separate pn-junction in cross section. To the knowledge of the author, such an investigation has never been performed yet.

3.4. Recombination-induced shunts

According to the well-known two-diode model of a solar cell, there are two exponential components of the dark forward current: (1) The diffusion current (described by I_{01}) showing an ideality factor of $n_1 = 1$, and (2) the recombination current (described by I_{02}) showing an ideality factor of $n_2 \leq 2$. While the diffusion current is essentially due to electron injection from the emitter into the base, the recombination current is due to recombination in the depletion region. It has been found by several authors that, in absence of other shunts (in monocrystalline material), I_{02} is not proportional to the area but to the circumference of a cell. Obviously here the non-passivated edge represents a local (2-dimensional) extended defect crossing the pn-junction, which dominates I_{02} of the whole cell. Indeed, this edge leakage current can be imaged by DLIT under forward bias, as shown in Fig. 6. This sample was a MC cell with laser-isolated edges, where the left part was broken off. The original edges (at the top, right, and bottom) clearly show a higher leakage current (bright line) under forward bias than the broken edge at the left. Moreover, there are two ohmic shunts at the top (appearing also under reverse bias) and a lot of other shunts in the area, which also appear only under forward bias. These are typical material-induced non-linear shunts, which are caused by recombination-active extended crystal defects like dislocations, grain boundaries, or precipitates (see [20]), or by local material pollutions. Also scratches at the surface or fresh cracks of the cell are leading to non-linear recombination-induced shunts [20]. In fact, for most crystalline solar cells, the recombination current I_{02} , which dominates at + 0.5V forward bias, is not governed by the lifetime in the material, as predicted by elementary diode theory, but is mostly due to local extended crystal defects crossing the pn-junction. In the absence of material-originated recombination-active local defects, the usually non-passivated edge is the dominating recombination-induced "shunt". Only if the edge is lying well-passivated below a thermal oxide, as it is common for very high quality solar cells like PERL or PERT cells, the influence of the edge current or other recombination-induced shunts to I_{02} may be negligible.

Fig. 6: DLIT image of a part of a MC solar cell, which was laser edge-isolated, measured under +0.5 V forward bias (a) and -0.5 V reverse bias (b)

4. Understanding ideality factors larger than two of the dark I-V characteristic

According to the Shockley-Read-Hall (SRH) recombination model assuming isolated point defects, the ideality factor of the recombination current n_2 should be 2 or below. However, in many cases large values of $n_2 = 3$ or above have been measured [25]. Moreover, the quantitative value of I_{02} is usually several orders of magnitude larger than expected for the given lifetime in the base material [26]. Finally, in contrast to the saturation-type reverse characteristic expected by standard

diode theory, the reverse characteristic of most solar cells is linear or even superlinear. All these deviations from classical diode theory can be explained by the fact that I_{02} is not due to homogeneously distributed point defects but to local extended defects crossing the depletion region, as it has been shown in the previous section. Ideality factor mapping, which can also be done by performing DLIT at two different forward biases [11], indeed has revealed that also in MC cells the biggest part of the area shows an ideality factor close to 1, whereas all shunts, including the edge, show a large ideality factor, which may exceed 4. Nevertheless, for some cells with non-passivated edges $n_2 = 2$ holds. To clarify this obviously different behavior, diamond scratches with different loads have been made at room temperature on PERT cells, which originally all showed an ideal I-V characteristic with an ideality factor < 1.5 over the whole bias range [27].

Fig. 7 shows the resulting bias-dependent ideality factors. Since the scratch was between two grid lines, the series resistance R_s to this "artificial shunt" was easy to calculate with the R_s -corrected results also given for the highest load in Fig. 7. We see that for the lowest load, where the scratch did not reach the pn-junction yet, the ideality factor increases but remains at or below 2, but for the highest loads it exceeds even 4 over a large bias range. Our interpretation is that for a low defect density the defects are still isolated, hence they behave according to the Shockley-Read-Hall (SRH) recombination model. If the local defect density drastically increases, since the scratch is cutting through the pn-junction, the SRH model is not applicable anymore, but multi-level recombination has to be considered. We have shown that already considering simple two-level pair recombination is sufficient to describe saturation effects, which may lead to ideality factors larger than 2 in a limited bias range [27]. However, a generally accepted theory for multi-level recombination is still missing.

Fig. 7: Bias-dependent ideality factor of different PERT cells after diamond scratching under different loads. Dashed: 27 g results R_s -corrected.

Also the reverse characteristic of the scratched PERT cells drastically changed [27]. In the original cells the reverse current was in the low nA range and saturation-type, but it increased by several orders of magnitude and became linear in the scratched cells. Nevertheless, the current under -0.5 V reverse bias was still some orders of magnitude lower than the forward (recombination) current, so that it was not visible in DLIT (as for the non-linear shunts in Fig. 6). The temperature dependence of the reverse current was linear over $1/T^{1/4}$ in a wide temperature range, which is an indication of hopping conduction [28]. We believe that this is also a consequence of the high local density of states in the shunting defects, which allows inter-level transport across the pn-junction.

5. Conclusions

Since the introduction of lock-in thermography, the degree of understanding shunts in silicon solar cells has drastically improved. It is clear now that only certain shunt types have an ohmic characteristic, but many others have a non-linear one. Here one has to distinguish the behavior under low bias (± 0.5 V) from that under large reverse bias (several Volts), where pre-breakdown occurs. In this contribution we have identified two different pre-breakdown mechanisms, which are Schottky-type breakdown at grid lines and high local fields at a non-planar pn-junction, but certainly there are more mechanisms. Since pre-breakdown sites are often occurring in positions of non-linear

shunts, we are proposing here that also the generation current of extended defects crossing the pn-junction may get avalanche-multiplied under high reverse bias, but this hypothesis still has to be proven. Non-linear shunts at low bias may be due to Schottky-type defects (direct contact of grid lines to the base) or may be recombination-type shunts. The latter are caused by locally extended defects crossing the pn-junction. These may be the unpassivated edge of the cell, grown-in recombination-active crystal defects like dislocations, grain boundaries, or precipitates, or technological faults like scratches or fresh cracks. Ohmic shunts are due to an incompletely opened emitter layer at the edge, cracks containing an emitter layer or metal paste, Al particles at the surface, laser cuts through a grid line, or SiC filaments in MC material. The non-ideal I-V characteristic of most commercial solar cells, consisting in an unexpectedly large recombination current with a large ideality factor and an ohmic or superlinear reverse characteristic, can completely be explained by the fact that both the recombination current under forward bias and the reverse current are dominated by local extended defects, leading to non-linear shunts. An essential contribution to this current, both for mono- and multicrystalline cells, is the unpassivated edge region. Depending on the local density of recombination states in these defects, the recombination current may show either an ideality factor of $n_2 = 2$ or below, as predicted by SRH theory, or a higher n_2 due to the increasing dominance of multi-level recombination. Also a linear or superlinear reverse characteristic can be explained by hopping conduction across shunting extended defects with a high density of states.

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Advances in Thin Film Crystalline Silicon Solar Cells

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1. Introduction

The vast majority of today's PV modules are based on crystalline Si (c-Si) wafers. The reasons for this dominance are numerous, the most important ones being a high (12-18%) module efficiency and an excellent long-term stability. Si wafer PV modules are still getting cheaper ($\text{€}/\text{W}_\text{p}$) and/or more efficient every year, making them a moving target for any competing technology. However, there is one catch with Si wafers - cost. Today's standard Si wafer PV modules cost 2-3.5 $\text{€}/\text{W}_\text{p}$ to make, and almost half of this cost is due to the Si wafers. To further reduce cost, the PV industry is moving towards ever larger wafers. Simultaneously, it aims at reducing wafer thickness as far as possible, as this increases the cell area that can be obtained from a Si ingot. The minimum wafer thickness will be determined by the wafer breakage rates in the factories. Larger wafers will require larger minimal thickness. For very large wafers, it appears that a thickness of at least 100 μm will be required to keep wafer breakage under control. Compared to today's technology, the reduction of the Si consumption ($\text{g}/\text{W}_\text{p}$) seems to be limited to a factor of ~ 2 for conventional wafer-based PV technologies. Hence, the scope for substantial further cost reductions of Si wafer based PV modules is limited. Given these cost constraints, the need for a less material intensive c-Si PV technology - a thin-film technology - exists.

Due to a massively reduced Si consumption compared to today's standard PV modules, all thin-film technologies have significant potential for reducing the cost of PV. When using foreign substrates, further significant reductions are possible by moving towards very large substrates ($> 1 \text{ m}^2$), enabling a cheaper Si deposition process per cm^2 and a more streamlined cell metallisation and interconnection process. A convenient way to distinguish between the different c-Si thin-film PV technologies is the temperature stability of the supporting material, giving low-T, intermediate-T and high-T approaches. The supporting material acts either as substrate or superstrate for the solar cells in the finished module. The superstrate configuration offers cost advantages since the supporting material can also take over the role of the module's front cover sheet. The standard low-T supporting material for thin-film PV is tempered soda lime glass. An important intermediate-T material is a borosilicate float glass (Boro-float33) from Schott AG. Important high-T materials are c-Si wafers, ceramics, graphite, and steel. The cost of the substrate is a major issue for most high-T approaches. The standard Si homoepitaxy method is thermal CVD (chemical vapour deposition) at high T ($\sim 1100^\circ\text{C}$) [1]. The most important intermediate-T epitaxy methods are MBE (molecular beam epitaxy), IAD (ion-assisted deposition), and LPE (liquid phase epitaxy). MBE and IAD are physical vapour deposition methods which use an e-beam to melt and evaporate Si. The standard low-T Si deposition method is PECVD (plasma-enhanced chemical vapor deposition) using silane, giving hydrogenated amorphous silicon (a-Si:H) [2].

2. Growth of c-Si thin-films on native supporting materials

Naturally, the best c-Si films can be grown on native supporting materials ("Si homoepitaxy"). A native substrate eliminates problems associated with a mismatch of the thermal expansion coefficients of substrate and c-Si film, providing high-quality epi films using thermal CVD. Cell efficiencies of up to 17.6% for 40- μm Si films have been realised on Cz wafers, confirming that the approach is capable

of high thin-film cell efficiency on high-purity substrates [1]. High-purity substrates are obviously incompatible with low-cost PV, and hence a crucial issue with the high-T approach is the diffusion of impurities from a lower-purity substrate into the growing Si film. Application of the 17.6% cell process to lower-purity Si wafer substrates such as block-cast mc-Si wafers and SSP (Silicon Sheets from Powder) wafers reduced the cell efficiencies to about 13% and 8%, respectively [1]. This shows that in the case of high-T Si film growth, at least a medium-purity Si substrate seems to be required to obtain good efficiency. Alternatively, low-purity Si substrates can be used if coated with a suitable barrier layer material, followed by the preparation of a high-quality seed layer and subsequent epitaxial thickening of the seed [3]. A cell efficiency of over 11% has been achieved with this approach [3].

The approach of using c-Si wafer substrates for epitaxial thin-film cells is now often referred to as EpiWE (Epitaxial Wafer Equivalents) [4]. The approach has recently been thoroughly investigated in a European project (“SWEET”) [4]. It has shown that, with the exception of the thin-film cell growth step and the surface texturing step, all cell and module fabrication steps are compatible with a standard Si wafer PV line using screen-printed contacts. EpiWE is thus a non-disruptive PV technology that should find its way into the factories. Using large heavily-doped PV-inactive high-purity block-cast mc-Si wafer substrates and high-T Si growth, screen-printed EpiWE cells with good efficiency of ~13.5% were realised in SWEET, using 20- μm Si films. This confirms that EpiWE is compatible with standard PV lines using screen-printed contacts and provides similar efficiency. Importantly, SWEET also showed that high-quality Si epi films can be grown in an *in-line* CVD reactor. It is possible that medium-purity multicrystalline Si wafers made via block casting or ribbon growth of “upgraded metallurgical-grade” (UMG) silicon will be sufficient for making efficient ($> 12\%$) EpiWE solar cells.

The epitaxial thin-film cells discussed above are based on low-cost Si wafer substrates, whereby these substrates are destined to end up in the final PV module. An alternative approach is to use a high-quality singlecrystal Si wafer substrate, to fabricate a separation layer on/in this substrate, to grow a singlecrystal Si thin-film diode on the separation layer, and then transfer the thin-film diode to a low-cost foreign substrate. The process cycle is then repeated many times, whereby the same Si wafer substrate is re-used for epitaxial film growth. To be competitive for PV, the key requirements of these *Si transfer processes* are low material consumption, a simple fabrication process, and a good PV efficiency ($> 15\%$). One example for such a technology is the PSI process [5] where a (100)-oriented sc-Si wafer is chemically textured (pyramids), followed by the formation of a thin porous Si separation layer. Then a thin-film Si diode is epitaxially grown at high T and transferred to a glass substrate. An efficiency of 12.2% has been realised [6]. Another layer transfer process has been developed by Sony Corp. in the 1990s. It uses a porous silicon double-layer stack on a sc-Si wafer substrate [7]. The buried porous layer has a high porosity and serves as the separation layer. The exposed porous layer has a low porosity. During a high-T anneal above 1000°C, structural changes occur in the porous double-layer stack. The low-porosity film converts into a singlecrystalline film with internal voids and a continuous top surface, whereby this film serves as a seed layer for high-T CVD epitaxy. Following epitaxy, the Si wafer substrate is separated from the thin-film structure and reused. Using a 12 μm thick epitaxial film that was detached from the substrate, Sony have obtained cell efficiencies of up to 12.5% [7]. Using related approaches, Bergmann *et al.* [8] at U Stuttgart achieved 16.6% cell efficiency for a 44.5 μm thick Si film and Brendel *et al.* [9] at ZAE Bavaria achieved 15.4% for a 25.5 μm thick cell.

3. Growth of c-Si thin-films on foreign supporting materials

3.1 High-T approaches

In the category of high-T foreign supporting materials, despite significant advances, no technology has advanced as yet to the pilot line stage. The most promising high-T supporting materials for thin-film

growth appear to be graphite [10] and ceramics such as silicon carbide [11], alumina [12], and glass ceramics [13, 14]. However, major breakthroughs are required before these PV technologies can be commercialized. The most important high-T Si deposition method is thermal CVD. Prototypes of production-type high-T CVD reactors for PV Si epitaxy purposes are presently being developed [15]. It is expected that such machines will reduce the costs of the Si epitaxy step to $\sim 10 \text{ €/m}^2$. The common issues of high-T resistant foreign supporting materials are cost, availability, and impurity content. Furthermore, many foreign materials have a porous structure, which makes conventional wet-chemical processing difficult. One way to overcome the problems associated with impurities and porosity is to encapsulate the supporting material with a smoothening barrier layer.

In 1997, a collaboration between ASE and Fraunhofer ISE resulted in 11.0% polycrystalline Si (pc-Si) thin-film cells on SiC-coated graphite [10]. Upon encapsulation of the substrate with SiC, a fine-grained 40 μm thick p^+ -doped pc-Si film was grown by thermal CVD. This p^+ film was then subjected to a ZMR step, giving a large-grained p^+ layer that served both as the seed layer for the epitaxial growth of the absorber layer and as the BSF layer of the finished cell. The active layer (15-30 μm) was made by thermal CVD. The n^+ emitter was formed by P diffusion. The cell process used dry processing (reactive ion etching, RIE) instead of wet-chemical processing. Despite the respectable efficiency of 11%, major improvements are required to make the technology economical compared to EpiWE.

Seed layers by AIC (Aluminium-Induced Crystallisation) of a-Si are also an interesting route for epitaxial cells on high-T substrates. Although developed for glass, researchers at IMEC have shown that the AIC process also works well on high-T substrates such as alumina [12] and glass ceramics [13, 14]. Prior to the AIC process, the alumina substrates are coated with a spin-on oxide to reduce the surface roughness. Using thermal CVD for epitaxial cell growth on AIC-seeded alumina substrates, efficiencies of up to 8.0% and voltages of up to 536 mV have been realised [12]. Total Si film thickness is in the 2-4 μm range. The n^+ emitter is a heterojunction emitter formed at low T by depositing doped a-Si, similar to Sanyo's HIT Si wafer cells [16]. The IMEC team has also applied the process to high-T resistant glass ceramics (Corning 9664), giving 5.4% cells [13]. However, glass ceramics are far too expensive for PV applications and hence are merely useful for process development purposes.

3.2 Intermediate-T approaches

Tremendous progress has been made in the last 15 years with intermediate-T approaches. By the late 1990s, Yamamoto *et al.* at Kaneka Corp. had achieved 10.1% initial efficiency for the STAR cell, which is a 2 μm thick $\mu\text{c-Si:H}$ cell grown by hot (up to 550°C) 13.56-MHz PECVD on a glass substrate coated with a conductive BSR [17]. Despite this excellent result, this work seems to have been abandoned and redirected towards low-T grown micromorph tandem cells. Work at another Japanese company, Sanyo Electric, during the early 1990s showed that solid phase crystallisation (SPC) at 600°C of a relatively thick ($\sim 5 \mu\text{m}$) PECVD-deposited a-Si film gives 9.2% efficiency on a metal substrate [18]. The cells featured a p^+ -doped a-Si heterojunction emitter on a n^+n pc-Si structure crystallised by SPC. The V_{oc} of 553 mV is the highest ever reported for a thin-film solar cell having a pc-Si absorber layer made at low or intermediate T. Despite these excellent results, this thin-film solar cell work seems to have been abandoned at Sanyo around 1996 and efforts re-directed towards a-Si heterojunction emitters on sc-Si wafers ("HIT cell") [16].

In the late 1990s, Pacific Solar, a spin-off company of the University of New South Wales (UNSW), successfully transferred the PECVD-based SPC approach to borosilicate glass (Borofloat33 from Schott AG). Major breakthroughs have been achieved in the following years in the areas of light trapping (novel glass texture [19]) and cell metallisation and interconnection (point contacts [20]). The best efficiency obtained so far with this so-called CSG (Crystalline Silicon on Glass) technology is 9.8%, realised in 2006 using a 96- cm^2 , 20-cell mini-module with a FF of 74.5%, a J_{sc} of 27.0 mA/cm^2 , and an average cell V_{oc} of 487 mV [21]. CSG devices feature excellent light trapping properties,

enabling short-circuit current densities of 27 mA/cm^2 with $1.5 \text{ }\mu\text{m}$ thin pc-Si films. To achieve light trapping, both surfaces of a borosilicate glass superstrate are textured with a dip coating process that leaves a monolayer of silica beads embedded in a sol-gel matrix. A silicon nitride AR coating is deposited onto one surface, followed by deposition using PECVD at 45 nm/min of a-Si having an n^+pp^+ structure. The Si-coated glass sheets are heated to 600°C in a batch oven for several hours to achieve solid-phase crystallisation. Crystallographic defects are annealed by heating the c-Si briefly to over 900°C , using a RTA process. Most of the remaining defects are passivated by exposure to atomic hydrogen [22]. Device fabrication starts by using a pulsed laser to slice the Si layer into a series of adjacent, $\sim 6 \text{ mm}$ wide strip cells. The module is then coated with a thin layer of Novolac resin loaded with white pigments to make it more reflective and thus improve light trapping in the cell. Next the openings for the n -type contacts (“craters”) are formed. This involves etching of openings into the resin layer (using an ink-jet printhead), followed by chemical etching of the Si. Then the openings for the p -type contacts are formed using the same ink-jet process. A blanket deposition of sputtered Al provides electrical contact to the n^+ and p^+ Si layers. The Al film is then sliced into a large number of individual pads using laser pulses. Each metal pad series connects one line of p -type contacts in one cell with a line of n -type contacts in the next cell [22]. The strengths of the CSG technology include a simple solar cell structure, a robust fabrication process, and an expected excellent long-term stability. In 2004 a group of investors acquired the technology and formed a new company, CSG Solar AG. The company has established the first CSG factory in Thalheim, Germany, with a rated capacity of $10 \text{ MW}_p/\text{year}$. Si is deposited in a KAI-1200 PECVD tool from Oerlikon, using 1.4 m^2 glass sheets. Best module efficiencies were around 7% at the end of 2006 and were improving steadily. A second KAI machine has been installed in 2007, doubling the rated factory capacity to $20 \text{ MW}_p/\text{yr}$. For a factory producing $20 \text{ MW}_p/\text{yr}$ of 8% efficient CSG modules, the expected module fabrication costs are $\sim 1.50 \text{ €/W}_p$ [22].

Independent research on PECVD-deposited n^+pp^+ SPC cells on glass (“PLASMA”) in the author’s group at UNSW has so far led to cell efficiencies of up to 7.0% [23]. The best cell has a V_{oc} of 491 mV, a FF of 70.5%, a J_{sc} of 20.1 mA/cm^2 , a cell area of 4.4 cm^2 , and a Si thickness of $4 \text{ }\mu\text{m}$. The main differences to the CSG devices mentioned above are alternative methods for creating the textured glass surface, the p^+ BSF layer, and the cell electrodes. It is noted that this 7% PLASMA cell has a full-area Al rear contact. Al performs poorly as a BSR, and particularly so on textured surfaces [24]. Hence, these PLASMA cells have rather modest light trapping properties. Significant improvements of the cell efficiency are expected from the implementation of an improved BSR. The metallisation of PLASMA cells is based on interdigitated comb-like grids ($\sim 500 \text{ nm}$ thick Al) for both cell electrodes. The glass texturing method is referred to by us as Aluminium-Induced Texturisation (AIT) [25]. It is based on a thermally activated chemical reaction between the glass and a sacrificial evaporated Al layer. Following this anneal, the reaction products are removed by wet-chemical etching. By modifying the Si deposition process, we have been able to improve the V_{oc} of non-metallised PLASMA samples to 528 mV and to reduce the contribution of $n=2$ recombination to negligible levels. This is the highest V_{oc} ever reported for a homojunction poly-Si thin-film solar cell on glass.

The intermediate-T cells discussed above were all deposited by PECVD. While this is a widely used Si deposition method in the display and PV industries, it suffers from a number of disadvantages including a low Si deposition rate ($< 50 \text{ nm/min}$), poor Si usage ($< 20\%$), and high equipment cost [26]. For example, for a glass size of 1.4 m^2 , a typical PECVD batch system costs over $\text{€ } 10$ million. For CSG Solar’s poly-Si on glass PV technology (Si film $1.5 \text{ }\mu\text{m}$), the PECVD silicon deposition process costs $\sim 30 \text{ €/m}^2$ and thus contributes about 25% to the total fabrication cost of the module [22]. Given the significant cost of PECVD-deposited Si films, it is not surprising that major efforts are devoted to the development of more cost-effective Si deposition methods. Techniques being explored include hot-wire CVD and electron-beam evaporation [26]. E-beam evaporation is particularly interesting as it has a very high Si deposition rate (up to $1 \text{ }\mu\text{m/min}$), a good Si source material usage,

avoids toxic gases, and is potentially a low-cost method [26]. Research at UNSW during recent years has shown that e-beam evaporation of Si in a non-UHV process produces a-Si precursor diodes that are well suited to SPC on borosilicate glass [26]. The resulting poly-Si thin-film solar cells are referred to as EVA cells (“solid phase crystallisation of EVApored Si”). The cell structure is glass/SiN/ n^+/n^- (or p^-/p^+). The deposition of the a-Si occurs at a glass temperature of $\sim 200^\circ\text{C}$ and at a pressure of about 10^{-7} Torr. To realise the desired dopant profiles, phosphorus and boron are added in-situ (i.e., during the Si deposition) via effusion cells. TEM images reveal that EVA cells are of good structural quality and that their grain size is of the order of 1 μm . The best V_{oc} of EVA samples realised so far is 517 mV [27].

One path towards improved pc-Si solar cells on glass is the seed layer concept where the material fabrication process is separated into two steps: 1) Formation of a thin, large-grained, heavily doped pc-Si seed layer on the (barrier-coated) glass pane; 2) Deposition of the remainder of the solar cell structure, exploiting the crystalline information of the seed layer. The seed layer can serve as either the emitter or the BSF layer of the cell. AIC (Aluminium-Induced Crystallisation) of a-Si is a seed layer method that has received a lot of attention in the Si thin-film PV community [12, 13, 14, 28]. The AIC method was invented in the 1970s to create epitaxial p^+ -type surface layers on sc-Si wafers. In the late 1990s, Nast *et al.* [29] at UNSW transferred the AIC process from Si wafers to glass substrates. The AIC method on glass was then refined by the author’s group at UNSW [30] and used as seed layer method in two different intermediate-T solar cells, ALICE and ALICIA. The AIC precursor structure is glass/SiN (~ 80 nm)/Al (~ 200 nm, evaporated)/a-Si (~ 300 nm, sputtered). This structure is annealed for 12 h at 450°C in a tube furnace and then the Al and the excess Si (“Si islands”) are removed. The crystal quality of the resulting AIC seed layers is very high.

ALICE stands for “ALuminium-Induced Crystallisation, solid-phase Epitaxy”. The idea behind ALICE cells is to deposit the absorber (plus BSF layer) onto a hydrogen-terminated AIC seed layer at very low T ($\sim 200^\circ\text{C}$) as amorphous material and then to crystallise the a-Si at elevated T ($\sim 600^\circ\text{C}$). This method is related to solid-phase crystallisation (SPC), however, because of the presence of a crystalline seed layer, it is actually a solid-phase *epitaxy* (SPE) process. The key feature in the ALICE process is a crystallographic transferral of information during the thermal anneal from the AIC seed layer into the crystallising a-Si overlayer. Texturing of the glass is realised with the AIT method. The AIC seed layer method works well on mildly textured AIT glass panes. The best V_{oc} of ALICE samples realised so far is 480 mV [31]. The best efficiency is presently 4.8% and was obtained with PECVD-deposited a-Si. ALICIA stands for “ALuminium-Induced Crystallisation, Ion-Assisted deposition” [32]. The idea behind ALICIA cells is to directly (i.e., *epitaxially*) grow the crystalline absorber layer (and the BSF layer) on a hydrogen-terminated AIC seed layer at relatively low Si epitaxy temperature ($\sim 600^\circ\text{C}$). For low-temperature epitaxy we use IAD (ion-assisted deposition) because this method is capable of high-rate Si growth at low (i.e., glass-compatible) temperature. The IAD process runs in a non-UHV environment but nevertheless, due to the high deposition rate, can give high-quality Si films [33]. The best V_{oc} of ALICIA cells is presently ~ 440 mV. Texturing of the glass is realised with the AIT method. The best efficiency of ALICIA cells on glass is presently $\sim 2.5\%$ and is limited by a short diffusion length of about 0.5 μm in the absorber layer and a poor back surface reflector (Al film) [24]. While the quality of the (100)-oriented grains of ALICIA material seems sufficient, the challenge with this technology seems to be the realisation of a sufficient crystal quality for (111)-oriented grains.

Another intermediate-T seed layer approach is the LLC (Layered Laser Crystallisation) process developed at IPHT in Germany [34]). In the baseline LLC process, a 13.56-MHz PECVD tool for doped a-Si is connected to two different lasers: a cw argon ion laser (6 W, 514 nm, 0.008 mm² beam area) and a pulsed KrF excimer laser (248 nm, 7 $\times$ 7 mm² cross section, 25 ns pulses). In a first step, a large-grained (> 100 μm) p^+ -doped seed layer is prepared on heated glass ($\sim 600^\circ\text{C}$) by PECVD deposition of doped a-Si:H (~ 400 nm) and subsequent row-by-row laser crystallisation with the Ar ion

laser. The row width is 50 μm and the laser scanning speed 5 cm/s. This seed layer is referred to as ISC layer (In-chamber Seed Crystallisation). In the second step, the hot PECVD deposition is continued for the growth of the p-type base ($\sim 5\text{ }\mu\text{m}$) and the thin ($\sim 100\text{ nm}$) n^+ -type emitter of the cell. During the PECVD deposition, the sample is irradiated in regular intervals with a single pulse from the excimer laser. Each laser pulse crystallises a 20-80 nm thick a-Si:H layer, whereby the illuminated area is $7\times 7\text{ mm}^2$. The resulting devices are referred to as ISC-CVD cells. ISC-CVD cells achieve good voltages of up to 510 mV and efficiencies of up to 4.8% [34]. To improve the industrial relevance of the LLC process, the IPHT researchers have implemented two major changes to their baseline sequence. First, the laser power used for seed layer crystallisation has been increased by more than two orders of magnitude. This was realised with a high-powered diode laser (cw, 750 W, 806 nm, 0.3 mm^2 beam area). Due to geometrical constraints within their PECVD tool, the IPHT team conducts the seed layer crystallisation outside the PECVD tool in ambient air. The method is referred to as ESC (External Seed Crystallisation). Compared to the ISC method, the ESC seed layer method is much faster. The second change to the baseline LLC process is the replacement of slow PECVD Si deposition by fast e-beam evaporation. Epitaxial thickening in the e-beam evaporator (EBE) is performed using the same excimer laser parameters as in the PECVD process. The resulting devices are referred to as ESC-EBE cells. ESC-EBE solar cells achieve good voltages of up to 506 mV and efficiencies of up to 3.8% [34].

3.3 Low-T approaches

Work in the 1970s has established hydrogenated a-Si (a-Si:H) deposited by PECVD at $\sim 200^\circ\text{C}$ as the baseline thin-film PV technology [35]. The technology possesses a number of excellent properties for low-cost PV, including a high optical absorption coefficient of the semiconductor (enabling very thin absorber layers of 300 nm), large-area Si diode deposition at low T onto rigid or flexible substrates, and monolithic series interconnection of the individual cells. The only reason why a-Si:H has not been able to conquer a significant share of the PV market is the low stable average efficiency of 6% or less of large single-junction PV modules [36]. One factor behind this modest efficiency is the Staebler-Wronski effect. Research is continuing into finding ways to reduce this effect, however, after two decades of intense research it seems that the prospects are limited. The highest confirmed stable efficiency for a single-junction a-Si:H cell is 9.5%, obtained by U Neuchatel [37]. Another reason are manufacturing related issues associated with the processing of large substrates, including spatial non-uniformities in the films [36]. There is scope for significant improvement in this area, and hence large single-junction a-Si:H modules with stable efficiency of 7-8% should soon be available. The a-Si:H PV technology shares research and infrastructure costs with the liquid crystal display (LCD) industry and hence benefits from the development of large-scale, high-throughput PECVD Si deposition systems for LCD applications. Several of the leading manufacturers of LCD equipment are now offering turn-key production lines for a-Si:H PV modules on large glass substrates. For 1.4 m^2 glass size, each PECVD machine now has a throughput of well over 10 MW_p/yr of single-junction a-Si:H PV modules.

A particularly attractive feature of the a-Si:H PV technology is that the low-T Si deposition process *immediately* produces device-grade Si material, i.e. it is not necessary to perform any post-deposition treatments on the diodes. Over the past 20 years, research has been conducted along the lines of preserving this attractive feature, but obtaining solar cells with higher stable efficiency. Using the very-high-frequency (VHF) PECVD method, researchers at U Neuchatel in the early 1990s succeeded to fabricate the first hydrogenated microcrystalline Si ($\mu\text{c-Si:H}$) cells at 200°C with reasonable efficiencies [38]. Importantly, the cell efficiency was stable under light soaking conditions, giving hope to significantly higher stable module efficiency than for a-Si:H modules. Microcrystalline Si is grown using strong hydrogen dilution of silane (silane concentration of $< 10\%$). The material has an optical absorption coefficient that is quite similar to that of pc-Si and its optical bandgap energy is $\sim 1.0\text{ eV}$ [2]. It contains both amorphous and crystalline regions. For suitable deposition conditions

films with columnar grains are obtained [39]. The crystalline growth starts at nucleation centres near the film/substrate interface. The columnar grains have widths in the 30-100 nm range and can be several μm long. The space between these crystalline grains is filled with a-Si and/or voids. The crystalline volume content of the films depends on the deposition conditions, in particular the silane content in the gas mix. When increasing the silane content from 2 to 10%, the crystalline volume fraction initially remains approximately constant up to $\sim 6\%$ and then drops rapidly. The regime around 6% silane concentration is called the “transition region” and gives the best $\mu\text{c-Si:H}$ solar cells [39]. By the end of the 1990s, low-T $\mu\text{c-Si:H}$ solar cells on glass had stable efficiencies of up to 8.5% [2]. However, due to the low deposition rate ($< 40 \text{ nm/min}$) of the $\mu\text{c-Si:H}$ film and technical difficulties with the development of industrial-scale VHF-PECVD systems, $\mu\text{c-Si:H}$ single-junction solar cells do not seem to be commercially viable at present. The same conclusion appears to apply to the 10% efficient $\mu\text{c-Si:H}$ solar cells developed at Kaneka using intermediate-T ($\sim 550^\circ\text{C}$) 13.56-MHz PECVD [17].

The industrial relevance of $\mu\text{c-Si:H}$ solar cells improves enormously if they are combined with thin a-Si:H top cells, forming a 2-cell tandem stack. U Neuchatel has pioneered this device in the early 1990s and coined the term “micromorph” for this tandem cell on a TCO-coated glass superstrate [2]. In 1994, the team reported an excellent initial efficiency of 13.1% [40]. The micromorph concept has been taken up by other organisations, most quickly by Kaneka in Japan, and in 2001 this company started a pilot production of their so-called “hybrid” thin-film PV cells [41]. The Si is deposited at low T by 13.56-MHz PECVD onto a large ($\sim 0.85 \text{ m}^2$) TCO-coated soda lime glass superstrate and metallisation is performed such that two separate PV modules are formed on the large sheet of glass [41]. The $\mu\text{c-Si:H}$ cell is about $2 \mu\text{m}$ thick, whereas the a-Si:H top cell is about 5 times thinner. Light trapping is realised as in the company’s *pin* a-Si solar cells, however, to further boost the efficiency a thin TCO interlayer is inserted between the a-Si:H and the $\mu\text{c-Si:H}$ cell. The purpose of this interlayer is to increase the current of the a-Si:H top cell, enabling a thinner a-Si:H cell and hence a more stable tandem device. Excellent initial efficiencies (aperture area) of over 12% were reported for these large (0.41 m^2) all-silicon modules. The best cell (area 1 cm^2) made so far has an initial efficiency of 14.5% [42]. The best stable efficiency confirmed as yet is 11.7%, realised by Kaneka in 2004 [43]. The strengths of the technology are the expected high stable average efficiency of 10% for large-area mass-produced modules and the fact that established large-area low-T processing equipment from the LCD industry can be used. Weaknesses are the requirement of a textured TCO layer and the relatively long deposition time ($> 30 \text{ min}$) for the $\sim 2 \mu\text{m}$ thick $\mu\text{c-Si:H}$ cell. Kaneka has recently announced that it will start to offer hybrid silicon thin-film PV modules with a glass size of 1.22 m^2 and a rated power output of 125 W_p . This corresponds to a total-area efficiency (stabilised) of 10.2%, suggesting that these will be the first commercial Si-based thin-film PV modules with an efficiency of above 10%. Several other companies have also announced to manufacture micromorph PV modules.

4. Conclusions

The field of c-Si thin-film materials for solar cells has been reviewed. The enormous interest in these Si materials results from the belief that they will enable long-term stable ($> 25 \text{ years}$) and efficient ($> 10\%$) PV modules that can be made at much lower costs than Si wafer based PV modules and without any material supply and toxicity issues. Progress in recent years has been excellent and the first c-Si thin-film PV technology is now in commercial production (CSG Solar), delivering large (1.4 m^2) modules with stable efficiencies in the 6-8% range. The rated capacity of the CSG factory is $20 \text{ MW}_\text{p}/\text{yr}$ and the fabrication costs of CSG modules have been estimated as $\sim 1.5 \text{ €/W}_\text{p}$. The CSG technology uses a very thin ($< 2 \mu\text{m}$) pc-Si film on a glass superstrate. For another c-Si related thin-film PV technology, the micromorph tandem cell (which consists of an a-Si:H top cell and a $\mu\text{c-Si:H}$ bottom cell on a glass superstrate), several factories are presently being built worldwide and will soon be

operational. Large micromorph modules are expected to have stable efficiencies in the 8-10% range and manufacturing costs of ~ 2 €/W_p. Progress has also been very good with other c-Si thin-film PV technologies, and several of these (including PLASMA, EVA, SOPHE, ALICE, EpiWE, silicon on graphite or alumina) are now ready for testing at the pilot line scale.

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Thin Solar Cells: Issues and Processing for High Efficiency

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The past three years we have assisted to a drastic reduction of wafer thickness in industrial solar cells, from an average of 330 μm in the beginning of 2004 down to 210 μm in 2007, with some companies producing cells on 180 μm substrates. Technically speaking, it should have been possible to maintain or even improve the conversion efficiency on thinner substrates; moreover, the lower silicon content should have brought down costs and prices of solar cells. Things went differently.

Commercial cell efficiencies decreased slightly, and prices increased significantly throughout the whole PV value chain. Feedstock prices rocketed, the increased margins due to the better efficiency of use of silicon stayed with polysilicon and wafer producers. The industry did well anyway, as the high subsidies allowed for the costs to be charged downstream, annoying policy makers and, throughout 2006, end costumers. There is not yet a consensus as of when and how PV market will go back on track -prices are now falling but potential for demand is still very high and the feedstock shortage is not yet over- but let's assume that, at some point, silicon prices would return to normality, that margins would be redistributed more evenly throughout the value chain and that thinner wafers would actually result -like they should- in a lower solar electricity cost.

All wafer manufacturers could easily switch their full production to 180 μm substrates today and to 150 μm in no more than two years, with some companies being confident in being able to deliver even 120 μm substrates at >90% yield within 5 years, if there would be buyers for it. But yield and efficiency losses in cell manufacturing are such that there is no demand for these substrates.

In this review, we will address the reasons for this technology bottleneck and the shortcomings of cell manufacturing. We will first discuss the necessity, if any, of processing thinner and thinner substrates by using a rough cost model for PV electricity. We will then review the technologies which can be potentially and actually used for the large scale production of thin cells, focusing on design issues, processing issues, local contact formation and surface passivation. Finally, we will report on actual cell results on large area ultra-thin substrates with industrially viable processes, to demonstrate that there exist solutions with a 2-3 years time to market. It is to be expected that wafer thinning in industry will proceed at least down to the 100-120 μm range.

Costs

We built up our cost model from publicly available data, information collected from wafer, cell and module manufacturers that will not be disclosed, and we used internal data to evaluate additional running costs and costs of ownership due to processing steps which have to be introduced to process ultra-thin substrates. We consider a typical module of 72 cells. We assume, unless otherwise specified, a feedstock price of 60\$/Kg. All other parameters are calculated assuming no profit. We take into account recycling and yield losses through the complete process chain and use a cell to module efficiency of 0.86-0.88. We scale the BOS costs with the efficiency of the module. For a multicrystalline silicon module with average cell efficiency of 15.7% (13.8% module efficiency), 220 μm cell thickness with 200 μm kerf loss, we derive a system cost of 4.84\$/Wp with a silicon usage of 9.6g-Si/Wp; for a monocrystalline silicon module with average cell efficiency of 17% (14.7% module efficiency) we derive a system cost of 4.89\$/Wp with 8.6g-Si/Wp¹. With an average yearly production of 1000 kWh/kWp and a lifetime of 20 years this would correspond to a PV electricity cost of 0.27\$/kWh.

¹ Photon International publishes cost figures up to 25% lower. Our data on module and cell processing may not reflect best practice. This would actually increase the sensitivity of the module cost on feedstock.

Figure 1. Module cost breakdown for a 220 μm mc-Si solar cell with 16% efficiency and influence of wafer thickness and feedstock price on module cost. No profit is assumed in the value chain after feedstock.

Reduction of processing costs in PV can be expected to take place rather smoothly, due to the fast pace at which production capacity is increasing which favours the economy of scale. Material costs, which represent an important fraction of module and wafer costs, may have a hard way to follow the same path (the cases of silicon and glass being the prominent ones). In this case, the reduction of material content per unit power is the primary way for further cost reduction. Even with a relatively fair pricing of silicon of 60\$/Kg, if we were able to produce 120 μm solar cells with the same efficiency that we have on 220 μm substrates, we would save 10% of the costs at module level. With an average purchase price of 110\$/Kg, this figure would increase to 17%. In the present situation, no doubt that going thinner would always pay off. As silicon prices will relax, it may be argued whether there is a real advantage in going *that* thin. The relative weight of kerf losses in the cost breakdown is bound to become larger and larger, reducing to some extent the positive effect of wafer thinning. Higher efficiencies -which today seems more likely on thicker substrates- could effectively reduce the grams of silicon per watt peak, making it less dominant and at the same time reducing the saving margins of thinner substrates. Introducing rear surface passivation and local contacts would make the production of thin substrates possible but would also introduce an efficiency premium on standard wafers. Unless the gain is substantial, the concern of possible yield issues would dissuade cell and module manufacturers to go below the 160-180 μm threshold, even if it were technologically feasible, and focus on other cost levers.

To try to comment on this we need to model, at least roughly, the evolution of system costs in function of different variables. We take into consideration 8 intervals of time, each corresponding to roughly one year and a decrease in 10 μm of the wafer thickness, bringing it from 180 μm (main wafer thickness by the end of next year) down to 120 μm . Over the same time span, we assume that efficiency will increase from 16% to final values of 17.25% for multicrystalline cells, and from 17.5% to 19.5% for monocrystalline cells. Kerf loss is assumed to decrease to a final value of 150 μm , module and cell processing cost to decrease at a rate of 5% per time interval and BOS cost at a rate of 10% per time interval. The results are shown in figure 2 (only the Cz-Si case is shown for clarity; mc-Si curves are nearly identical).

Even with efficiency growing to nearly 20% wafer thickness would remain a dominant cost factor, resulting in differences of nearly 9% at module level between 180 and 120 μm substrates. Thinking of the timescale which is involved it's realistic to assume that processing cost can be reduced at a faster pace than efficiency can be improved (relative to its impact on cost/Wp). This means that the relative weight of feedstock cost in the system breakdown will increase, in future, despite higher cell efficiencies.

Figure 2. Cost difference between a constant 180μm wafer thickness and a variable thickness (down to 120μm) scenario for monocrystalline industrial cells.

With reference to Figure 2, consider that a 19% cell of 180μm at T8 would yield the same system cost of a 17% cell of 120μm. Within certain boundaries it makes even more sense to go thinner than to increase cells' efficiency. Looking at the graph and at the experience of the past years there should be enough time to address yield losses in manufacturing and margins to tolerate a slightly higher breakage rate.

Technology

We want to achieve higher efficiencies on thinner substrates in order to reduce the costs further. It is now widely accepted that this cannot be done with conventional full area screen printed aluminum BSF and that there should be a migration to structures with better optical confinement, surface passivation and local contacts. 150μm substrates will probably set the threshold where electrical losses cannot be compensated by lower production costs, irrespective of the process yield.

The first efficiency limiting factor that appears in industrial solar cells below 200μm is an internal rear surface reflectance that for typical cells is in the range of 50%. The thinner the cell, the worse the influence of surface recombination at the Al BSF contact, which results in a strong reduction of the carrier collection efficiency and, to a lesser extent, of open circuit voltage. We may attempt to tackle this issue either by radically innovating the solar cell process design, possibly aiming at very high efficiency as a means to compensate for increased process complexity and cost, or by incremental technology improvements; In this paper we will only focus on the latter approach.

The lowest quality of surface passivation that is necessary to avoid additional recombination losses when thinning a solar cell is easily determined and we will repeat here the analysis which we proposed in [1]. The rear surface recombination velocity (SRV) has to be lower than the effective 'bulk recombination velocity' S_{bulk} that is, the integral recombination rate between a point W at given distance from the junction and the rear surface of the device, divided by the minority carrier density at that point. For simplicity, consider a pn junction and an infinite, homogeneous p-type base. We may write

$$S_{bulk}(W) = \frac{1}{\Delta n(W)} \int_W^{\infty} U(z) dz \quad (1)$$

given that

$$\Delta n(z) = \Delta n(0) \cdot e^{-z/L} \quad (2)$$

and

$$U(z) = \frac{\Delta n(z)}{\tau} \quad (3)$$

it is easy to demonstrate that S_{bulk} is a constant and equal to the ratio D/L , D being the minority carrier diffusion coefficient and L the bulk diffusion length. With a rear surface recombination velocity $S_{\text{rear}}=S_{\text{bulk}}$, the base saturation current of the solar cell and (hence) the collection probability profile $f_c(z)$ remain the same whichever the base thickness. In other words, as long as the generation profile is the same the cell(s) performance will be the same. The smaller the diffusion length and the higher² the resistivity, the larger the admitted rear surface recombination velocity. The D/L ratio for standard 1-2 Ohm.cm mc-Si material, assuming a fairly good diffusion length of 300 μm , is about 900-1000 cm/s, a value well above the surface recombination velocities that can be achieved e.g. with intrinsic amorphous silicon or hydrogenated silicon nitride layers but still challenging for the surface recombination velocities that can be attained with aluminum-alloyed back surface fields.

The importance of the rear surface reflector is coupled with the cell thickness as well as the bulk diffusion length and surface recombination velocity. As long as $L < 2W$ (W being now the base thickness) and $S_{\text{rear}} < D/L$, the rear surface reflector is less critical: a reflectance above 50% would be enough to increase the photocurrent on thinner substrates. By 'less critical' it should be clear that we mean relatively to the process on thick wafers. In absolute terms, of course, the higher the reflectance, the higher the current. When $L \sim 2W$, like in practical cells below 200 μm , a reflectance of at least 80% should be targeted.

With the rapid evolution of laser processing local point contacts can be formed rather easily through most dielectric layers. There are substantially three routes which are being followed to realize them in production: firing through local contacts, laser fired contacts (LFC) and selective contacts alloying. Of all the additional steps which would need to be introduced to manufacture high efficiency cells on thin substrates this is actually the one in the most advanced phase of development. The techniques which have been proposed meet without problems throughput requirements, seem to be cost effective and at least in the case of LFC and selective alloying they provide both an ohmic contact and an effective local back surface field. There are also several valid alternatives to implement a good optical reflector, using metals and/or dielectrics. The real issue today seems to be the integration of an effective rear surface passivation layer. Boron BSF and thermal silicon oxide are known to perform better than aluminum BSF but they are difficult to apply on low quality substrates. Very few groups have succeeded to demonstrate better efficiencies than those that can be attained by aluminum BSF on commercial substrates and even less by using commercially relevant processes.

Last but not least, a few words on manufacturing of thin substrates. While tests indicate that there is no significant yield problem in module assembly down to at least 120 μm , cell manufacturing equipment will have to be adapted to thinner and thinner substrates in the years to come. The main problem remains handling, a reason for which it would be desirable to move to fully inline belt processing system. However, to name one example, belt diffusion furnaces are still not up to POCl_3 tubes in term of performance. It has also been observed that breakage can depend on the chemical surface conditioning steps. Many questions are still open on how to treat very thin wafers, but these will probably be addressed thoroughly only once thinner wafers will actually enter in production.

Rear surface passivation

There is still little understanding of why many dielectrics that seem to have excellent surface passivation properties do not perform as well as expected when integrated in a solar cell electrode. Hydrogenated

² And not lower; this was an oversight in [1].

silicon nitride, silicon carbide [2] and silicon carbonitride, aluminum oxide [3], aluminum fluoride, aluminum oxide/titanium dioxide alloys [4], amorphous silicon/silicon oxide, amorphous silicon/silicon nitride stacks have all shown surface recombination velocities below 50 cm/s at injection levels of 10^{14} - 10^{15} cm⁻³ on polished float zone wafers and often obtained fairly low values on commercial materials with different surface preparation. Nevertheless they have all failed, to public knowledge, to yield better cell efficiency than screen printed aluminum BSF on industrial type solar cells. This looks even more surprising since silicon nitride, silicon carbide, amorphous silicon have already been used as rear surface passivation layers in small area, lab type solar cells with conversion efficiencies above 20% [5,6,7]. For amorphous silicon stacks the explanation is quite straightforward. The thermal stability of these layers is lower than the typical temperatures which are reached during firing conditions. Deposition prior to firing is therefore not possible. However, surface cleaning is crucial, and performing this step after front side metallization and firing is not trivial. In-situ plasma cleaning in the deposition chamber could be one solution; having the possibility to use low temperature metallization techniques would be ideal for this type of approach. In the case of silicon nitride and silicon carbide things are more complicated. It may be argued that nitrides and carbides that are known to be best in surface passivation (e.g. Si-rich nitrides) are not thermally stable either and therefore it is to be expected that they degrade during the repeated high temperature processing steps that occur in cell manufacturing. On the other hand any skilled user can deposit layers which show low surface recombination velocities after deposition as well as after a typical firing RTP profile. However, we should not forget that the surface morphology in these cells, even when chemically etched in order to reduce the surface damage, will always be very defected, thus harder to passivate, compared to the wafers which are used for lifetime experiments and high efficiency solar cells. We experienced that the density of interface states D_{it} which is measured at silicon/PECVD SiNx:H interfaces, for example, grows one order of magnitude from semiconductor polish to flat-etched solar wafers, from 10^{11} to about 10^{12} cm⁻²eV⁻¹. This means that the dielectric field induced by the positive charge present in the layer is crucial to maintain a low SRV. The presence of the metal over the dielectric would not only induce a parasitic shunting at the local point contacts but would likely and more importantly induce a shift in the surface potential of silicon, hence affecting SHR recombination at the interface. In theory, for instance, an Al/SiNx/silicon structure should induce a surface potential corresponding to an effective charge in the order of $3\cdot 7\cdot 10^{11}$ cm⁻², sufficient to induce the semiconductor in weak inversion and therefore strongly increasing the surface recombination velocity. In practice, no correlation has been observed between the degradation of the surface passivation properties and the work function of the different metals which have been used in our experiments, leading to think that there is either a pinning of the Fermi level due to the presence of surface states or that there are concurrent phenomena in play which influence S_{eff} . The fact that deposition, or print, of a full area metal layer on top of a SiNx layer introduces an additional source of surface recombination has been consistently observed with a variety of metals (Al, Ag, Pd, Ti...) and cannot be related to metal diffusion or pinholes, which were carefully controlled and avoided. Removal of the metal layer restores the initial conditions and the effective surface recombination velocity is improved. These findings have been reproduced and confirmed at solar cell level as well as with QSSPC lifetime measurements, CDI and μ -PCD lifetime mapping, as shown in figure 3.

We should stress that this is an hypothesis. There are additional observations (e.g. the very high leakage currents of these MIS structures) that point to other explanations. For those who want to develop the nitride or carbide route to rear passivated solar cells there is definitely the need for further investigation of their behavior in actual devices. We stopped at a fact: D_{it} in these layers is still fairly high; their SRV in solar cell structures is significantly higher than the one which is measured by QSSPC, hence we looked for possible alternatives.

Figure 3. Effect of a capping aluminum layer on τ_{eff} for a fired CZ wafer passivated on both sides with SiNx:H , measured by μPCD . A thick film of aluminum paste has been printed on one side, in the shape of a rectangle (left half of the wafer in the picture), prior to firing. The effective lifetime of the wafers has then been mapped by $\mu\text{-PCD}$, probing the sample from the side opposite to the aluminum film. As it can be seen in the μPCD map on the left hand side, the surface covered with aluminum is heavily degraded and shows a recombination velocity in the order of 10^3 cm/s . The mechanism is reversible. If we etch the aluminum from the surface in hot HCl and re-measure the same wafer, the surface recombination velocity is fully ‘recovered’ (map on the right hand side)

Oxide/Nitride stacks

If, on one hand, the implementation of silicon nitride for rear surface passivation brings about a handful of complications, on the other this material has several properties which are still functional to solar cell processing. To name a few, it is thermally resistant, it can be used as a mask, it contains or can store a significant amount of positive charges, and it can release hydrogen.

For this reason nitrides have already been extensively studied e.g. in stacks with thermal silicon oxides [e.g. 8-10]. Thermal oxides yield good surface passivation in combination with nearly any silicon nitride, irrespective of their thickness. There is a general agreement that this depends on the high density of positive fixed charges that is observed in the system combined with a reduced density of interface states of the SiO_2/Si with respect to the SiN/Si interface. It has been argued whether there is any observable hydrogenation effect during nitride deposition and/or belt furnace treatment of these stacks. We can confirm, by a series of experiments and ESR measurements which will be published elsewhere, that for thermally grown oxides there is no measurable improvement of the SiO_2/Si interface due to the hydrogen out diffusion from the overlying SiNx:H layer. Things can work differently for low quality oxides. With ‘low quality’ we mean materials that are deposited on the silicon surface -e.g. by spin coating or CVD- and that, at this stage, would not be good enough to passivate the rear surface of a solar cell. Effective lifetimes of 1.5 $\Omega\cdot\text{cm}$ FZ wafers coated with ‘low quality’ SiOx could be improved from a couple of microseconds to several hundreds of microseconds (and up to the milliseconds) range after nitride deposition and firing (as measured with QSSPC at $\Delta n = 10^{14} \text{ cm}^{-3}$). The effect of hydrogen on the surface can be measured directly by monitoring the evolution of the density of trivalent interfacial silicon traps (the so called P_b centers, $\text{Si}_3\equiv\text{Si}^\cdot$, which are the dominating defect in unpassivated SiO_2 interfaces). Molecular hydrogen interaction with the P_b centers can be expressed in the simplest way with the concurrent passivation and dissociation reactions

where the two rate constants k_f and k_d are given by Arrhenius expressions of the type $k_f = k_{f0} \exp(-E_f/kT)$ and $k_d = k_{d0} \exp(-E_d/kT)$. Passivation and dissociation energy E_f and E_d are actually subject to a significant spread the major effect of which, when the full interaction case is taken into account [11], is the increase of the optimal temperature of the process and a decrease of the fraction of centres that will be passivated. In optimal conditions, molecular hydrogen can reduce the fraction of active P_b centers to a few ppm of their initial concentration (in this case other interface defects will surface and dominate recombination). P_b centers and other type of defects can be very accurately measured with electron spin resonance. In figure 4, we show three typical cases for a well passivated silicon/thermal SiO_2 interface (which serves as a reference), a silicon/ SiO_x interface, and a fired silicon/ $\text{SiO}_x/\text{SiN}_x$:H stack.

Figure 4. ESR spectra for a well passivated Si/ SiO_2 interface (reference), a Si/ SiO_x interface, and a fired Si/ $\text{SiO}_x/\text{SiN}_x$:H stack.

The only clear feature which is detectable in the reference spectrum is the marker, indicating a good surface passivation, consistent with a measured value of S_{eff} of 150-200 cm/s. In the case of the low quality oxide we see immediately the appearance of P_{b0} and P_{b1} centers characteristic of <100> surfaces. S_{eff} is measured to be in the order of $5 \cdot 10^3$ cm/s. The bottom graph represents the ESR spectrum of a Si/ SiO_x sample coated with SiN_x :H and fired. The two main findings are: the P_{b0} and P_{b1} centers have been perfectly passivated and a double donor center is created, likely at the $\text{SiN}_x/\text{SiO}_2$ interface, consistent with the positive charge of 10^{11} - 10^{12} cm $^{-2}$ which we measured in nearly all $\text{SiN}_x/\text{SiO}_2$ stack systems. This data is further confirmed by a S_{eff} of less than 50 cm/s, which -by comparison to the thermal SiO_2 interface- may only be attained with a larger surface potential. There is, therefore, a concurrent effect of hydrogenation and charge build up. But what is most important, is that the physical interface is sensibly improved and that these layers work at cell level, providing a metallized SRV which has been calculated to be in the range of 400 to 600 cm/s. These nitride/oxide stack systems have also the remarkable characteristics of being thermally resistant. They can actually be fired several times without losing their

surface passivation properties. They can be designed in such a way that they are an effective, inert mask for metals, thereby providing a very easy way to create local BSF contacts in the underlying silicon wafer during the contact firing step. The stacks can be easily structured by laser, e.g. ablating local points with a desired pitch. Printing or depositing aluminum over the locally ablated stack and firing provides a very simple way to create a passivated rear surface with local BSF contacts.

Solar cells based on this process, called *i*-PERC, are processed today in IMEC's pilot line on substrates with an average thickness of 80 to 150 μm on Cz-Si and 120 to 180 μm on mc-Si. Since we first presented this process average and top efficiencies are steadily improving. Using the pilot process, 16.7% has been reached on 156 cm^2 130 μm mc-Si [12]. Top efficiencies on 100 cm^2 substrates are of 17.6% on 130 μm thick Cz-Si and 17.4% on 180 μm thick mc-Si [13]. 17.3% and 16.6% have been reached, respectively, on 105 and 80 μm monocrystalline substrates (the efficiency limiting factor being a fill factor below 74%). A significant improvement is observed in both short circuit current and open circuit voltage of the *i*-PERC solar cells with respect to the reference, full area screen printed Al BSF standard process. According to substrate thickness, we typically observe a boost of 10 to 15 mV in V_{oc} and 2 to 3 mA/cm^2 in J_{sc} .

Conclusions

Processing thinner wafers is necessary in order to achieve a significant long term cost reduction of crystalline silicon solar cells. The strong wafer reduction we have assisted to in the last three years is coming to a slow down due mainly to the fact that most of cell manufacturers are not yet in the condition to process substrates at or below 180 μm . Beyond this limit it would be necessary to integrate structures with rear surface passivation and local contacts in *all* wafer-based silicon cells. While this is standard in the very high efficiency cells, cost effective technologies that would allow to use these structures on average industrial solar cells are still in an early stage of development. Low quality oxide/nitride stacks have been, thus far and to the knowledge of the authors, the only surface passivation layer applicable to screen printed solar cells (that is, transferable to production) that has proven to be better than the conventional full area, aluminum BSF process in actual devices. Given the increasing effort in R&D on the topic of surface passivation, other solutions should make their way through in the coming years. As a result, it should be expected that in 2 to 3 years we will see the first cells based on these technologies entering in production and the drive towards thinner wafer continue at least to the 100-120 μm range.

Acknowledgements & References

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Scanning tunneling luminescence of large-grained polycrystalline silicon thin films.

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ABSTRACT

We investigate the light emitted during scanning tunneling microscopy (STM) measurements of silicon thin films. Evidence that the tunneling luminescence is excited by electron-hole recombination –in analogy to photoluminescence– is supported by measurements of the photon intensity versus tip bias, tunneling luminescence spectroscopy, and examination of emission patterns in the far field. In combination with STM, we apply this scanning tunneling luminescence (STL) to obtain defect maps of polycrystalline silicon thin films with much improved resolution.

In scanning tunneling microscopy (STM), energetic tunneling electrons can stimulate the emission of photons. Since first reported by Gimzewski et al. more than three decades ago,¹ scanning tunneling luminescence (STL) has been observed on a variety of metallic structures,^{2–4} semiconductors,⁵ and molecular assemblies.⁶ The nature of this tunneling luminescence depends on the object under study –this is summarized by Sakurai et al. in Ref. 7. For metallic structures, the luminescence is inherently plasmon mediated. In semiconductors, light is emitted by electrons tunneling into the semiconductor and subsequently recombining with available holes –or vice versa, depending on the polarity of the semiconductor. In molecular assemblies, fluorescence can be stimulated by direct transitions between molecular orbitals.

The reconstructions of the silicon surface are fundamentally important in surface science and the first observations of light in STM measurements attracted great interest among researchers. Downes and Welland⁸ reported on the photon emission from the Si(111)-(7 × 7) surface and suggested the localized plasmon to be responsible for the luminescence. Thirstrup et al.⁹ and Sakurai et al.^{7,10} investigated silicon dangling bonds on hydrogen-terminated Si(001)-(3 × 1) and -(2 × 1) surfaces and attributed the highly localized photon emission to dipole transitions between the surface state of the tip and surface states of the silicon. In these studies, photon emission arising from electron-hole recombination is excluded because the optical transition in silicon is *indirect*, implying that a phonon with precise energy and momentum is required in the emission of photons. This selection rule is responsible for the very low emission efficiency of silicon.

In this letter, we report on STL measurements in silicon thin films with application to solar energy conversion. The observed tunneling luminescence appears to be excited by electron-hole recombination with quantum efficiency comparatively much better than that of photoluminescence. STL is then applied to defect mapping of silicon thin films. The mapping obtained by STM achieves much improved resolution when compared to cathodoluminescence.

Our STM is based on a multi-axis nanopositioning system integrated into a scanning electron microscope (SEM) equipped with cathodoluminescence optics, as described elsewhere.^{11,12} In this configuration, an ultrasharp tip (electrochemically etched PtIr tips are used) is positioned in the focal point of a parabolic mirror for maximum collection of the luminescence. The tip approaches the

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specimen at 45° to minimize eclipsing of the excited luminescence. A cryo-cooled CCD camera (Roper Scientific Silicon EEV 1340×400) can be configured to acquire either the emission spectrum or the emission pattern of the STL.

We have performed STM/STL observations on silicon thin films obtained by different processes in order to validate the universality of our findings. Here we illustrate the potential of this microscopy in the defect mapping of polycrystalline (pc-Si) thin films obtained by hot-wire chemical vapor deposition (HWCVD) using standard conditions at NREL: $\phi(\text{SiH}_4) = 20$ sccm, $P = 10$ mTorr, I (hot wire) = 16 A, and T (substrate) = 650°C . Prior to the STM measurements the silicon oxide (SiO_2) is removed with diluted HF but no *in situ* treatments are performed inside the electron microscope. In the vacuum conditions of the SEM (10^{-6} mbar) a clean, oxide-free surface cannot be preserved for the time needed to run the measurements, but our expectations is that the *ex situ* treatment helps to minimize artifacts in the STM images due to non uniformities in the SiO_2 .

Figure 1 shows the photon intensity versus the voltage applied to the tip (V) for this film. The counts per second are measured by integrating the emission pattern acquired with the CCD. The STM is operated in constant current mode with the tunneling current (I_t) set to 10 nA. We observe a near linear increase of the tunneling luminescence above a threshold voltage of $V_{th} \sim 2.5$ V. This threshold is in good agreement with the energy invested in the generation of secondary electrons and holes (e-h) in silicon, which is 2-3 times the bandgap energy. The STL spectrum is shown in the inset of Fig. 1, recorded at $V = +2.9$ V and $I_t = 20$ nA. This spectrum is identical to the one excited by cathodoluminescence and its energy position does not depend on V . Both of these findings suggest that electron-hole recombination is responsible for the tunneling luminescence. In contrast, the localized plasmon reported for the $\text{Si}(111)-(7 \times 7)$ surface and the dipole transition in H-terminated $\text{Si}(001)$ predict the energy position of the spectrum to be very sensitive to V and I_t . This is not the case in our films.

Fig. 1. Photon intensity (measured in counts per second) versus the voltage applied to the tip (V) from STL measurements on silicon thin films. $I_t = 10$ nA. A linear increase is observed above a threshold voltage of $V_{th} \sim 2.5$ V. The inset shows the STL spectrum.

When the plasmon localized at the tip participates in the luminescence an extra annular feature can be seen on the emission pattern—this is reported and described in detail elsewhere.¹³ Fig. 2(a) shows the emission pattern obtained during STM measurements on the HWCVD silicon film $-V = +2.9$ V and $I_t = 20$ nA— and, for comparison, a pattern of the plasmon luminescence from a gold substrate in Fig. 2(b). The extra annular feature of the localized plasmon is missing from the emission pattern in Fig. 2(a). This is yet further evidence that plasmons are not responsible for the luminescence that we observe.

Figure 2. (a) Emission pattern of the tunneling luminescence from a silicon thin film obtained by HWCVD. $V = 2.7$ V, $I_t = 20$ nA, acquisition time of 30 s. (b) Emission pattern from atomically flat gold substrates. $V = 2.3$ V, $I_t = 10$ nA, acquisition time of 30 s. An extra annular feature is observed when the emission is mediated by plasmons.

In the case of direct dipole transition, photon emission is seen for both polarities of V and for both n -type and p -type Si substrates (Sb-doped: $1 \times 10^{18} \text{ cm}^{-3}$ or B-doped: $1 \times 10^{18} \text{ cm}^{-3}$). In our case, the doping is light (p -type: $\sim 1.5 \times 10^{16} \text{ cm}^{-3}$) and the surface is terminated by both hydrogen (from the HF treatment) and oxygen (from adsorption in atmosphere). In contrast to the direct dipole transition, the tunneling luminescence is specific to the polarity of the tip: STL is stimulated when a positive voltage is applied to the tip $V > 0$ and not for $V < 0$. This is the opposite of what is expected: for $V < 0$, tunneling electrons recombine with holes available in the p -type semiconductor. Therefore, the observed polarity dependence points to the presence of an inversion layer near the surface of the silicon underneath the tip as a critical element in the excitation of tunneling luminescence. We hypothesize that secondary electrons generated by impact ionization diffuse toward and are confined to the inverted surface of the silicon when $V > 0$, which represents a *potential well* for electrons. Such confinement may ease the selection rules for the energy and momentum of the phonon, resulting in an increase of quantum efficiency. Indeed, we estimate the conversion efficiency for this process to be $\sim 1.5 \times 10^{-5}$ photons/electron, relatively high for an *indirect* bandgap semiconductor (the quantum efficiency of semiconductors with a *direct* transition is about $\sim 1 \times 10^{-4}$ photons/electron). At $V < 0$, on the other hand, electrons diffuse into the semiconductor and the absence of confinement yields low quantum efficiency. Similar results can be obtained for n -type pc-Si. In this case, holes are confined to the inverted surface when $V < 0$.

We now demonstrate the much better resolution achieved by photon intensity maps based on STM over those of cathodoluminescence in thin film silicon. The sources of contrast in STL are also discussed.

Figure 3. (a) Morphology of the silicon thin film under the electron microscope. (b) Corresponding cathodoluminescence map. Electron-beam energy $E_b = 15$ keV, electron-beam current $I_b = 1$ nA.

Fig. 3(a) shows the morphology of the film under the electron microscope. Relevant to our discussion, those grains with $\langle 100 \rangle$ orientation –as confirmed by electron backscattered diffraction (EBSD)– are much rougher than those with an orientation other than $\langle 100 \rangle$ (preferentially towards $\langle 110 \rangle$). The roughness is a result of the development of pits. Fig. 3(b) shows the corresponding cathodoluminescence map. This film has a number of very active nonradiative recombination centers (most likely associated with precipitates) revealed by the decrease in photon intensity. A closer examination finds that these extended defects are preferentially located in grain interiors with orientation other than the $\langle 100 \rangle$ and near grain boundaries. This specimen is used in the STM/STL measurements.

The first prerequisite to perform tunneling luminescence mapping is for the tip to be able to reproduce consistently the topography. These films correspond to the base of the cell (p -type: $\sim 1\text{--}5 \times 10^{16} \text{ cm}^{-3}$) and the resistance from the tip to the terminal contact (R) can cause the operation of the microscope unstable. Furthermore, because of the sensitivity of the tunneling current to the local environment, a nonuniform SiO_2 will inevitably introduce artifacts in the STM image –this is partially resolved with the *ex situ* pretreatment in HF. We have investigated systematically different (V , I_t) settings and achieved satisfactory operation for $V \gtrsim +1.5$ V and $I_t < \sim 2$ nA with R below or within the 100 k Ω range.

Fig. 4(a) shows a constant current STM image of the film at $V = +1.7$ V and $I_t = 1$ nA, which reproduces with confidence the topography of the surface as seen in the electron microscope [Fig. 3(a)]. In a second scan, photon maps of the tunneling luminescence are generated increasing V to $+2.7$ V and I_t to 20 nA. Additional features are seen on the STM image in Fig. 4(b) when compared to the first scan [Fig. 4(a)], amplified by the V and I_t settings and due to differences of the work function, driving the tip to approach the surface for sensing the high tunneling current of 20 nA needed for STL measurements. There is an obvious correspondence between Fig 4(b) and the photon intensity map of Fig. 4(c). These features are similar to those revealed by cathodoluminescence and, in agreement with Fig. 3(b), they are

seen on grain interiors with orientation other than $\langle 100 \rangle$ and preferentially located near grain boundaries. STL provides much better resolution of the recombination associated to extended defects than cathodoluminescence does. We have chosen three extended defects (*A*, *B*, and *C*) on the photon map of the tunneling luminescence for further discussion [see Fig. 4(c)]. For the triangular feature labeled as *A* there is no one-to-one correspondence between Figs. 4(b) and 4(c): only the boundary, and partially, is seen in the constant current STM mode. The work-function contrast in the STM is confined to the surface, but the tunneling electrons diffuse tens of nanometers into the silicon. Therefore, the photon map shows more of the extended defect, which only intersects partially the surface of the film along its boundary. The same argument can be applied to *B*. This extended defect is seen on the photon map but does not contribute to the contrast of the STM image. Therefore, *B* is located under the surface and do not affect substantially the work function sensed by the tip.

Figure 4. (a) Constant current STM image of the thin film at $V = + 1.7$ V and $I_t = 1$ nA. I -Gain = 10, P -Gain = 11. (b and c) STM image and simultaneous map of the photon intensity obtained in a second scan at $V = + 2.7$ V and $I_t = 20$ nA. Time/pixel = 125 ms.

Grain boundaries are also revealed in the tunneling luminescence map—a number of them are indicated by the arrows in Fig. 4(c). We have selected the grain boundary *C* for our discussion because such boundary cannot be identified in either Figs. 4(a) or 4(b). *C* runs along two grains of similar orientation and intersects extended defects which were thought to be in the grain interior. This is additional evidence that precipitation occurs at grain boundaries.

In summary, (i) we have detected tunneling luminescence in silicon that is consistent with electron-hole recombination; (ii) the quantum efficiency of this process is relatively high for a semiconductor with an indirect bandgap and; (iii) recombination at extended defects in silicon can be investigated with improved resolution by STM/STL.

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Fundamental Mechanisms in the Fire-Through Contact Metallization of Si Solar Cells: A Review

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ABSTRACT

Metallization-firing of Si solar cells is simple to perform, but it involves a complex synergism of many mechanisms. (1) dissolution of (SiN:H) antireflection coating by the constituents of the Ag ink, followed by Si-Ag interactions at the front contact; (2) diffusion of hydrogen from the interface into the bulk of the cell for impurity and defect passivation; and (3) alloying of the back Al contact to form a back-surface field (BSF). Currently, the firing conditions that yield the best cell efficiency are determined empirically. Such an empirical determination may not represent the highest achievable cell performance. To achieve the highest efficiency, each of these functions must be **maximized**. In addition, the finished contact must also meet other requirements such as mechanical strength, minimum stress, and thermal cycling. We will review the current understanding of contact formation mechanisms and describe the results of our recent work towards developing a coherent understanding of the physics of various mechanisms involved in a fire-through process. We will also present a model for the resistance of a solar cell due to the front contact.

INTRODUCTION

Fire-through metallization is the most common method for forming front-metal contact on a silicon solar cell. In this process, a solar cell is coated with an antireflection film consisting of about 750 Å of SiN:H. A front metallization pattern of Ag-based ink is then screen-printed on top of the SiN:H layer. In many cases, an Al-based contact is also screen printed on the back side of the cell so that both contacts can be co-fired. Next, the cell is fired (≈ 160 secs) in an IR belt furnace in which the cell experiences a temperature profile that peaks typically at about 800°C. This process results in interaction of Ag particles with Si to form an ohmic contact at the front interface. In a co-firing process, an ohmic contact is also formed at the back side due to Al-Si alloying. Furthermore, during this step, H diffuses into the bulk of the cell passivating impurities and defects. Thus, optimization of contact formation involves synergism of three processes:

1. Front contact formation to produce a uniform, low-resistance, ohmic contact with high shunt resistance. Such a contact will produce a high open-circuit voltage (V_{oc}) and high fill factor (FF).
2. Diffusion of H deep inside the material and association of H with impurities and defects to passivate them. Good bulk passivation will yield a high short-circuit current density (J_{sc}) and high V_{oc} .

3. Formation of Si-Al alloyed region on the backside to produce a large field which can lead to a low surface recombination on the backside with a concomitant high Voc.

A metallization firing influences each of the functions simultaneously. The best cell performance can only be obtained if each of the functions is maximized. However, one can intuitively argue that a process condition that favors maximization of one of the above function may not maximize the other two processes. For example a mild firing may lead to formation of a good front contact but may not diffuse H deep into the bulk. Likewise, a strong firing is required to form a good BSF, but it can cause shunting of the front junction and out diffusion of H. Therefore, it is important to study details of all three of these phenomena and examine how one can select a suitable choice of inks and processes that can maximize the cell performance. One approach to maximizing the cell performance is to tailor the parameters of the SiN:H, front-side ink, and back-contact ink so that each of these functions can be maximized by the same firing cycle, i.e., temperature-time (T-t) profile. This approach requires detailed studies that can separate the mechanisms of each function. This paper will describe the results of our recent work to develop a coherent understanding of the physics of various mechanisms involved in a fire-through process. Because this is ongoing work, we will present results that we have obtained to date. We will also present brief reviews of work published in the literature, which forms the basis of current understanding. Emphasis of this paper is on the front contact formation.

It is important to point out that although the fire-through process is not well understood, it is very successfully used in commercial cell fabrication. As discussed later in this paper, the success of the fire-through process is, in part, due to the formation of the back contact and the diffusion of hydrogen, which have somewhat large process windows and seem to be less sensitive to the process parameters. However, the front contact formation is more critical and difficult to control. This problem is because a good ohmic contact requires Ag to interact with a very shallow layer of Si. In most situations, Ag can locally go deeper toward a junction resulting in the formation of “spikes.” Consequently, the FF of solar cells with screen-printed, fire-through contact is typically lower than those formed by photo lithographically that defines a pattern in SiN:H followed by direct deposition of the metallic contact.

MECHANISM(S) OF FRONT CONTACT FORMATION

A good, front contact on a solar cell must have several features, which include: (i) a uniform ohmic contact at the interface typically produced by Si-Ag alloy formation, with a large ratio of Si-Ag/Si area; (ii) a continuous electric contact within the metallization pattern for lateral transport of current with low resistance; and (iii) a minimum coverage of the metal to prevent “shadowing” of the cell by the contact and minimize Si-metal interface.

Silver paste (ink) used for front contact is composed of many ingredients, which undergo a variety of interactions during firing to yield proper electrical, mechanical, and thermal properties. Various ink manufacturers have their proprietary compositions, which can vary to accommodate different requirements. In general, the paste consists of three major constituents: (a) a fine powder of Ag, typically 0.1 to 0.3 μm in size, (b) a glass frit, which can be a mixture of several glasses containing a host of metal oxides such as lead borosilicate glass, B_2O_3 , ZnO , BiO_3 ,¹⁻⁸ and (c) an organic binder⁹. The metal pattern is applied via screen printing which, consists of

squeezing the ink through a screen template that has an opening in the form of the metal pattern¹⁰.

The formation mechanism of the fire-through contact that lead to these steps is quite complex and interdependent. There are many hypotheses that speculate on chemical interactions that occur between various constituents of ink during the firing step. While Cheek et al¹¹ suggested it was liquid phase sintering, Ballif et al¹² have suggested that Si and Ag get dissolved in the glass frit and on cooling the Si recrystallizes and the Ag crystallites grow randomly on silicon. This explanation was based on the observations in over-fired samples. Hillali et al¹³ have also suggested dissolution of silver particles in glass layer and subsequent recrystallization of the silver particles upon cooling. This explanation however is counter intuitive because one would expect that under normal firing conditions a significant dissolution of Ag in glass cannot occur. This conclusion was also reached by Schubert et al¹⁴ who performed experiments that indicate it takes a long time for silver particles to get dissolved at normal cell firing temperatures. Schubert et al¹⁵ have suggested that the lead oxide gets reduced by the Si. The generated Pb alloys with the Ag. The Pb-Ag alloys dissolve <100> silicon planes and inverted pyramids get formed. On cooling Ag crystallizes on <111> planes of pyramid. According to Schubert et al, Pb is the transport media of the Ag. Although, we agree with the some part of this model, in our studies, we did not see any pyramids for optimal fired cells.

Young et al¹⁶ have suggested that metal oxide at firing temperatures, in the glass is reduced by Si (i.e. $x\text{Si} + 2\text{MO}_x = 2\text{M} + x\text{SiO}_2$). This effect would mean that “solvent metal” (M) is present everywhere glass and Si are in contact. It would also suggest the existence of a thin layer of SiO_2 at the interface. However, a detailed explanation as to what happens in the micro scale is lacking.

Although there are many proposed mechanisms and a great deal of work has been published, a coherent story of the sequence of Si-Ag alloying requires answers to the following questions:

1. What is the actual temperature at which Si-Ag form an alloy and is this alloy formation aided by the presence of M.
2. To what degree does the melting of Ag particles occur?
3. Does Ag get dissolved in glass and re-precipitates as proposed in some references.....?
4. How much Si is consumed in a typical contact formation?

To answer these issues we have performed the experiments as described in the next section, aimed at:

(i) Precise determination of temperature at the Si-metal location during contact formation, so that one can apply information from phase diagrams as a guide to project the degree of melting and composition of the Si-Ag alloy.

(ii) Identification of spatial distribution of various constituents in the ink after firing. This problem arises because interface analysis is typically done by cleaving a fired sample. Because the wafers are typically multicrystalline, the cleavage is typically irregular. Cleavage quality is further degraded by stress in the wafer produced by presence of ink. To overcome this problem, we have developed a cross-sectioning technique. Furthermore, many experiments are done in unrealistic conditions that may not occur during a typical contact formation. In this paper we describe some results of our studies aimed at identifying the precise temperatures at the Si-metal

interface, metal distribution inside the contact using a new cross-sectioning technique that produces highly flat cross-sections.

EXPERIMENTAL PROCEDURE

SiN:H-coated, N+/P cells on single-crystal and multicrystalline (mc)-Si wafers are screen printed with front and back metallization patterns and fired in a static optical furnace —a computer-controlled furnace that applies a predetermined optical flux as a function of time to the cell. We used Ferro's (Ag-based and Al-based) inks of different properties such as composition and particle size, as metallization pastes. The resultant temperature distribution over the cell is measured as a function of time by multiple thermocouples attached to the cells.

Figure 1. Set up for (T – t) profile measurement

K-type thermocouples were cement bonded on to the wafers maintaining the same thermal mass (Fig 1). One was directly below the busbar while the other was away from it. The output was measured through special software. Temperature distribution profile of the cell was generated during actual firing.

The fired cells are analyzed by dark and illuminated current-voltage (I-V) measurements to determine cell parameters (V_{oc} , J_{sc} , and FF), series resistance and shunt conductance, and by a variety of analytical techniques including secondary-ion mass spectroscopy (SIMS), Fourier transform infrared (FTIR) spectroscopy, and electron-beam methods.

To perform a detailed statistically meaningful characterization of Si-metal interactions, we have developed a new procedure for cross-sectioning large-area solar cell samples using chemical-mechanical polishing (CMP). This polishing technique generates a large, planar cross-section of the composite (stratified) device that can be analyzed by atomic force microscopy (AFM), conductive AFM (C-AFM), scanning Kelvin probe microscopy (SKPM), and other electron-beam techniques to measure penetration and distribution of metal into Si, and electric potential and field distributions at the Si-Ag and Si-Al interfaces. Because this cross-sectioning technique produces a highly planar surface, it provides access to various components in a segregated composition (such as glass, Ag, Si-Ag alloy in a contact). In comparison, a fractured cross-section (particularly of a mc-Si sample) has artifacts that can interfere with a good image quality.

Fig.2a is an image of the Si-Al interface of a cross-sectioned cell showing a planar view of Al grains in a glass matrix. Fig. 2b is a similar image of the Si-Ag interface (having a much finer

particle size of Ag). It is important to point out that a standard procedure of wafer cleavage or breakage produces fracture lines and non-planar regions of different layers that are difficult to image with such clarity.

Figure 2. SEM images of a cross-sectioned, fired cell showing: (a) Al back-contact, and (b) Ag front-contact.

Figure 3. Formation of Al-alloyed regions and the BSF.

Fig.3 shows the Al-Si interface of a cross-sectioned cell in which the unmelted Al was etched away; one can see the Al grains, Si-Al alloy, as well as the BSF. We have studied the formation of BSF and Al alloyed regions for a host of T-t profiles. We found that such regions are nonuniform, but they can produce wide BSF regions.

These analyses are used to measure the following: (1) Distribution of Ag penetration into Si (N+/P), change in the particle size of Ag upon firing, and distribution of solvent metal(s) in the glass matrix, and electric potential and field as a function of depth from the Ag-Si interface. These parameters and the temperature profiles at the metal allow us to establish the chemistry of Ag contact formation; (2) Changes in the H distribution in the SiN:H and near the Si surface; and (3) Dissolution rate of SiN:H in glass, penetration of Ag and Al in Si. Each of these mechanisms is also modeled theoretically to get further insight into the physics of the process.

RESULTS AND DISCUSSION

The above characterization techniques have led to some salient results, described below as examples.

1. Temperature distribution of a cell during firing: Screen-printed cells can exhibit a large difference in temperature between regions with and without front metallization. Fig. 4 shows the cell temperature profiles directly under the front metal, and away from it, during a typical fire-through process. The optical flux density profile is also shown. From Fig. 4, it can be seen that the maximum temperature reached under the metal is less than 800°C. This has significant importance in identifying interactions between Si and Ag. This temperature is much below the eutectic point of Ag-Si (835°C)¹⁷⁻¹⁹ and melting point of Ag (961.9°C).

The time duration at higher temperatures was only a few seconds. It is believed that there can be no net migration of Ag particles within the finger or busbar in such a short amount of time. There is increase in the particle size because the adjoining particles fuse together. This can only be explained by invoking mechanisms that can depress the eutectic melting point of Ag-Si, such as the presence of other metals and interface energy. It also suggests a need for carefully designed temperature measurements during solar cell processing.

Figure 4. Measured temperature profiles (in °C) under a busbar (green) and away from it (red) during a fire-through process corresponding to the input optical flux (blue).

A direct implication of lower temperature under the front metallization manifests itself in the difference in the hydrogen profile under and away from the metal busbar (see Fig. 5). It is seen that H diffuses deeper in the regions away from the metallization. Because metallization alloys at the surface of N⁺ region, it can consume the heavily doped surface (see Fig. 6). These results show that significant consumption of P occurs during the Si-Ag interaction, and hydrogen

Figure 5. SIMS profiles of H under the metal busbar and away from it. Metal was etched before SIMS analysis.

Figure 6. SIMS profiles of P profiles under the metal busbar and away from it, showing consumption of P by the metal

diffusion is retarded under the metal (creating a lower voltage directly under the metal).

2. Potential, field, and current distributions at the Si-Ag interface. A cross-sectioned cell lends itself to measurements by scanning large-area AFM, SKPM, and C-AFM, without destroying the probe tips. The results provide information on the grain size of the metal, quality of the Si-Ag contact, and structure of the alloyed interface. Fig. 7 shows SKPM measurements at a Si-Ag alloyed region (potential and field profiles are along the white line in the topographic image). Fig. 8 shows a C-AFM image identifying glass phases as insulating regions of low current. Analyses of such images for different T-t profiles show that under optimum alloying conditions, a dense Si-Ag alloy is formed at the interface.

3. Dynamics of H diffusion: Our experiments show that there is bilateral flow of hydrogen from SiN:H into Si and into air. This flow is mediated by the damaged layer (and the H trapped in this layer). Because diffusivity of H at the firing temperatures is very large, we expect that extended

firing (i.e., higher temperatures and/or longer times) can result in depletion of H from the bulk of the cell (due to evolution into air and possibly from the backside). It is important to determine the role of the Al back-contact, which can confine H within the cell. Such confinement may occur because of a physical barrier and because of the BSF, which can either aid or retard H ions. These results can play an important role in passivation kinetics and may account for differences in the cell performance between co-fired and separately fired contacts.

Figure 9. CAFM images of a portion of a silver front contact. Photos mapping various elements i.e., Si, Pb, Ag and Bi are presented

Fig.9 above shows photos of the presence and distribution of various constituent elements in the front contact of a standard solar cell. A big eye-shaped cavity is observed at the Ag-Si interface. We believe this is a void created by the burn-off of a volatile organic vehicle. Based on the T-t profile and the SEM images of the cross-sectioning, we have come up with the contact formation mechanism that is explained in the diagram below (Fig.10).

The contact formation involves a series of interactions between the ink, nitride, and Si. It is generally accepted that in the initial stage of heating (up to 400°C), the frit softens²⁰ and the softened glass dissolves the SiN:H layer under the paste. Furthermore, molten glass allows some exchange of metal across the boundary of Ag and glass. In particular, M can migrate toward Ag, forming a thin liquid around the particles. As the temperature is increased, many Ag particles agglomerate and fuse together into bunches. At the peak temperature, some of the agglomerates close to the surface react with Si to form a thin alloy layer between Ag particles and Si²¹. It may be pointed out that the alloy formation is not continuous over the Si surface, as shown in the next section. The composition of this molten alloy depends on many factors such as the composition

of the glass frit (particularly metal ions) and the highest temperature during firing etc. The thickness of the layer depends on factors such as temperature, time, and the concentration of P at the Si surface (sheet rho of the N+ layer at the surface). The third stage of the process involves the cool-down. During this stage the molten constituents solidify. As the Si-Ag-M alloy solidifies, it is likely to produce a grading in the composition of interface between Si and Ag¹⁴.

Figure 10.
Contact
formation
mechanism

The top part of the Fig. 10 is a schematic of the Ag finger containing Ag particles and glass frit. The bottom part is the SEM image of the area below the finger or busbar after the Ag finger or busbar has been etched away. In this figure the Ag rich and Si rich area can be clearly seen. The top part explains the possible contact formation mechanism as well as the current transport mechanism. Parallel ohmic, schottky, & tunneling contacts are formed. The amount of each will strongly depend on the contact formation mechanism. As firing temperature increases, there is increase in the particle size because the adjoining particles fuse together. It can be seen that Ag-Si interactions lead to the formation of Ag-rich and Si-rich phases. Formation of an Ag-rich phase depends on many factors, including size of the Ag particles, process conditions, and ink composition. Because the regions of an Ag-rich phase form ohmic contacts at the Si interface, it is desirable to have a large fraction of an Ag-rich phase to produce a cell with a high FF. These results show that the current transport at the front Si interface has two components: a direct Si-Ag ohmic component, and a Si-glass-Ag tunneling component.

CONCLUSION

Some of the important results obtained are: (i) Screen printed cells can exhibit a large ($\sim 30^\circ\text{C}$) difference in temperature between regions with and without front metallization. Typically, the maximum temperature reached under the metal is less than 800°C , which is much lower than below the eutectic point of Ag-Si. (ii) A direct implication of lower temperature under the front metallization results in a lack of hydrogen diffusion directly under the metal busbar. However, significant consumption of phosphorous occurs during Si-Ag interaction. (iii) Ag-Si interactions lead to formation of Ag-rich and Si-rich phases. Because an Ag-rich phase forms an ohmic

contact at the Si interface, it is desirable to have a large fraction of an Ag-rich phase to have a high fill factor of the cell. (iv) Al-alloyed regions are not uniform but can produce wide BSF regions. One approach to maximizing the cell performance is to tailor the parameters of SiN:H, front-side ink, and back-contact ink so that each of these functions can be maximized by the same firing cycle, i.e., temperature-time (T-t) profile.

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ADVANCED METALLIZATION FOR CRYSTALLINE SILICON SOLAR CELLS

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INTRODUCTION

The front structure of an industrial screen-printed solar cell differs strongly from the one of a laboratory high-efficiency cell with photolithographically defined contacts resulting in an efficiency reduction of about 1.7% [1] including shading, resistive and recombination losses. Nevertheless, there seems to be no thick-film metallization technology which is able to improve the front side structure significantly compared to a screen-printed one. In order to overcome this limitation a two-layer contact structure is thought to be the “magic bullet”. This structure has the great advantage that both layers can be optimized individually. The first layer should form a good electrical and mechanical contact to the preferable lowly doped emitter, be stable in oxidizing ambient and long lifetime. In addition it should act as a seed layer for the plating process, used to form the second layer. This second layer needs to have a good line conductivity to minimize resistivity losses in the finger, which is the reason, why silver or copper are preferred materials. Applying this two-layer contact structure changes the requirements for the seed layer and hence also for the deposition technology. The probably most important demand for the applied deposition technology is the ability to create fine-line contacts. The contact height (and finger conductivity), formerly the limiting factor for many deposition technologies, is of secondary importance. Ideally the deposition technology is direct-write, non-contact, stress-free and has a high throughput rate. As reported elsewhere [2] different technologies to create the seed layer are under current investigation at Fraunhofer ISE, including nickel plating, laser micro sintering [3], metal aerosol jet printing [4], fine-line screen-printing and pad printing.

INFLUENCE OF CONTACT WIDTH AND RESISTIVITY

The dependence of ohmic and shading losses on the contact width and contact resistivity for the two layer contact structure was theoretically analyzed for a solar cell of size 15.6 x 15.6 cm² and two busbars. For simulation a final contact consisting of a thin deposited contact layer (thickness <1 µm), isotropically thickened by light-induced silver plating, was assumed. This results in a final finger width w_f of twice the finger height h_f plus the seed contact width w_c . The reference screen-printed contact was 120 µm wide and had an averaged height of 15 µm. Electrical busbar losses have not been taken into account, as they do not influence this grid optimization.

Fig. 1 shows the loss caused by the front metal grid plotted versus the contact width assuming emitters of different sheet resistance. For each contact width the optimal finger spacing and height was calculated and the total loss is shown in Fig. 1. With decreasing contact width the loss caused by the front grid is reduced up to the point at which the contact resistivity becomes the limiting

factor. Compared to a screen-printed contact the loss can be reduced by 2.5%_{rel} for a solar cell with a sheet resistance of 55 Ω/sq solely by decreasing the contact width. With increasing emitter sheet resistance, which is desired to reduce recombination losses, the importance of fine-line printing is even strengthened to keep losses caused by the front grid as low as possible.

The influence of the contact resistivity on the total power loss fraction in dependence on the seed layer width is illustrated in Fig. 2. A contact with a contact resistivity below 0.1 $\text{m}\Omega \text{ cm}^2$ has no significant influence on the total loss for a contact width $w_c > 8 \mu\text{m}$. With increasing contact resistivity the minimum of the total loss is found at broader contact widths. Hence if the contact resistivity ρ_c is not sufficiently low, fine-line printed contacts can even increase the total loss fraction p . Nevertheless, even for standard thick-film pastes assuming a contact resistivity of 3 $\text{m}\Omega \text{ cm}^2$ the contact width can be reduced down to 27 μm before total loss rises again.

Fine-line printing of the contact layer becomes even more advantageous for solar cells with an increased number of busbars and when considering that the fraction of light impinging on the finger that is reflected into the active cell area also increases with decreasing finger width.

Fig. 1: Total loss p , finger height h_f and finger separation distance s for different sheet resistance emitters plotted versus the contact width w_c . In addition the total loss p for a screen-printed (SP) cell is illustrated.

Fig. 2: Total loss p of a solar cell with an emitter sheet resistance of $R_{sh} = 55 \Omega/\text{sq}$ in dependence of the contact width plotted for different contact resistivities.

LIGHT-INDUCED PLATING

Light-induced silver plating is the key technology to form the highly conductive layer of a two-layer contact structure [5]. This plating technique has been optimized for high-efficiency cells since 1992 at Fraunhofer ISE and constitutes a fast method to homogeneously thicken metal contacts on n-doped material. A schematic drawing of the light-induced plating process is presented in Fig. 3. The ability of the solar cell to generate a photocurrent under irradiation is the key factor allowing a light-induced plating process. As the cell is illuminated the n-doped front side is negatively charged. The positively charged metal cations in the solution are then deposited on the negatively charged surface. To establish a closed electrical system an electrical contact has to be made to the cell. Due to the photovoltaic effect it is sufficient to establish this contact at the

rear side. There is no need to contact any of the fine electrodes at the front side, which simplifies the handling process enormously. A significant efficiency increase on $15.6 \times 15.6 \text{ cm}^2$ industrial multicrystalline cells of 0.3% could be demonstrated.

Fig. 3: Scheme of the light-induced plating process. The positively charged metal cations are deposited onto the negative doped front surface, induced by the photovoltaic effect under irradiation.

HIGH-EFFICIENCY SCREEN-PRINTED AND PLATED CONTACTS

Solar cells of size $2 \times 2 \text{ cm}^2$ with fine-line screen-printed and plated contacts were processed on 4 inch boron-doped FZ-wafers ($\rho_b = 0.5 \Omega \text{ cm}$) one part having an Al-BSF, the other part having a laser-fired contact (LFC [6]) rear side structure. The production sequence for both cell types is presented in Fig. 4.

Fig. 4: Process flow diagram of manufactured solar cells featuring screen-printed front contacts thickened by light-induced plating and an Al-BSF (left-hand) and a LFC (right-hand) rear side structure.

Table 1: IV -parameters and series resistance values of the best solar cells featuring an Al-BSF and a LFC rear side structure. r_s was determined by comparing illuminated and dark IV -curve. *Calibrated measurement at Fraunhofer ISE (CalLab).

Wafer. Cell-ID	R_{sh} [Ω/sq]	rear side	V_{oc} [mV]	j_{sc} [mA/cm ²]	FF [%]	η [%]	r_s [$\Omega \text{ cm}^2$]
32_6.4	40	Al-BSF	632	35.2	81.2	18.1	0.46
33_7.1		LFC	639	36.7	80.0	18.8	0.6
32_15.4	60	Al-BSF	632	35.6	81.2	18.3	0.49
33_13.1		LFC	647	37.1	79.6	19.1	n.a.
32_24.4	90	Al-BSF	640	36.5	79.8	18.7	0.74
33_19.2		LFC	655*	38.2*	76.9*	19.3*	1.19

The best solar cell results for each type of emitter and cell structure are presented in Table 1. The emitter with a sheet resistance of 90 Ω/sq was successfully contacted leading to efficiencies up to 18.7% for a cell with a conventional Al-BSF and up to 19.3% for the ones with a LFC rear side structure. Thus, an efficiency gain of about 0.6% to 0.7% absolute was achieved for the laser fired contact cells. This is due to the strong gain in j_{sc} and V_{oc} , which can be explained by the improved internal reflectance and the high-quality passivated rear side, achieved by the thermally grown oxide and the laser-fired point contacts. The improvement of the rear side reflectance and of the internal quantum efficiency is illustrated in the spectral response measurements in Fig. 5. The increasing reflectivity and the slightly higher internal quantum efficiency in the long wavelength region with increasing emitter sheet resistance for the LFC cells are related to the reduced free-carrier absorption in the emitter layer [7].

However, whereas the fill factor for cells with a sheet resistance of 40 Ω/sq was already on a relatively high level of 75% before the plating step, the fill factor for cells with a sheet resistance of 60 Ω/sq and 90 Ω/sq was low. Measurements revealed a high contact resistance increasing the series resistance significantly which is responsible for the low fill factor. After thickening these contacts by light-induced silver plating, a remarkable improvement was observed. The fill factor increased from a very low level to values between 75% and 80% even for the 90 Ω/sq emitter. Contact resistance measurements were performed on these cells again showing an improvement to values down to 3 $\text{m}\Omega \text{ cm}^2$.

Fig. 5: Internal quantum efficiency (symbols) and reflectance measurements (solid lines) of solar cells with different rear side structures and emitter sheet resistances. Clear improvement for the LFC rear side structure for long wavelengths and for higher sheet resistance emitters in the short wavelength region.

MICROSTRUCTURE ANALYSIS

The improvement of the contact resistance by the plating process was confirmed by contact resistance measurements on a high quantity of test structures. Microstructure analysis have shown that the crystallite density under a screen-printed finger contacting an emitter with a sheet resistance of $90 \Omega/\text{sq}$ is significantly lower compared to the density of a cell with $R_{sh} = 40 \Omega/\text{sq}$. This probably explains the high contact resistance prior to the plating process.

However, next to the screen-printed contact structure the SiN_x antireflection coating was covered by a layer of glass (see Fig. 6). This region consists of holes and precipitates (presumably silver or lead). A current path between this edge zone and the plated silver might have been established.

A cross section of the contact finger was prepared by focused ion beam (FIB) machining at the Fraunhofer IWMH. Fig. 7-a presents an overview of the cross section, showing the random pyramids textured silicon surface and the about $90 \mu\text{m}$ broad hotmelt screen-printed contact, which is covered by a $5 \mu\text{m}$ to $10 \mu\text{m}$ thick plated silver layer. Fig. 7-c shows the interface layer of the thick-film contact and the silicon surface. A layer of glass (confirmed by EDX measurements), which is at some locations very thin, completely wets the silicon surface. A direct (screen-printed) silver-silicon contact was not observed over the whole cross section. The interface between plated silver and silicon surface is illustrated in Fig. 7-b. It seems as if a direct contact between both materials was created. Fig. 7-d shows a section of the right side of the contact. Clearly visible is the interface layer between the plated and the screen-printed silver and a high quantity of precipitates located in the glass layer.

Fig. 6: Top view showing the edge of a screen-printed contact.

Fig. 7: Cross section SEM images of a screen-printed and plated contact. The cross section was prepared by focused ion beam (FIB) machining.

The schematic drawing of a plated thick-film contact in Fig. 8 illustrates possible current paths between silicon surface and conductor. The porous screen-printed contact is covered by a thin layer of plated silver. It is likely that during the plating process some of the silver also fills the top layer of the contact structure.

The first three current paths (Fig. 8: case 1-3) have been reported for a conventional screen-printed contact [8,9]. The limiting factor to achieve a low contact resistance between the silicon

surface and the bulk silver is the non- or very low conductive glass layer [10], which is located in-between. For low contact resistance, either the glass layer needs to be very thin allowing a quantum mechanical tunneling of electrons [8] (Fig. 8: case 3), or precipitates in the glass layer allow a multiple quantum mechanical tunneling of electrons [9] (Fig. 8: case 1), or the glass layer is locally completely removed, so that the silicon surface or silver crystallites are in direct contact with the bulk silver [10,11] (Fig. 8: case 2).

For the plated silver layer the latter four illustrated current paths could be created (see Fig. 8: case 4-7). It is likely that during the firing process either glass leaks out of the printed contact structure and/or a layer of glass is left behind as the contact shrinks in width. This glass etches the SiN_x layer. It seems as if the right constitution of silver, lead and glass is flushed out to the edge and crystallites are formed. It is likely that some of these crystallites are in direct contact to the plated silver. Due to the reported low contact resistance between crystallite and silicon surface [12,13], just a few crystallites in direct contact with the plated silver would be sufficient to reduce the contact resistance significantly (Fig. 8: case 4). At locations at which the SiN_x layer is completely penetrated and the plated silver has a direct contact to the silicon surface a current path is created (see Fig. 8: case 5). Even if the silicon surface is completely covered by a layer of glass, plated silver might be in direct contact to the silicon through holes in the glass layer, which have been observed by optical investigations (AFM and SEM). Optical analysis also proved a large amount of precipitates in the glass layer next to the thick-film contact. Direct tunneling or multiple tunneling (via metal precipitates in the glass layer) of electrons from the silicon surface and/or silver crystallites to the plated silver might be possible (see Fig. 8: case 6). It is probable that silver ions out of the plating bath infiltrate at least the top layer of the porous screen-printed contact structure. At the edge where the contact is thinnest plated silver might be in direct contact to a crystallite and/or the silicon surface (see Fig. 8: case 7).

Fig. 8: Schematic drawing of a plated thick-film contact, illustrating different current paths between emitter surface and metal conductor.

FURTHER PROGRESS IN METAL AEROSOL JET PRINTING

Metal aerosol jet printing is a promising alternative to create contacts of small width [4]. Opposite to many other metallization technologies applied for solar cell processing the metal aerosol jet system [14] is a non-contact direct-write technique, making it suitable for printing on uneven surfaces and thin and fragile wafers. Compared to an inkjet system, which has been also used for solar cell metallization [15,16], the metal-containing ink is not printed directly. Instead, an aerosol is created and transported to the deposition head via a heatable tube, in which the viscosity of the ink can be controlled. The deposition head is the key part of the metal aerosol jet printer (see Fig. 9). In the head, a metal containing aerosol is surrounded by a second gas flow, which focuses the aerosol to a small diameter, prevents contact between aerosol and nozzle tip and accelerates the droplets. As the aerosol stream is focused by the laminar gas stream, the width of the deposited line can be much smaller than the width of the nozzle tip (see Fig. 10-a). After leaving the tip, droplets have enough momentum to remain collimated, which means that the distance between tip outlet and surface may vary a few millimeters without a significant change of the deposited line width. Fig. 10-b shows a cross section of a metal aerosol jet printed contact plated with silver.

Fig. 9: Schematic drawing of the working principle of the deposition head.

a)

b)

Fig.10: a) Microscope picture of metal aerosol jet printed line using a metal organic Ag ink and a nozzle with a 100 μm outlet diameter. b) Metal aerosol jet printed and plated contact using modified screen-printing paste (marked area points out the contact layer).

With this technology solar cells were processed on 12.5 x 12.5 cm^2 , 1 Ωcm , boron-doped Cz-silicon wafers with a thickness of 250 μm . The cells exhibit a textured surface covered by a SiN_x antireflection coating and an emitter sheet resistance of 45 Ω/sq . The rear side was conventionally screen-printed and dried. After the contact layer of the front grid was deposited the wafers were fired in a lab-type fast firing furnace. Then the front contacts were thickened by light-induced plating, sintered under room ambient and edge isolated by laser scribing and breaking. Reference wafers were processed applying the hotmelt screen-printing technology [17]. The achieved efficiency of 18.3% shows the high potential of the process. Nevertheless, the full potential of the metal aerosol jet system will be achieved when using optimized inks giving a low contact resistivity to a lowly doped silicon surface.

Table 2: IV -parameters of 12.5 x 12.5 cm^2 Cz Si solar cells with aerosol jet printed + plated and hotmelt screen-printed contacts.

front side metallization	V_{oc} [mV]	j_{sc} [mA/cm 2]	FF [%]	η [%]	PFF [%]	r_s [Ωcm^2]	r_p [k Ωcm^2]
metal aerosol jet + LIP	624	36.1	81.0	18.3	82.5	0.4	10
hotmelt screen-printing	624	36.2	79.1	17.9	-	-	-

CONCLUSION

Applying the two-layer contact structure, front contacts of small width and good electrical properties were manufactured. Efficiencies up to 18.7% were achieved on $2 \times 2 \text{ cm}^2$ FZ silicon solar cells with fine-line screen-printed and plated contacts on the front and an Al-BSF on the rear. In combination with a laser-fired rear-contact structure, even efficiencies up to 19.3% were achieved. We believe that a further efficiency increase is achieved by applying new deposition technologies to create the contact layer. With metal aerosol jet printed and plated contacts efficiencies up to 18.3% on large area monocrystalline silicon solar cells were achieved. In order to improve the understanding of the contact formation process of plated and fine-line printed fingers, micro-structure analyses were performed and an extension of the existing model was presented, illustrating new current paths between the emitter layer and the metal finger.

ACKNOWLEDGEMENT

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Department of Energy's Solar America Initiative (SAI)

Briefing for Crystalline Silicon Workshop

Vail, Colorado 6 August 2007

Jeffrey Mazer
Solar Energy Technologies Program
Office of Energy Efficiency and Renewable Energy

<http://www1.eere.energy.gov/solar/>

DOE Photovoltaic Budget Trends

Solar America Initiative has dramatically increased PV funding:

FY	DOE PV Budget (\$ millions)	
2005	67.2	
2006	60.6	
2007	140.5	(no earmarks)
2008	145.3	(lower of the House/Senate marks)

Global Photovoltaic Markets Are Quickly Expanding

Demand Exceeds Global Supply

- Global sales projected to double every 2 yrs:
 - 2006: 2,500 MW¹
 - 2010: 10,000 MW (\$72B)²
- Driven by incentive programs, including the U.S. EPACT of 2005, buy down programs in various U.S. states, feed-in tariff in Germany, etc
- In 2006¹, U.S. produced 202 MW of modules; Japan produced 928 MW

1. *PV News* (Prometheus Institute), vol. 26, March 2007
2. Photon Consulting, *Annual Industry Assessment*, Aug 2006;

Production Growing Rapidly in Spite of Constraints

- Direct module manufacturing costs continue to decrease (below \$2 / W); but the shortage of electronic grade silicon feedstock limits production and increases module prices
- Capacity is mostly crystalline-silicon based (92% in 2006 down from 94% in 2005)
- Thin-film technologies are growing because of shortage of electronic-grade Si feedstock as well as low production costs
- In U.S., thin film PV doubled in 2006¹ (to about 91 MW)

1. *PV News* (Prometheus Institute), vol. 26, March 2007

The Solar America Initiative (SAI)

Three Solicitations Emphasize Major Cost Reductions

Making Solar Energy Cost-Competitive—PV at 5 to 10 ¢/kWh—by 2015

Solicitation 1:
R&D Partnerships (TPPs)

Industry led public-private partnerships pursue system and component technologies; demonstrate manufacturing approaches that deliver low cost, high reliability products.

Solicitation 2:
Market Transformation

Market transformation efforts tackle non R&D barriers to market penetration.

Solicitation 3:
PV Incubator

Targets R&D of PV system and component prototypes; emphasis is on barriers to 2010 commercialization.

SAI Will Bring Increasingly Cost-Competitive PV Systems to Market between Now and 2015

Market Sector	Current U.S. Market Price Range (¢/kWh)	Cost (¢/kWh) Benchmark 2005	Cost (¢/kWh) Target 2010	Cost (¢/kWh) Target 2015
Residential	5.8-16.7	23-32	13-18	8-10
Commercial	5.4-15.0	16-22	9-12	6-8
Utility	4.0-7.6	13-22	10-15	5-7

SAI R&D Partnerships Solicitation (Technology Pathway Partnerships or TPPs)

- > \$360 million over 3-year duration; includes over 50% cost-share
- Two topical areas: systems and subsystems
- Each TPP award is led by industry
- Award size ≤ \$10 M / yr for systems; ≤ \$4 M / yr for subsystems
- Twelve TPPs have been competitively selected; funding has started

See <http://www.doe.gov/news/4855.htm>

The Twelve FY 2007 (Year One) TPP Awards

Involve 50 companies, and 14 universities, in 20 states across the United States

Lead Company (Systems)

Project Description

Amonix	High Concentration PV Systems for Utility Power
Boeing	High-Efficiency Concentrating PV Power System
BP Solar	Grid Parity Using BP Solar Crystalline Silicon Technology
Dow Chemical	Building-Integrated PV Energy Generation
General Electric Energy	Value Chain Partnership to Accelerate U.S. PV
Miasolé	Flexible Integrated PV System
Nanosolar	Grid-Parity PV on Flat Commercial Rooftops
SunPower & Powerlight (merged)	Grid-Competitive Residential and Utility PV;
	Fully Automated PV Systems Technology
United Solar Ovonic	Thin-Film Building-Integrated PV Systems

(Subsystems)

GreenRay	Development of an AC Module System
Konarka	Building-Integrated Dye Cell / Organics PV
Soliant	Concentrating PV for Rooftops

Technology Pathway Partnerships Year-One Breakout

Lead Company

DOE Cost (\$ millions)

SunPower & Powerlight	8.8
Nanosolar	8.5
GE Energy	8.2
Boeing	7.9
BP Solar	7.6
Miasolé	7.2
United Solar Ovonic	4.6
Dow Chemical	3.3
Amonix	3.2
Soliant	2.2
Konarka	1.3
GreenRay	0.6

Total DOE Funding for TPPs in Year One \$ 63 M

SAI Market Transformation Solicitation ~ \$5 M from DOE in FY 2007

- Assist in codes, regulations and standards for solar electric
- Promote certification of solar installers and code officials
- Develop and promote national rating system for solar module performance
- Provide outreach to utilities and states on technical solar issues
- Provide technical assistance to cities, states, and private developers
- Funding has started

SAI Photovoltaic Incubator Solicitation

- Intended for small businesses and non-federal research institutes
- Prototypes must have demonstrated proof of concept for manufacturing
- 20% cost share
- Successful companies can compete in the 2010 round of TPP solicitations
- \$27 M from DOE in first 18-month budget period (starting in CY 2007)
- Possible 18-month follow-on
- 10 companies have been selected; funding starts in Aug 2007

SAI Incubator 18-Month Funding Breakout

Project	DOE Cost	Cost Share	Location	Technology
AVA Solar	\$3,000,000	\$13,830,000	Fort Collins, CO	CdTe thin film
Blue Square	\$2,990,000	\$1,530,000	North East, MD	Thin c-Si grown on m-Si
CallSolar	\$3,000,000	\$8,300,000	Menlo Park, CA	c-Si from poor feedstock
EnFocus	\$2,900,000	\$1,020,000	Sunnyvale, CA	Low profile high-conc sys
MicoLink	\$2,550,000	\$650,000	Niles, IL	High-efficiency Bi-V conc cell
Plextronics	\$3,000,000	\$750,000	Pittsburgh, PA	Organic thin film
PrimeStar	\$2,900,000	\$8,630,000	Golden, CO	CdTe thin film
Solaris	\$2,600,000	\$2,020,000	Fremont, CA	2X conc flatplate
SolFocus	\$2,000,000	\$2,280,000	Palo Alto, CA	500X conc module
SolarPower	\$2,370,000	\$26,930,000	Milpitas, CA	Flexible CIGS thin film
18 Month	\$27,390,000	\$43,960,000		
	TOTAL	\$71,350,000		

University Funding Opportunities

DOE is releasing several university solicitations in 2007:

- one for universities and companies to perform research on post 2015 (post SAI) photovoltaic topics (closed June 28)
- one for university support of industry efforts to achieve the SAI 2015 goals (closes Sept 12)
- 20% cost-share
- total DOE funding ~ \$ 4 - 8 million per year per solicitation depending on the final House / Senate agreement for solar

Conclusions

- The photovoltaics (PV) industry is rapidly expanding worldwide
- Crystalline Si dominant to at least 2015; however, thin films are expanding quickly in the United States
- DOE SAI will greatly lower \$/Watt values, improve system reliability, and expand manufacturing capabilities, to allow PV to become an important part of the national energy mix by 2015
- SAI is oriented around industry led partnerships (TPPs), and will work closely with the national labs and universities

**High-Efficiency Si Solar Cell Processing Requirement:
Why $0.5 + 0.5 \neq 1$ (i.e., >3)**

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The wafer-silicon photovoltaics industry is at a crossroads. High-efficiency ($>20\%$) commercial cells require high-lifetime ($>>500$ microsecond) mono-silicon wafers and alternative contacts, whereas "standard" cells can be made with almost equal performance from mono- or multi-Si "solar-grade" wafers. Although this is acknowledged in manufacturing, the consequences have not yet been incorporated into the thinking of the fundamental research and development (R&D) community.

Richard Swanson, at the 13th Silicon Workshop, had outlined a pathway to high-efficiency cells, now commercially pursued successfully by SunPower Corp. and Sanyo. Table 1 reproduces Swanson's [1] semi-empirical analysis on combined factors contributing to higher efficiency.

Table 1. Swanson's table on how to achieve higher commercial Si solar cell efficiencies.

Row	Material or Device Enhancement Measure	Commercial Cell Eff. (%)
1	"Conventional" Silicon Cell	14.7
2	High-Lifetime Base	14.8
3	Back-Surface Field (BSF)	15.6
4	Rear Local Contacts (RLC)	16.5
5	Passivated Emitter (PE)	16.8
6	Selective Emitter (SE)	17.1
7	BSF + PE	18.3
8	SE + RLC	19.7
9	High-Lifetime + SE + RCL	21.2

As seen from Table 1, it is reasonable to expect improved performance by combining high-lifetime, selective (or buffered) emitters and collectors. The Si photovoltaic (PV) community is now also acknowledging another example of interactive processing. As wafers are thinned—driven by the need to conserve Si material—the passivation of the back-contact becomes more critical. If losses simply added up, the same back-contact

passivation would result in similar cell performance for a given absorber quality, independent of the absorber thickness. But the latter case is clearly not observed.

Solar cell optimization is ineffective if optimization schemes focus on a single aspect of the device at a time and if analytical methods divide losses into individual loss mechanisms—for example, in wafer and surface recombination losses. The observations about thin-cell performance clearly suggest that a third dimension (in this instance, wafer thickness) will determine bulk and surface recombination losses, not merely the bulk and junction “quality.”

Understanding the interactive nature of losses is extremely important. It also suggests abandoning previously practiced solar cell optimization schemes of optimizing a single device feature at a time. For example, Wang et al. [2] recently reported that in fabricating heterojunction solar cells, the cell voltage improved when both the front and back contact are hetero-contacts. Conventional “systematic” cell optimization studies that would change only one device aspect at a time (e.g., the front contact from a p/n junction to a heterojunction contact) might actually miss the benefit of hetero-contacts by not implementing them simultaneously at the front and rear of the cell. Solar cell theory is in desperate need of correctly accounting for and predicting the interactions of various performance-altering factors.

At the 15th Silicon Workshop [3], I presented a simple model to explain some of the interactive nature of optimization. The open-circuit voltage (V_{oc}), limited in all “standard” (full-surface heterojunction) solar cells to about 620 mV, must be limited by the splitting of the quasi-Fermi levels in the Si wafer (or, more generally, the cell absorber). Because higher lifetime wafers ordinarily do not result in “standard” cells with greater voltage, it is argued that the splitting of the quasi-Fermi levels in standard cells is limited by the contacts, and the essentially infinite recombination of the contacts reaches into the wafer to limit V_{oc} . Accepting this mechanism, it becomes clear that replacing a solar-grade wafer with a high-lifetime mono-Si wafer in a standard cell will not improve cell voltage. Because of higher wafer quality, the essentially infinite recombination of the contact will reach even further into the absorber. Consequently, higher and lower voltages have been reported when processing solar-grade and high-lifetime mono-Si wafers into solar cells without reoptimization of the junction for each wafer type.

The solution to the problem is to minimize the influence of the contacts, either by going to selective-emitter and rear-localized contact structures, or by using heterojunctions and “buffers” as in a “HIT” or MIS solar cell structure. Current analyses concluded that these latter solar cells have better passivated surfaces. This statement is correct, but many scientists incorrectly conclude that this was accomplished by reducing the number of defects in the cell’s junction area, which is not the case. For example, in developing HIT solar cells, it has been reported that a-Si:H(n)/wafer/a-Si(p) structures have a lower cell voltage than a-Si:H(n)/a-Si(i)/wafer/a-Si:H(i)/a-Si:H(p) structures [4]. However, it can easily be argued that inserting the intrinsic (i) thin layers adds to the total number of defects near the junction. Inclusion of these layers enhances V_{oc} not because of defect

reduction, but rather, because these layers reduce the effect of how contact recombination reduces the quasi-Fermi level splitting in the absorber. A 4-nm-thick i-layer typically used in HIT solar cells, after light exposure, contains midgap defects on the order of $1\text{--}2 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$. This adds an equivalent of 10^{11} to 10^{12} cm^{-2} surface defects to the junction area, yet enhances cell V_{oc} .

Observing how commercial module efficiencies have progressed, I argue that it is important to develop better solar cell theories that explain all results, both expected and unexpected. Figure 1 shows the progress made as expressed by the specification sheets for the highest-efficiency modules commercially available. For the sake of completeness, non-wafer Si PV technologies are also included. Note that this figure represents a combination of the potential of a given PV technology and the manufacturing maturity of actual manufacturers. Often, when a new manufacturer first introduces a new product for sale, it is less efficient than a similar product from a more mature established manufacturer.

Figure 1. Average best commercial module technologies since 2004, averaged by PV technology.

It is noteworthy to realize that progress has been “slow” in recent years in all PV technologies, except perhaps for CdTe technology. To me, this suggests that while solar-grade Si has resulted in cell efficiencies much larger than previously thought (say perhaps 15 to 20 years ago), most of the advances possible with standard solar cell materials have been achieved. Hence, I project that there is little future progress with standard solar cells using solar-grade materials. It is also unlikely that current efficiencies can be

maintained by using even lower-grade Si feedstocks (such as upgraded metallurgical-grade Si) for fabricating solar wafers or ribbons.

Producing commercial cells with efficiencies $>20\%$ requires two new approaches: (1) non-standard contacting approaches, and (2) wafers with very high lifetimes ($>>500\ \mu\text{s}$, probably $>1000\ \mu\text{s}$). Currently, such wafers can only be produced from single-crystalline wafers and electronic-grade feedstock. A good correlation between wafer lifetime and cell voltage has been established [6] for such high-efficiency cells. My analyses project that these technologies will eventually provide the most cost-effective Si solar cells [5]. Sanyo and SunPower are already pursuing this manufacturing approach on a commercial scale. Implementing only one of the aforementioned improvements will result in little or no improvement in cell efficiency, as predicted by Swanson in Table 1. To continue commercialization of these high-efficiency approaches, it is important to assure that enough high-lifetime mono-Si wafers will be produced for the PV industry and that enough electronic-grade feedstock will be available for their production.

The Si PV community has sometimes argued that they are the dominant PV technology. This historic observation is rapidly changing, especially for US-located manufacturing. Figure 2 shows the annual shipments through 2006 on a logarithmic scale grouped by PV technology and geographical region. From hereon onwards, high-efficiency lower cost thin-film PV technologies and “non-standard” mono-Si wafer based technologies will gain market share more rapidly than Si wafer/ribbon based PV approaches. In 2006, 45% of all US-produced modules were made using a thin-film PV technology. A rationale for the cost benefit of various PV Technologies has also been developed [5].

Figure 2. Annual PV shipments as reported by *PV News* (Maycock), grouped by technology and geographical region.

As a final remark, I want to stress the importance of these observations. Because losses are interactive, solar cell analyses that separate losses contributing to less-than-ideal performance into individual recombination contributions may not improve the understanding of solar cell operation, but rather, omit important information. Solar cell optimization schemes that optimize one cell feature at a time may lead to overlooking better cell structures that can only be obtained by combining the correct processing and new device features.

The best historic example, in the context of this workshop, is that modern processing of solar-grade wafers has resulted in cells with efficiencies believed to be impossible on the basis of the impurity and defect content in solar-grade wafers. Much fundamental cell theory based on Shockley-Read-Hall recombination treats recombination losses as if they simply add arithmetically. However, observations suggest that the interactive nature of losses can be more important and have a larger effect on cell performance compared to individual loss contributions. This dilemma needs to be resolved in the future.

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ABSTRACT

Interaction of hydrogen with extended defects in Si

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Keywords: Passivation of dislocation states, Hydrogen molecules in voids, platelets,

A well known and technologically important aspect of hydrogen incorporation into semiconductors is the passivation of electrically active defects. On the other hand hydrogen induced defects are usually detrimental for device performance and processing steps are needed to circumvent their generation.

The presentation addresses both aspects the passivation and generation of defects due to the interaction of hydrogen with extended defects in silicon. The following subjects will be discussed:

- the passivation of electrical levels due to dislocations. In contrast, the dislocation related D-band luminescence is not passivated. The changes in the luminescence spectra after hydrogenation points to the origin of the D-band recombination process.
- the generation of extended defects by high dose implantation of hydrogen. After hydrogen implantation Si-H bonds are formed and internal strain builds up. After annealing, the relaxation of the implanted layers is found to be connected with the formation of hydrogen saturated vacancies and larger voids. Further thermal treatments lead to blistering and defoliation of thin silicon layers.
- In hydrogen plasma treated samples, where well defined platelets on {111} planes are found to trap hydrogen molecules. New broad photoluminescence spectra are associated with locally strained areas in the sample. Thermal annealing of the platelets leads to strain reduction at the expense of dislocation formation.

Only the combination of low temperature photoluminescence and Raman spectroscopy, X-ray diffraction, optical microscopy (visible and infrared) and DLTS measurement made it possible to achieve a consistent picture of the studied hydrogen induced processes.

Introduction of H into Si from a SiN_x coating: Role of the SiN_x density and the Si/SiN_x interface

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Abstract

A quantitative comparison has been made of the concentrations of H that are introduced into a Si model system by the post-deposition annealing of high-density and low-density SiN_x coatings, that is, by the hydrogenation process used to passivate defects in multicrystalline Si solar cells. Experiments have also been performed in which the processing of the SiN_x/Si interface was modified to compare how properties of the interface and properties of the SiN_x film itself affect the concentration of H that is introduced into the Si bulk.

Hydrogen is commonly introduced into multicrystalline Si solar cells to passivate defects in the Si bulk and improve solar-cell performance.¹⁻⁷ A low-cost method to introduce H that is widely used is by the postdeposition annealing of a hydrogen-rich SiN_x layer that is deposited onto the solar cell for use as an antireflection coating. The effect that the post-deposition annealing of a SiN_x layer has on solar-cell performance has been widely studied in order to develop a more fundamental understanding of this hydrogenation method.⁸⁻³⁰ A difficulty that has been encountered in such studies is that the concentration of H introduced into the Si bulk under ordinary circumstances is too small to detect and quantify by methods such as secondary ion mass spectrometry (SIMS) even when D is used to improve the detection limit ($\approx 10^{15}$ cm⁻³).^{31,32}

The correlation between the SiN_x film density and the effectiveness of the passivation of defects in the Si bulk has been investigated recently.^{18,25-29} Denser films have been reported to be more thermally stable and more effective for bulk passivation (as measured, for example, by the Internal Quantum Efficiency of solar cells at long wavelength). While the SiN_x film density can be measured directly, a convenient strategy has been developed by researchers at the Energy Research Center of the Netherlands (ECN) in which IR spectroscopy is used to characterize the SiN_x film properties.^{18,25,26} The integrated intensity of a broad Si-N IR absorption band at near 820 cm⁻¹ has been found to be proportional to the SiN_x film density and an optimum film density has been identified. The positions and intensities of Si-H and N-H IR absorption lines that have been used to characterize the hydrogen content of SiN_x films have also been found to be correlated with the intensity of the Si-N IR line and the SiN_x density. The Si-H line is more

intense in lower density SiN_x films and decreases in intensity and shifts to higher frequency as the film density increases. Dekkers *et al.* found that the SiN_x film density depended monotonically on deposition temperature in their experiments and that SiN_x films deposited at a temperature of 425 °C were approximately 13 % denser than films deposited at a temperature of 300 °C.²⁷⁻²⁹

While great progress has been made, several issues have remained controversial because it has been difficult to provide definitive answers to questions about the SiN_x hydrogenation process when the H that is introduced into the Si bulk cannot be directly detected. For example, some groups believe that the density of the SiN_x film is of primary importance for hydrogenation effectiveness, with more dense films leading to better bulk passivation, while other groups have reported that the SiN_x/Si interface and the hydrogen that can be trapped there are of primary importance.³⁰

To help address questions for which quantitative information about the H concentration would be insightful, a Si model system has been developed in which hydrogenated impurities in the Si bulk can be detected by IR spectroscopy with a sensitivity sufficient to determine the concentration of H introduced by the post-deposition annealing of a SiN_x coating.^{33,34} It was found previously that H could be introduced into the Si bulk with a concentration up to $\sim 10^{15}$ cm⁻³ and that the concentration of H that is introduced is sensitive to processing methods, for example, the SiN_x deposition conditions and annealing procedure.³⁴ A hydrogen concentration of $[H] \leq 10^{15}$ cm⁻³ is an interesting range. This concentration is sufficiently low to be less than the detection limit for SIMS measurements, but sufficiently high to passivate the typical concentrations of traps found in solar cells fabricated from multicrystalline Si.

In the present paper, a quantitative comparison is made of the concentrations of H that are introduced into our Si model system by the post-deposition annealing of high-density and low-density SiN_x films that have been well characterized by IR spectroscopy. Furthermore, we have performed experiments in which the processing of the SiN_x/Si interface was varied to compare how properties of the interface and properties of the SiN_x film itself affect the concentration of H this is introduced into the Si bulk.

For our experiments, Pt impurities, to be used as traps for H, were diffused into Si samples grown by the floating-zone method at a temperature of 1050°C for an indiffusion time of 72 h. The resulting Pt concentration is estimated to be $\sim 2 \times 10^{16}$ cm⁻³ from solubility data in the literature.³⁵ While Pt is not an impurity that is typically found in solar cells, its properties as a trap for H make it an ideal model trap for our experiments. When Pt in p-type Si traps hydrogen, it forms a neutral PtH⁰ complex with an IR line at 1880 cm⁻¹ whose intensity has been calibrated so that the concentration of hydrogen can be determined.^{36,37} The PtH⁰ complex is dissociated by annealing at 650 °C so that at temperatures near 750 to 800 °C where H is typically introduced from SiN_x layers, H diffuses rapidly.³⁴ When a sample cools, the H in the sample becomes stably trapped to form PtH⁰ complexes that are readily detected by IR spectroscopy.

SiN_x layers were deposited onto Si samples by plasma-enhanced chemical vapor deposition (PECVD) using 50 kHz and 13.6 MHz reactors. The substrate temperatures for the depositions were 425°C and 300°C for the 50 kHz and 13.6 MHz reactors, respectively. Several samples received an NH₃ pretreatment before SiN_x deposition. The pretreatment is an NH₃ plasma process step (only NH₃ in the ambient) performed in the same PECVD reactor. The nitride layer thickness and index of refraction were determined by ellipsometry at 632.8 nm for several of our SiN_x layers. Layer thicknesses were found to be between 68 and 78 nm and the index of

refraction was found to be between 1.98 and 2.01. Post-deposition anneals to introduce H (750 °C for 1 min) were performed by rapid thermal processing (RTP).

IR absorption measurements have been made to characterize the SiN_x layers and also the hydrogenated Pt impurities in the Si bulk. IR spectra were measured with a Bomem DA3 FTIR spectrometer equipped with a KBr beamsplitter. An InSb detector (77 K) was used for measurements of H-stretching modes and a Si bolometer (4.2 K) was used for Si-N modes.

To characterize the SiN_x layers, measurements were made with the probing beam at normal incidence and with the sample at room temperature. The baselines of transmission spectra were corrected with a procedure developed by Maley.³⁸ The method of Connell and Lewis³⁹ was used to account for multiple reflections in the sample so that the absorption coefficient vs frequency could be determined from a baseline corrected transmission spectrum.

For studies of the PtH⁰ vibrational line at 1880 cm⁻¹, measurements were made for samples in a multiple-internal-reflection (MIR) geometry to increase the sensitivity of vibrational spectroscopy for the detection of small concentrations of H-containing defects. Samples with dimensions 15 x 18 x 1.5 mm³ were made from p-type Si into which Pt had been diffused. The ends of the samples were beveled at 45°. The probing light was introduced through one of the beveled ends so as to be multiply reflected many times from the internal surfaces as it passed through the sample. Samples were cooled for IR measurements of the PtH⁰ line to near 4.2 K with a Helitran, continuous-flow cryostat. (The PtH⁰ IR line is narrow at low temperature, improving the detection limit of the IR measurements.)

The SiN_x layers deposited with the 50 kHz and 13.6 MHz reactors were characterized by IR spectroscopy. Fig. 1 shows IR spectra (absorption coefficient vs frequency) for the Si-N, Si-H, and N-H stretching bands of SiN_x layers that had been deposited on double-side polished Si substrates. The integrated absorption $[\int (\alpha/\bar{\nu}) d\bar{\nu}]$ of the Si-N band at 820 cm⁻¹ for the films

Fig. 1. IR spectra (room temperature) for SiN_x layers approximately 75 nm thick deposited on Si substrates. The Si-N, Si-H, and N-H stretching bands are shown. Spectra drawn with solid lines are for high-density SiN_x films and spectra drawn with dashed lines are for low-density SiN_x films. The upper spectra are for films deposited with an NH₃ pretreatment of the Si substrate and the lower spectra are for films deposited without an NH₃ pretreatment.

deposited at 50 kHz with a substrate temperature of 425 °C is comparable to that measured by others for high-density films.^{27,28,40} The integrated absorption for films deposited with the 13.6 MHz reactor with a substrate temperature of 300 °C is reduced by 15%, similar to results in the literature for lower density films.²⁷⁻²⁹ In the following, we will refer to the SiN_x films deposited with the 50 kHz reactor as high-density films and the SiN_x films deposited with the 13.6 MHz reactor as low-density films. The behavior of the Si-H IR bands shown in Fig. 1 strengthens our comparison to the results for SiN_x films reported by others;^{18,25,26} the lower density films show a stronger Si-H absorption band that is at lower frequency (2160 cm⁻¹) as compared to the weaker Si-H absorption band seen for high-density films that is shifted to higher frequency (2190 cm⁻¹).

In our experiments, we will compare results for SiN_x films deposited both with and without an NH₃ plasma pretreatment of our Si samples. Fig. 1 shows IR results for SiN_x films that had been deposited both with and without this NH₃ pretreatment. The pretreatment did not appreciably affect the IR spectra measured for the SiN_x films, and, therefore, did not affect the densities of the films as characterized by IR spectroscopy.

Several experiments have been performed to compare the concentrations of H introduced into the Si bulk by the post-deposition annealing of SiN_x films. The concentration of PtH⁰ complexes can be determined from the area of the 1880 cm⁻¹ IR absorbance line with the relationship,³⁷

$$[\text{PtH}^0] (\text{cm}^{-3}) = 2.6 \times 10^{16} \text{ cm}^{-1} \left(\int A_{SP} d\bar{\nu} \right) / x. \quad (1)$$

Here, $\bar{\nu}$ is the frequency in wavenumber units, and A_{SP} is the absorbance for a single pass through the absorbing layer at normal incidence which can be readily determined from MIR measurements from the known geometry of the sample.⁴¹ The thickness x of the hydrogenated layer is unknown (although 500 μm is a reasonable estimate),⁴² so that the product of the PtH⁰ concentration times the layer thickness, or the areal density, can be determined from the area of the absorbance line. Our previous experience with the trapping of H by Pt to form PtH complexes indicates that the majority of H introduced into the Si bulk will be trapped when the Pt concentration exceeds the H concentration as is the case here.^{34,36,37} Therefore, under the present experimental conditions, the concentration of PtH⁰ complexes reflects the total concentration of H introduced into the Si from the SiN_x layer.

Experiments have been performed to compare the concentrations of H introduced by high density and low density SiN_x films. Fig. 2 compares the strengths of the PtH⁰ vibrational lines produced by different hydrogenation treatments. Table I gives the corresponding areal densities of hydrogenated impurities determined from the intensities of the IR lines with Eq. (1). Pretreatments of the Si surface are often used prior to SiN_x deposition and provide a method to modify the SiN_x/Si interface; in our experiments, the effect that pretreatment has on the effectiveness of bulk hydrogenation has also been examined. The following results were obtained:

- (i) The SiN_x coatings with higher density were most effective at introducing H. A comparison of the results from spectra (a) and (c) (Fig. 2 and Table I) shows that the high density SiN_x film deposited after an NH₃ pretreatment introduced 20x more H than the low density film with similar surface pretreatment.
- (ii) The NH₃ pretreatment of the Si surface prior to SiN_x deposition increased the concentration of H that was introduced. For the high density SiN_x films [spectra (a) and (b) and Table I], NH₃ pretreatment increased the concentration of H that was introduced by a factor of 3. This beneficial effect of pretreatment of the Si surface was not reflected in the densities of the SiN_x

coatings as probed by IR spectroscopy of the Si-N IR band. For the lower density films [Fig. 2, spectra (c) and (d) and Table I], pretreatment did not affect the concentration of H that was introduced appreciably.

Fig. 2. IR spectra (4.2 K) for Si:Pt samples hydrogenated by the postdeposition annealing (750°C, 1 min) of H-rich SiN_x layers. The absorbance for a single pass of the probing light through the sample was determined from MIR measurements made for samples with known dimensions. The left panel shows spectra for high density SiN_x layers deposited (a) with and (b) without an NH₃ pretreatment. The center panel shows spectra for low density SiN_x layers deposited (c) with and (d) without an NH₃ pretreatment. The right panel shows spectra for (e) a sample with a thin high density SiN_x layer followed by the deposition of a low density SiN_x layer and (f) a sample onto which a high density SiN_x layer had been deposited followed by removal by etching and the deposition of a low density SiN_x layer. It should be noted that the absorbance scale for the left panel differs by a factor of 10 from the center and right panels.

Table I. Results for the introduction of H into Si by the postdeposition annealing (750 °C, 1 min) of SiN_x layers. Deposition method and the areal density of hydrogen in the Si bulk, as determined from the area of the 1880 cm⁻¹ PtH⁰ vibrational line, are shown. Sample labels correspond to the labels of the spectra shown in Fig. 2.

sample	treatment	PtH ⁰ areal density (cm ⁻²)
a	SiN _x (50 kHz, 425°C) NH ₃ pretreat	22x10 ¹²
b	SiN _x (50 kHz, 425°) no pretreat	6.9x10 ¹²
c	SiN _x (13.6 MHz, 300°C) NH ₃ pretreat	1.1x10 ¹²
d	SiN _x (13.6 MHz, 300°C) no pretreat	0.9x10 ¹²
e	thin SiN _x (50 kHz, 425°C) NH ₃ pretreat add SiN _x (13.6 MHz, 300°C)	3.0x10 ¹²
f	SiN _x (50 kHz, 425°C) NH ₃ pretreat etch and add SiN _x (13.6 MHz, 300°C)	1.7x10 ¹²

Further experiments were performed to probe whether H trapped at the Si/SiN_x interface is the dominant source of H that is introduced into the Si bulk or whether the characteristics of the SiN_x layer itself determine the concentration of H that is introduced. An experiment was performed in which a thin layer (10 nm) of high density SiN_x was deposited (with NH₃ pretreatment) followed by the deposition of a layer of low density SiN_x to produce a total layer thickness near ~75 nm, similar to other samples studied here. This two-layer scheme was intended to produce a Si/SiN_x interface typical of that produced by the deposition of high-density SiN_x but with a nitride layer of predominantly low-density SiN_x. In this case, the quantity of hydrogen introduced by post-deposition annealing was ~3x greater than for a low density SiN_x film alone, but much less hydrogen was introduced than from a high-density SiN_x film alone [comparing spectrum (e) with spectra (c) and (a) in Fig. 2 and the corresponding areal densities given in Table I].

An additional experiment was performed in which a layer of high density SiN_x was deposited (with NH₃ pretreatment) to attempt to create a hydrogen-rich damage layer near the Si surface that has been suggested to be an important source of hydrogen.³⁰ The high density SiN_x was then removed by etching with HF/H₂O and a layer of low density SiN_x was deposited. A post deposition anneal of this low density SiN_x layer introduced a concentration of H similar to that of a sample coated only with a layer of low density SiN_x [comparing spectra (f) and (c) in Fig. 2 and the corresponding areal densities given in Table I]. That is, an attempt to produce a hydrogen rich layer near the Si surface by a deposition of high density nitride had only a small effect in our experiments.

The H that is introduced by the post-deposition annealing of a SiN_x coating has been investigated for a Si model system in which the H can be detected and quantified. The results of our experiments provide quantitative information about the concentration of H that shows that the optimization of the quantity of hydrogen that is introduced to passivate defects in the Si bulk requires that neither the properties of the SiN_x film nor the Si/SiN_x interface can be neglected. High density SiN_x films deposited after a NH₃ pretreatment were found to be most effective for the introduction of hydrogen, introducing 20x more hydrogen than low density films. If the Si surface did not receive an NH₃ pretreatment prior to SiN_x deposition, the quantity of H that was introduced into the Si bulk was found to be reduced by a factor of 3, even though IR measurements of the Si-N, Si-H, and N-H IR bands of the SiN_x film showed no obvious change in the properties of the SiN_x. Our results also indicate that while pretreatment of the Si surface has a significant effect on the concentration of H that is introduced, H trapped at the Si/SiN_x interface³⁰ is not the primary source of H introduced into the Si bulk; in the present study, a high density SiN_x film has been found to be necessary to optimize the quantity of H that is introduced into the Si bulk.

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40. The integrated absorption coefficient is 7000 cm^{-1} for the high-density films shown in Fig 1. A precise comparison of the value of the integrated absorption coefficient with values in the literature is difficult because different procedures have been used to analyse transmission data. Nonetheless, this value differs from values in the literature by only a small factor. Comparisons of data analyzed in the same study are more reliable.
41. A_{SP} , the absorbance for a single pass through the sample at normal incidence, is the absorbance measured in an MIR experiment divided by $N \sec(\theta)$ where $N = L \cot(\theta) / w$ is the number of passes the light beam makes through the absorbing layer. L is the length of the MIR sample, w its thickness, and θ the bevel angle ($= 45^\circ$ here).
42. We have found previously that the penetration depth of H introduced by the post-deposition annealing (750°C) of a SiN_x surface layer is close to the depth that is predicted from the diffusion coefficient determined by Van Wieringen and Warmoltz, [*Physica* **22**, 849 (1956)] or, for a 1 min anneal at 750°C , approximately $500 \mu\text{m}$. With this hydrogen penetration depth, an areal density of $2.5 \times 10^{13} \text{ cm}^{-2}$ corresponds to a local hydrogen concentration of $[\text{H}] = 5 \times 10^{14} \text{ cm}^{-3}$.

Silicon Solar Cell Passivation using Heterostructures

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Abstract

Standard surface passivation schemes for crystalline silicon solar cells use SiO₂ or SiN_x. The c-Si surface passivation mechanisms related with these schemes have been elucidated within the framework of interface recombination modeled by an extended SRH formalism: interface recombination centers characteristic of the SiO₂ passivation have larger electron (e^-) than hole (h^+) capture cross sections and SiO₂ yields thus poorer passivation of lower resistivity p -type c-Si, while SiN_x layers lead to the occurrence of a large fixed charge density leading, for instance, to parasitic leakage currents that adversely affect the performance of SiN_x rear passivated p -type c-Si solar cells. An alternative to these two major schemes is hydrogenated amorphous silicon (a-Si:H). In this paper, we determine first differences between the natures of the electronic recombination centers. To understand the passivation properties of a-Si:H, we then introduce an interface recombination model based on the amphoteric nature of silicon dangling bonds. We show experimentally and theoretically that a-Si:H is a high performance and broad range surface passivation material as its e^- and h^+ capture cross sections on neutral defects are similar, while additional field effect passivation can be tuned by further growth of doped a-Si:H layers. The quality of the passivation is illustrated with a lifetime of 7ms reached on lightly p -type doped c-Si passivated with intrinsic a-Si:H, which is to the best of our knowledge the highest ever measured value for a-Si:H passivated wafers. By using our modeling of the a-Si:H/c-Si interface recombination as a guidance for interface and solar cell improvement, we are able to fabricate full a-Si:H/c-Si heterojunction devices reaching a maximal open-circuit voltage of 713mV and a maximal efficiency of 19.1% on flat c-Si wafers, using very high frequency plasma enhanced chemical vapor deposition (VHF-PECVD).

1. Introduction

Within the actual trend towards thinner and more efficient silicon solar cells, surface passivation is becoming a more and more important issue. At the crystalline silicon (c-Si) surface, the abrupt discontinuity in the crystal structure results in a high density of dangling bonds, creating a large density of defects in the bandgap. Passivation schemes allow terminating these dangling bonds properly, and by consequence the number of recombination centers can be considerably decreased. Silicon dioxide (SiO₂) and silicon nitride (SiN_x) are the standard surface passivation materials. An alternative to these two major surface passivation schemes is hydrogenated amorphous silicon (a-Si:H) [1], that attracted the photovoltaic community's attention due to the success of Sanyo's a-Si:H/c-Si heterojunction (HJ) solar cells. Using stacks of intrinsic plus doped a-Si:H layers to form both the emitter and the back surface field (BSF), Sanyo's HIT solar cells hold the world record open-circuit voltage (V_{OC}) of c-Si based solar cells [2].

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SiO_2 , SiN_x and a-Si:H have all inherent advantages and drawbacks: SiO_2 yields the lowest interface state densities [3] but only when grown at high temperatures ($\sim 1000^\circ\text{C}$) followed by a subsequent anneal and it suffers from long term stability issues. SiN_x is an excellent antireflection coating and is grown at lower temperatures ($\leq 400^\circ\text{C}$), but, because of the presence of a large fixed charge, the effectiveness of the passivation depends on the Si doping type and level. In particular, parasitic current flows through p -type BSFs can occur [4]. a-Si:H provides excellent surface passivation [5], passivates all Si doping types and levels and can be used to form both the emitter and the BSF. It is grown at temperatures as low as 200°C , but it does not withstand temperatures higher than 400°C . Additionally, for solar cell front passivation, only ultra-thin a-Si:H layers can be tolerated due to their high blue light absorption. It becomes therefore obvious that the choice of the best passivation layer is strongly influenced by the device structure and by the fabrication process sequence.

The main experimental parameter used for the quantification of the c-Si surface passivation's quality is the lifetime (LT) of the overall excess (photo-generated) carriers. Using high bulk LT c-Si substrates, the surface passivation properties of an overlying material can be studied independently. The modeling of the injection level dependent passivation yields insight into the specific surface passivation mechanism provided by a material. Finally, the injection level dependent LT measurements allow the determination of upper limits for the V_{OC} and the maximum power point of complete, contacted Si solar cells. Conversely, together with the measurements of the final solar cell's current-voltage (IV) curve, injection level dependent LT measurements allow for device diagnostic whenever the predicted upper performance limits are not reached.

2. Injection level dependent surface passivation

The injection level dependent LT of extra charge carriers photo-generated in the c-Si bulk is most easily evaluated by measuring the excess carrier density (ECD) decay, during or after a short light pulse with the quasi-steady-state photo-conductance (QSSPC) and the photo-conductance decay (PCD) techniques [6]. The measured effective LT τ_{eff} results from excess carrier recombination within c-Si and at its surface and is therefore given by $\tau_{eff}^{-1} = \tau_{c-Si}^{-1} + \tau_{surface}^{-1}$. Bulk c-Si recombination is composed of intrinsic radiative, intrinsic Auger and extrinsic SRH recombination, hence $\tau_{c-Si}^{-1} = \tau_{rad}^{-1} + \tau_{Aug}^{-1} + \tau_{SRHbulk}^{-1}$. Lightly doped (intrinsic recombination is only limiting at high injection levels) FZ (few bulk defects, high $\tau_{SRHbulk}$) wafers are the most appropriate to explore the upper LT limits imposed by various surface passivation schemes.

Figure 1. State of the art surface passivation of lightly doped p - (left) and n -type (right) FZ c-Si.

Figure 1 compares the passivation performances of SiO_2 , SiN_x and a-Si:H on such lightly doped FZ wafers. The c-Si bulk LT is parameterized according to Kerr *et al.* [7]. The results for a-Si:H have been obtained at the University of Neuchâtel. Before loading wafers into the PECVD chamber, we just take them out of box, as received from the commercial supplier, and dip them into diluted HF.

Alnealed SiO_2 such as grown by Kerr *et al.* yield the highest LTs ever measured on c-Si wafers [3]. Record passivating SiN layers (stoichiometric) achieve slightly lower passivation performances [7]. Our VHF-PECVD intrinsic a-Si:H passivation scheme results in almost the same passivation quality as Kerr's SiN on lightly doped *p*-type c-Si. For the lightly doped *n*-type wafers, we intentionally show a curve with a poorer passivation of a-Si:H than SiN . Such results are obtained when using HF of low purity (frequent re-use or poor DI water quality – however, VLSI grade is not required). With freshly prepared diluted HF, the outstanding a-Si:H passivation LT of 7ms on $130\Omega\text{cm}$ *p*-type c-Si is repeatedly reached.

Our best surface passivating intrinsic a-Si:H (*i* a-Si:H) layers are 50nm thick. To be used in stack with doped a-Si:H layers to form a-Si:H/c-Si HJ solar cells, the *i* a-Si:H thickness has to be reduced to avoid undesired blue light absorption and/or increase in device series resistance. Figure 2 shows thus the passivation performance of HJ solar cell precursors. These are structures consisting of asymmetrical stacks of 4nm intrinsic plus 25nm doped p^+ and n^+ a-Si:H layers. In this example, *n*-type $1\Omega\text{cm}$ and *p*-type $0.5\Omega\text{cm}$ c-Si wafers are used. The implied V_{OC} of the full solar cell is extracted from the injection level dependent LT curves [8] and its value is above 700mV for *n*- and close to 700mV for *p*-type c-Si. The complete HJ device is obtained after contact formation by ITO sputtering on the front and ITO/Ag(Al) on the back of the precursor. The real V_{OC} s as measured by 1-sun *IV* curves amount to 713mV on $1\Omega\text{cm}$ *n*-type, and 695mV on $0.5\Omega\text{cm}$ *p*-type c-Si, close to the implied values.

Figure 2. HJ solar cell precursor's passivation. **Figure 3.** *i* a-Si:H HMI textured c-Si passivation.

To enhance photo-generation within the c-Si by minimizing optical reflection losses, c-Si solar cell surfaces are not flat but textured – at least on the front side. Using textured c-Si, the above mentioned cleanliness issue is of much more importance: purchased, random pyramidal textured $1\Omega\text{cm}$ *n*-type wafers preconditioned the same way as the flat polished c-Si wafers – out of box, HF-dip – are limited to LTs of 0.1ms when passivated with the same *i* a-Si:H layers. Textured wafers with a high quality 100nm thermal oxide, removed with the same HF-dip treatment, perform slightly better when passivated the same way, but LTs of only 0.2ms are reached. In contrast, Fig. 3 shows that the optimal surface preconditioned textured wafers prepared at the Hahn-Meitner Institute [9] (only HF-dipped before VHF-PECVD deposition) are

well passivated by the *i* a-Si:H layers leading to implied V_{OCs} of 725mV on 1Ωcm *n*-type and 720mV on 1Ωcm *p*-type c-Si. The LT of the 1Ωcm *p*-type c-Si drops to 0.1ms at an injection level of 10^{14}cm^{-3} , but nevertheless a solar cell having such an injection level dependence could reach a fill factor (*FF*) of 79%. However, up to now, in contrast to the case of flat c-Si wafers, we did not succeed to maintain the quality of passivation obtained with thick *i* a-Si:H by the subsequent deposition of doped a-Si:H for emitter and BSF formation on thinner *i* a-Si:H layers.

3. Surface recombination modeling

The injection level dependent LT curves such as measured on c-Si FZ wafers passivated with SiO₂ and SiN have noticeably different shapes for different doping types, as can be seen by comparing the left and right of Fig. 1. By modeling the injection level dependence of the c-Si surface recombination in various configurations (e.g. c-Si doping type and level) and comparing to experiment, the mechanism of a specific surface passivation scheme can be elucidated. There are in fact two mechanisms for reducing interface recombination: On one hand, the density of interface states is reduced by e.g. hydrogen passivation of interface dangling bonds, on the other hand, the c-Si surface density of either electrons or holes is reduced by field effect. The latter is achieved by the presence of (fixed) charges within the passivating layer, at the interface with c-Si or on the passivating layer's outer surface. The resulting c-Si surface band bending – and thus the surface carrier densities of electrons and holes n_s and p_s – is usually calculated by the extended SRH surface recombination model [10]. In analogy to bulk SRH recombination, the surface recombination rate U_{SRH} for single level surface states is given by

$$U_{SRH} = \frac{n_s p_s - n_i^2}{(n_s + n_1)/\sigma_p + (p_s + p_1)/\sigma_n} v_{th} N_S [\text{cm}^{-2}\text{s}^{-1}].$$

Real surface states are distributed throughout the whole bandgap, with energy dependent capture cross sections for electrons and holes. The measurement of these energy dependent surface parameters is sophisticated, but the single level case considering only the midgap capture cross sections holds in first approximation.

Experimentally measured injection dependence of effective LT data fitted with this formalism by Aberle *et al.* [11], indicate that the injection level dependence of SiO₂ is mainly governed by the larger capture cross section for electrons than for holes. The left of Fig. 4 shows the surface plot of $U_{SRH}(n_s, p_s)$ with the capture cross section ratio $\sigma_n/\sigma_p = 100$. As $\tau_{eff} \sim ECD/U_{SRH}$, the trajectories on the surface plot (zero surface band bending assumed) reproduce the main tendencies observed on the injection level dependent LT curves for SiO₂ on lightly doped c-Si shown in Fig. 1: The LT decrease at low *ECDs* observed for SiO₂ passivating 150Ωcm *p*-type c-Si corresponds to the flattening of the equivalent trajectory curve in Fig. 4.

Figure 4. $U_{SRH}(n_s, p_s)$ with $\sigma_n > \sigma_p$ (left), $\sigma_n < \sigma_p$ (right).

Figure 5. Amphoteric $U_{DB}(n_s, p_s)$.

Aberle *et al.* [12] identified too that the passivation effect of SiN_x is mostly due to large fixed positive charges within the SiN_x layers. Schmidt *et al.* [13] identified three different interface defects with extremely different electron to hole capture cross section ratios – 1000, 10 and 0.01 – supposed to be Si dangling bonds with different back bond configurations. Which defect dominates, depends on the SiN_x deposition method. The right of Fig. 4 shows the surface plot of $U_{SRH}(n_S, p_S)$ for low frequency direct PECVD deposited SiN_x – supposed to damage the c-Si surface – where the defect with $\sigma_n/\sigma_p = 0.01$ dominates [14].

Passivating low doped c-Si with *i* a-Si:H results in interface dangling bonds that are neutral. However, the amphoteric nature of these defects makes that the SRH model is no more sufficient to describe the results obtained on various wafers. Thus, in the aim of disposing of a suitable model to describe interface recombination at the a-Si:H/c-Si HJ, we extended the model previously established for bulk a-Si:H recombination based on amphoteric defects [15,16] to c-Si/a-Si:H interface recombination [17]. This gives a direct access to the interface recombination center density and to the charges creating the field effect passivation. These charges depend on the capping doped layers, microdoping of the *i*-layer and on band discontinuities at the interfaces. Figure 6 shows the distribution of recombination centers in the bulk a-Si:H bandgap. In first approximation, recombination in band tails is neglected, leading (as sketched in Fig. 7) to two parallel co-existing recombination paths, both consisting of two successive capture events.

Figure 6. a-Si:H density of states. **Figure 7.** a-Si:H recombination steps (successive, parallel).

With the further hypothesis of medium illumination level [16], the calculation of the recombination rate can be reduced to the case of a discrete recombination level possessing three charge conditions. In analogy to the resulting bulk recombination rate, the surface recombination rate U_{DB} can be written as:

$$U_{DB} = \frac{n_S \sigma_n^0 + p_S \sigma_p^0}{\frac{p_S}{n_S} \frac{\sigma_p^0}{\sigma_n^+} + 1 + \frac{n_S}{p_S} \frac{\sigma_n^0}{\sigma_p^-}} v_{th} N_S \text{ [cm}^{-2}\text{s}^{-1}\text{]}.$$

The four capture cross sections depend on the carrier type and on the state of charge of the defect. By analyzing recombination curves on a wide variety of configurations [17], we found best accordance between theory and experiment with $\sigma_n^0/\sigma_p^0 = 0.05$ and $\sigma^{+,-}/\sigma^0 = 500$. Figure 5 shows the surface plot of $U_{DB}(n_S, p_S)$ given above. In contrast to SRH recombination, there exists a local minimum in the DB recombination rate. Its position is determined by the value of σ_n^0/σ_p^0 while its width depends on the value of $\sigma^{+,-}/\sigma^0$. In this minimum, recombination is limited by the larger free carrier density, which is opposite to the SRH case. When the density of one carrier type becomes much higher than the other, U_{DB} reduces to U_{SRH} as denoted by the empty surface in Fig. 5. The trajectories on the surface plot in Fig. 5 show $U_{DB}(n_S, p_S)$ for three different lightly doped c-Si wafers as resulting from surface passivation with 5nm *i* a-Si:H. In general, surface

recombination is examined in terms of the effective surface recombination velocity $S_{eff} = U/EC D = (W/2) \cdot (\tau_{eff}^{-1} - \tau_{c-Si}^{-1})$ to get rid off the dependence on the c-Si wafer thickness W . Figure 8 shows the translation of the trajectories on the surface plot in Fig. 5 into $S_{eff}(ECD)$ curves together with the measured surface recombination velocities of these three different lightly doped c-Si wafers passivated with 5nm *i* a-Si:H. Figure 8 additionally shows that – without further capping layer – these ultra-thin passivation layers are not stable with respect to ambient air storage due to their outer surface potential modification. Plagwitz *et al.* [18] use them in stack with SiN layers as a good illustration of benefiting from advantages while eliminating drawbacks by combining several single layer passivation schemes: thicker a-Si:H layers would absorb too much light and a-Si:H can not act as antireflection coating, while SiN layers with optimum refractive indexes for antireflection coating have no passivating effect on p^+ emitters.

Figure 8. 5nm *i* a-Si:H on different c-Si.

Figure 9. a-Si:H field effect passivation.

While corona surface charging of SiO₂ passivation layers permits the tuning of field effect passivation for examination purpose [19], the deposition of a doped a-Si:H overlayer can produce such a field effect passivation permanently. This is illustrated in Fig. 9, which shows the injection level dependence of the surface recombination velocities of symmetrically grown stacks consisting of 10nm *i* a-Si:H plus 30nm doped a-Si:H passivating 60Ωcm *n*-type c-Si. A second possibility of shifting the Fermi level (i.e. modifying the average state of charge of the recombination centers) in the passivating a-Si:H layers without increasing the defect density consists of microdoping the *i* a-Si:H layers. Figure 9 shows well the equivalent effect of stack deposition and microdoping. The low injection level discrepancies are due to the simplifying assumptions made to obtain the analytical function for U_{DB} .

4. On lifetime measurements and final solar cell performances

A full description of the electrical properties of HJ devices would require, in addition to the parameters extracted from the LT measurement, a precise knowledge of the band positions and band discontinuities which have been shown to be critical [20]. However, the injection level dependence of the effective LT can be transformed into an illumination vs. implied V_{OC} curve and further on into a predicted IV curve. This allows a useful determination of the limits on V_{OC} and FF solely imposed by recombination. Comparing this IV curve with the one measured on the complete contacted device permits to diagnostic any effect of the ITO deposition on the a-Si:H/c-Si HJ precursors. The Suns V_{OC} [8] data of complete solar cells comprises further losses due to shunting, whereas the 1-sun IV curve finally includes series resistance effects.

Figure 10 shows Si HJ solar cells formed on $2.8\Omega\text{cm}$ n -type c-Si. The V_{OC} of the solar cell on the left is limited by surface recombination. The final ITO deposition does not enhance recombination and introduces only small series resistance losses. The precursor on the right should result in a solar cell with a V_{OC} exceeding 700mV. But as seen from the Suns V_{OC} curve, the ITO deposition is detrimental as it causes increased recombination and consequently diminishes the V_{OC} . The final comparison of the Suns V_{OC} and the 1-sun IV curves indicates appreciable "series resistance" losses.

Figure 10. LT (without ITO), Suns V_{OC} and 1-sun IV curves evidence the effect of ITO deposition.

To investigate the reason of the low measured LTs limiting the left cell's V_{OC} to around 680mV, we first checked the c-Si surface preconditioning by fabricating a 50nm thick i a-Si:H passivation LT test sample. As Fig. 11 shows, its passivation would have implied a V_{OC} of 715mV. Thus, the preconditioning is appropriate. Suspecting then that the p -layer deposition deteriorates the overall LT as observed by De Wolf *et al.* [21], the passivation performance of the

Figure 11. a-Si:H passivation of n -type $2.8\Omega\text{cm}$ c-Si.

i/p stack was tested. But the implied V_{OC} falls only down to 690mV. Surprisingly it was – as clearly shown in Fig. 11 – the remaining i/n stack, which was the dominating recombination source limiting the V_{OC} of the solar cell on the left of Fig. 10. Improving the growth conditions of the n -layer ($n2$ stack) resulted in the same implied V_{OC} as achieved by the i/p stack. Using after an additional chamber cleaning this i/n stack for a-Si:H/c-Si HJ solar cell formation yields the LT curve of the cell shown on the right of Fig. 10.

5. Conclusions

SiO_2 and SiN_x are the most widely spread crystalline silicon surface passivation schemes. Intrinsic hydrogenated amorphous silicon is also a highly performing surface passivation material due to its broad range applicability on all kind of c-Si substrates – including all doping types,

levels and surface texture. By modeling the injection level dependence of surface recombination, the surface passivation mechanisms of a specific material can be determined. SiN_x is for example characterized by its high fixed positive charge density. In contrast, with intrinsic amorphous silicon, the magnitude of the field effect passivation can be tuned by fixing its outer surface potential when capping it with doped amorphous silicon layers. Such stacks form the emitter and back surface field of amorphous/crystalline silicon heterojunction solar cells. A key point to our approach, which resulted in the fabrication of high open-circuit voltage heterojunction solar cells, is the interpretation of lifetime measurements on heterojunction test structures that allowed a rapid development by a fast device diagnostic procedure. In particular, by VHF-PECVD, full heterojunction devices with open-circuit voltages higher than 700mV and efficiency up to 19.1% can be fabricated on flat wafers.

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Grid-Competitive Systems Technology A Systems Driven Approach to Cost Reduction

SunPower Corporation
17th Workshop on Crystalline Silicon Solar Cells &
Modules: Materials and Processes
August 5 - 8, 2007
Vail Cascade Resort, Vail, Colorado USA
Terry Jester

1

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2

Ingot Wafer Solar Cell Solar Panel Unitary Product Integrated System

Develop high-efficiency, turn-key PV systems
for the residential and commercial markets to
delivery electricity at grid parity by 2010 - 2015

3

SunPower Corporation
Supplier of the world's highest performance solar modules commercially available

SunPower Corporation, Systems
Leading systems integrator in U.S. with most extensive systems performance database

Solaix Corporation
Developer of breakthrough ingot growth manufacturing technologies

Silicon Genesis Corporation
Developer of BeamSaw wafering technology

Massachusetts Institute of Technology
Research center for direct-write dopants using inkjet printing technology

Dow Corning Corporation
Leading manufacturer and supplier of silicon-based materials in the world

Specialized Technology Resources, Inc.
Leading manufacturer of encapsulant materials for photovoltaic cells

Xantrex Technology, Inc.
Leader in advanced power electronics

New Power Technologies
Leader in optimal siting of solar DG

4

SUNPOWER

Ingot Growing

Key Activities:

- Continuous Cz ingot growth
- Low-oxygen, high-lifetime material
- Development of hot zone for N-type material
- FBR polysilicon process development and implementation
- Crucible durability
- Commercialization of technology licensed from NREL

Participants:

Solaicx

9

SUNPOWER

Cell Efficiency Roadmap

Improvements:

- Passivation
- Optics
- Patterning

10

SUNPOWER

Cell Cost Reduction

Key Activities:

- Step reduction
- Process improvement with focus on manufacturability
- Inline manufacturing

Participants:

SunPower, MIT, NREL

11

SUNPOWER

Laminates and Modules

Key Activities:

- Develop next-generation laminates for integrated products:
 - In-roof and on-roof residential
 - Commercial roof-top
 - Commercial ground mount
- 2nd generation automation

Participants:

SunPower, Dow Corning, STR

12

SUNPOWER Unitary Products

Ground

Roof

Concept Overview:

- Factory manufactured systems
- Module integrated mounting
- Optimized for automated assembly and rapid deployment

Benefits:

- Lower cost:** Leverage standard manufacturing cost reduction practices
- Higher quality:** Controlled manufacturing environment
- Scalable:** Achieve economies of scale at relatively low volumes; fast installation, more productivity

13

SUNPOWER Cells to Systems Factory

Cells → Cells-to-Systems Factory → Unitary Products → Shipping → Installed System

Cells to Systems Factory

- Module Fabrication
- System Assembly
- Module Fabrication
- Project Kitting

Shipping

- Commercial Ground
- Commercial Roof
- Production Homebuilder
- Residential Roof

Installed System

- Ground Tracker
- Unitary Roof
- Residential Roof

Concept Overview:

- Achieve cost-effective, integrated, systems-level manufacturing
- Optimize manufacturing for customer applications

Benefits:

- Reduce costs:** simplified logistics channel, improved automation
- Eliminate redundancy**
- Opportunity for **regional manufacturing**

14

SUNPOWER Automated Deployment

Engineer-To-Order

- Automatic generation of system design based on site features and design rules
- Automatic generation of BOM, costs, scheduling
- Automatic generation of design drawings

Benefits:

- Lower cost:** Reduced design time and cost
- Higher quality:** Automatic enforcement of engineering rules
- Scalable method:** Project internal design expertise to the VAR channel

Optimal Siting:

- Analytic solution to locate high-value sites

Benefits:

- Increased value:** Site selection based on utility system value
- Reduced costs:** Great reduction in transaction cost
- Scalable methodology:** Business model to serve vast market

15

SUNPOWER Task 1 Summary

Ingots Growing Technology Development

Develop and commercialize continuous Cz silicon ingot growing

Key Activities:

- Development of Hot Zone for N-Type Material
- Hot Zone Improvements
- FBR Polysilicon Process Development and Implementation
- Crucible Durability Improvements
- Optimize growth process

Milestones:

- Demonstrate ability to meet the LCOE target costs using the ingot growing technology developed on this project.

Participants:

- Solaiex
- SunPower

16

Wafering Technology Development

Develop production-scale processes that reduce thickness to 145 microns

Key Activities:

- Optimize and determine limitations of slurry abrasive technology
- Investigate break-through wafering technologies such-as fixed abrasive wire and cleaving

Milestones:

- Demonstrate high-speed wafering of 145 um thick wafers with yield of >95%
- Demonstrate feasibility and cost potential of potential break-through technologies

Participants:

- SunPower
- SiGen

17

Inline manufacture of back-contact cells

Develop processes and tools for high volume and low cost production of high efficiency solar cells

Key Activities:

- Improve cell efficiency through combination optimized cell processing and design to reach 23% efficiency
- Reduce cost by process improvement, optimization, and focus on manufacturability
- Develop tools, tool configurations, and automation to support cost reduction and yield improvement in cell manufacturing
- Establish manufacturability of inline and automated steps

Milestones:

- Demonstrate 22% prototype transition process cell (12 months)
- Demonstrate 23.0% production process beta cells (24 months)
- Demonstrate 23.0% production process cell (36 months)

Participants:

- SunPower, MIT, NREL

18

Low Cost, High Performance Modules

Design modules compatible with downstream systems integration and installation processes

Key Activities:

- Develop in-roof and on-roof laminates for residential applications
- Develop modules for rooftop and ground-mounted commercial applications
- Develop modeling tools and common technologies for module platforms
- Develop adhesive and encapsulation materials and application systems

Milestones:

- Complete analysis of field test results for prototype on-roof module
- Demonstrate next-generation production module for commercial applications
- Complete Gen 3 component cost reduction, demonstrating cost reduction of 10% relative

Participants:

- SunPower
- Dow Corning
- STR

19

Unitary Product Development

Develop a family of products that builds on the success of PowerLight product suite and that leverages the advantages of the unitary systems for Commercial Roof, Production Home, Residential Retrofit, and Commercial Ground markets.

Key Activities:

- Integrate structural and mounting functions into a single package that is readily site installed

Milestones:

- Production release of next-generation:
 - Modular tracker
 - Commercial rooftop system
 - BIPV rooftop product
 - Retrofit product

Participants:

- SunPower, SunPower Corporation, Systems

20

Cells-to-Systems Factory

Design, develop, and implement processes and equipment for the unitary product factory

Key Activities:

- Implement an automated module manufacturing line specific to system level products for residential market
- Implement semi-automated manufacturing line to convert laminates to unitary system products for residential and commercial markets

Milestones:

- Complete design of the automated laminate line
- Assess manufacturing cost and comparison against targeted LCOE for all segments
- Complete of process and equipment specifications to allow rapid scaling in regional markets
- Integrate of system manufacturing into module manufacturing lines

Participants:

- SunPower, SunPower Corporation, Systems

21

Engineer-to-Order System: Design & Deployment

Design, develop, and implement processes and equipment for the unitary product factory

Key Activities:

- Develop a fully automated systems design function that accounts for site-specific geometries and topographies.
- Optimize PV systems value by developing siting analysis procedure that accounts for generated electricity's value based on interconnection location

Milestones:

- Demonstrate automated generation of mechanical and electrical layouts, project costing, and BOM
- Develop capability to analyze utility network for high-value solar DG sites
- Perform real-time structural load analysis and system sizing
- Remote evaluation of high-value solar sites based on aerial photography and satellite imagery

Participants:

- SunPower, SunPower Corporation, Systems, New Power Technologies

22

Portable Workshop for Distributors

Develop and implement processes and fully-equipped systems kit to increase efficiency in the downstream product delivery channel.

Key Activities:

- Complete design of on-site, portable materials delivery kit & workshop
- Deploy prototype portable workshops with fully equipped systems kits for residential and commercial distributors

Milestones:

- Demonstrate 80% reduction in installer's warehousing space required based on installer survey
- Implement design software system for translating system configuration to packing list and component specs for kit

Participants:

- SunPower, SunPower Corporation, Systems, Independent Energy Systems

23

Performance Modeling and Monitoring

Improve the accuracy of computer-simulated PV system models. Develop a web-based, customer accessible, system monitor service.

Key Activities:

- Benchmark simulation against weather and system parameters at 300+ sites
- Update model to incorporate new loss assumptions and engineering equations
- Benchmark updated simulation model to determine improvement in accuracy

Milestones:

- Validate of BOS and environmental loss factors through field performance
- Validate of all improvements incorporated in performance model

Participants:

- SunPower, SunPower Corporation, Systems

24

15-Year Warranty Inverter

Improve the accuracy of computer-simulated PV system models.
Develop a web-based, customer accessible, system monitor service.

Key Activities:

- Reduce parts count in mechanical assemblies
- Component lifetime optimization and predictive failure
- Assess failure statistics and design solutions for PV related applications.
- Develop More Rigorous Production-Line Testing and Process Control

Milestones:

- Achieve 2:1 performance ratio, e.g. 20% reliability improvement at 10% cost increase; objective of 6:1 PR
- Demonstrate commercialization
- Complete UL1741 certification and official CEC efficiency testing

Participants:

- SunPower, Xantrex Technology, Inc.

Accuracy in Solar Cell and Module Measurements and Approaches to Improve Them

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Abstract

The electrical performance of Si cells, modules, and systems are rated in terms of their maximum electrical power with respect to a total irradiance, temperature, and spectral irradiance. The impact of the reference conditions, measurement procedures, and equipment on the performance rating is discussed. A high-speed manufacturing environment often requires rapid bin sorting with a repeatability of better than 1%. This constraint, along with estimated uncertainties from module calibration laboratories, is discussed, along with strategies for accurate testing in high-volume production.

I. INTRODUCTION

The current internationally accepted standard reference conditions (SRC) for terrestrial non-concentrating (flat-plate) photovoltaic (PV) devices has been in place since 1985 [1]. Intercomparison of primary terrestrial and extraterrestrial reference cells between and within a calibration laboratory indicates that an uncertainty of less than $\pm 1\%$ in the short-circuit current (I_{sc}) with respect to SRC is not justified [2–7]. Most customers receive secondary calibrations from a primary calibration laboratory, so the uncertainty in I_{sc} is typically even larger. Intercomparisons are important for determining if the quoted uncertainty of a given calibration laboratory is consistent with other calibrations labs' estimated uncertainty. In the PV business, the accuracy or uncertainty is typically quoted with a 95% confidence interval, or in the standard uncertainty analysis method described in the ISO Guide to the Expression in of Uncertainty in Measurement with a coverage factor of 2 [8].

For well-behaved packaged Si reference cells with temperature sensor and separate voltage and current wires attached, Fraunhofer ISE typically quotes $\pm 2.5\%$ in I_{sc} and $\pm 3\%$ in efficiency [9], whereas NREL quotes $\pm 1.4\%$ in I_{sc} and $\pm 1.5\%$ in efficiency [10]. The uncertainties are higher for samples without wires or temperature sensors attached. Many groups mix repeatability, reproducibility, accuracy standard deviation, and uncertainty. The ISO GUM in Ref. [8] requires identifying all random and nonrandom error sources and classifying them as statistical (average of multiple measurements with a standard deviation) and a single-point measurement. For many applications, the random error can be minimized, giving a manufacturer the ability to bin sort at the limits of their random error, with a nonrandom offset between various calibration labs and test beds.

II. SOURCES OF RANDOM ERROR

In bin sorting cells or modules, nonrandom errors do not affect the ability to accurately sort. The goal would be to freeze all nonrandom error sources over as long a time period as possible

and to minimize all random error sources. This would allow the sorting of results into bins with the only uncertainty being a multiplicative offset in the magnitude. These nonrandom errors do not change over time periods of years. These nonrandom errors are typically related to reference cell calibration and probing geometry. There are a variety of random error sources in evaluating the performance of a Si cell or module. Table 1 lists these errors in I_{sc} , fill factor (FF), open-circuit voltage (V_{oc}), and the maximum power (P_{max}) for a hypothetical state-of-the-art Si-cell production-line tester/sorter prior to ribbon attachment. It is assumed that some kind of automatic probing is used.

The spectrum of a solar simulator shifts with bulb age. This is not an error if all cells have the same relative quantum efficiency and it is identical to the relative quantum efficiency of the reference cell. Process variations in the lifetime of Si, antireflection coatings thickness and index of refraction, and surface recombination conspire to cause some variation in spectral error as the bulb ages. Most commercial testers do not correct for intensity fluctuations during the measurement, so random fluctuations in the light level between the time when it was measured and when the portion of the current-voltage (I-V) curve where I_{sc} and P_{max} are determined may have a different intensity. The spatial nonuniformity will change with each bulb change and this will appear as a varying error with each bulb change.

Because of the high-current, low-voltage nature of PV devices—along with probes being used or simulator ribbons being attached—the fill factor depends critically on the probe-to-metal contact resistance and the surface area of the contact. In a factory setting, these differences can be fixed, with the only differences being from variable contact surface area or resistance. For this reason, large differences in FF have been observed between labs relating to probing [11].

The day-to-day variation in cell temperature can be due to the changing thermocouple calibration of $\pm 1^\circ\text{C}$, factory floor temperature, thermal contact to a temperature-controlled surface, or surface temperature of the temperature-controlled surface.

With modern electronics, commercial testers rarely are a significant source of error, as long as the signal levels are greater than 10% of the full-scale range.

The strategy employed in using reference cells to set the light source can be a significant source of random error depending on how they are used.

Table 1. Random Error Sources for a Hypothetical Si Production Tester

<u>Error Source</u>	<u>Magnitude of Error (%)</u>
Light-source related (mostly in I_{sc} , P_{max})	
Spectral error changes with bulb age	1
Spatial nonuniformity between bulbs	1
Intensity fluctuations with real-time correction	0.1
Intensity fluctuations in light measured once	2
Probing related (mostly in FF, P_{max})	
Spring-loaded probe card (superstrates)	2
Variable current contact surface area	1
Variable contact resistance if not using separate V contacts	>2
Temperature (mostly in V_{oc} , and P_{max})	
$\pm 0.5^\circ\text{C}$ temperature-controlled plate	0.2
$\pm 3^\circ\text{C}$ factory floor temperature	1.5

Electronics to measure current and voltage	<0.1%
Reference cell calibration	
Different cells each week calibrated by same lab	1.5
Single reference cell transferred to working standards	0.5
Data acquisition	
Current at a fixed voltage	<1
V_{oc} , I_{sc} , P_{max} algorithm	<1

III. PROCEDURES TO MINIMIZE ERRORS

In a production setting, recalibration of the reference cell or module can cause a substantial change in the test cell's or module's measured current. The random error in a cell or module from a competent calibration lab can easily exceed $\pm 1\%$. This source of variation in a factory setting can be eliminated by fossilizing the calibration value at some value—typically an average of the previous three calibrations. This method has its drawback because of an extreme reluctance to change the fossilized value if the reference degrades. A long-term compromise would be a running average of the previous three calibrations.

For probing fixtures, it is important to have a regular maintenance procedure to clean the probes and verify that all of the probes are functional. Dirt or fingerprints on the reference device can affect the calibration at the 1% level for a packaged device and much more for unencapsulated reference cells. A standard inspection and possibly cleaning procedure should be followed prior to use of a reference device. Errors at the 0.5% level for commercial data acquisition systems are possible, especially if the voltage and current are at the low end of the range. Equipment specifications are typically quoted at full scale whereas the data may be taken at 10% to 50% of full scale. The more accurate the data acquisition system, the lower are these error sources.

Spatial nonuniformity can be a significant source of error, especially when the test and reference devices are different sizes such as a small-area cell used to set the light level of a large-area module simulator. These errors are most noticeable when a bulb is changed, giving a different nonuniformity pattern than before. ISO 9001 or 17025 quality systems require that the measurement system be evaluated on a regular basis to confirm its proper operation. This can be best achieved by measuring the performance of one or two cells or modules of the same type and size as what is normally measured on a regular basis and automatically comparing with previous measurements. The comparison software would red flag any parameters (I_{sc} , V_{oc} , P_{max} , FF) that have drifted too far from their nominal values. “Too far” is a qualitative term, but values of 1% to 2% would be typical.

To be confident that P_{max} measured on the factory floor is comparable to P_{max} measured by a calibration agency, reference modules should be calibrated periodically by the major calibration labs around the world. The quality system for these calibration labs requires periodic proficiency testing. Supplying the calibration lab with data from other labs on the same sample satisfies this requirement. In some cases, calibration fees may be waived if another calibrations lab is made available. The temperature can also be a significant source of day-to-day variation if it is not actively controlled or measured and corrected for. The temperature coefficient on P_{max} is about $0.5\%/^{\circ}\text{C}$, so a 1% difference in data on the production line can occur just because a thermocouple was changed. This is why the PV performance group prefers thermistor- or RTD-

based temperature sensors. Most commercial testers correct for temperature to 25°C to minimize errors related to factory-floor temperature.

IV. STATE-OF-THE-ART

The state-of-the-art in I-V cell and module measurements typically exists at national calibration facilities. These facilities in the United States and around the world are listed in references 3–7. These groups measure the light level with primary reference cells calibrated internally or by another national calibration facility and use equipment and procedures designed to minimize all sources of uncertainty. Typically, these systems do compromise accuracy in order to achieve higher throughputs. Results from these labs typically include spectral correction and do not assume that their reference devices match what they are testing.

In calibrating modules using simulators, a dominant error source is the spatial nonuniformity of the light source. For this reason and others, most of the terrestrial national calibration facilities maintain an outdoor testing capability where errors related to spatial nonuniformity are minimized. Manufacturers eliminate this source of uncertainty by using a reference module. A recent formal intercomparison of commercial modules between national calibration facilities and certified module testing or qualification laboratories indicated that a range of 7% in $P_{\max}$ and 5% in I_{sc} was observed between labs. This range is larger than the 4% range observed in I_{sc} in a previous formal intercomparison [2]. The reasons are not clear, although the previous PEP'87 intercomparison modules included a temperature sensor, a representative cell, and a cell in a module package for spectral responsivity measurements and a “matched” reference cell to set the simulator light level. Figure 1 summarizes the differences in I_{sc} , FF, and $P_{\max}$ for Si modules from the recent module intercomparison [12]. With one exception, nearly all of the differences in $P_{\max}$ can be attributed to differences in I_{sc} .

IV. SUMMARY

The performance of PV cells and modules are rated in terms of their maximum electrical power produced under illumination by the reference spectral irradiance at a given total irradiance and temperature. This rating serves as the basis for comparisons of the efficiency between various technologies. The PV community is attempting to standardize a rating based on the PV energy produced over a given period of time divided by the total irradiance over that same time. The specifics of the time interval (daily, seasonal, or annual) and the air temperature and the total and spectral irradiance versus time are an active area of research.

A variety of artifacts and procedural differences can cause substantial differences in the efficiency. For this reason, the PV community has relied on national laboratories to serve as an independent efficiency verification agency and to be aware of and minimize artifacts and procedural ambiguities.

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Figure 1. Comparison of mono-Si and multi-Si module performance between certified module qualification and performance characterization labs and national PV calibration facilities around the world [12].

Results of European “Performance” Project on PV Module Testing

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Abstract

The EC-funded Integrated Project PERFORMANCE commenced in January 2006 includes a subproject which is dedicated to the improvement of the comparability of PV module performance measurements between European test laboratories and to elaborate guidelines for harmonised measurement practices in PV-Industry. Recently published results of international round-robin tests with PV modules revealed measurement differences between laboratories [1,2,3], which proved to be significant for thin-film and multi-junction devices. This shows a clear need for development of new and adapted measurement procedures suitable also for use in PV industry. With this background, comprehensive intercomparison tests with PV modules were performed that reflected the state-of-the-art of present PV technologies. In particular, several high efficiency c-Si technologies have been involved, for which problems are known if measured with pulsed solar simulators [4,5,6,7]. It must be pointed out that for the first time our investigations did not only focus on the comparison of STC performance data but were also aiming to understand and analyse measuring effects. Therefore, technology specific measurement programmes were defined. For example, this includes variation of measuring parameters of the solar simulator and preconditioning by light exposure. In addition, the variety of measuring equipment (i.e. solar simulator performance) and measurement techniques in use have been documented. This paper presents the results of the first round-robin performed with 5 PV module types covering the range of commercially crystalline silicon cell technologies (size, wafer type, high efficiency). Our investigations revealed a 2% spread in maximum power for 6 participating test laboratories. The resulting data basis enables laboratories to further develop their measurement hardware and techniques. Furthermore, guidelines and adapted measurement procedures for PV industry can be elaborated.

1 Introduction

For documenting measurement discrepancies between test laboratories as well as between PV industry and test laboratories, round robin tests with PV modules are common practice. Results which have been published in the past on PV conferences [1,2,3] mainly concentrate on the PV module performance data at STC. They did not include data analyses which require discussion between the participants on the measurement equipment such as solar simulators and the measuring practices in use. However, this is a condition for understanding of measurement effects and for being able to harmonise measurement procedures in test laboratories. With regard to that, the round robin tests in the “Performance” project are aiming to create specific data basis for PV technologies that can be used to derive best practices.

Two separate round-robin tests with 5 modules different crystalline silicon cell technologies and 7 commercially available thin-film PV modules have been initiated. The c-Si round robin has been completed in May 2007 whereas the thin-film round robin is still ongoing and will be completed by end of 2007. This paper contains the final results of the round-robin test with crystalline silicon modules.

2 Participating test laboratories

The following six European test laboratories have been involved in the crystalline silicon round-robin:

- Arsenal research, Vienna (Austria)
- Ciemat, Madrid (Spain)
- Fraunhofer-ISE, Freiburg (Germany)
- Joint Research Centre, Ispra (Italy)
- SUPSI, Lugano (Switzerland)
- TUV Rheinland, Cologne (Germany)

Table 1 gives an overview of the used test equipment and a description of the measurement technique for determination of the STC performance of PV modules. A detailed inventory of the laboratories through questionnaires revealed a great variety of measuring hardware and measurement practices in use which proved to be a good condition for creating comprehensive data basis for the investigated cell technologies.

Test laboratory	Simulator type	Test
Arsenal	Berger, PSS8	Outdoor calibration of I_{sc} and I-V measurement with pulsed solar simulator (module delivers outdoor I_{sc} , etc)
Ciemat	Belval, Pasan IIIb	I-V measurement with pulsed solar simulator, outdoor measurement for verification of indoor results
ISE	Belval, Pasan IIIb	I-V measurement with pulsed solar simulator, multflash measurement if required (I-V segment), module SR measurement to compensate spectral mismatch
JRC	Indoor: Spectrolab, LAPSS Outdoor: The sun	Indoor measurement of I_{sc} and SR for all modules, outdoor I-V measurement (I_{sc} scaled to indoor measured mismatch corrected I_{sc}), for comparison and evaluation of sweep time effects also indoor I-V measurement
SUPSI	Belval, Pasan IIIa	Single-flash I-V measurement with pulsed solar simulator for non-critical technologies, multflash test method for modules with high efficiency cells (1 data point per flash)
TUV	OSRAM HMI 4000W (steady-state)	I-V measurement with steady-state solar simulator, use of spectrally matched reference devices (mini-modules)

Table 1: Description of test equipment and test methods in the participating test laboratories

3 Measuring programme

Five different cell types have been identified for the round-robin test. The technical data of the test samples are summarised in Table 2. We included 3 mono-Si and 2 poly-Si cell technologies. Two high efficiency cells (SunPower, Sanyo) were selected that are known as critical if measured with pulsed solar simulators.

Of each module type three test samples have been shipped. STC measurements were performed on two modules. One of these was additionally used for an extended measurement programme with pulsed solar simulators which is described below. For the purpose to investigate the influence of spectral mismatch correction the third module was used for spectral response measurements at JRC and ISE.

Cell manufacturer	Cell type	Cell size	Cell interconnection circuit of the module
SunPower Corporation	A-300, back contact	125 x 125 mm (psq)	72s1p and 36s2p
Sanyo Electric Co. Ltd.	HIT	125 x 125 mm (psq)	72s1p
Microsol International LL Fze.	MONO 156 MPSQ	156 x 156 mm (psq)	36s1p
SCHOTT Solar	EFG 12530	125 x 125 mm	72s1p
Qcells AG	Q8TT3-1580	210 x 210 mm	36s1p

Table 2: Cell technologies included in the round robin test

Regarding creation of specific data basis the influence of the following measurement parameters was investigated within an extended test programme for pulsed solar simulators:

- Direction of I-V scan : $V_{OC} \Rightarrow I_{SC}$, $I_{SC} \Rightarrow V_{OC}$
- (Effective) Duration of I-V measurement time: 2 ms .. 30 ms
- Full I-V curve measurement in a single-flash measurement or segmental measurement by multi-flash measurement
- Determination of temperature and irradiance correction parameters

4 Results

The spread of results is shown in Figures 1 to 4. In the diagrams the discrepancies are referred to the average values for P_{MAX} , I_{SC} , V_{OC} , I_{MP} and V_{MP} of each test sample. The following major results can be pointed out:

- The spread of P_{MAX} plotted vs. the test sample no. (Figure 2) reveals an untypical high spread for one of the modules with EFG cells. As the measured maximum output power proved to be considerably lower than the rated output power there were justified doubts that the electrical performance of the module is stable. Therefore, this module will not be considered further.
- The spread for P_{MAX} (Figure 1) lies within $\pm 2\%$ (excluding the above mentioned EFG test sample). The absence of differences between “standard” and high efficiency cell technologies proves that adequate measurement methods exist for the latter (although they may not be routine).
- The comparison between laboratories shows that Laboratory 6 tends to measure a 1% lower P_{MAX} (Figure 1) which can be explained by lower than average voltage measurement (Figures 3 and 4). Laboratory 5 tends to measure a slightly higher P_{MAX} (Figure 1) which is correlated with I_{SC} measurement (not shown) and therefore possibly explained by calibration of reference device. Laboratory 4 tends to measure a considerably higher V_{OC} for modules with high

efficiency cells (Figure 3) which partially compensates the lower Isc measurements (not shown). This effect might be explained by the characteristics of the electronic load.

- The large majority of I_{SC} data points lies within $\pm 1\%$ spread (Figure 3) indicating that traceable calibration procedures for irradiance measurement are in place. After excluding the data points from Laboratory 4 (apparent outliers) in Figure 3 all remaining data points fall within or on the border of the 1% box.

Figure 1: Discrepancies of maximum output power at STC between the participating test laboratories. The data are referred to the average of the test sample.

Figure 2: Discrepancies of maximum output power at STC plotted for each test sample. The assignment of symbols to laboratories is identical to Figure 1. The unusual high spread for test sample EFG 1 lead to the decision not to consider the module data in the round-robin.

Figure 3: Discrepancies for short-circuit current and open circuit voltage at STC displayed for all measurements. The assignment of symbols to laboratories is identical to Figure 1.

Figure 4: Discrepancies for maximum power current and maximum power voltage at STC displayed for all measurements. The assignment of symbols to laboratories is identical to Figure 1.

5 Conclusions

Generally it was found that it is advantageous that test laboratories apply different test procedures and have different measuring equipment in use. This variety can reveal systematic failures in a single laboratory and avoid them when considering the combined results.

The actual spread for P_{MAX} lies in the range $\pm 2\%$. High or systematic discrepancies for laboratories could be either explained by deficits of the measuring equipment or measurement procedures. The

project target is to achieve comparability for P_{MAX} of $\pm 1\%$ between test laboratories. With regard to that, the initial round-robin test provided a comprehensive data basis and information source that can now be used by the laboratories for their follow-up work. A second round robin with new test samples will be started in 2008 to monitor improvements achieved through the project.

As there is a clear trend to high efficiency solar cells, laboratories need to develop procedures to decide whether PV technologies are critical or non-critical for indoor performance measurement with pulsed solar simulators. A guideline will be developed in the project. Knowledge on advanced measurement techniques for critical c-Si technologies must also be transferred to hardware suppliers to enable them to improve their measuring equipment, in particular for use in PV industry. With that regard, systems suppliers shall be more aware of the industry needs. A checklist containing recommendations and hardware requirements will be important. Also training of personnel in industry shall not be neglected.

PV Industry requires additional information from laboratories describing how modules shall be measured. Just reporting STC data for reference modules is not sufficient. For example, information should be added to the test protocol stating whether the technology is sensitive to transient effects or not and to give recommendations for optimal transfer of calibration. With regard to that a guideline will be elaborated in the project. Also a technical assessment of measuring hardware in production lines by experts from test laboratories may become necessary.

Based on the experiences of the round-robin test a second round-robin will be defined in 2007, which will also include indoor performance measurements at low irradiances and other module temperatures as such information is required for energy rating.

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Valence-Mended Si(100) Wafers for Improved Cell Efficiency

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A valence-mended Si(100) surface is accomplished by depositing a single atomic layer of Group VI atoms on the surface. This surface passivation technique has been demonstrated to reduce contact resistance between Si and a proper metal, and at the same time reduce surface recombination velocity. The simultaneous reduction in contact resistance and surface recombination promises significantly improved efficiency in wafer-Si cells. This paper reviews our research on valence-mended Si(100) surface as pertaining to PV applications and point out ways for cost-effective incorporation of this technique in wafer-Si cells.

INTRODUCTION

Surface recombination has been identified as a major limiting factor to high efficiency in wafer-Si based PV cells [1]. Surface passivation is also listed as one of the limiting factors to high efficiency in film-Si based PV cells [2]. Further complication comes from the requirements for low-resistance ohmic contacts to wafer-Si PV cells, which often contradict the requirements for low surface recombination. In many commercial wafer-Si cells, a film of a dielectric material, such as thermal SiO₂ or PECVD SiN_x, is used to reduce surface recombination. Such an insulating film prohibits ohmic contacts to the passivated surface. In this paper, we propose a new surface passivation technique for single-crystalline Si(100) wafers, i.e. valence-mended Si(100) surface [3]. This technique can simultaneously reduce contact resistance and surface recombination in wafer-Si cells, thus having the potential to significantly improve cell efficiency.

The concept of “valence mending” was proposed by Kaxiras [4], and it intends to eliminate dangling bonds on a semiconductor surface. For Si(100) surface, valence mending is accomplished by depositing a single atomic layer of sulfur (S), selenium (Se) or tellurium (Te) on the surface [5]. This technique has been demonstrated to drastically reduce the contact resistance between Si and a proper metal [6], and at the same time reduce surface recombination velocity to ~60 cm/s on a single-side passivated CZ wafer [7]. Both the contact resistance and surface recombination velocity can be further reduced by optimizing the passivation conditions. In this paper, we will summarize our research on valence-mended Si(100) surface as pertaining to PV applications and point out ways for cost-effective incorporation of this technique in wafer-Si cells.

VALENCE-MENDED SILICON (100) SURFACE

On a nascent Si(100) surface, each surface atom possesses two dangling bonds, as shown in Fig. 1(a). These dangling bonds increase the energy of the surface, making it chemically and electrically more active than bulk Si. Chemically, they adsorb H₂O, CO₂ or O₂, and native oxide is formed as soon as the surface is exposed to air [8]. Adsorption helps the surface to reduce its energy. Electrically, surface states originated from dangling bonds pin the surface Fermi level. At a metal/Si interface, Fermi-level pinning makes the Schottky barrier height more or less independent of the metal work function and primarily controlled by surface states, or more appropriately, interface states [9]. Similarly, interface states are present in high densities at non-native dielectric/Si interfaces. For Si(100) surface, valence-mending atoms include only

Group VI elements, S, Se and Te. As shown in Fig. 1(b), they can bridge between two surface atoms and nicely terminate dangling bonds on Si(100). We have investigated S, Se and Te passivation of Si(100), but the results reported in this paper are from Se passivation.

Fig. 1. Atomic structure of (a) nascent Si(100) surface and (b) valence-mended Si(100) surface. The hatched circles are Se atoms.

Fig. 2. TEM micrographs of the interface between Ni and (a) bare Si(100) annealed at 400°C, (b) bare Si(100) at 500°C, (c) bare Si(100) at 600°C, (d) Se-passivated Si(100) at 400°C, (e) Se-passivated Si(100) at 500°C and (f) Se-passivated Si(100) at 600°C.

Ni/Si interface as shown in Fig. 2. For bare wafer annealed at 400°C, silicidation is observed and a 2-layer silicide stack is formed between Ni and Si (Fig. 2(a)). This confirms an early TEM study of Ni silicidation by Foll et al. [14] and they concluded the 2-layer stack as Ni₂Si and NiSi, respectively. After 500°C anneal, a single layer of Ni silicide is present at the Ni/Si interface for

A critical aspect of valence-mending Si(100) surface is to deposit precisely one atomic layer of Se atoms on the surface. Anything less than a monolayer leads to incomplete passivation. Anything beyond a monolayer leaves unsaturated Se atoms, and thus new dangling bonds, on the otherwise passivated surface. It should be noted that even the most advanced process control has difficulty in achieving the precise monolayer control here. For example, a 99.9% coverage of Si(100) surface with Se will leave $6.78 \times 10^{11} \text{ cm}^{-2}$ dangling bonds on the surface, which is >10 times higher than the interface state density routinely obtained with the SiO₂/Si interface. A thermodynamically self-limited process to deposit precisely one atomic layer of S, Se or Te on Si(100) wafers has been developed and patented [5,10]. The precise control of monolayer deposition is accomplished by controlling the equilibrium between condensation and evaporation of Group VI atoms on Si(100) wafers.

SUPPRESSION OF SURFACE CHEMICAL REACTIVITY

One consequence of terminating dangling bonds on a Si(100) surface is that the chemical reactivity of the surface is suppressed. A dangling bond, which is created when a covalent bond is broken, is chemically unstable. Experimentally, it has been shown that dangling bonds on Si(100) surface act as reaction sites, i.e., they form new bonds with reacting species [11,12]. With dangling bonds terminated by a monolayer of Se, the valence-mended Si(100) surface should be chemically less reactive than the bare Si(100) surface since reaction sites are no longer available.

We have experimentally demonstrated the suppression of chemical reactivity of Si(100) surface with Se passivation by examining Ni silicidation on the surface [13]. A 50-nm Ni film is deposited on two Si(100) wafers, one passivated with a monolayer of Se and the other without Se passivation. Silicidation is performed by heating these samples in N₂ from 400 to 700°C for 60 seconds, and TEM is used to examine the

bare wafer (Fig. 2(b)). However, the behavior of the Se-passivated wafer is quite different from the bare wafer. After anneal at 400°C (Fig. 2(d)), there is no silicidation between Ni and Se-passivated Si and the interface is abrupt. After 500°C anneal, there is still no noticeable reaction between Ni and Se-passivated Si (Fig. 2(e)). Only after 600°C (Fig. 2(f)) does Ni react with Se-passivated Si to form a single layer of Ni silicide. Therefore, Ni silicidation is delayed by over 100°C with Se passivation. This sets the upper limit for processing temperature when this passivation technique is incorporated in wafer-Si cells.

Fig. 3. Low-temperature I-V characteristics of Ti contacts on Se-passivated and bare n-type Si(100) wafers.

Fig. 4. Linear fittings of data from circular transmission-line measurements of Se-passivated and bare Si(100) wafers with a 50-nm Ti.

0.2-eV lowering in barrier height.

Specific contact resistance is measured between Ti and Si(100) wafers, with and without Se passivation, using the circular transmission-line method [16], as shown in Fig. 4. The method to extract specific contact resistance in Fig. 4 is well established [16]. The passivated sample shows a much lower contact resistance than the bare sample, $6.23 \times 10^{-6} \Omega \cdot \text{cm}^2$ vs. $1.82 \times 10^{-4} \Omega \cdot \text{cm}^2$. This is a 29-time reduction in specific contact resistance between Ti and n-type Si(100) by Se passivation. More importantly, this reduction in contact resistance is applicable to lightly-doped Si wafers, as is often the case for many wafer-Si cells. Low Schottky barrier on p-type Si(100) surface has also been demonstrated in our laboratory [17].

REDUCTION OF CONTACT RESISTANCE

Electrically, termination of dangling bonds on Si(100) surface results in minimization of surface states [3], which have been a showstopper in semiconductor technology since the Bardeen era. One consequence of minimized surface states is that the Mott-Schottky theory will be obeyed, i.e., the Schottky barrier height between metal and Si will be close to the difference between metal work function and Si electron affinity. Therefore, low-resistance ohmic contacts can be realized by employing a low work-function metal on n-type Se-passivated Si(100) wafer or a high work-function metal on Se-passivated p-type Si(100) wafer. We have demonstrated potentially-negative Schottky barrier between Ti and Se-passivated n-type Si(100) surface [15], which has lead to a drastically lower contact resistance for n-type Si(100) wafers [6].

The contact resistance between metal and Si is an exponential function of the Schottky barrier height, and a 0.1-eV lowering in barrier height can reduce contact resistance by a factor of ~ 100 . Fig. 3 shows the effect of Se passivation on current-voltage (I-V) relation between Ti and n-type Si(100) surface. The Si(100) wafers are doped to low 10^{15} cm^{-3} . The bare wafer starts to show signs of rectification at 244 K, while the passivated wafer displays ohmic I-V at 141 K, the lowest temperature achievable in our laboratory. A simple-minded fitting of the I-V curves by the thermionic model indicates a barrier height of $<0.3 \text{ eV}$ for the bare sample. In comparison, the passivated sample shows a barrier height $<0.1 \text{ eV}$, i.e. a

REDUCTION OF SURFACE RECOMBINATION VELOCITY

A CZ wafer is passivated with a monolayer of Se on one side, i.e. the polished side. Its surface recombination velocity is measured to be ~ 60 cm/s [7], which is comparable to that of thermal SiO₂ passivated wafers.

FUTURE DIRECTIONS

The valence-mending technique has demonstrated its capability to simultaneously reduce contact resistance and surface recombination for Si(100) wafers. Its thermal stability up to 500°C adds flexibility for its incorporation into wafer-Si cells. However, further research is needed to take full advantage of this technique.

Fig. 5. TEM micrograph of the adsorbate film between Ti and Se-passivated Si(100) wafer.

The reduction in specific contact resistance, 29 times, is much less than what one would expect from a 0.2-eV lowering in Schottky barrier height. This can be explained by an adsorbate film formed between Ti and Si, as revealed by TEM in Fig. 5. The Se-passivated wafer is exposed to air when it is transferred from the passivation chamber to the evaporation chamber. The 1.5-nm amorphous film introduces a tunneling barrier, whose removal will further reduce the contact resistance. Further reduction in surface recombination can be achieved by employing a FZ wafer or a CZ wafer with a gettering step. In addition, 2-side passivation of a wafer is needed to reveal the full effect of valence mending.

Most importantly, this passivation process has to be performed in a low-pressure CVD reactor for high throughput and high quality, in which both sides of a wafer can be passivated and a large number of wafers can be processed in a single batch. The passivation process reported in this paper is molecular beam epitaxy, which is not suitable for high-volume solar cell manufacturing.

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Structures and Properties of Defects in Cast-grown Polycrystalline Silicon

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Abstract

The metal impurities, defects, and these complexes determine the average of minority carrier lifetime of the cast-grown polycrystalline silicon. Therefore, the distributions of iron and nickel, the structures of defects that attract the metal impurities, and the electrical properties of boundaries are studied by synchrotron-based X-ray microprobe analysis, TEM and EBIC observations. There are small-angle grain boundaries, nano-size defects between the micro-twins, and the amorphous-like poor-quality crystal regions in the cast grown silicon crystal. After the gettering process, some iron atoms are trapped at these regions and segregated as iron silicide, while most of irons are removed to the phosphorus diffusion layer. These defects efficiently attract the metal atoms and deteriorate the electrical properties. The distribution of nickel after the gettering is not the same as that of iron. This indicates that the trap abilities of the defects change depending on a kind of metal.

1. Introduction

Crystalline silicon (Si) technology has dominated the production of solar cells, which contributed 95% of the world's PV production. Because of the lower cost and relatively better conversion efficiencies, the poly- crystalline Si solar cells are dominant in the crystalline Si solar cell market. Therefore, to improve the conversion efficiency of the polycrystalline Si solar cells and to reduce the cost of them are most important for the further growth of solar cell market.

So far, since the grain boundaries act as recombination centers and determine the solar cell performance, many works have been done for increasing the grain size of polycrystalline Si to improve the conversion efficiency [1-5]. Now, the larger grain size exceeding 1 cm was obtained by cast-grown method, which is large enough as compared with the minority carrier diffusion length (0.25 mm) in B-doped polycrystalline Si. However the expected high conversion efficiency has not been realized. In the region where the lifetime is relatively short, there are many defects, which appear as etch-pits by the Secco etching. The relationship between the etch-pit density and the minority carrier lifetime suggested that these defects acted as a recombination center and that they mainly determined the lifetime. In the present cast grown Si, there are many residual carbon atoms, which are mainly contaminated during the crystal growth. A larger amount of carbon atoms exist in the region where the lifetime is shorter as compared with in the region with longer lifetime [6]. These carbon atoms might be one of the reasons to create the defects. X-ray microprobe fluorescence measurement results suggested that irons were corrected at these defects, and that the defect and heavy metal complex might deteriorate the minority carrier lifetime [7]. However, the structures of these defects, the effect of a kind of metal on the trap ability, and these electrical properties are not clear yet. In this paper, we study the defect structures, the difference in the distributions of iron and nickel, and the electrical properties of the regions with grain boundaries and defects.

2. Experiment

The polycrystalline Si used in this study was grown by the cast method. Before measurements, the saw-induced damaged layer was etched off by the HNO_3/HF solution. For lifetime measurements, the Si surface was passivated by iodine (I). The lifetime mapping was obtained by laser microwave photoconductance decay (PCD) measurement. The step size used for generating the lifetime mapping was 1mm and 523 nm He-Ne laser was used as a carrier injection source. The electrical properties were evaluated by electron beam induced current (EBIC). The wafer surface was Secco etched for 10 minutes and it was studied by the optical microscopy and scanning electron microscope (SEM). The crystalline orientations were analyzed by electron backscatter diffraction pattern (EBSP). The defects structures were observed by the cross-sectional transmission electron microscope (TEM) observations. Iron and nickel distributions and these electric structures were studied by X-ray microprobe fluorescence (XRF) measurement and X-ray absorption in near edge structure (XANES) at BL37XU line of Spring-8. The used exciting energy was 10 keV and the beam size was focused to 5 μm .

3. Results and Discussion

Fig. 1. XRF spectra of Iron. (a): before gettering, (b): after gettering.

Fig. 2. XANES spectra of iron.

The iron distributions before and after gettering processes are shown in Fig. 1. They were obtained by XRF measurements. The distribution of residual iron atoms before the gettering is not uniform. Some iron atoms exist in a grain and at some particular points. The spectra of XANES before gettering process is shown in Fig. 2. The spectrum is almost the same as that of iron oxide, indicating that the iron existed as Fe_2O_3 . After the gettering process, many residual iron atoms disappeared, which moved away to the phosphorous-doped region. On the contrary, iron concentrations increases at the several points along the grain boundaries. The energy at the highest absorption became higher as shown in Fig. 2, which corresponds to the value of the iron silicide and indicates the change in the chemical state. The absorption around 7.13keV is relatively lower than that for the iron silicide. This suggests that these iron atoms exist as the iron silicide partially mixed with the iron oxide.

The EBIC and optical images after the gettering process are shown in Fig. 3. Some dark lines along the grain boundaries are observed in EBIC image. EBSD measurements suggested that the B1-B2, B2-B3, and B3-B4 grain boundaries were $\Sigma 3$, and that A1-A2

was a small angle grain boundary. Large amount of irons existed at the small angle grain boundary and the electrical property of the boundary was poor. The small angle boundaries might introduce edge and screw dislocations, which act as a sink of iron atoms.

Fig. 3. (a): EBIC image. (b): optical image

boundary is shown in Fig. 6. There are many micro-twins and some defects exist in the grains between twin boundaries. These small defects deteriorated the electrical property. Although the precise mechanism that gives rise to these micro-twins is not known yet, the possible influence of impurities, such as carbon and nitrogen, and the induced stress by them might be considered. TEM image and the selected area diffraction pattern at the position where the electrical property was poor in EBIC observation are shown in Fig. 7. Hallow like pattern suggests the amorphous-like poor quality crystal was grown in this region. We consider that the crystallization delayed at this region because of the large amount of impurities in the melt, and that the induced large stress and the segregated precipitates deteriorated the crystal quality.

Fig. 4. Cross-sectional TEM image at B1-B2 boundary.

Fig. 5. Cross-sectional TEM image at A1-A2 boundary.

Fig. 6. Cross-sectional TEM image at B1-B2 boundary and structure of micro-twin.

The cross sectional TEM image at the B1-B2 boundary is shown in Fig4. The diffractions indicate that the boundary has twin structure, which corresponds to the EBSD results. Since $\Sigma 3$ grain boundary is high-symmetric, the ability as functions of impurities sink and recombination centers at this boundary is considered low. However, there are some defects along the boundary, where some iron atoms would be trapped and the electrical property was relatively poor. TEM image at A1-A2 boundary is shown in Fig. 5. There is a small size iron precipitate. By the high temperature annealing, many iron atoms were trapped at this grain boundary and they were precipitated as iron silicide. TEM image at B2-B3

The trap ability at these boundaries and defects changed depending on a kind of metal impurities. Before the gettering process, both iron and nickel atoms existed near the same boundary. However, after the gettering process, the nickel atoms exist at the boundary as shown in Fig. 8, while the iron atoms are removed.

Fig. 7. Cross-sectional TEM image at poor electrical property region.

Fig. 8. XRF images of metal distributions after gettering process. (a): nickel. (b): iron.

4. Summary

The distribution of metal impurities, structures of defects attracted the metal impurities, and the electrical properties of grain boundaries were studied by synchrotron-based X-ray microprobe analysis, TEM, and EBIC observations. There were small-angle grain boundaries, nano-size defects between micro-twins, and the amorphous-like poor-quality crystal regions. After the gettering process, some iron atoms were trapped at these regions and segregated as iron silicide. It was also shown that the trap ability at the boundaries and defects changed depending on a kind of metal impurities.

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Characterization of Metal precipitate located on the grain boundary in as-grown cast mc-Si.

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Abstract

In order to analyze the influence of impurities to Silicon Photovoltaics, we observed the as-grown cast Multi Crystalline Silicon (mc-Si) by SEM/AES. A metal precipitate was found in the grain boundary. The main component was Ni Silicide, and complex of Cu, C and O was found nearby Ni Silicide. Any Fe was not found in and around the precipitate.

Introduction

Polycrystalline Silicon has been manufactured by the “Bell Jar” method and has been used as the feedstock of Silicon Semiconductor. It is well known the Silicon made by the method contains impurities quite low.

In these days, there is great demand for the polycrystalline Silicon as the feedstock of Silicon Photovoltaic. Polycrystalline Silicon made by the Bell Jar method is used for both Single and Multi Crystalline Silicon. One of the large problems of Silicon Photovoltaic is its cost, and there is large requirement to develop more economical process of manufacturing Solar Grade Silicon (SOG Silicon). Recently several new methods to manufacture the SOG Silicon have been developed. Generally, SOG Silicon made by new methods contains much more impurities than Semiconductor Grade Silicon (SEG Silicon).

There would be large possibility that the impurities induce bulk recombination, current leakage and shunt, and then the conversion

efficiency would be worse^{1), 2), 3)}. Several reports about impurities in mc-Si, which are made of SEG Silicon, have been published and the influence to the efficiency has become clear. But it is less understood that the impurities in the SOG Silicon made influence on the mc-Si and the efficiency. To make these things clear, we have characterized mc-Si. In this time we will show our previous works.

Experimental

Samples cut from cast mc-Si were polished with 0.5 μ m diamond slurry to mirror. To make the impurity-conformation of as-grown mc-Si clear, any farther treatment, like chemical etching or thermal treatment, are not done to the samples. The surfaces of each polished sample are observed by SEM after surface Ar⁺ sputtering. The metal precipitate located at the grain boundary was identified by Auger Electron Spectroscopy (AES). The SEM/AES was PHI700 (ULVAC-PHI, INC).

Result & Discussion

By the SEM observation, large foreign substance was found in the grain boundary of as-grown cast mc-Si (Fig.1). Its length was about $2.5\mu\text{m}$ and width was about $0.9\mu\text{m}$. There were several scratches, which would be made during polishing, through the substance. It means the substance was not particle on the surface but the precipitate in the grain.

Fig.1 These four SEM images are taken in the same place of as-grown cast mc-Si. The difference of each image is the magnification limit. And the viewing condition of the image Fig1-(d) was different to the other because the precipitate had high brightness.

AES was used to identify the precipitate. The AES point analyses revealed the elements of precipitate (Fig.2). In the Point 1, on the right side of precipitate, several elements (Si, Cu, C

and O) were detected. In the Point 2, in the middle of precipitate, only Si and Ni were detected. On the other hand there was nothing but Si in the crystal grain (Point3).

Fig.2-(a) SEM image

Fig.2-(b) AES Spectra

Fig.2 Fig.2-(a) indicated the analysis points of AES. The AES spectra of each point were showed in Fig.2-(b).

In this way, several impurities were distributed in the precipitate. The AES mapping analysis revealed the distributions of each atom (Fig.3). Ni mapping indicated that large part of precipitate contained Ni (Fig3-(a)). The

comparison of Ni mapping and Cu mapping made it found that Ni and Cu didn't exist in the same place. Most of Cu existed in the upper side of the precipitate, and O and C were co-existed in the same place. It was very interesting that Fe was not found in and around this precipitate (Fig3-(c)).

Fig.3 AES mapping analysis of each atom, Ni, Cu, O, C, Si and Fe.

As mentioned above, Nickel was the main component of the precipitate. To make the chemical state of Ni precipitate clear, more detail analyses of AES spectrum had been done (Fig.4). In the region from 800eV to 880eV originated Ni LMM, the spectrum of Ni precipitate was much more similar to Ni Silicide than to Metal Ni (Fig.4-(a)). In the same way, in the region from 1540eV to 1640 originated Si KLL, the spectrum of Ni precipitate was much more similar to Ni Silicide than to Silicon wafer (Fig.4-(b)). In this way the precipitate would be Ni Silicide.

T.Buonassisi et al. found metal nanoprecipitates (diameter < 200nm) and metal particles (several microns) in mc-Si by μ -XRF⁴⁾. The metal nanoprecipitates existed along the grain boundaries and typically consisted of metal Silicides (FeSi_2 , NiSi_2 , Cu_3Si , etc.). Compared to the nanoprecipitates, Ni Silicide found in this study was too large. There is high possibility that phosphorus diffusion, passivation and gettering couldn't make such a large precipitate fully inactive and the efficiency would be decreased.

There are several possibilities why such a large metal precipitate was contained in mc-Si, feedstock, crucible, carbon component, the atmosphere and the condition of crystal growth.

So we have investigated the source of metal impurities and will investigate the influence to the conversion efficiency.

(a) Spectra originated Ni LMM

(b) Spectra originated Si KLL

Fig.4 The detail analyses of AES spectra. (a) Spectra originated Ni LMM, (b) Spectra originated Si KLL.

Conclusion

The precipitate, its length $2.5\mu\text{m}$, was found in the grain boundary in as-grown cast mc-Si. AES mapping analysis revealed the main impurity of it was Ni. The AES spectra of both Ni LMM

and Si KLL matched to Ni Silicide, and it concluded the precipitate would be Ni Silicide. In addition to that the complex of Cu, C and O was found nearby Ni Silicide. But Fe was not detected in and around the precipitate.

It is not certain the source of impurity and the influence to the conversion efficiency. Further investigation will make these things clear.

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Possible reduction of recombination lifetime due to compensated dopants

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Abstract

Dopant compensation is a convenient way to use all available solar grade silicon, and still arrive at the required wafer resistivity by mixing differently doped pieces of silicon. We review the possibility that compensated dopants can be a significant source of recombination in silicon solar cells, based on a variety of results in literature. The capture cross section of the ionised dopants for minority carriers is large, and not limiting recombination. Rather, the capture cross section of the neutral dopants for majority carriers is the rate-limiting parameter. There is very large variation in literature data of this neutral dopant capture cross section, between about 10^{-15} and 10^{-22} cm². If the higher values are correct this would mean that compensated dopants can be a very significant recombination channel in solar cells. A value below, but not much below, 10^{-17} cm² is most likely based on literature results, which would mean the effect would be noticeable in strongly compensated material, but not very important.

Introduction

Compensation occurs in wafers from solar grade silicon due to the mixing of differently doped sources of silicon. In particular, to reduce costs, new solar grade silicon production techniques [1] will generally be less effective in removing dopants than the conventional Siemens route to high-purity polysilicon for the semiconductor industry. Therefore, there may be a mix of p- and n-type dopants present in wafers produced from such silicon. Furthermore, generally as much of the available silicon is used for PV production as is possible. This means that n-type doped waste silicon is recycled and mixed with p-type silicon or compensated by adding p-type dopants, in order to produce ingots of roughly standard resistivity.

Compensation will increase the number of scattering centers for charge carriers and thus may reduce the mobility and diffusion length. Dopants could possibly also form complexes or defects with other impurities or crystal defects, and thus change the charge transport and recombination in the silicon wafer. The topic discussed in this paper is whether compensated dopants as such (without considering any interaction with other defects or impurities) can have a significant impact as recombination centers.

Little attention seems to have been paid in published PV literature to effects of compensation. The seminal impurity studies by Westinghouse [2] have investigated the topic in monocrystalline Cz ingots. Their results show a slight suppression of cell efficiency for a phosphorous density larger than 2.5×10^{17} cm⁻³ in p-type ingots of resistivity 4 Ωcm. However, as the baseline cell efficiency and effective diffusion length

in the Westinghouse cell process was quite low (for example, no BSF was used), it is possible that currently a more significant effect could be expected.

Acciarri et al. have studied intentionally compensated Eurosolare ingots [3]. They focussed on effects on mobility, but also solar cells were made. Probably due to variability of mc-Si properties (especially variation of crystal defect density), in studying two ingots of the same resistivity the compensated one showed the higher mobility and a cell efficiency 1.3% higher than the uncompensated one. Modelling showed that effects of compensation on mobility should actually be negligible at room temperature.

To our knowledge, apart from the above references, there have been few, if any, explicit results of the effects of compensation reported in open PV literature. In this paper, we will therefore also use literature results outside the PV field to assess the possibility that compensated dopants cause significant recombination. It will turn out that this is a possibility based on some results, but also that there is a lot of variation in published values of the relevant defect parameter (the majority capture cross section). Therefore, experiments to determine recombination lifetime in controlled bulk samples would be useful as a sensitive test for this phenomenon. Such experiments are in preparation.

Compensated dopants as recombination centers

A compensated dopant in silicon is a shallow impurity near the minority-carrier band-edge. Generally, shallow impurities are expected to be not very effective as recombination centers, because the occupation probabilities of the two charge states of the center are very asymmetric. For example, in the case of phosphorous in p-type silicon (alternating between P^+ and P^0) the occupation of the neutral state is very low, hole capture is therefore very unlikely, and the recombination rate might be expected to be low. Rather, shallow levels are often expected to act as traps (capturing and releasing minority carriers).

However, for the typical resistivity of PV wafers, and a significant compensation fraction, the density of the shallow defect levels can be much higher than typical metal impurity levels. This high defect density could potentially offset the low level occupation, and result in a significant recombination rate.

In this paper we will apply the Shockley-Read-Hall (SRH) model to evaluate quantitatively the recombination rate in compensated silicon. One could worry that the SRH model would not be valid for this purpose, since in its commonly used form it is only applicable when the density of recombination centers is 'small'. This arises from the assumption that the non-equilibrium carrier densities Δn and Δp must remain almost equal, which does not hold if the recombination centers 'trap' a significant fraction of carriers. Macdonald and Cuevas [4] investigated the range of validity of the SRH model. They found that the SRH model is valid if the recombination center density N_t is at least one order of magnitude lower than a critical level N_{crit} . For the very shallow levels near the band edges that are considered in this paper, N_{crit} is very high, above 10^{18} . So, perhaps surprisingly, it is therefore valid to use the SRH model from this perspective. This reflects the fact that, although the shallow compensated dopants will indeed trap carriers, they will re-emit them quickly enough to avoid trapping problems.

Applying the usual SRH equation then,

$$\tau_{SRH} = \frac{\tau_{no}(p_o + p_1 + \Delta n) + \tau_{po}(n_o + n_1 + \Delta n)}{n_o + p_o + \Delta n}$$

$$n_1 = N_c e^{(E_t - E_c)/kT}; \quad p_1 = N_v e^{(E_t - E_g - E_c)/kT};$$

$$\tau_{po} = \frac{1}{N_t v_{th} \sigma_p}; \quad \tau_{no} = \frac{1}{N_t v_{th} \sigma_n}$$

In the case of shallow levels ($E_c - E_t \approx 0.045$ eV), for net p-type doping, $n_1 \approx 5 \times 10^{18} \text{ cm}^{-3}$ and p_1 is negligible. Therefore, in p-type material (n-type is similar):

$$\tau_{SRH} = \tau_{no} + \tau_{po} \frac{n_1}{p_o + \Delta n}$$

Hence, the majority carrier capture time constant (τ_{po} in p-type) limits the recombination lifetime, being multiplied by e.g. a factor 500 if the net doping density is 10^{16} cm^{-3} . The calculations in Fig. 1 illustrate that SRH recombination at compensated dopants could be of relevance in standard mc-Si solar cells, depending on the neutral dopant capture cross section (σ_p in p-type).

Incidentally, this dominance of majority capture time constant differs from the situation for deep levels where the minority capture time constant is usually limiting [5]. Thus, the fact that the minority carrier capture cross section will be very high (due to Coulombic attraction) is hardly relevant.

Figure 1. Bulk recombination lifetimes calculated for various capture cross sections of neutral donors. Left: $0.5 \text{ } \Omega\text{cm}$ resistivity, right: $5 \text{ } \Omega\text{cm}$ resistivity. Injection level 10^{14} cm^{-3} , p-type silicon, donor level $E_c - E_t = 0.045$ eV. In the calculation of the compensation fraction, the carrier mobilities are assumed to be unchanged by the compensation. In reality the lines would probably not be straight due to dopant-dopant-interaction.

Published results about capture cross sections

Most information in literature about capture rates or capture cross sections of dopant impurities in silicon is from photoluminescence (PL) experiments, almost exclusively at low temperature. Some data is available from investigations of bipolar transistors.

Concerning the minority carrier capture (i.e., capture by ionised dopants), it is generally accepted that the capture cross section is very large [6]. In ref [7] the capture rate of electrons by P^+ at $T=3K$ corresponds to a cross section of $6 \times 10^{-11} \text{ cm}^2$.

Concerning the more important majority carrier capture, there is much more spread in results. The capture rate of neutral In for electrons corresponds to a cross section of $2 \times 10^{-22} \text{ cm}^2$ at $T=80K$ according to [8]. In [9] the cross section is given as function of T , and extrapolation to room temperature results in about 10^{-21} to 10^{-22} cm^2 , too small to be of importance. Other experiments [10] yielded values of 10^{-16} to 10^{-18} cm^2 , the high side of this range would be of importance in PV materials. In [11] from fits of the beta of IC transistors, the capture cross section of neutral acceptors as well as donors is even found to be as high as $1.3 \times 10^{-15} \text{ cm}^2$. In strongly compensated ($N_i=10^{16} \text{ cm}^{-3}$) 1 Ωcm material this latter result would yield a recombination lifetime of 3 μs !

Discussion

The variation in literature for the capture cross section of neutral dopants is too large to give a somewhat reliable prediction of the effect of compensation on recombination lifetime. According to the previous section, literature values would result in lifetimes between a few μs and infinity. Nevertheless, some further estimates are possible based on other results as described below.

A special situation where compensation could be important is the emitter of solar cells. For the highest value of the capture cross section reported ($1.3 \times 10^{-15} \text{ cm}^2$) the recombination lifetime in the emitter would be orders of magnitude lower than due to Auger recombination. Since generally no large discrepancies seem to be observed between experimental emitter recombination currents and modelling based on Auger recombination[12], the upper bound on the capture cross section should be of order 10^{-17} cm^2 . In turn, this would give a lower bound on the recombination lifetime in strongly compensated ($N_i=10^{16} \text{ cm}^{-3}$) 1 Ωcm material of order 300 μs .

Looking in detail at the Westinghouse results [2] for compensation, the largest observed reduction of cell parameters is just a few percent. In two cases the net doping of test and reference ingots are closely similar: one ingot (W092) with $\rho \approx 4 \Omega\text{cm}$ and $N_D = 2.8 \times 10^{16} \text{ cm}^{-3}$ showed no reduction of cell I_{sc} or V_{oc} , or carrier lifetime; the other (W116) with $\rho \approx 0.47 \Omega\text{cm}$ and $N_D = 1.0 \times 10^{17} \text{ cm}^{-3}$ showed 2% reduction in I_{sc} , but no significant reduction in carrier lifetime measured by open circuit voltage decay (1.4 μs in test and reference ingot). According to the model by Westinghouse, the recombination due to compensation in ingot W116 would be approx. 20 μs , which corresponds to $\sigma_p \approx 4 \times 10^{-18} \text{ cm}^2$. Obviously there is large uncertainty in this number. Moreover, the I_{sc} -reduction could probably be also due to reduced mobility.

Conclusions

As new sources of silicon feedstock are used in silicon PV, and at the same time efforts towards high cell efficiency are increasing, it is becoming more and more important to understand whether recombination via compensated dopants can be a significant issue in solar cells. From Shockley-Read-Hall theory it is likely that capture of majority carriers by neutral dopants is the rate-limiting step. Reported values for the capture cross section vary enormously. Results obtained on bipolar transistors suggest that compensated dopants would be a very significant recombination channel in solar cells, whereas some photoluminescence results suggest an insignificantly small carrier capture cross section. From other results a value below, but not much below, 10^{-17} cm^2 is most likely, which would mean the effect would be noticeable in strongly compensated material, but not very important. Given the large uncertainties further investigation will be useful.

Acknowledgments

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An Optical Technique for Measuring Surface Recombination Velocity

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ABSTRACT

The surface recombination velocity is a critical and important parameter in silicon device applications. In this work, we have developed and applied a contactless optical-microwave technique to provide quick, contactless measurement of the surface recombination velocity. The basic mechanism is to probe the excess carrier lifetime in the surface and bulk regions of a semiconductor wafer. By comparison of the surface and quasi-equilibrium bulk lifetime, one can extract the surface component of recombination. Here, we will demonstrate a theoretical model and provide experimental data that verify the calculated effects.

INTRODUCTION

The influence of surface recombination on device performance is well known. The evaluation of silicon-wafer quality prior to device processing is even more critical. One issue in such evaluation is that the surface recombination usually masks the bulk recombination lifetime. In this case, a temporary surface recombination process, such as iodine/methanol immersion, is frequently required. The latter process may be quite time consuming, and requires surface etching and other chemical-hood processing. Here, we will describe an optical and contactless technique that can provide a rapid assessment of the surface recombination component.

BACKGROUND

A number of contactless optical techniques have been described in the literature for measuring the surface recombination velocity and bulk lifetime [i,ii,iii]. Here, we will describe a contactless, noninvasive technique that is quick and quite easy to apply. Our prior work [iv] has used the approximation of an infinitely thick wafer to provide the theoretical analysis for our experiments. This simple analysis produces a value for the initial or surface lifetime that is a simple function of absorption coefficient, surface recombination velocity, and bulk lifetime. In this case, the instantaneous lifetime at $t=0$ is [v]:

$$\tau_1 = \frac{\tau_B}{1 + \alpha S_1 \tau_B}. \quad (1)$$

When the surface component is much shorter than the bulk lifetime, one can write:

$$\tau_1 = \frac{1}{\alpha S}. \quad (2)$$

After some period of time, the excess carriers diffuse until the excess carriers are distributed in the volume symmetrically in the wafer. In this case, the lifetime is given by [vi]:

$$\frac{1}{\tau} = \frac{1}{\tau_B} + \left(\frac{2d}{S} + \frac{d^2}{\pi^2 D} \right)^{-1}. \quad (3)$$

In this work, we used a continuously tunable pulsed light source to provide verification of the technique. In practice, a two-wavelength laser might be adequate. A YAG laser, operating in the fundamental and doubled mode, might well suffice to provide quality data for silicon analysis. The techniques here are resonant-coupled photoconductive decay (RCPCD) and microwave reflection (MWR) to measure the transient photoconductive decay. For strongly absorbed light, the initial ($t=0$) decay time is a strong function of the absorption coefficient, α , and the surface recombination velocity. The effective bulk lifetime is a well-known function of the two surfaces (interfaces) and the true bulk lifetime. The effective bulk lifetime is measured by using very weakly absorbed light, or by measuring the asymptotic decay rate of strongly absorbed light. The latter occurs after diffusion has produced a quasi-equilibrium condition in the wafer. For asymmetric surfaces (such as a wafer polished on one surface only), the measurement with strongly absorbed light is made at both wafer surfaces.

THEORETICAL ANALYSIS

To get a more accurate analysis of a real wafer-sample system, we used a modal analysis of the photoconductive transient that has been described elsewhere [vii]. This analysis allows for the diffusion of excess carriers away from the surface of incidence and rapid interaction with the back surface. The redistribution of excess carriers from an initial Beers' law profile has been calculated [7]. One can write the excess carrier density as the Fourier modes:

$$\rho(t) = \exp(-t/\tau) \sum_{n=1}^{\infty} \exp(-\beta_n t) \left(A_n \cos \alpha_n x + \frac{S}{\alpha_n D} \sin \alpha_n x \right). \quad (4)$$

The coefficients α_n are determined by calculating the diffusion currents at the two surfaces. The solutions are found from the nonlinear equation, where:

$$\tan(\alpha_n d) = \frac{2d^2 \alpha_n S / D}{(\alpha_n d)^2 - S^2 d^2 / D^2}. \quad (5)$$

When the surface recombination S is zero, the solutions are:

$$\alpha_n = 0, \pi/d, 2\pi/d, 3\pi/d, \dots$$

and

$$\beta_n = 0, D\pi^2/d^2, 4D\pi^2/d^2, 9D\pi^2/d^2, \dots \quad (6)$$

We see from these values that the time constant of the various modes increases rapidly with mode number. In other words, the decay constant becomes increasing faster for the higher-order modes.

The coefficients A_n are Fourier components of the initial Beers' law carrier distribution and d is the sample thickness. These solutions are a fairly complex function of α_n , the absorption coefficient α of the incident light pulse, the minority-carrier diffusion coefficient D , and the surface recombination velocity S . The final solution gives the excess carrier concentration as a function of spatial dimension and time:

$$\rho(x, t) = \exp(-t/\tau) \sum_{n=1}^{\infty} A_n \exp(-\beta_n t) \left(\cos \alpha_n x + \frac{S}{\alpha_n D} \sin \alpha_n x \right) \quad (7)$$

The photoconductive decay dynamics can be simulated by integrating Eq. 6 over the width, d , of the sample:

$$\rho(t) = \int_0^d \rho(x,t) dx. \quad (8)$$

SIMULATION RESULTS

We simulated a case where the bulk lifetime is 40 μ s and S is 10,000 cm/s. The excess carrier profiles are shown at various times in Fig. 1 with an assumed electron mobility of 1000 cm²/Vs. At 0.1 μ s, the carrier profile has diffused from the initial Beers law distribution provided by excitation at 700 nm. Also, appreciable recombination has occurred at the front surface as shown by the depression of the carrier density there. The steady-state effective lifetime is reduced to about 5 μ s because of the very large surface recombination velocity. The initial Beers law charge distribution at the front surface produces an initial, very high recombination rate. The latter decreases as the carrier distribution becomes symmetrical about the midpoint of the wafer.

Figure 2 shows the integrated excess charge distribution as a function of time. The material parameters are the same as those used for Fig. 1. The integrated excess carrier density/mobility product is the quantity measured by transient photoconductive decay instruments. When the wavelength is scanned from the visible to infrared wavelengths, the transient photoconductivity displays the behavior shown in Fig. 2 when the surface is unpassivated.

Figure 3 shows the simulated decay with the surface recombination velocity reduced to 1.0 cm/s. The decay curves do not show the steep initial slope and the curves overlap to a great degree. These behaviors have been observed in the laboratory for wafers immersed in iodine-methanol solution.

Figure 4 shows simulated decays with the excitation wavelength at 500 nm and the surface recombination velocity increasing in decades from $S=1$ to $S=10000$ cm/s. We see that the highest sensitivity at this wavelength occurs between $S=1$ and $S=100$ cm/s.

MEASUREMENT TECHNIQUE

The RCPCD technique has been described extensively in the literature and will not be discussed here. Microwave reflection (MWR) was first described by Kuntz and Beck and is now commercially available. No MWR data are shown here, but the technique is capable of measuring shorter lifetimes than RCPCD. The pulsed light is provided by an optical parametric oscillator (OPO) that is driven by a tripled YAG laser.

EXPERIMENTAL RESULTS

Figure 5 shows the decay of an unpassivated wafer with a resistivity of about 100 ohm-cm. The photoconductive decay was measured at wavelength varying from 500 to 1100 nm. The initial decay time increased rapidly for wavelengths greater than about 800 nm. These results are in quantitative agreement with the simulation results of Fig. 2. A data fit is somewhat laborious at this time because of the infinite-series character of the theory. Figure 6 shows the same sample after an HF etch and during immersion in iodine-methanol solution. The excitation wavelength was 900 nm and the injection was varied

over two orders of magnitude. The decay curves are nearly “pure” exponentials and are independent of the excitation wavelengths. These data are in qualitative agreement with the simulations shown in Fig. 3.

CONCLUSIONS

Using transient photoconductive decay measurements, when combined with a variable-wavelength light source, one may observe the influence of surface recombination in real time. Further research will focus on methods to obtain quantitative data from measurements of this type.

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FIGURE CAPTIONS

Fig. 1. The excess carrier profile calculated by the mode method described in the text. The material parameters used in the calculation are indicated in the figure legend.

Fig. 2. The simulated photoconductive decay for the material parameters of Fig. 1. The excitation wavelength was varied from 500 to 1000 nm, as indicated in the figure. The surface recombination velocity was taken as 10,000 cm/s.

Fig. 3. The simulated photoconductive decay with the material parameters of Fig. 1, but with the surface recombination velocity reduced to 1 cm/s.

Fig. 4. The simulated photoconductive decay with the excitation wavelength at 500 nm and S varying in decades from $S=1$ to $S=10,000$ cm/s. Other parameters are shown.

Fig. 5. The photoconductive decay of an unpassivated, 100 ohm-cm CZ wafer as measured by the RCPCD technique. The wavelength was varied from 500 nm to 1100 nm for these measurements.

Fig. 6. The photoconductive decay of the wafer of Fig. 4, but with the wafer immersed in iodine-methanol solution. The decay time was independent of excitation wavelength, but the data in the figure were measured at 905 nm. The injection level was varied by a factor of 100 using neutral-density filter.

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Figure 1

Figure 2

Figure 3

Figure 4

Figure 5

Figure 6

Progress in the Determination of the Stress optics coefficient in Thin Polycrystalline silicon wafers

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Introduction

This paper addresses the topic of the anisotropy of the stress optic coefficients in polycrystalline silicon. The stress optic coefficients relate to the transmission of near infrared light which is used in the measurement of in-plane residual stress. Our work has focused on development of an optical (non-contact) polariscopy technique^{1, 2} to obtain in-plane residual stresses. The unique issues pertaining to these measurements are that: thin wafers are especially troublesome in causing refraction and, polycrystalline wafers with grains ranging from several millimeters to several centimeters require knowledge of the effect of the orientation of the crystal structure on the IR light transmission. We use the phase stepping and fringe multiplier techniques to extract residual stresses from thin silicon wafers and the details of these techniques have already been published.³ Measurements of polycrystalline wafers also require knowledge of the refraction of the IR light at various crystallographic orientations and that is the subject of this paper.

Some specific details of the IR polariscopy techniques

Our work has dealt with near IR transmission through thin silicon wafers and the capture of images by the rotation of a quarter wave plate and a polarizer. One special detail of this measurement technique involves the use of four-point bending of silicon beams to calibrate the residual stress. The beams are composed of large crystals so the transmission of the IR light will depend on the crystallographic orientation of the grains. Figure 1 shows a schematic diagram of the polariscope system and figure 2 shows a typical image obtained from a polycrystalline beam.

Figure 1: System Configuration of the Polariscope.

Figure 2: Typical image of the transmitted IR light

The stress optic law can be used to obtain the shear stresses in the beam if the stress optic coefficient is known. The stress optic law is shown in equation 1.

$$\sigma_1 - \sigma_2 = \frac{\lambda}{2 \pi t C(\theta, \varphi)} \delta \quad (1)$$

Where C is the stress-optic coefficient which is a function of θ (the principle stress orientation and φ (the crystal grain orientation), t is the thickness of the sample, λ is the wavelength of the light source, and σ_1 , σ_2 are the two principal stresses. δ is the phase retardation which can be measured by the six step phasing method.⁴

Each grain in the image of figure 2 is oriented differently relative to the incoming beams so determining the shear stress $\sigma_1 - \sigma_2$ depends on knowledge of the stress optic coefficient as it varies with orientation.

Crystallography determination

Back Laue x-ray diffraction, done at Oak Ridge National Laboratories, was performed on 16 beams (intended for four point bending) and 10 wafers. Grains larger than 5mm in diameter were selected for the x-ray study. About 10-15 grains' orientations were found for each beam and about 15-35 were found for each wafer. The orientations were categorized into 22 groupings with miller indices below 5. Orientations with miller indices of 5 or greater (except for [500]) would not be more than 3 degrees from any one of the orientations with miller indices 4 or less.

A graph summarizing the frequency of the grain orientations is shown in Figure 3. As can be seen, the principle orientations are (100), (011), (111), (211) and (321). Typical orientation results for one beam can be found in Table 1 and Figure 4 which shows a photo image of that beam. Table 1 lists the orientations (corresponding to the θ value in equation 3) and the rotations (which is the pole angle corresponding to the φ value in equation3).

Figure 3: Orientation Frequency (Number) versus orientation (hkl).

Table 1. Crystalline cauterization of the beam used for 4-point bending

Grain (identification shows in Fig. 4)	3	6	8	9	10	14	16	17	24
Orientations(ϕ)	344	211	100	211	321	432	321	211	321
Rotations(θ)	-23	-69	60	-71	-100	-42	60	31	131

Figure 4: Photograph of the beam

Calibration of the Anisotropy and the Stress-optical Coefficients

Four-point bending, shown in Figure 5, was used to introduce known stresses so as to calibrate the anisotropic stress optic coefficients. The residual stresses in the wafers were assumed to be negligible compared to the applied stresses.

Figure 5. Four-point bending experiment setup

Figure 6 shows a typical result of the retardation δ of one of the beams. The physical size of the measured area is 250×50 pixels, or 50×10 mm. It can be seen that the retardation is uniform along the longitudinal direction and the color of the image indicates that it is symmetric around the neutral axis along the transverse direction. The non-uniformity in the longitudinal direction provides evidence of anisotropy in the stress optic coefficient for the various crystal grains.

Figure 6. The calibration result of four-point bending of a silicon beam

The stress optic coefficient is related to the slope of the retardation, $d\delta/dy$, which can be determined with high accuracy using a linear least-square fit. Figure 7 shows a typical least-square fit of the retardation. The correlation coefficient of the linear fit is 0.99. The principal stresses for pure bending are,

$$\sigma_1 = \frac{M}{I} y, \quad \sigma_2 = 0 \quad (2)$$

Where $I = h^3 t / 12$ is the moment of inertia of the cross section, M is the applied moment, and y is the vertical location from the center. By substituting Equation 2 into Equation 1, the stress-optic coefficient can be obtained in terms of the slope of the retardation,

$$C = \frac{d\delta}{dy} \bigg/ \left(\frac{2\pi t}{\lambda} \frac{M}{I} \right) \quad (3)$$

Figure 7. Least-squares fit of retardation along transverse direction

The average slope is used to determine the stress-optic coefficient, C , using Equation 3. Table 2 shows some coefficients of typical grains with certain pole angles. Table 2 shows that the minimum of the stress-optic coefficient is $1.75\text{E-}11$ and maximum is $2.75\text{E-}11$.

Table 2. stress optics coefficient of some grains with certain pole angle

Orientations (ϕ)	100	111	111	111	210	211	321	322	421
Rotations (θ)	20	53	-5	65	-8	31	-100	106	73
Stress optics coefficient($10^{-11} \times \text{Pa}^{-1}$)	2.40	2.54	2.53	2.55	2.08	2.75	1.87	2.35	1.75

Conclusions

- The stress optic coefficients vary with orientations and pole angles from 1.75×10^{-11} to $2.75 \times 10^{-11} \text{ Pa}^{-1}$.

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“Minicaster”- A Research-scale Directional Solidification Furnace

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Introduction

A program aimed at expanding the supply of silicon feedstock for producing ingots by the directional solidification technique was funded by the Pennsylvania Energy development Authority and executed at Solar Power Industries, Belle Vernon, Pennsylvania. Solar Power Industries is a vertically integrated manufacturer of multi-crystalline silicon solar cells. It currently has 13 commercial directional solidification furnaces that cast 265 kg silicon ingots. A research-scale crystallization furnace was constructed to screen candidate silicon feedstock materials and to explore experimental processes to enable their use.

Production scale ingots have melt volumes of 0.629 m^3 and a mass of approximately 265 kg, whereas the research furnace charge size was scaled down by a factor of 15 or more to a melt volume of 0.042 m^3 at ingot mass near 10 kg. Production of high quality solar cells begins with controlling processing variables during ingot casting. Since casting of commercial size 265 kg ingots is expensive and requires times of approximately 48 hours, there was a need to develop a capability to efficiently cast small ingots for research. The smaller size of the minicaster will allow for the evaluation of candidate feedstock sources and growth techniques on less material having faster turn around times. This paper describes the development and capabilities of the minicaster which is used to conduct research on variables such as silicon feedstock, doping and solidification cycles.

Description of the Minicaster

In the minicaster, the silicon charge resides in a $195 \text{ mm} \times 195 \text{ mm} \times 108 \text{ mm}$ vitreous quartz crucible. Graphite plates surround the crucible and serve as mechanical support for the crucible once it begins to soften above 1200°C . A graphite block rests atop pedestal supports and serves as a heat sink for the crucible during growth. Surrounding the crucible is a bank of resistive heaters that uniformly heats the charge.

A movable insulation cage serves as the primary means by which the desired cooling rate and directional solidification growth is achieved. Temperature monitoring is conducted using three thermocouples and an optical pyrometer. These sensors are positioned in specific positions throughout the hot zone to aid the thermal profile and modeling. Encapsulating the hot zone is a water-cooled chamber where pressure and inert atmosphere can be regulated.

Operation of the minicaster

Figure 1 is a plot of a time-temperature cycle for research solidification which is about 12 hours. The primary features of the casting cycle are illustrated in the figure. The crucible that is loaded with silicon feedstock is heated slightly above the silicon melting point of 1410°C . Time at full melt is restricted to minimize the incorporation of impurities from the crucible and heater power is reduced to achieve melt temperatures just below the melting point.

Figure 1 – Temperature control scheme for the minicaster.

Nucleation of silicon crystals at the crucible bottom begins, followed immediately by the onset of grain growth. The insulation cage is slowly raised to cool the melt approximately 50°C over an extended growth time. Once solidification is completed, the temperature is

lowered to an annealing temperature to relieve internal stresses in the ingot and the system is cooled to room temperature for ingot removal.

Finite Element Modeling of the Solidification Process

In order to assess the design of the “minicaster” hot zone prior to fabricating the components, thermal modeling was carried out using the ALGOR Professional Heat Transfer Analysis finite element package. Questions to be answered included the power and time required to melt the silicon charge, temperature profiles within the melt and system components at the beginning of solidification (no gap in the insulation), the required insulation gap to achieve controlled directional solidification, and the shape of the melt-solid interface during solidification. Temperature dependent material properties (density, thermal conductivity, specific heat, and emissivity) were used for silicon, the quartz crucible, the graphite crucible holder and heat sink, the graphite heaters, and the graphite insulation board.

The latent heat of fusion for silicon was incorporated into the model via a spike in the silicon specific heat over a five-degree range starting at the melting point (1410°C). Heat transfer via radiation and conduction were incorporated into the model.

Case 1: Transient solidification process with 30 mm insulation lift

Solidification process begins from the bottom of crucible. The ALGOR model was used to calculate thermal profiles in the minicaster ingots. Figure 2 shows the temperature distribution of minicaster during growth period. It is clearly seen that the surface solidification is initiated before the main silicon crystal grows from the bottom to the melt surface. Solidification at the top of the molten silicon is undesirable and thought to be due to the shorter graphite heater and low heater position. The heater could not provide enough heat to the top part of silicon melt to maintain a temperature higher than melting point.

Figure 2: Case 1: Temperature distribution of minicaster furnace with 30mm insulation lift, showing solidification on the top surface.

First “Mini”-Ingot

Weight of the initial ingot was 5.5 kg, with ingot dimensions of 195 mm × 195 mm × 62 mm which is suitable for 156 mm square solar cell substrates. As shown in figure 3, most of the ingot surface is flat and smooth, but there are some regions at the top of the ingot where the solidification proceeded erratically. This is thought to be associated with an undesired solidification at the top of the melt which initiated while solidification was occurring from the bottom upward. Such a solidification was predicted by the finite element thermal model of the growth. Since silicon expands upon solidification, the last of the melt to freeze may have been partly trapped between the solidified lower portion and upper portion of the ingot and have been squeezed out along the edges of the ingot to give the shape observed.

To eliminate the surface solidification, the following were considered: 1) Increase the heater power level; 2) Change the graphite heater position; 3) Change the insulation lift distance.

Figure 3: Photograph of first silicon ingot produced in August 2006, before being removed from the minicaster. 6 kg, 195 mm × 195 mm × 62 mm.

Case 2: 30 mm insulation lift with higher heater power level

To eliminate surface solidification, the graphite heater power level was increased by 25%, the temperature distribution of which is shown in figure 4. With more heat introduced into crucible, the surface solidification has been eliminated. However, since more heat has been added from side walls of crucible, the solidification interface is much more convex to the melt which will make it take much longer time for corner growth after central growth finished. Such a long period of time may increase the chance of contamination from crucible or graphite parts of the furnace into silicon melt.

Case 3: 30 mm insulation lift with higher heater position and power level

In addition to increasing the heater power level by 25%, the heater position was also raised. Fig. 5 shows the temperature distribution of the minicaster during the solidification process. No surface solidification was predicted during the growth process. The solidification interface is flat and a little convex to the silicon melt which is beneficial for high quality silicon crystal growth.

Figure 4: Case 2: 30 mm insulation lift and 25% increase of graphite heater power level showing a highly convex solidification profile.

Summary of modeling results

In the current minicaster design, the graphite heater position is relatively lower than the production DSS furnace. Such low position might give surface solidification during growth process. Several possible solutions have been provided. Increasing the heater power may cause longer growth process time which will enhance the chance of the secondary contamination from other thermal components inside furnace.

Figure 5: Case 3: 30 mm insulation lift with higher graphite heater position and 25% increased heater power level.

By adjusting the graphite heater to a higher position, the temperature of silicon melt surface can be maintained higher than melting until the solidification interface reaches the surface.

Another effective way to adjust the thermal gradient is by adjusting the insulation lift distance. More research will be done in the future. Moreover, the thermal model will be calibrated using experimental data from minicaster furnace operation.

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Hydrogen Incorporation into Czochralski Silicon Wafer and Hydrogen Passivation of Grain Boundary in a Hybrid Orientation (110)/(100) Direct Silicon Bonded Wafer

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ABSTRACT

Hydrogen incorporation into CZ (Czochralski) silicon wafer was studied using wet chemical etching and boiling in water processes. It was found that boiling in water incorporated more hydrogen into deeper region compared to wet chemical etching treatments. Hydrogen passivation of grain boundary in silicon was investigated using hybrid orientation (110)/(100) direct silicon bonded wafer. After hydrogenation, minority carrier recombination lifetime was enhanced, but lifetime improvement was not quantitatively correlated with the amount of introduced hydrogen.

I. INTRODUCTION

Multi-crystalline silicon (mc-Si) wafers include low and high density structural defects regions. Impurities are incorporated into the ingot during crystal growth. Dislocations and grain boundaries (GBs) are internal gettering centers and are usually decorated by incorporated impurities. Our research [1] has revealed that gettering is not effective in the highly defective regions which occupy most of mc-Si wafer. It was suggested that segregated impurities are not released from the high density structural defects at 900° C resulting in poor gettering performance. Hydrogen passivation is likely affected by the impurity contamination level at GBs in mc-Si [2]. The effects of the hydrogen passivation on the mc-Si wafers have primarily been characterized by the averaged minority carrier lifetime, and there are few papers on their effects on the GBs and the intra-grain defects. Hybrid orientation direct silicon bonded wafer consisting of a thin ~200nm (110) transfer layer on top of a (100) substrate is fabricated using the direct silicon bonding technique [3]. The bonding interface can be treated as a grain boundary between (110) and (100) grains. Fig. 1 shows a schematic drawing with a cross-sectional TEM image. This sample was used as a model-defect for hydrogen passivation of GB with or without deliberate contamination. In this study, hydrogen incorporation into silicon will be investigated first and hydrogen passivation of (110)/(100) GB without intentional contamination will be explored briefly through minority carrier recombination lifetime evaluation.

II. EXPERIMENTAL

CZ grown silicon wafer was used to investigate the injection of hydrogen into silicon by wet chemical etching and boiling in water. The boron doping concentration is $1 \times 10^{15} \text{ cm}^{-3}$, as determined from C-V measurements. Gold was deposited on the backside of the wafer by thermal evaporation, and driven-in by 850° C, 1hr annealing, which was terminated by quenching in ethylene glycol. The near surface region was removed by isotropic silicon

etching (CP4, HNO_3 :HF: CH_3COOH in the ratio 5:3:3 for 30 sec). Subsequently, annealing was performed at 500°C for 10 min. to dissociate hydrogen related complexes introduced by chemical etching solution. Six different kinds of processes were applied to introduce hydrogen (see Table I.).

Cleaning process (Piranha solution 1 part H_2SO_4 + 1 part H_2O_2) and boiling in water treatment were selected for the injection of hydrogen into the hybrid orientation wafer. Before hydrogen treatment, samples are annealed to remove hydrogen in as-received sample. For hydrogen passivation evaluation, minority carrier recombination lifetime was measured by photoconductance decay technique. Surface passivation was applied using quinhydrone methanol solution for more than 1 hour [4]. A 904 nm GaAs laser with a Si penetration depth of $\sim 30\ \mu\text{m}$ was used as a carrier injection source.

TABLE I. Process for the injection of H

A. 1%HF, 10%HF, 49%HF for 1M
B. Piranha for 2M $\rightarrow$ 7%HF for 30s $\rightarrow$ Piranha for 30s
C. Boiling in water for 10M
D. HNO_3 :HF: CH_3COOH , 5:3:3 for 30s

Figure 1. (a) Schematic drawing and (b) cross-sectional TEM image of a hybrid orientation direct silicon bonded wafer with a thin (110) layer on top of (001) Si substrate.

III. RESULTS and DISCUSSION

1. Hydrogen incorporation in CZ silicon wafer

For as-received CZ silicon wafer, boron was neutralized to a depth of about 3 microns (see Fig. 2(a)). It is widely known that the chemical-mechanical wafer polishing introduces fast-diffusing species which passivate the acceptors in the sub-surface region [5]. DLTS (Deep Level Transient Spectroscopy) showed electrically active impurities, such as transitional metals, were not involved in boron passivation in the near surface region. The possible candidates for these species include atomic hydrogen, vacancies, and interstitial impurities such as Na^+ , Li^+ or Cu^+ . Before H injection process, the near surface region was removed by isotropic silicon etching, and the etched sample was annealed at 500°C to remove the H introduced during etching.

Hydrogen gold pair is strong indication of introduced hydrogen into silicon. Table II summarizes the activation energies and capture cross sections of hydrogen related gold pair, gold donor, and gold acceptor deep levels in p- and n-type samples [6]. Fig. 2(b) shows that H-Au pairs (labeled G2) were detected by DLTS. They appeared in DLTS spectra for all six hydrogen injection processes we examined. It was found that the level of H-Au pairs is two orders of magnitude lower than H-B pairs. Most of introduced hydrogen is captured by boron preferentially. Thus, the total amount of introduced hydrogen for each

Figure 2. (a) Depth profile of active boron concentration of as-received and hydrogenated CZ wafer by boiling in water (measured by Schottky diode C-V profiling). (b) DLTS spectra of gold diffused hydrogenated CZ by boiling in water.

hydrogen injection process was calculated from the decrease of active boron concentration by C-V profiling.

Fig. 3 shows the depth profile of introduced total hydrogen according to the different hydrogen injection processes. Compare with immersion in HF solutions and Piranha cleaning processes, boiling in water treatment and isotropic silicon etching can introduce more hydrogen into deeper regions. It was found that hydrofluoric acid concentration was not a factor affecting the amount of introduced hydrogen.

TABLE II. Activation energies ΔE and majority-carrier capture cross sections of the deep levels in p- and n-type samples. [Ref. 6]

Peak	ΔE (eV)	$\sigma_p(\text{cm}^2)$	$\sigma_n(\text{cm}^2)$	T (K)
G2	0.21	1.7×10^{-15}		100-125
Au ^{0/+}	0.35	1.0×10^{-15}		150-180
G3	0.47	5×10^{-16}		228-250
Au ⁻⁰ + G4	~0.53			
G1	0.19		1×10^{-17}	90-120
Au ⁻⁰ +G4	0.56		1×10^{-16}	260-300

2. Hydrogen passivation of (110)/(100) grain boundary in silicon

Four samples were prepared for lifetime measurements (see Table III.). They are one as-received sample, one sample with the bonded layer and GB removed to measure the bulk lifetime, one sample boiled in wafer, and one sample went through the Piranha → HF → Piranha cleaning process. Before H injection, the samples had been annealed at 900°C to remove possible H existed in the as-received sample. Compared with the as-received, the lifetime was improved after hydrogen injection. However, lifetime improvement is not quantitatively consistent with the amount of introduced hydrogen. The minority carrier recombination velocity at GB was calculated from the substrate bulk lifetime and the

lifetime of each H passivated sample, see Table III. Currently, we tentatively understand that GB are hydrogen passivated. Electric potential barrier near GB could hinder hydrogen passivation at GB. For our experiments, hydrogen was introduced at low temperatures compared to hydrogenation methods used to fabricate solar cells, which could affect the effectiveness of hydrogen passivation of GB.

TABLE III. Minority carrier recombination lifetime

Samples	τ (μ s)	$*S_{GB}$ (cm/s)
As-received	1.71	6,000 ~ 10,000
Piranha $\rightarrow$ HF $\rightarrow$ Piranha	2.72	1,300 ~ 1,800
Boiling in water	2.74	1,300 ~ 1,800
Bulk without GB	3.25	

* S_{GB} : grain boundary recombination velocity

Figure 3. Depth profile of incorporated total hydrogen in CZ silicon wafer

IV. CONCLUSIONS

Based on knowledge of hydrogen injection efficiency into CZ silicon wafers, boiling in water and isotropic etching were used to introduce hydrogen into hybrid orientation wafers for GB passivation. Increased minority carrier recombination lifetime was observed due to the hydrogen passivation of GB. Future plan is to explore hydrogen passivation of transition metals contaminated GB and thermal stability of hydrogen passivation.

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Intragrain defect characterization of solar grade silicon using near-field optical beam induced current

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Abstract

Thermally induced stress in block cast multicrystalline silicon generates intragrain dislocation clusters, which act as minority carrier recombination centers that reduce overall cell efficiency. Near-field scanning optical microscopy (NSOM) is used to characterize the recombination strength of these defects, using photoinduced current variation (NOBIC) as the contrast mechanism. Recombination along dislocation lines is imaged, and a Green function solution of the carrier steady state continuity equation is used to quantitatively model the photocurrent images near the defect.

Introduction

The presence of intragrain dislocations due to thermal stress is a common phenomenon encountered in the manufacture of block cast multicrystalline silicon^{1,2}. Thermal gradients generate high dislocation densities during melt cooldown near the growth crucible edges. Such dislocations either pile up along grain boundaries, or form shallow grain boundaries, thereby acting as recombination centers, which degrade the minority carrier lifetime and ultimately reduce solar cell efficiency. In addition, these dislocation clusters act as gettering sites for light element or metallic impurities, which are incorporated through the contact of the silicon melt and crystal with the crucible walls. The recombination behavior of these intragrain dislocation clusters is not well understood, largely because the size of the defect (<100 nm) is smaller than the spatial resolution available to existing characterization techniques. It is thus desirable to complement existing microscopy techniques with one that can offer nondestructive, submicron resolution.

Near-field scanning optical microscopy (NSOM) is a submicron resolution characterization method that can provide both qualitative and quantitative information about collection efficiency at small angle grain boundaries. In the NSOM technique³, a fiber optic probe with a subwavelength aperture is placed several nanometers from the sample surface, in such a way generating “near-field” light of high spatial resolution. In this work, NSOM is used to map the recombination behavior of dislocation clusters in multicrystalline silicon using near-field optical beam induced p-n junction photocurrent as the contrast mechanism. The near-field optical beam induced current (NOBIC) technique⁴⁻⁹ is the near-field equivalent of the laser beam induced current (LBIC) technique. With NOBIC, the increase in resolution compared to LBIC is achieved due to the use of the evanescent waves that compose the near field light.

Theory

Modeling of the photocurrent distribution begins with the steady-state continuity equation associated with the photoexcited carrier density generated from the near-field beam:

$$\frac{\partial n}{\partial t} = \frac{D}{e} \nabla \cdot \mathbf{J} - \frac{n}{\tau} + S = 0 \quad (1)$$

where n is the photoexcited carrier density, D is the diffusion coefficient for silicon, e is the electron charge, τ is the recombination lifetime, S is the excess carrier generation rate and $\mathbf{J}$ is the current density. The photocurrent response is described by two major processes: carrier generation and carrier diffusion. A uniform bulk sample harbors a volume of excess carriers. Under near-field illumination, a point-like excitation volume results under the probe due both to diffusion within the material and relaxation or recombination of excess carriers inside the volume.

In reality, the near-field aperture is not a point but a circular aperture; because of this, the light intensity profile is modeled as a Gaussian distribution. The highest light intensity (and thus carrier density) is under the tip¹⁰. The diffusion profile, spherical for a uniform bulk sample, is constrained by the surface and defects in the layer. Since the layer thickness is much smaller than the diffusion length of carriers in the material, the steady-state equation becomes a two-dimensional problem¹¹. The steady-state equation is again reduced, to one dimension, given the linear nature of the intragrain defect. When the probe tip moves towards or away from the defect, the carrier profile varies strongly in form and magnitude. This one-dimensional problem is considered in this work. The diffusion equation and photocurrent integral thus simplify to:

$$\frac{\partial^2 n(x)}{\partial x^2} - \frac{n(x)}{D\tau(x)} + \frac{S(x)}{D} = 0, \quad (2)$$

$$I = \int \bar{J} dx = \int \frac{n(x)}{w} e|v_{dr}| dx = \frac{N(x)}{w} e \frac{w}{\tau_{dr}} = \frac{N(x)e}{\tau_{dr}}, \quad (3)$$

where, $n(x)$, $\tau(x)$ and $S(x) = S_0 2R\delta(x-x_0)$ (R = tip radius) are the carrier density, carrier lifetime due to drift current across the p-n junction, and photon generation rate, respectively.

To solve for the carrier density $n(x)$ in Equation (3), the carrier ‘lifetime’ in the layer $\tau(x)$ must be defined. The carrier lifetime behavior of a line defect of width $2a$ located at $x = 0$ is modeled as a step function:

$$\tau(x) = \begin{cases} \tau_d, & 0 < x < a \\ \tau_{df}, & a < x < \infty \end{cases} \quad (4)$$

where $\tau_{df}(x)$ is the defect-free carrier lifetime, and $\tau_d(x)$ the defect carrier lifetime. The solution to Equation (3), using the lifetime condition of Equation (4), is a Green function, which describes the carrier density distribution as it emanates from a point source. The solution is calculated by matching the Green function solution in four regions: at the two boundaries of the defect-free and defect regions, and on the two sides of the carrier injection site, i.e. the probe tip. Two cases are needed to fully describe the current profile: 1) when the probe position is located outside the defect region $2a$, and 2) when the probe is inside the defect. Integrating each $n(x)$ expression over each interval and adding terms gives an excess carrier number $N(x_0)$ of:

$$N(x_0) = S_1 L_1 \left[\exp\left(\frac{a-x_0}{L_1} - \frac{2a}{L_2}\right) - \frac{L_2}{L_1} \left\{ \exp\left(\frac{a-x_0}{L_1} - \frac{2a}{L_2}\right) - \exp\left(\frac{a-x_0}{L_1}\right) \right\} - \left\{ \exp\left(\frac{a-x_0}{L_1}\right) - 1 \right\} + 1 \right] \quad (5a)$$

for the defect-free region, and

$$N(x_0) = S_2 \left[L_1 \left(\exp\left(\frac{a-x_0}{L_1} - \frac{x_0-a}{L_2}\right) - \exp\left(\frac{-x_0-a}{L_2}\right) \right) + L_2 \left(\exp\left(\frac{-a-x_0}{L_2}\right) - \exp\left(\frac{-a-x_0}{L_2}\right) + \exp\left(\frac{-a+x_0}{L_2}\right) - 1 \right) \right] \quad (5b)$$

for the defect region, where x_0 is the fiber optic tip position, a is the defect size in nanometers, S_1 and L_1 and are the diffusion lengths and $S(x)$ terms of the defect-free region, S_2 and L_2 are the same for the defect region.

The carrier number $N(x)$ is a photogenerated population from an circular aperture, therefore it is desirable to correlate the Gaussian light intensity from the fiber optic probe to the carrier density. To correlate the light intensity to the carrier density, a convolution $C(x)$ of the two expressions is done, which generates a scaled error function solution:

$$C(x) = \frac{-S(x)\tau_{df}}{4\sqrt{2\pi}\sigma^2} \left[\exp(\Phi_1) [-1 - \text{erf}(\phi_1)] + \frac{L_2}{2L_1} [\text{erf}(\phi_1) - \text{erf}(\phi_2)] [\exp(\Phi_2) - \exp(\Phi_1)] + [\text{erf}(\phi_2) - \text{erf}(\phi_3)] [1 - \exp(\Phi_2)] + [\text{erf}(\phi_3) - 1] \right] \quad (6a)$$

where:

$$\Phi_1 = \left(\frac{\sigma^2}{2L_1^2} + \frac{a-x}{L_1} - \frac{2a}{L_2} \right), \Phi_2 = \left(\frac{a-x}{L_1} - \frac{\sigma^2}{2L_1^2} \right), \phi_1 = \left(\frac{-a-\lambda}{\sqrt{2}\sigma} \right), \phi_2 = \left(\frac{a-\lambda}{\sqrt{2}\sigma} \right), \phi_3 = \left(\frac{x_o-\lambda}{\sqrt{2}\sigma} \right), \lambda = x - \left(\frac{\sigma^2}{L_1} \right) \quad (6b)$$

for the defect-free case, and

$$C(x) = \frac{S(x)\sqrt{\tau_d\tau_{df}}}{4\sqrt{2\pi\sigma^2}} \left(\exp(\Phi_3) [\text{erf}(\phi_4) - 1] - \exp(\Phi_4) [-1 - \text{erf}(\phi_5)] \right) + \frac{S(x)\tau_d}{4\sqrt{2\pi\sigma^2}} \left[[\text{erf}(\phi_5) - \text{erf}(\phi_6)] (\exp(\Phi_4) - \exp(\Phi_5)) + [\text{erf}(\phi_7) - \text{erf}(\phi_8)] (\exp(\Phi_6) - 1) \right] \quad (7a)$$

in the defect region, where:

$$\Phi_3 = \left(\frac{a-x}{L_1} + \frac{x-a}{L_2} - \frac{\sigma^2}{L_1L_2} + \frac{\sigma^2}{2L_1^2} + \frac{\sigma^2}{2L_2^2} \right), \Phi_4 = \left(\frac{-x-a}{L_2} - \frac{\sigma^2}{2L_2^2} \right), \Phi_5 = \left(\frac{a-x}{L_2} + \frac{\sigma^2}{2L_2^2} \right), \Phi_6 = \left(\frac{-a+x}{L_2} + \frac{\sigma^2}{2L_2^2} \right) \quad (7b)$$

$$\phi_4 = \left(\frac{x_o-\xi}{\sqrt{2}\sigma} \right), \phi_5 = \left(\frac{-a-\chi}{\sqrt{2}\sigma} \right), \phi_6 = \left(\frac{a-\chi}{\sqrt{2}\sigma} \right), \phi_7 = \left(\frac{a-\nu}{\sqrt{2}\sigma} \right), \phi_8 = \left(\frac{x_o-\nu}{\sqrt{2}\sigma} \right), \quad (7c)$$

$$\xi = \left(x - \frac{\sigma^2}{L_1} + \frac{\sigma^2}{L_2} \right), \chi = x - \left(\frac{\sigma^2}{L_2} \right), \nu = x - \left(\frac{\sigma^2}{L_2} \right)$$

These expressions for C(x) are substituted for N(x) in Equation (3).

Experimental

The NOBIC measurements were performed using a homemade NSOM setup by modifying a commercial Digital Instruments Nanoscope I, along with electronics and data acquisition software designed for our experiment. The fiber optic near-field probe was etched and coated with aluminum to create the subwavelength aperture³. The illumination source used was a 632 nm diode laser from Meredith Instruments. The probe-sample separation distance was controlled using the shear force feedback method¹²⁻¹⁴. In such a way, topographic and photocurrent images are acquired simultaneously.

The defect recombination behavior of a 5 x 5 in², SiN passivated cast silicon wafer provided by BP Solar was characterized using microwave photoconductive decay (μ PCD), Nomarski differential interference contrast optical microscopy, and electron beam induced current (EBIC), which confirmed the existence of electrically active dislocation clusters¹⁵⁻¹⁶. For NOBIC analysis, wafers from the same silicon block with dislocation clusters were cut and sent to BP Solar for phosphorus annealing to create p-n junctions. To delineate areas of interest on the sample, p-n “mesas” several millimeters in diameter were created by placing hot wax on the region of interest, Secco etching the remainder of the phosphorus layer, then removing the wax using acetone.

Results

The scanned NOBIC image, which is composed of one hundred vertical line scans, and the corresponding background-subtracted topographical map is shown in Figure 1. Two line scans from the NOBIC image, labeled “A” and “B”, were picked for analysis. These particular line scans are chosen to highlight the reproducibility of the photocurrent model, in spite of the drop in background signal due to laser instability from line scan “A” to “B”, and to correlate areas of defect height to enhanced areas of NOBIC contrast. The NOBIC line scan models, shown in Figure 2, consist of piecewise functions where the defect-free and defect solutions best match the measured data. Using Equations (3), (6) and (7), the defect-free model is valid to within 500 nm of the 10 nm defect, otherwise the defect model holds. The asymmetry in the measured data, which is not modeled, causes much of the model-data parameter variation.

Figure 1. Correlation of NOBIC contrast to surface topography. NOBIC (left) and topographical images of $4.8 \mu\text{m} \times 4.8 \mu\text{m}$ scan region showing linear region, of reduced photocurrent. Line scans “A” and “B” are chosen to show the decrease in the NOBIC background signal.

We find similar qualitative features in our one-dimensional model around a line defect as Xu *et al.*¹¹ does for a two-dimensional model around a point defect. In the theoretical case, resolution is determined by the larger of the aperture size or defect size. In our measurements, the aperture size dominates. The aperture size $2R$ is estimated to be $\lambda/3.2 = 200 \text{ nm}$, which is larger than the 10 nm defect size used in our model. The best NSOM probes can resolve optical point sources, such as fluorescent molecules, to about $\lambda/50 = 12 \text{ nm}$ ¹⁷⁻¹⁸, so it is reasonable to assert that the aperture size will be the dominating factor in determining resolution. The diffusion lengths L_1 and L_2 of the defect free and defect regions are dependent on the diffusion constant D , for silicon and the recombination lifetimes of each region. Using the diffusion constant for bulk silicon of $10 \text{ cm}^2/\text{s}$ of approximately 300 nm , we estimate the defect free lifetime τ_{df} to be 500 ps , and the defect lifetime τ_{d} to be 100 ps , corresponding to diffusion lengths of 707 nm and 316 nm , respectively.

Figure 2. Plot of the NOBIC photocurrent values of line scans “A” and “B”, from Figure 1 and their overlaid photocurrent model (solid line). The photon generation rates S_1 and S_2 for the defect-free and defect regions are $6.28 \text{ E } 10$ and $6.13 \text{ E } 10$ photons/nm s, respectively, for line scan “A” and $5.95 \text{ E } 10$ and $5.84 \text{ E } 10$ photons/nm s, respectively, for line scan “B”.

Conclusions

In summary, we have presented a characterization tool, with NOBIC, capable of imaging intragrain defects in multicrystalline silicon. We have proposed a one-dimensional measurement geometry, in order to model the photocurrent in the scan direction. Using near-field photocurrent values from generated by NOBIC and our model, we are able to image variations in recombination strength of dislocations and dislocation arrays, and model its behavior. It is unclear at this stage whether the images presented are due to the recombination at the intragrain defects *per se*, or recombination due to impurity gettering at these defects. Further analysis using transmission electron microscopy (TEM), X-ray diffraction (XRD), and deep level transient spectroscopy (DLTS) is required to fully ascertain the dislocation and impurity behavior within the BP Solar material.

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Correlation of Polycrystalline Silicon Wafer Mechanical Properties with Minority-Carrier Lifetime

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1. Introduction

Light element impurities, e.g., O, C, N, and structural defects (dislocations, twins, and grain boundaries) are known to influence the mechanical properties of mono and multi-crystalline silicon. For example, Yonenaga and Sumino [1] showed that yield stress in silicon is a function of both the initial dislocation density and the interstitial oxygen content. It has also been found that in silicon containing point defects, dislocations, and planar defects, either the influence of oxygen on the movement of dislocation, or the blocking of dislocations by planar defects, such as grain boundaries or twin boundaries, may control the mechanical behavior [2, 3].

Since the above mentioned impurities and defects are linked directly to the minority-carrier lifetime in silicon and therefore to its efficiency as a solar cell, we investigated in this study the mechanical properties of polycrystalline silicon in order to determine if the conversion efficiency is related to easily measurable mechanical properties. Accordingly, the dependence of hardness, elastic modulus, and fracture toughness on the wafer minority-carrier lifetime using a nanoindentation technique has been investigated in this work.

2. Materials and Methods

A cast 5x5 inch polycrystalline silicon wafer (175 mm thick) produced by BP Solar was tested. This wafer was cut from a region near a corner of the quartz crucible. Minority-carrier lifetime mapping was performed on a 7% HF passivated wafer using an AMECON JANUS 300 microwave photoconductive decay (μ PCD) system.

Nanoindentations were made on selected low and high lifetime areas using a Hysitron TriboIndenter. Two different indenter tips were employed having centerline-to-face angles of 45° (cube corner) and 65.3° (Berkovich). Loads were varied from 0.25 to 9 mN and loading/unloading rates were kept at 1 mN/s. Five measurements were made for each load in order to check reproducibility of the data. After testing, all the hardness impressions were imaged using atomic force microscopy (a unit attached to the Hysitron TriboIndenter), and a JEOL 6400F field emission scanning electron microscope (FESEM) in order to determine the sizes of the contact impressions and the lengths of the radial cracks. Crack length and indent size were measured from FESEM images approximately 24 h after indentation and the average values were calculated for each load.

3. Results and Discussion

Figures 1a and b are the μ PCD map and corresponding lifetime histogram, respectively. The microstructure of the poly silicon wafer was overlaid onto the μ PCD map after scanning the wafer in order to correlate the microstructure with the lifetime map, see Fig. 1a. Low lifetime bands observed in Fig. 1a at the bottom and right hand

Fig. 1. A μ PCD map of the polycrystalline Si wafer (a) with the corresponding lifetime histogram (b).

edges of the wafer correlate with ingot edges attached to the quartz crucible. The low lifetime bands are likely due to impurities diffusing from the crucible wall. Selected high and low lifetime regions A and B, see Fig. 1a, were cut from the wafer and polished for nanoindentation analyses.

Figure 2 shows typical nanoindentation load- displacement (P - h) curves of the low and high lifetime regions at three different peak loads using a Berkovich indenter. A unique material behavior called “elbow” occurs in all curves during the unloading period. It has been shown to be associated with the formation of localized amorphous silicon regions [4]. Another important feature in Fig. 2 is the similar loading slope of the curves for each region as the

Fig. 2. Nanoindentation P - h curves in the low and high lifetime regions at different peak loads using a Berkovich indenter.

indentation load is increased, while a significant variation is evident between Regions A and B. This behavior indicates that different mechanical properties exist between Regions A and B. Figures 3 and 4 show the measured hardness and elastic modulus of the low and high lifetime regions as a function of the indentation load, respectively. The low lifetime region has higher hardness (~15% more) than that of the high lifetime region as a

Fig. 3. Variation of hardness and elastic modulus of low and high lifetime regions with peak loads

function of the peak load. The elastic modulus of the low lifetime region also shows ~17% higher value than that of the high lifetime region. This is consistent with the results reported for Czochralski-grown silicon, which shows increased mechanical strength with increasing oxygen and nitrogen concentrations [5]. Even though the increased hardness of the low lifetime region can be attributed to the higher level of impurities and the possible higher density of dislocations than that of the high lifetime region, the variation of the elastic modulus values needs further work to be adequately explained. One possible reason could be the different crystallographic orientation between the two regions. Ebrahimi and Kalwani [6] reported elastic modulus variations in silicon from 130 to 169 GPa when the crystallographic orientation changed from (001) to (110).

Comparing the P - h curves obtained by Berkovich and cube corner indenters for regions A and B, Fig. 4, shows that the sharper cube-corner indenter produces larger peak-load displacements and a greater proportion of permanent plastic deformation after unloading than the Berkovich indenter. The cube corner indenter also produces load-displacement discontinuities during unloading called “pop-outs”, which corresponds to the formation of metastable Si-XII/Si-III crystalline phases [7].

Nanoindentation impressions produced by cube corner indenter were imaged as a function of indentation load using FESEM (images are not shown). Radial cracks were measured from these images and the fracture toughness (K_c) in the low and high lifetime regions was calculated using the following equation [8]:

$$K_c = \alpha \left(\frac{E}{H} \right)^{1/2} \left(\frac{P}{c^{3/2}} \right)$$

where, E is the elastic modulus, H is the hardness, P is the applied load, c is the length of the radial cracks, and α is an empirical constant that was taken as 0.032 for a cube corner tip. Figure 5 summarizes the experimental results of the fracture toughness of low and

high lifetime regions at different loads. As can be seen in Fig. 5, the fracture toughness of Regions A and B appears to be independent of the load applied during nanoindentation, which demonstrates the applicability of nanoindentation technique to determine fracture

Fig. 4. Comparison of the P-h curves in the low and high lifetime regions using Berkovich and cube corner indenters.

Fig. 5. Fracture toughness of the low and high lifetime regions as a function of indentation load.

toughness. The average fracture toughness values of the low and high lifetime regions are 0.93 ± 0.04 and 0.65 ± 0.03 MPa m^{0.5}, respectively. The fracture toughness follows a trend similar to that of the hardness and elastic modulus of the low and high lifetime regions.

4. Conclusion

Hardness, elastic modulus, and fracture toughness of low and high carrier lifetime regions in polycrystalline silicon was evaluated using nanoindentation technique. The results obtained in this study indicate that mechanical properties of poly silicon are highly influenced by both the impurity levels and dislocation density and therefore can be correlated directly with the minority carrier lifetime. In order to better understand the observed variation in mechanical properties, grain orientation measurements (e.g., back-reflection Laue method) along with a detailed imaging technique(s) to reveal the various defects would be necessary.

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Passivation of ideal, high-angle grain-boundaries

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Abstract

This paper reports on the effect, hydrogenation has on the electrical properties of an ideal high-angle silicon grain-boundary. Temperature dependent capacitance measurements and deep-level transient spectroscopy was used to evaluate the distribution of interface states following hydrogenation. Although a slight decrease in the overall interface charge was observed, the most significant difference was a narrowing of the interface states distribution from a broad band, to an energy-band concentrated close to mid-gap. The possible impact the state distribution has on the recombination efficiency, is also discussed.

1. Introduction

Much work has been published over the years characterizing the electrical, structural and mechanical/defect properties of various forms of commercial polycrystalline silicon, ranging from cast ingots, to string ribbon and molded wafers. One thing that is patently clear from all this work on pc-Si is that it is very difficult to generalize or transfer results from one growth system, process line or passivation scheme to another. Because of the inherent complexities in these commercial products, the photovoltaic/ microelectronic silicon materials group at NC State U has recently initiated a broad characterization program of a newly developed silicon IC device wafer based on direct bonding of {110} oriented samples on a {100} substrate [1,2]. By varying the twist/tilt between the bonded wafers, the grain-boundary properties can be well controlled. The end result is the production of a broad set of sample variables, uniquely compatible for performing both fundamental impurity gettering and passivation studies, as well as simulating real world GB and intra-grain electrical and mechanical behavior.

2. Experimental details

The as-bonded (110)Si/(100)Si structure consists of a thin 200nm thick (110)Si transfer layer on-top of a (100)Si substrate. In order to systematically study the electrical effects of the bonding interface depth, the as-bonded 200nm thick (110)Si transfer layer was epitaxially thickened by chemical vapor deposition to a thickness of 2.3 μ m. Hydrogen was introduced by boiling the samples in water for 10min. Electrical measurements were performed using Schottky contacts formed by depositing 2mm diameter Al-contacts onto the (110) surface and scratching Ga-In eutectic onto the back-surface. The 1MHz capacitance-voltage and deep-level transient spectroscopy (DLTS) measurements were performed using a BioRad DL8000 digital DLTS system.

3. Results and Discussion

Following the approach used by Broniatowski [3], the traps present at the bonding interface can be deduced from DLTS measurements performed using different trap filling pulse conditions. During the reverse bias pulse, the trapping of holes at the interface is expected to result in a large non-equilibrium interface charge. Analogous to conventional DLTS, periodic reverse bias pulses are then used to vary the occupancy of states at the bonding interface. The decay of excess positive charge can then be monitored by observing the recovery of the zero-volt interface capacitance following the reverse bias pulse.

Figure 1 During a reverse bias pulse, holes reaching the interface are captured at available states above the quasi-Fermi level. For a band-like distribution of states, the hole transitions to higher energy states as the levels reach internal equilibrium during the filling pulse. Following the filling pulse, the holes are emitted in order to reach equilibrium with the valence and conduction bands.

Figure 1 illustrates the capture and emission processes expected at an interface with a uniform distribution of states. Hole capture will predominantly be to available states positioned close to the interface quasi-Fermi level, E_{Fa} . If the interface charge is able to redistribute by means of inter-level transitions, the captured hole will eventually occupy the highest available states above E_{Fa} . Hole Emission from the interface states will be dominated by emission from the lowest occupied energy states. Since the degree of band occupation is controlled by the redistribution of charge during the hole capture process, the transitions related to hole emission is expected to be time sensitive, saturating at the time needed to occupy all levels above the quasi-Fermi level. Following this description of the capture and emission processes, the complete distribution of states should be discernible when using different biasing (changes in E_{Fa}) and filling pulse periods.

We start by considering the capture and emission transitions of an un-passivated (110)Si/(100)Si grain-boundary. Figure 2 shows a selection of emission spectra obtained using different measuring conditions. The biasing and pulse periods were varied across a wide range, but omitted for brevity. For a small filling bias of 2V, and a pulse period of 0.1ms, a well defined hole trap is observed, having an activation energy of $E_T - E_V = 0.41\text{eV}$, and a capture cross-section, $\sigma = 2 \times 10^{-16} \text{ cm}^2$. As the bias is systematically increased, the spectra become slightly broader, but widen dramatically when the filling pulse is extended to longer periods. Considering the mechanism described in Fig. 1, hole emission is initially dominated by transitions from states near mid-gap, transitioning to emission from lower, occupied interface states. Within the limit of our biasing conditions, the interface state distribution appears to extend down to roughly 0.19eV from the valence band maximum. The possible impact of hydrogen on the interface state distribution can then be evaluated by repeating the measurements on a hydrogenated grain-boundary.

Figure 2 Measured DLTS spectra of an un-passivated (110)Si/(100)Si DSB interface. The position of each peak maxima remains constant for short filling pulses, with the spectra broadening towards lower temperatures as the filling pulse period is further increased. The high- T sides nearly coincide throughout the different measurements. The state distribution appears to consists of both band-like and localized components [4].

Figure 3 gives the DLTS spectra obtained following the hydrogenation of the bonding interface. The spectra have a significantly reduced energy distribution, with the transition dominated by hole emission from a level at $E_T - E_V = 0.57\text{eV}$. The introduction of hydrogen therefore appears to have passivated the density of states present in the lower half of the forbidden gap, with a high density of states remaining near mid-gap.

In order to determine whether the same effect can be observed in a thin, as-bonded wafer, the capacitance-voltage characteristics of a Schottky barrier diode was used to detect changes in the interface charge density. The capacitance of a Schottky diode is increased by the close proximity of the DSB interface. As a results, the space-charge capacitance demonstrates a noticeable temperature dependence due to gradual freezing of carriers at the interface states. Figure 4 compared the temperature dependence of the capacitance-voltage curves obtained for an un-passivated and passivated grain-boundary. The voltage was swept from 0V to 10V and maintained at zero-bias between temperature steps. Carriers are systematically frozen at energies above the quasi-Fermi determined by the voltage conditions used. For the un-passivated diode, the capacitance decreases gradually with decreasing temperature, with a slight knee observed at roughly 175K. We verified that this drop in capacitance is not due to a calibration problem of the capacitance meter. Since the capacitance of the un-passivated grain-boundary therefore predominantly follows the shift in the Fermi-level with decreasing temperatures, the interface state density appears to be uniformly distributed over a large energy range. In the case of the passivated diode, however, the capacitance decreases sharply between 200K and 150K. This pronounced step is suggestive of a narrow distribution of interface states, with the observed change in the space-charge density related to a density of $N_T = 1.8 \times 10^{10} \text{ cm}^{-2}$. Although the interface charge was slight decreased following hydrogenation, the main response is a significant narrowing of the state distribution at mid-gap energies. Whether the upper half of the interface state distribution is affected by hydrogenation, still remains to be determined.

Figure 3 The filling pulse dependence of a passivated (110)Si/(100)Si grain-boundary. The normalized, $V_R = 2\text{V}$ spectra are indistinguishable, suggesting that the spectra is composed of discrete energy levels. The Arrhenius plots gave $E_T - E_V = 0.57\text{eV}$, $\sigma = 5 \times 10^{-14} \text{ cm}^{-2}$. The spectra have been shifter vertically for clarity.

An interesting consideration is the manner in which the energy distribution of the interface/grain-boundary states might translate into its recombination efficiency. According to Shockley-Read-Hall statistics, the recombination efficiency of individual energy levels within the forbidden gap is nearly equivalent across most of the forbidden gap [5]. Since the degree of band-bending associated with the pinning of the Fermi-level at the boundary controls the efficiency by which minority carriers are collected, the distribution of state will largely determine the recombination efficiency at the interface. The mechanism by which the interface charge equilibrates during minority carrier recombination with trapped majority carriers, however, also requires the capture of holes reaching the interface by means of thermionic emission over the potential boundary.

Figure 4 Temperature dependence of the capacitance vs. voltage curves of an as-bonded (110)Si/(100)Si grain-boundary. The un-passivated (a) zero-volt capacitance decreases uniformly with the shift in the Fermi-level, whereas the passivated (b) interface has a distinctive temperature step associated with carrier freezing.

Although the recombination at individual levels might be relatively insensitive to the energy level of deep traps, a variation in distribution could therefore produce notably different recombination efficiencies: in the case of a band that extend up to the valence band maximum, majority carries could efficiently migrate to higher energies, quickly occupying mid-gap states. For a narrow energy distribution of deep states, as observed for the passivated (110)/(100) boundary, the interface is expected to be comparably less efficient due to a large potential barrier for holes and a slower rate at which internal equilibrium is reached.

4. Conclusions

The distribution of states at a (110)/(100) large-angle grain-boundary was determined by observing the temperature dependent relaxation of majority carriers at the interface. The grain-boundary was characterized by a broad distribution of states that displayed a band-like behavior during hole capture. Following hydrogenation, the total interface charge density appeared relatively unchanged. The electronic states associated with the grain-boundary, however, had a significantly reduced energy distribution, concentrated near mid-gap.

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FTIR Studies on Multicrystalline Cast Silicon Edge Slab

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Introduction

Multicrystalline cast silicon is often used as a substrate material in solar cells because of its low cost and ease of production. Many grains in this material have a high dislocation density. Impurities can aggregate at these dislocations as well as at grain boundaries, leading to regions on a wafer with poor minority carrier lifetimes. Some of the impurities present in the silicon originate in the feed stock. The rest come from the quartz crucible and the furnace environment. During production, the regions of a cast silicon ingot that come in to direct contact with the crucible or the environment are removed prior to wafering. Typically, wafers used for testing come from the interior of the ingot. Understanding the impurity and defect distribution at the interior of the ingot requires knowledge of their origin. Profiling the distribution of impurities from the typically removed periphery of the ingot can determine their origin.

Experimental

A multicrystalline silicon ingot grown BP Solar was cut from a region that directly touched the quartz crucible walls during casting. The sample was 2 mm thick, 25 cm long, extending from the top to the bottom of the ingot, and 15 cm wide from the crucible edge into the ingot bulk, as shown in Fig. 1.

Three samples for use in Fourier Transform Infrared (FTIR) spectroscopy were cut from the slab parallel to the ingot base. They were taken at elevations of 1, 7, and 21 cm from the base of the ingot, as indicated in Fig 1. These samples were approximately 2 cm tall and extended 12 cm from the edge of the ingot into the bulk. Each sample was chemically polished in a mixture of nitric, acetic, and hydrofluoric acids in a ratio of ~2:1:1. The samples were then dipped in HF to strip any remaining oxide. FTIR was performed on each sample using a Bio-Rad FTS-6000 according to ASTM Standard F1188. Measurements were taken using a 5 mm square aperture in 5 mm steps along the length of each sample. A microwave photoconductance decay (MW-PCD) scan was taken for the original sample as well as the three FTIR samples. These lifetime maps were taken with the samples coated quinhydrone/methanol solution for surface passivation.

Results and Discussion

A MW-PCD lifetime scan in Fig. 1 shows a low lifetime band at the edge of the ingot. This band extends about 3 cm from the base of the ingot into the bulk. It extends 4.5 cm from the sidewall edge at the bottom and tapers off towards the top of the ingot.

Figure 1: At left, image showing original sample. Pieces used for FTIR are highlighted. At right, MW-PCD map of original sample. The sample is roughly 2 mm thick, 25 cm high, and 15 cm wide. The low-lifetime band occurs where the ingot was in contact with the quartz crucible used in casting.

1 cm elevation

Figure 2 shows a MW-PCD scan of the 1 cm elevation sample. This FTIR sample was taken from the very base of the original slab. We expect that the oxygen concentration is nearly identical across this sample as it is all in contact with the crucible base, thus a complete profile was not taken. Measurements taken at 3 cm intervals confirmed this, as all scans yielded oxygen concentrations close to $2.7\text{E}17\text{ cm}^{-3}$.

Figure 2: MW-PCD scan of 1 cm elevation sample. The sample is 2 cm tall and 10 cm wide at its base. The FTIR determined oxygen concentration was nearly constant across the entire sample.

7 cm elevation

Figure 3 shows a MW-PCD scan of the 7 cm elevation sample and a corresponding plot of its oxygen concentration distribution. In this sample we see the oxygen concentration drop from a maximum of $2.3\text{E}17\text{ cm}^{-3}$ at 0.5 cm from the ingot edge to a value of $8.8\text{E}16\text{ cm}^{-3}$ at 3 cm from the ingot edge. The concentration profile is level over the rest of the sample with an average value of $9.1\text{E}16\text{ cm}^{-3}$. The low lifetime band extends beyond the region of high oxygen concentration suggesting oxygen is not the cause of reduced lifetimes.

Figure 3: MW-PCD scan and corresponding FTIR determined oxygen concentration distribution for the 7 cm elevation sample. The concentration drops steeply and levels at a constant value ~3 cm from the ingot edge. The low lifetime band extends beyond the region of increased oxygen concentration, suggesting oxygen is not the cause.

Figure 4: MW-PCD scan and corresponding FTIR determined oxygen concentration distribution for the 21 cm elevation sample. The concentration remains fairly constant over the length of the sample and no drop in concentration is observed near the crucible edge.

21 cm elevation

Figure 4 shows a MW-PCD scan of the 21 cm elevation sample and a corresponding plot of its oxygen concentration distribution. This sample was located approximately 4 cm from the top of the ingot. We do not observe the same drop and leveling off in concentration that we did in the 7 cm elevation sample. Instead, the oxygen concentration remains fairly constant with an average value of $9.4\text{E}16\text{ cm}^{-3}$.

Conclusions

We have examined a unique sample of multicrystalline cast silicon in that it has intact the edges of the ingot that were in contact with the quartz crucible and the environment. MW-PCD lifetime maps of the sample show the expected low lifetime band at the edges of the sample that touched the crucible. FTIR profiles of interstitial oxygen concentration show that the oxygen concentration was lowest at the top of the ingot, likely due to evaporation. At regions lower in the ingot that were in contact with the crucible wall, the oxygen concentration drops steeply and levels to a constant value approximately 3 cm from the ingot edge. Oxygen concentrations range from $9\text{E}16$ to almost $3\text{E}17\text{ cm}^{-3}$, considerably higher than that found in Float Zone silicon (1 to $10\text{E}15\text{ cm}^{-3}$) and lower than that in Czochralski silicon (6 to $12\text{E}17\text{ cm}^{-3}$).

The low lifetime band extends beyond the regions of increased oxygen concentration, indicating that oxygen is likely not the only cause of reduced lifetime in this part of the ingot. Thus more testing is required and FTIR will be used to quantify substitutional carbon levels, while Deep Level Transient Spectroscopy (DLTS), will identify metallic impurities.

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Characterization of polycrystalline sheet silicon with improved lifetimes

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Abstract

This paper discusses improvement in the mean lifetime (from 1.2 μ s to 2.7 μ s) of polycrystalline sheet silicon samples produced by the molded wafer process. A complimentary set of characterization methods, i.e. preferential etching and EBIC studies have been used in conjunction with FTIR and EDS measurements to achieve correlation between the lifetime and the presence of inclusions or precipitates, their density and morphology, impurity concentration and associated dislocation cluster densities. EBIC and etching studies clearly shows that the low lifetime samples have higher defect density and smaller grain sizes. Deep level contaminations per cm of dislocation length varied from 10^4 to 10^6 for high and low lifetime samples respectively. Further, FTIR and EDS measurements confirmed the presence of C, N, and O based inclusions and precipitates, although with varying sizes and distributions.

Introduction

The production of continuous polycrystalline sheet silicon using the molded wafer process [1], providing low cost wafers without any sawing waste, needing minimal surface preparation and having a suitable shape for high density packing [1, 2, 3]. However, use of low-cost and impure silicon feedstock renders the sheet with smaller grain size and higher impurity concentration [4]. Various authors have studied and demonstrated the impact of these impurities and defects (dislocation, inclusions, precipitates etc.) on achievable lifetime in the polycrystalline sheet silicon samples [1, 5-9].

Previous studies by Lu et al, on similar samples have shown that the minority carrier lifetime varies between 0.5-3 μ s and grain sizes are in range of 0.1-1 mm [3-6]. These studies subsequently guided the optimization of film growth parameters to achieve improved overall cell performance and better lifetimes. Comparatively, newer samples displayed bigger grain structures with fewer inclusions or precipitates [3, 5, 7]. Furthermore, samples depicted a band of high and low lifetime regions, with maximum lifetime $\approx 10\mu$ s in regions corresponding to higher lifetime. In this work, the etching and EBIC studies are performed on the sheet silicon samples to investigate the observed high and low lifetime band formation behavior. Particle density and chemistry, associated dislocation cluster morphology and grain structure have been correlated with minority carrier lifetime.

Experimental

Polycrystalline sheet silicon wafers studied in this work were produced by molded wafer process at GE Energy Inc. The wafer thickness ranged from 600 to 800 μ m. On processed wafers, photoconductance decay (PCD) studies were carried out to map the excess minority carrier lifetime. Figure 1 exhibits lifetime maps of samples A-D, quarters of the same wafer following different gettering cycles. Note the high lifetime band across the quarters A and C. An

exceptional lifetime ($\approx 10\mu\text{s}$) was observed in the bands of high lifetime present in C quarter (fig. 1). Samples selected from high (labeled - H1 and H2) and low lifetime (labeled - L1 and L2) regions, were chemically-mechanically polished to remove 70-80 μm from the top surface. Further, samples were Secco etched for 40 s to study microstructure, detailing grain structure and defect density and morphology. In addition, Electron Beam Induced Current (EBIC), Fourier transform infrared microspectroscopy (FTIR), Energy Dispersive Spectroscopy (EDS) studies were also carried out for above identified samples.

Fig. 1 – (a) PCD map of complete wafer displaying quarters A-D. (b) Positions of the Samples H1 & H2 and L1 & L2 on the quarter C.

Results and Discussion

PCD measurements on both high and low lifetime samples show increasing mean lifetime with increasing injection levels. The current studies on samples were done with photon fluxes ranging from 1.5×10^{19} to $4 \times 10^{20} / \text{cm}^2 \text{s}$, which corresponds to normalized injection levels of 5 to 60, depending on minority carrier concentration for high lifetime sample ($N_s = 4 \times 10^{15} \text{ cm}^{-3}$) approximately half of that for low lifetime samples ($N_s = 7 \times 10^{15} \text{ cm}^{-3}$). These conditions thus suggest the higher injection levels compared to seen for sunlight.

Figure 2 shows etching and EBIC images of samples from high and low lifetime regions. Note that sample H2 shows very few inclusions (dislocated regions) compared to the sample L1. In addition, darker contrast in intra-grain regions of the EBIC image for L1 sample confirms presence of more defects, which are affecting the electrical activity in the sample. Typically, we see a dislocation cluster of size $\approx 20\text{-}25 \mu\text{m}$ and $\approx 50\text{-}60 \mu\text{m}$, respectively for high and low lifetime sample. For the high lifetime sample, the grains are nearly devoid of any dislocations. Also, on average, the grain size of the H2 is larger compared to L1.

Comparing these results with studies done by Lu et al. [3-6], the number of inclusions or precipitates and associated dislocation cluster densities and sizes has been reduced to large extent, thus explaining the approximately two times increase in lifetime for current sheet silicon samples. Another interesting fact to note is that the presence of “denuded zones” across the depth of the previous samples is not present here. The possible reasoning might be the much better

thermal profile across the wafer thickness resulting in a homogenous distribution of these inclusions or precipitates. The results also confirm that the current samples have reduced particle entrapment and precipitation of oxides, carbon and oxynitrides. These extended defects, oxygen and carbon precipitates, included particles and associated dislocation clusters, limits lifetimes in the processed wafers.

Fig. 2 - Sample from high (a & b) and low (c & d) lifetime areas were polished and Secco etched for 40 Sec. The images on left are micrographs at 4X-1.25X and on middle are at 40X-1.25X. (e) & (f) – EBIC images of Schottky Diode on high and low lifetime samples.

EBIC studies were also carried out from room temperature to 100 K for both high and low lifetime samples in order to estimate the electrical activity variations due to dislocations and contaminating impurities. It is observed that high lifetime samples exhibit increasing contrast with decreasing temperature, whereas low lifetime sample show only a slight increase contrast. Thus, it can be concluded that the high lifetime sample represents weaker contamination (Type 2, 10^4 - 10^5 deep level impurities per cm dislocation length) and low lifetime sample depict higher contamination levels (mixed type, 10^5 - 10^6 deep level impurities per cm dislocation length)[10] .

FTIR measurements were carried out on double-side polished samples using a 1 mm diameter probe. Infrared absorption peaks, see fig. 3, show the presence light elements, O, C and N with local vibrational modes, in their dissolved, complexed and precipitated states. Similar FTIR results were observed with polycrystalline sheet sample studied by Lu et al. [3]. The peaks 4-9 corresponds to silicon oxynitride absorption (associated to SiO, SiN, SiOH, and NH groups) depending on nitrogen to oxygen ratio, while, 4, 5 and 6 represents the Si-N stretching mode for the α - Si₃N₄ phases. Peaks at 605 and 1109 cm⁻¹ are due to substitutional carbon and interstitial oxygen (SiO stretching mode), respectively. The distinctive absorption peak at 1039 cm⁻¹ corresponds to Si-O-Si stretching mode, which was convoluted within the broadened oxy-nitride absorption in previous studies due to presence excess [O_i]. From the FTIR data the relative peak heights indicate that there has been a drastic reduction in interstitial oxygen [O_i], which is likely

due to better feedstock, reduced impurity levels and lesser associated microdefect nucleation centers. These microdefect nucleation centers facilitate $[O_i]$ precipitation, thus controls $[O_i]$ in precipitated form, which is detrimental to lifetime [4].

Fig. 3 – (a) FTIR plots for samples taken from the G7-C {H=High Lifetime, L=Low lifetime}, (b) FTIR spectrum for the sheet silicon sample reported in literature [3].

EDS measurements were performed on polished and Secco etched samples (H2, L1, and cross-section) using Hitachi S-3200 ESEM with 20 kV acceleration voltage. EDS probe measurements on the planner sample showed presence of the C, N and O peaks with silicon peaks (Fig. 4). Also, the SEM micrograph clearly displays the pits around the particles, representing are dislocations clusters revealed during the Secco preferential etch. Further, EDS measurements using probes 1-4 on the same locations with different particles showed varying chemistry with different C and N content (fig. 4). In comparison to studies by R. Zhang et.al. [7], EDS peaks recommend reduced oxygen content and SEM micrographs suggest smaller particle sizes. It is also observed that for high lifetime sample the size of the dislocation cluster around the particle is smaller.

Fig. 4 – (left) EDS spectra of clean area and particle, (right) 1-4 probes on 4 different particles from same location (probe 2 is on clean silicon region).

Thus FTIR and EDS results determine that irrespective of small concentration variation between samples of high and low lifetime, two competing factors: (i) particle size and (ii) their spatial distribution are controlling factors for lifetime. As minority carrier diffusion length in polycrystalline sheet silicon samples are of 50-100 μm , defects with spatial distribution less than 100 micron will adversely affect lifetime [8]. In case of low lifetime sample, though large particle might be several hundreds of micrometers apart, but the larger dislocation clusters (some time large enough to overlap) around them negate the separation effect. Whereas, for high lifetime samples the smaller sized dislocation cluster around well distributed particles favors lifetime improvement. Thus extended defects, as dislocation clusters, around the particles or inclusion are the responsible factor in limiting lifetime.

Conclusion

Studies on present sheet silicon sample showed more than twice improvement in mean lifetime. The comparison of current results with previous studies, suggest that improvement in lifetime is due to optimized process parameters which reduced interstitial oxygen $[\text{O}_i]$ concentration, improved grain morphology, and reduced level of defect and contamination. Also, the comparison between high and low lifetime samples, enumerates that spatial distribution of extended defects, i.e. inclusions and precipitates and extent associated dislocation cluster is main controlling factor for lifetime. Low temperature EBIC studies suggest that high lifetime sample are type-2 and low lifetime samples are mixed type, with 10^4 - 10^5 and 10^5 - 10^6 deep level impurities per cm dislocation length respectively.

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Determination of Surface Recombination Velocities for Thermal Oxide and Amorphous Silicon on Float Zone Silicon

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Introduction

Recombination at the surface of a silicon solar cell is an important factor in determining the cell efficiency. The descriptive parameter is surface recombination velocity, S . Generally, S increases as the doping of the surface increases, just as the lifetime of carriers within the crystal (τ) generally decreases as the bulk doping increases. Thus, in a comparative study of candidate surface treatments, it is important to choose a silicon surface doping level which is typical of common cell designs. Furthermore, because standard measurement techniques cannot distinguish between recombination at the crystal surface and recombination within the crystal bulk, it is desirable to choose a silicon crystal with high bulk lifetime in order to improve the sensitivity of the technique to surface recombination. In this study, 100 mm diameter float zone (FZ) silicon wafers, double side polished, with a (100) surface and 300 μm thickness were chosen, both p-type (boron-doped) nominally 3 $\Omega\text{-cm}$ and n-type (phosphorus-doped) nominally 1.2 $\Omega\text{-cm}$. The primary comparison was made between surfaces passivated with a thermally-grown oxide and those passivated with amorphous silicon deposited by the hot wire chemical vapor deposition (HWCVD) method. In addition, the degree of surface passivation associated with the thin chemical oxide created by RCA cleaning was measured, as was that associated with a temporary iodine-methanol treatment.

Sample Preparation

Samples for the thermal oxidation study were prepared by cutting the 100 mm diameter FZ wafers into quarters. All four quarters from each wafer were subjected to the RCA clean:

RCA1: 5:1:1 DI H_2O : NH_4OH (29%): H_2O_2 (30%) at 80°C for 10 min, then 10 min rinse;

HF Dip: 99:1 DI H_2O :HF(49%) at room temperature for 1 min, then 1 min rinse;

RCA2: 6:1:1 DI H_2O :HCl(95%): H_2O_2 (30%) at 80°C for 10 min, then 10 min rinse/dry.

Note that a thin chemical oxide resulting from the RCA2 step, estimated to be approximately 7 Å thick, is left in place (no final HF dip). Two of the wafer quadrants were put aside as reference samples so that the excess carrier lifetime in the starting wafer can be measured, while the remaining two wafer quadrants were oxidized.

Thermal oxidation was carried out in a standard quartz tube, 145 mm in diameter. Prior to wafer oxidation, the tube was cleaned using Trans 1,2-Dichloroethylene ($\text{C}_2\text{H}_2\text{Cl}_2$), known as Trans-LC, from Air Products (Schumacher). When combined with oxygen, Trans-LC produces HCl to facilitate cleaning of the tube. The reaction is:

With the Trans-LC bubbler held at 15°C and 130 sccm of N_2 carrier gas passing through the bubbler, 90 sccm of HCl gas is produced. This is 3% of the 3000 sccm of O_2 , the main gas flowing through the tube. The tube was cleaned in this way for three hours at 1050°C.

Wafer quarters were then oxidized at 1000°C for 150 min. In an effort to minimize the oxide/silicon interface state density, Trans-LC was introduced into the gas ambient as a source of HCl during the oxidation [1]. The gas flows were 3000 sccm of O₂ and 100 sccm of N₂ carrier gas flowing through the Trans-LC bubbler at 15°C. This combination is chosen to provide an optimum flow of HCl, which is 2.3% of the main O₂ flow. In this way, a chlorinated oxide approximately 1200 Å thick was produced, as determined by ellipsometry measurements. The oxidation was followed by an anneal in forming gas (10% H₂ and 90% N₂) flowing at 3000 sccm at 450°C for 30 min in the same tube. Both n-type and p-type FZ wafer quadrants were processed together through oxidation and forming gas anneal (FGA).

For the amorphous silicon deposition, rectangular blanks 25 mm × 45 mm in size were cut from the FZ wafers and subjected to an aggressive cleaning sequence [2]. Amorphous silicon layers were deposited by hot wire chemical vapor deposition, similar to that described previously for heterojunction cell fabrication [2, 3]. On one side of the crystalline silicon blank, undoped amorphous silicon was deposited from an SiH₄ source to a thickness of approximately 4 nm. This intrinsic layer is capped by a second amorphous silicon layer doped n-type with PH₃ to give an a-Si:H(i,n) structure. The opposite side of the blank had a similar intrinsic amorphous silicon layer, again capped by a second amorphous silicon layer doped p-type with B₂H₆ to give an a-Si:H(i,p) structure. After depositing these amorphous silicon layers on both sides, the sample was measured to assess the surface recombination velocity.

To obtain a fully accurate value of bulk lifetime, it is necessary to completely eliminate surface recombination. This condition is approached by applying a temporary chemical passivation, consisting of iodine dissolved in methanol, to the wafer surfaces. First, any surface oxide is removed by a dip in 10:1 DIH₂O:HF(49%) followed by a 30 sec rinse in DI H₂O and an N₂ blow dry. Both sides of a wafer are then coated with a solution of 280 mg of I₂ per liter of CH₃OH. The wafer is then placed in a transparent plastic zip-lock bag for lifetime testing using the photoconductivity decay (PCD) technique.

Method

The effective lifetime is determined by measuring the rate at which photogenerated excess carriers ($\Delta n = \Delta p$) return to their equilibrium concentrations [4]. Factors contributing to effective lifetime (τ_{eff}) include Shockley-Read-Hall recombination in the crystal bulk (τ_{SRH}), Auger recombination in the crystal bulk (τ_{Auger}) and recombination at the crystal surface (S). For a symmetric structure, as employed in this study, the relationship is:

$$1/\tau_{\text{eff}} = -(1/\Delta n)(d\Delta n/dt) = 1/\tau_{\text{SRH}} + 1/\tau_{\text{Auger}} + 2S/W \quad (2)$$

where W is the thickness of the wafer. If the effective lifetime is measured and corrected for Auger recombination (since equilibrium carrier concentration is known and excess carrier concentration is measured at each instant of time), Eq. 2 can be rewritten as:

$$1/\tau = 1/\tau_{\text{eff}} - 1/\tau_{\text{Auger}} = 1/\tau_{\text{SRH}} + 2S/W \quad (3)$$

If it is further assumed that all recombination occurs at the surface and none occurs within the crystal bulk ($\tau_{\text{SRH}} \rightarrow \infty$), then an upper bound for the surface recombination velocity, S_{max} , can be determined as:

$$S_{\max} = \frac{1}{2} (W/\tau) \quad (4)$$

Since high-lifetime FZ wafers were used, the true value of surface recombination velocity is expected to be only marginally lower than this upper bound. This expectation of high lifetime is checked by PCD lifetime measurements with iodine-methanol surface passivation.

Experimental Results

PCD lifetime measurements and analysis were done using the Sinton WCT-boule tester [5]. A linear fit of Auger-corrected lifetime as a function of excess carrier density was used to determine the lifetime at zero excess carrier density which is cited in this study. An example is shown in Fig. 1, in which data are accumulated over an excess carrier density ranging from $1.8 \times 10^{15} \text{ cm}^{-3}$ to $1.2 \times 10^{16} \text{ cm}^{-3}$. The intercept of the fitted curve at $\Delta n = 0$ is 1110 s^{-1} , corresponding to a lifetime of $903 \text{ } \mu\text{s}$. From Eq. 3 it can be seen that no variation of lifetime with excess carrier density is considered, and the shallow slope of Fig. 1 indicates this is approximately true.

Fig. 1. Plot of Auger-corrected inverse lifetime versus excess carrier density for sample T3316-pFZ showing a τ value of $903 \text{ } \mu\text{s}$ at $\Delta n=0$, corresponding to $S_{\max}$ of 17 cm/s .

Results are summarized in Table 1. In addition to τ and $S_{\max}$ which is calculated from it, the Sinton tester also determines a value of Implied V_{oc} at one sun from the measured excess carrier densities. This parameter has been found to be a reliable indicator of potential V_{oc} in the finished cell. Measurements with a Bare Si surface are those for samples having only the very thin chemical oxide remaining after the RCA2 clean. The value of $S_{\max}$ for such a surface is quite high, while the same sample with iodine-methanol surface passivation has a very low value of $S_{\max}$ and a corresponding high lifetime. It is clear that measurable surface recombination is present for the thermally oxidized samples, and that the p-FZ sample suffered degradation in bulk lifetime as well. For the samples passivated with a-Si, the $S_{\max}$ values are quite low, comparable to those obtained with iodine-methanol, and give high values for Implied V_{oc} of approximately 700 mV .

Table 1. $S_{\max}$ and implied V_{oc} inferred from transient PCD lifetime data.

Sample ID	ρ (Ω -cm)	Thickness (μ m)	Surface	$\tau(\Delta n=0)$ (μ s)	$S_{\max}$ (cm/s)	Implied V_{oc} (mV)
n1-FZ	1.2	300	Bare Si	6	2600	532
n1-FZ	1.2	300	Iodine-Methanol	1530	10	690
n3-FZ	1.2	300	Thermal Oxide	241	64	650
n3-FZ	1.2	300	Iodine-Methanol	1340	12	690
p2-FZ	3.0	300	Bare Si	2	8900	501
p2-FZ	3.0	300	Iodine-Methanol	2080	7	700
p4-FZ	3.0	300	Thermal Oxide	81	60*	613
p4-FZ	3.0	300	Iodine-Methanol	114	-	634
T3300-nFZ	1.2	300	a-Si(i,n)/a-Si(i,p)	1200	13	694
T3316-pFZ	3.0	300	a-Si(i,n)/a-Si(i,p)	903	17	700

* S (not $S_{\max}$) calculated from thermal oxide and iodine-methanol data with 7 cm/s for iodine-methanol.

Summary

PCD lifetime studies on (100) polished FZ silicon wafers indicate an upper bound for surface recombination velocity of 64 cm/s for a chlorinated thermal oxide with FGA and 13 cm/s for HWCVD a-Si:H passivation on 1.2 Ω -cm n-type. These values correspond to Implied V_{oc} values of 650 mV and 700 mV, respectively, consistent with what is frequently achieved for V_{oc} in finished cells having these surface passivation layers. Values of 60 cm/s and 17 cm/s, respectively, were obtained for 3.0 Ω -cm p-type FZ silicon. An upper bound for surface recombination velocity associated with iodine-methanol chemical surface passivation as low as 7 cm/s was obtained, illustrating its value in facilitating accurate bulk lifetime measurements. The initial high bulk lifetime (1530 μ s) determined for n-type FZ silicon was essentially preserved through the 1000°C thermal oxidation for 150 min (1340 μ s). However, a corresponding high initial lifetime (2080 μ s) in p-type FZ silicon was not maintained through the same oxidation (114 μ s), presumably because of the formation of recombination centers involving boron complexes during oxidation.

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Reducing the Concentration of Interstitial Iron in Crystalline Silicon Solar Cells via Low ($\leq 500^\circ\text{C}$) Temperature Annealing

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Abstract

We demonstrate the effect of low-temperature ($\leq 500^\circ\text{C}$) annealing, guided by iron point defect time-temperature transformation (TTT) diagrams, to reduce iron point defect concentrations and hence improve solar cell device efficiencies, as proposed by M. D. Pickett. When a low-temperature annealing step is implemented after P-diffusion but before glass etch, the reduction in Fe point defect concentration can result in a significant J_{sc} -driven efficiency improvement. These findings raise interesting points: (1) as cell architectures improve, necessary reductions of $\text{Fe}_i\text{-B}_s$ to enable high J_{sc} may be achieved via this low-temperature annealing method; (2) the effect of SiN_x firing (typically between $400\text{-}500^\circ\text{C}$) must be re-evaluated, not only in terms of passivation, but also in terms of Fe point defect re-distribution; (3) contact metallization firing should be kept as short and as low-temperature as possible, to avoid the re-dissolution of precipitated iron; (4) even longer low-T annealing times may further improve solar cell devices; and (5) an optimum annealing temperature can be found for each transition metal species, guided by TTTs.

1. Introduction

In crystalline silicon photovoltaic devices, iron point defects can be a major cause of bulk minority carrier lifetime degradation, resulting in lower cell efficiencies. Interstitial Fe point defects in p-type Si are stable at room temperature, forming pairs with substitutional boron ($\text{Fe}_i\text{-B}_s$ pairs) [1]. Although the bulk solubility at room temperature of iron point defects should be $\sim 10^{-24}$ atoms cm^{-3} (as determined via extrapolation of high-temperature solubility data to room temperature [2]), in reality $10^{12}\text{-}10^{14}$ cm^{-3} $\text{Fe}_i\text{-B}_s$ exists in as-grown c-Si materials (Fig. 1). The reason for this is the large FeSi_2 nucleation energy barrier, which must be overcome for Fe precipitation to initiate [3].

Fig. 1: Reproduced from [4]. Iron-boron point defect concentrations for different as-grown c-Si materials, compared to total bulk Fe contents. Note that the solubility of iron point defects is $\sim 10^{-24}$ atoms cm^{-3} at room temperature, yet the actual concentration in solar cell materials is orders of magnitude higher, indicating a precipitate nucleation energy barrier.

High $\text{Fe}_i\text{-B}_s$ concentrations in finished solar cells result in low bulk minority carrier diffusion lengths, hence low short circuit currents and efficiencies [5]. Consequently, in the finished device it is important to have $\text{Fe}_i\text{-B}_s$ concentrations $\leq 10^{10} \text{ cm}^{-3}$ to enable 100 μs minority carrier lifetimes (an enabler for 18+% efficient cells). While gettering techniques are capable of reducing $[\text{Fe}_i]$ to these levels in high-purity, single-crystalline silicon wafers, such low $\text{Fe}_i\text{-B}_s$ levels are difficult to achieve in materials with higher as-grown metal concentrations and structural defects, such as multicrystalline silicon.

2. Reducing Iron Point Defect Concentrations Using “TTT Diagrams”

Recently, M. D. Pickett proposed to reduce $[\text{Fe}_i\text{-B}_s]$ in solar cell devices by the aid of time-temperature transformation (TTT) diagrams [3], which are well known in metallurgy, as well as in the integrated circuit community. The premise is that an optimum temperature for iron precipitation ($\text{Fe}_i\text{-B}_s$ reduction) can be found, for a given structural defect density and bulk $\text{Fe}_i\text{-B}_s$ concentration, by identifying a temperature sufficiently *low* to create a large driving force for Fe precipitation (i.e., supersaturation) to overcome the nucleation energy barrier, which at the same time is sufficiently *high* to allow Fe to diffuse to and aggregate at bulk or surface precipitates. For FZ-Si, this temperature is an astonishingly low 500°C [6].

In this contribution, we apply the idea proposed by M. D. Pickett [3] to multicrystalline silicon solar cell materials and devices. Firstly, we determine the optimum annealing temperature by measuring $\text{Fe}_i\text{-B}_s$ concentrations in as-grown and post-annealed devices, essentially reproducing Henley’s TTT diagram [6] for mc-Si. Using a Semilab microwave photoconductivity decay ($\mu\text{-PCD}$) mapping tool equipped with a flash lamp for $\text{Fe}_i\text{-B}_s$ pair dissociation, iron-boron pair concentrations were measured before and after annealing for 30 min. at temperatures between 300°C and 600°C followed by quenching to room temperature. It was found that the optimal temperature for $\text{Fe}_i\text{-B}_s$ pair reduction in as-grown mc-Si occurs between 400°C and 500°C (Fig. 2), surprisingly close to previous studies concerning FZ-Si.

Fig. 2: Time-temperature transformation diagram of iron point defects in multicrystalline silicon, shown only at one time (30 min). Each data point represents one wafer; three wafers were annealed at each temperature. Despite the scatter, a maximum reduction in $\text{Fe}_i\text{-B}_s$ can be determined between 400°C and 500°C.

3. Efficiency Improvements Using “TTT Diagrams”

To test whether this effect has any impact on actual solar cell efficiencies, we implemented the low-temperature anneal (500°C, 30 min.) immediately after P-diffusion annealing but before the glass etch, to enhance Fe diffusion to and precipitation at the glassy layer (which is subsequently etched off). While the annealing temperature is sufficiently high to allow Fe to diffuse, it does not affect the distribution of P in the emitter. Note that this post-diffusion anneal is similar in nature to that proposed by

Manshanden and Geerligs [7], albeit at a much lower temperature guided by the TTT diagram. Batches of wafers were processed into cells as shown in the 2-by-2 matrix below, to test the effect of low-temperature annealing in combination with feedstock quality.

	Wafers From High-Purity Feedstock	Wafers From Fe-Rich Feedstock
Low-T Gettering (500°C, 30 min, implemented after P-diffusion)		
Control (standard cell processing)		

Illuminated IV-curve measurements were employed to determine device efficiencies and short circuit currents for all solar cells described above. The results, shown in Fig. 3, demonstrate that low-temperature gettering can indeed lead to J_{sc} -driven efficiency improvements in wafers grown from Fe-contaminated feedstocks.

Fig. 3. Comparison of (a) short circuit currents and (b) solar cell efficiencies for a batch of wafers annealed at low temperature after P-diffusion but before glass etch (labeled “Low-T Gettered”), and a control batch processed simultaneously (labeled “Control”). All wafers shown above were grown from an Fe-rich feedstock. Note the pronounced J_{sc} -driven efficiency improvement due to low-temperature gettering.

Despite the statistically significant increase in efficiency noted for Fe-contaminated feedstock, little to no effect of low-T gettering is observed in wafers grown from “high-purity” feedstock. This is another clear indication that the low-T gettering is indeed manipulating Fe_i distributions. If one were to implement a high-efficiency device architecture during cell processing, the authors believe that one could expect cell efficiency to be more sensitive to bulk minority carrier lifetime (as opposed to being limited by other parameters, such as surface recombination and series resistance). In this case, a beneficial effect of low-temperature annealing may be observed even for high-purity feedstock.

4. Implications of Low-Temperature Annealing on Solar Cell Fabrication

The implications of low-temperature annealing on cell fabrication are multiple: Firstly, as industrial solar cell architectures (efficiencies) improve, they will become more sensitive to bulk minority carrier lifetime, and as such, residual Fe_i - B_s concentrations. Low-T gettering, as demonstrated herein, has the potential to further improve the performance of **high-efficiency solar cell devices**, possibly even those made of “high-purity” feedstocks.

Secondly, the effect of **hydrogen passivation** must be re-evaluated, in the context of redistributing Fe point defects. While other passivation processes are likely to occur, part of the beneficial impact of H-passivation during SiN_x firing (typically performed between 400°C and 500°C) on mc-Si material may simply be due to the re-distribution of Fe point defects. Obviously, this effect is expected to be strongest in material with high as-grown Fe point defect concentrations and sub-optimal P-diffusion annealing. In a sense, SiN_x firing, by virtue of its temperature alone, may be able to “compensate” for sub-optimal processing and material quality.

Thirdly, the influence of the last high-temperature step of solar cell processing, i.e., **contact metallization firing**, must be carefully evaluated in terms of dissolving and re-distributing precipitated Fe atoms. For this reason, short firing times and low temperatures are preferred. Alternatively, if pn-junction spiking can be avoided, low-temperature annealing of fully-processed solar cells may have a similar beneficial effect [8].

Fourthly, we demonstrate the significant effects of a 30 min. low-temperature annealing step. However, prior results demonstrate an even greater effect for **longer annealing times**. It can thus be expected that longer anneals may result in even lower Fe_i-B_s concentrations, and hence, greater J_{sc}-driven efficiency improvements.

Lastly, the TTT diagram approach can and should be applied to other impurity species in mc-Si that are more recombination active as distributed point defects than in precipitates. Note that the optimum annealing temperature is a function not only of element-dependent properties such as diffusivity and solubility, but also the concentration of a given metallic species and the density of heterogeneous nucleation sites. Nevertheless, one could envision a cooldown from P-diffusion gettering as consisting of multiple plateaus, to force precipitation of transition metal species.

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Cross-sectioning Si Solar Cells: Mechanics of Polishing

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ABSTRACT

A damage-free polishing method has been developed to prepare large cross sections of a solar cell for optical- and electron-beam analyses. The sample is held by wax inside a chuck and its edge is sequentially polished by progressively reducing the grit sizes. The final polishing is done by chemical mechanical polishing. This polishing procedure produces a high-quality, flat edge, with excellent interfaces between metal contacts and the Si cell. The planarity of the wafer edge makes it possible to perform a variety of AFM, CFM, SKPM, and other scanning analyses over large areas. The large cross section is very valuable for optical examination of various regions such as metal fingers, BSF, and metal penetration into the front for statistically meaningful analyses. We present results of the cross-sectioning and discuss issues related to cross-sectioning large regions of a solar cell (or any other multilayer device).

INTRODUCTION

Fabrication of a high-efficiency solar cell requires a very precise control of various reactions between the materials that form the solar cells. The reactions of the most interest involve diffusion of the dopant (such as P diffusion into P-type Si), interaction of front metallization with the N⁺ region, alloying of Al to form a back-surface field, and interactions between SiN:H and Si. In most cases, these interactions can be studied by depth profile of a specific element by methods such as SIMS, Auger, EMPA, or EDX using the cell surface itself. In other cases, the detailed information can only be obtained by cross-sectioning the wafer or the device and performing high-resolution imaging and analyses. The greatest benefit of this technique is that it allows optical investigation of a relatively large length of cross-sectional samples. This can prevent the generalization of the results of a small-area sample that could lead to conclusions that don't represent the bulk cell properties.

In many cases, one can cleave the wafer for cross-sectional investigations. This approach sometimes works well for single-crystal wafers and can be useful for examination techniques that use large beam sizes such as Auger or microprobe analyses. However, sample cleaving can produce fracture patterns that can interfere with analyses such as AFM, CAFM, and other high-resolution methods. Cleavage can produce very undesirable surface morphologies for multicrystalline Si (mc-Si) wafers or devices that have a multilayer structure with different materials. There are several issues with cross-sectional polishing of a multilayer device. Two major problems in polishing a multicomponent sample are: (i) the polishing rate of each component can be different, and (ii) the interface can exhibit "grooving" because of mechanical stresses and differences in the electrical potential between each material.

Chemical mechanical polishing (CMP) has been successfully used for surface polishing single- and multicrystalline Si wafers [1,2]. It has also been used for cross-sectioning single-crystal and mc-Si wafers. For this purpose, a mounting mechanism that avoids the complications of epoxy by using a low-temperature wax and a mechanism that simultaneously provides good support to the sample edge is desired [3,4]. More recent work has adapted this technique for the cross-sectional CMP of a solar cell made of several different materials. In this work, it was shown that polishing parameters such as pressure, slurry flow, polishing time, and edge support need to be carefully controlled in order to obtain a good-quality edge [5]. Here we describe an extension of this approach that allows relaxation of many polishing requirements and is suitable for cross-sectioning large lengths of wafers/solar cells at any step of the solar cell fabrication process. In this approach, the wafer or device is cut along the edge to be cross-sectioned, mounted in a special fixture, and then sequentially polished by progressively reducing the grit sizes. The final polishing is done by CMP.

POLISHING PROCEDURES

The solar cell to be cross-sectioned is cut into 1.6" x 1.6" samples with straight edges, using either a laser scribe or a dicing saw (Disco Automatic dicing saw – DAD-2H/6T). The sample is mounted in a chuck (shown in Fig. 1a). A schematic cut section of the sample holder is given in Fig. 1b and described in detail in reference [3].

Fig. 1. A photograph and a schematic of the sample mounting chuck

To mount the sample, the spring-loaded pressure plunger is pulled out and the sample is placed inside the sample chamber so that it is sitting on top of the four pads with about 0.1 mm protruding from the bottom of the chuck; then the plunger is released to support the sample. Pieces of wax (Crystalbond 509, M.P. of 120 °C) are then introduced to the funnel-shaped side of the chuck, which also has two circular openings for the dual heaters (typically 200 W power). As the wax seeps out from the bottom of the chuck, it forms a thick layer around the protruding edge of the sample. The heaters are then taken out from the chuck, and wax is allowed to slowly cool.

The wax around the sample edge is then formed using a specially modified soldering iron tip, and then it is ready for polishing. The wax meniscus mechanically supports the edge, which helps prevent rounding and maintains edge quality, as illustrated in Fig. 2. A good wax support in the form of a plateau around the front contact and SiN_x is shown in Fig. 3.

Fig. 2. Schematic of sample protruding out of chuck with wax support

Fig. 3. As-cut sample after wax mounting

The solar cell edge is mechanically polished on a laboratory-style polishing machine. The polishing grit is mixed in a solution of ethylene glycol (EG) and distilled water (40:60) and dripped onto the polishing pad. This solution composition with EG was done to overcome some of the problems we encountered when grit was mixed with water. The problems included:

1. Build up of wax on the sample edge and around it during polishing
2. Discoloration resulting from gamma alumina in a water-based solution.

The initial polishing is done with a de-agglomerated alpha alumina (Buehler Micropolish II) to remove about 5 to 10 μm of the edge (primarily the saw damage). After this process, the pad is cleaned and 0.3 microns of alpha alumina is used to remove about 2 to 5 μm of the edge. Next, the pad is again cleaned and polishing is continued with 0.05 microns of gamma alumina. The final step is CMP, which removes residual damage from 0.05- μm grit and also removes surface contaminants from the sample. In this method, CMP is done only for a very short time, which circumvents problems of differential polishing rates of different materials. The sample is then demounted and edge is cleaned. To further examine the quality and characterize the different layers of the cross-section, optical microscope images are acquired and analyzed.

Better results of cross-sectioning can be obtained by replacing the Suba IV polishing pad with a slightly harder and denser pad but with a different surface texture, such as a Suba 1200. Because of higher hardness and lower compressibility, it offers a flatter surface during polishing with a concomitant flatter cross section.

(a)

(b)

Fig. 4. Comparison of edge rounding with (a) Suba IV pad and improved flatness with (b) Suba 1200 pad

RESULTS AND DISCUSSION

Figure 5a is a Nomarski photo of the edge after 15 minutes of polishing with 1.0-micron grit and a 60/40 distilled water/ethylene glycol solution on a Suba 1200 pad. Saw marks have been completely removed, but some scratches due to 1- μm grit can be seen. Figure 5b is of the same finger after 0.3-micron grit polishing. An improved flatness can be observed (indicated by the reduced number of color bands). Figure 5c is the photo after 0.05- μm grit polishing. Figure 5d is a Nomarski photo after CMP showing one color band across the entire photo. From these photos, we can see that as polishing progresses, flatness increases.

Fig. 5. Progression of sample at different grit sizes: (a) after 15 min of 1.0- μm polishing (b), 2 hr of 0.3- μm polishing (c), 3 hr of 0.05- μm polishing, and (d) 20 s of CMP on Suba IV.

Figure 6 compares SEM photos of cleaved samples with polished ones. Cleaved samples (6a, c, and e) have fracture marks and the surface is non-planar, whereas polished samples (6b, d, and f) have almost planar surfaces with no fracture marks. The glass frit and particles can be distinguished in Fig. 6b. Figure 7 shows another example of the quality after polishing of the front and back contact of the cell.

20 μm
(a)

20 μm
(b)

1 μm
(c)

1 μm
(d)

200 nm
(e)

200 nm
(f)

Fig. 6. SEM comparison of (a, c, e) cleaved samples with (b, d, f) cross-sectioned samples.

Fig. 7. SEM images of (a) back Al metallization and (b) front Ag of a standard solar cell

CONCLUSION

We have developed a technique to cross-section large lengths of wafers/solar cells at any step of the solar cell fabrication process. This method produces large solar cell samples that can be used in performing a variety of AFM, CFM, and other scanning analyses. This polishing method produces a flat, high-quality edge with excellent interfaces between metal contacts and the Si cell. The large cross section is very valuable for optical examination of various regions such as metal fingers, BSF, and metal penetration into the front for statistically meaningful analyses. Various issues and their impact related to cross-sectioning large regions of a solar cell (or any other multilayer device) were presented.

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Surface Photovoltage Technique: Renewed interest in Si-PV Measurements and Diagnostics

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ABSTRACT

The surface photovoltage (SPV) technique is a very simple way to measure minority carrier diffusion length—a parameter that directly relates to solar cell performance. However this measurement is typically done at an injection level, which is much lower than the injection level at which a solar cell operates. This technique can be enhanced for the silicon PV applications by using diffused samples, diode arrays, or finished solar cells with constant background illumination and computer automation. This technique is very valuable for making measurement of Fe in Si. These applications are briefly discussed in this paper.

INTRODUCTION

Surface photo-voltage (SPV) technique was one of the earliest methods for measurement of minority carrier diffusion length (L) in Si. It was used to determine the quality of photovoltaic (PV) Si wafers and perform studies on the effect of impurities and other crystal defects on L , and on the solar cell performance. The SPV technique takes advantage of an inversion type of layer, which may either exist or can be readily formed by a proper wafer preparation. When a wafer with an inversion type of surface layer is illuminated with light, it produces a photovoltage. A measurement of the spectral dependence of this photovoltage can yield information to determine L (as discussed in the next section). Because the photovoltage can be produced by chopped light, one can use capacitive contact to measure the generated ac voltage. This makes the measurement rather easy and non-contact.

Because the minority carrier diffusion length is directly related to the cell performance, SPV technique is very useful for solar cell applications. Another advantage of SPV technique is that one can use a constant SPV mode (as described below) in which the measurement is insensitive to the surface recombination (if the wafer thickness is larger than $4L$). This is a major advantage because all other technique for measuring minority carrier lifetime are very sensitive to the surface recombination. However, because SPV measurement is made under low intensity light (i.e., low injection level) there is some concern about the pertinence of SPV-measured values of L to the solar cell, which operates at an injection level of about 2×10^{15} carriers/cm². This paper presents a number of applications where SPV measurement is very valuable for Si solar cell

diagnostics. We also present a potential approach of making light-biased measurements on wafers with junctions, solar cells, and on diode arrays (a technique for characterizing solar cell substrates and for studying influence of impurities and defects on the solar cell performance).

SPV METHOD FOR MEASUREMENT OF L

Figure 1 is a schematic of a typical SPV experimental setup. In this setup, the light emanating from a microscope illuminator is filtered with a narrow-band filter, chopped, and then focused on the wafer through a transparent electrode. Typically a filter wheel, which has 7 filters in the wavelength range of $1.00\ \mu\text{m}$ to $0.8\ \mu\text{m}$ is used. Thus, the wavelength of the illuminating light is changed by rotating the filter wheel. The wafer is placed on a grounded metal chuck and the signal produced by the chopped light is capacitively coupled and fed into a lock-in amplifier.

Figure 1. A schematic of an SPV setup.

Figure 2. Typical SPV plot of photon flux Vs. $1/\alpha$

The value of L is determined as follows: The sample is sequentially illuminated with filtered light, and the light intensity (as number of photons) is monitored. The light intensity required to keep the SPV signal constant at each illumination is measured. A plot of light intensity Vs. inverse absorption coefficient ($1/\alpha$) is made, as shown in figure 2. The intercept of the line with the ($1/\alpha$) axis gives the value of L .

In the rest of the paper we want to discuss some important details, which need to be addressed if SPV is to be usefully employed as PV characterization technique.

Effect of wafer thickness

It is known from the physics of the SPV technique that the measured value of L is accurate only if thickness of specimen is larger than $4L$. For thinner specimens, the effective measured diffusion length, L_{eff} , depends on the surface recombination velocity, S , and is different than bulk diffusion length L .

The relation between L , L_{eff} , and S is given by the following expression:

$$\Phi \propto 1/\alpha_\lambda + L_{eff}$$

$$\Phi \propto \left[\frac{\alpha_\lambda \tau}{\alpha_\lambda^2 L^2 - 1} \left(\frac{A}{C} + \frac{B}{C} \exp(-\alpha_\lambda d) - 1 \right) \right]^{-1}$$

$$A = (S^2 * L/D + S * \alpha_\lambda * L) * \sinh(d/L) + (S + \alpha_\lambda * D) * \cosh(d/L)$$

$$B = (S - \alpha_\lambda * D)$$

$$C = (S^2 * L/D + D/L) * \sinh(d/L) + 2S * \cosh(d/L)$$

where Φ denotes the effective photon flux responsible for carrier generation, D is minority carrier diffusivity, S represents surface recombination velocity (same for both sides), d is wafer thickness and α_λ indicate wavelength-dependent absorption coefficient.

The relation between L_{eff} vs. specimen thickness, d , is plotted in Figure 3, for a wafer whose actual bulk diffusion length, L , equals to $614 \mu m$. It can be observed in the figure that if d is lower than $2.5L$, L_{eff} starts to diverge from L . In a special case when d equals to L , the measured L_{eff} varies from 300 to 900 μm , depending on surface recombination velocity. It is also clear that generally for thin samples L_{eff} can be larger or smaller than L . Thus, it can be stated that in such case an accurate value for S on both sides on the wafer need to be known in order to obtain L .

Figure 3. L_{eff} Vs wafer thickness for different surface recombination velocities.

Measurements on solar cells and diode arrays

SPV technique can also be applied to wafers that have one-sided diffusion and after all other processes including the finished solar cell. One simply uses either the open circuit voltage (if there is no metallization) or short circuit current (after metallization) as the signal instead of SPV. Although, this configuration is somewhat different from a wafer because of the presence of a finite thickness of junction and its associated depletion region, this effect can be negligible for nearly all practical situations. Likewise, this technique can be applied to diode arrays used for substrate characterization. Figure 4 is a minority carrier diffusion length map of a diode array fabricated on a mc-Si wafer.

Figure 4. A L-map of a mc-Si sample with 100 mil diodes fabricated on it. Measurements were made on the diodes.

Corrections for surface properties

To accurately perform SPV test, one needs to know the absorption as a function of depth below the surface of the wafer for the wavelengths used in the measurement. For a planar wafer, it is sufficient to know the absorption coefficient, α . However, for a wafer with rough or textured surface the absorption is a function of surface condition as well as specimen thickness. Likewise, if a cell has an antireflection coating and back metallization, their influence on the measurement must be included. The absorption can be calculated theoretically using *PV Optics* code.

Fe diffusion

A very important application of SPV method is determination of Fe content in p-type silicon wafers. The sensitivity of SPV is very high; concentrations in the range of $10^{11} - 10^{13} \text{ cm}^{-3}$ can be measured. In measurement, one exploits difference in the L values between the interstitial Fe and Fe-B pairs. Figure 5 shows measurements of Fe concentration in a number of samples, which were diffused with Fe under different conditions.

Figure 5. Measured Fe concentrations for different samples. See text for explanations.

6. Automated measurement

We have fully automated the SPV measurement system using LabView. Figure 6 shows a flow chart for LabView control.

Figure 6. A flow chart for automated measurement of L using a Labview control

We have shown some applications of the SPV technique for PV-Si. Use of biased light to operate at higher injection levels and automation of the measurement make this technique well suited for PV diagnostics.

ELECTRICAL INVESTIGATIONS ON SiC PRECIPITATES FOUND IN BLOCK-CAST SOLAR SILICON

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Abstract In multicrystalline silicon solar cells linear shunts were found, which were caused by silicon carbide precipitates. These silicon carbide precipitates have been isolated from the bulk material to investigate their electrical properties and to investigate the shunt mechanism. Current-voltage characteristics and four-point probe measurements were performed on the silicon carbide precipitates. In addition to the investigations on isolated silicon carbide precipitates, current-voltage and capacitance-voltage characteristics were measured on precipitates, which were still embedded in the silicon bulk material. The results show that the silicon carbide precipitates are highly n-conductive, and a simulation of the shunt shows that the shunt current flows inside the silicon carbide material. Photoluminescence and cathodoluminescence measurements on the silicon carbide precipitates reveal that they emit green light and therefore should be detectable by luminescence methods.

1. Introduction

In solar cells, which were made of block-cast multicrystalline (mc) silicon, one finds shunts decreasing the efficiency of the affected solar cells. A well-known technique to detect shunts in every kind of silicon solar cells is dark lock-in thermography DLIT¹. Briefly, a pulsed bias of 0.5 V (which corresponds approximately to the working point of a commercial silicon solar cell) is applied to the cell. A thermo camera detects local heat sources, which occur on the cell. These local heat sources correspond to shunts. Different shunt types, which were detectable with LIT are known and were described elsewhere². A so-called linear or ohmic shunt is given, if the signal, detected by the camera at 0.5 V forward bias at a certain area on the cell, has the same magnitude as the signal, which is detected at -0.5 V reverse bias at the same area.

In further studies^{3,4} it was found that in block-cast multicrystalline silicon for solar cells several precipitates occur and are responsible for shunting. We have found silicon carbide (SiC) cluster, silicon nitride (Si₃N₄) rods and SiC filaments. There are SiC filaments, which grow from SiC clusters within the crystallites, and SiC filaments, which grow in grain boundaries.

Al-Rifai et al.³ showed that SiC filaments may cause linear shunts, but nothing was known about the electrical properties of the SiC and the linear shunt mechanism at this stage of investigation. It was assumed that an inversion channel is formed at the interface between the solar cell substrate material (p-type silicon) and the SiC precipitates² and that the shunt current flows in this inversion channel, but the correct shunt mechanism was not clear so far.

The main aim of this paper is to describe investigations of the electrical properties of SiC precipitates in mc solar silicon, to describe a model of the linear shunt mechanism and to show a new possibility how to detect SiC precipitates in mc silicon wafers.

2. Experimental

The first problem to investigate the SiC precipitates separately is to isolate them from the bulk material. To find the precipitate positions we use DLIT to detect all linear shunts in mc Si solar cells. The shunted areas of the cell are cut out and polished from both sides. After that we image the sample with an infrared microscope and can identify different precipitates, which are shown in Fig 1a).

To perform different electrical measurements on the precipitates, it was necessary to isolate them from the bulk. For that we use a 1:3 mixture of HF (50%) and HNO₃ (65%), where we put in the Si sample containing the precipitates in a Teflon funnel. Since SiC and Si₃N₄ are chemically resistant against the HF-HNO₃ mixture, they remain in the acid mixture and can be separated from the liquid. A scanning electron microscope (SEM) image of the different precipitates is shown in Fig. 1b).

The second problem to investigate the SiC precipitates was that their diameter is in the range of some micrometers. For this we use two nanomanipulators within a SEM. These manipulators give us the opportunity to probe the precipitates very carefully. Each manipulator is equipped with a platinum-iridium (Pt-Ir) tip to contact the SiC filaments electrically. The manipulators can be also equipped with a four-point probe to get information about the doping type of the precipitates. To get the voltage-current (I-V) characteristics we use a picoamperemeter with an internal voltage source (Keithley 6487, ≤ 2 fA noise). For the voltage-capacitance (C-V) measurements we use a Booton 7200 capacitance meter and the four-point measurement was performed by a Veeco FPP-5000. Electron beam induced current (EBIC) measurement on SiC filaments, which are still embedded in Si bulk material, were performed with a self made amplifier and show us the electronic structure of the heterojunction SiC – Si. To test the ability of the detection of SiC precipitates in Si wafers by luminescence measurements, we used cathode luminescence (CL) measurements in a SEM and performed photo luminescence (PL) measurements in a Raman spectrometer.

Fig. 1: SiC and Si₃N₄ precipitates found in a mc Si solar cell wafer after polishing the shunted area of the cell a), SEM image of SiC filaments, SiC cluster and Si₃N₄ rods after isolation from the bulk b).

3. Results

The two-point probe measurements of the SiC filaments, which can be seen in Fig. 2a), shows a linear behavior, and a resistance in the order of 15 Ω can be calculated from the slope of the curve (Fig 2b). By using the geometric dimensions of the SiC filaments, the specific resistance ρ can be calculated to be $\rho = 0.002 \Omega\text{cm}$. To find out the doping type of the SiC filaments, a four-point probe measurement was performed on several SiC filaments (see Fig. 2c). It turns out that all the SiC filaments are n-type doped. Using ρ and a carrier mobility of 400 V/cm² for the electrons, the carrier density of the SiC can be estimated to be in the order of $8 \times 10^{18} \text{ cm}^{-3}$.

Fig. 2: Two-point probe measurement of a SiC filament with two Pt-Ir tips a), I-V characteristic of the SiC filament b), and four-point probe measurement of a SiC filament c).

Since the SiC filaments are embedded in the p-type solar cell material, it would be interesting to measure the electrical behavior of the heterojunction n-SiC to p-Si (here, n stands for n-type doped and p for p-type doped material). Figure 3c) shows the I-V measurement of the heterojunction. The I-V curve is rectifying and behaves like a p-n junction, as expected. By performing a C-V measurement on the heterojunction and extrapolating the $1/C^2$ -view of the C-V curve to $1/C^2=0$, the diffusion voltage was determined to be $U_D = 1.1$ V. In Fig. 3b) an EBIC image of the interface between n-SiC and p-Si is shown. The EBIC signal at the interface leads to the conclusion that there is a barrier for the electrons.

Fig. 3: SEM image of a contacted SiC filament, which is still embedded in the bulk a), EBIC image of the same SiC filament b), and I-V & C-V characteristics of the system SiC – Si with simulated curves c).

We performed cathodoluminescence (CL) and photoluminescence (PL) measurements to check whether the SiC filaments emit light. The image in Fig. 4a) shows SiC filaments, the corresponding CL measurement can be seen in Fig 4b). A broad peak of the CL intensity appears with a maximum at about 2.4 eV. In Figure 4c)-e) a PL measurement at a grain boundary, which contains SiC filaments, is shown. The PL intensity in the Si area is negligible, only the Si Raman shifted peak at 500 nm is observable, but the PL intensity of SiC the filaments is strong. A maximum of the PL intensity appears at 2.4 eV, which corresponds to a light wavelength of about 508 nm (green light) and is consistent with the CL measurement.

4. Discussion

Since the SiC filaments are highly doped and therefore highly conductive, they may cause ohmic shunts in solar cells by short-circuiting the emitter with the backside contact of the solar cell. We have to mention that the SiC is doped by nitrogen, which acts as a shallow donor in SiC. The existence of N in the material is proven by the appearance of Si_3N_4 precipitates in Si bulk material.

The question, whether the shunt current flows in the filaments or in an inversion channel around them², can be answered by simulating the electrical properties and electronic structure of the heterojunction and regarding the simulated band diagram. We simulate the I-V and C-V curves of the system n-SiC – p-Si with AFORS-HET⁵. In Fig. 3c) one can see a quite good

correlation between the measured and simulated I-V and C-V curves. With the parameter set, that shows this good correlation, we simulated the band structure of the heterojunction. It turns out that there is a very low positive conduction band offset at the interface. Since the barrier is very low (some ten meV) and very narrow, because of the highly doped SiC, the electrons can overcome or tunnel through this barrier very easily and no inversion channel will be formed on the interface between SiC and Si.⁶

Fig. 4: SiC filaments in a grain boundary a), and the corresponding CL spectra with a peak at 508 nm b), light microscope image of a grain boundary containing SiC filaments c), and the corresponding PL mapping d). In e) the PL spectra of the cross-marked points are shown. The PL spectra of the Si shows only the Si Raman peak (black dotted line), the PL spectra of the SiC filament (red solid line) shows a broad peak at 508 nm. For PL a Laser with $\lambda=488$ nm was used.

5. Conclusion

Ohmic, material induced shunts in mc Si solar cells are often caused by SiC filaments, which grow in mc Si blocks. The SiC filaments are highly n-doped by nitrogen and are highly conductive. Our model of the shunt mechanism shows that the shunt current flows in the SiC filaments. SiC filaments emit green light if they were excited by photons or electrons during CL or PL measurements. Therefore PL and CL measurements are methods to detect SiC filaments in mc Si wafers and maybe for avoiding shunts.

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SURFACE PASSIVATION OF HETEROJUNCTION SOLAR CELLS USING PECV- DEPOSITED HYDROGENATED AMORPHOUS SILICON OXIDE LAYERS

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ABSTRACT

The surface passivation properties of n-type crystalline silicon wafers by hydrogenated amorphous silicon sub oxide [a-SiO_x:H] films for use in hetero-junction (a-Si/c-Si) solar cells are analyzed. The a-SiO_x:H films are deposited by decomposition of silane (SiH₄), **carbon dioxide (CO₂)** and hydrogen (H₂) as source gases using plasma enhanced chemical vapor deposition (PECVD). A high-transparent window layer is obtained by adding oxygen to the a-SiO_x:H layers. Raman spectra reveal the existence of Si-(OH)_x and Si-O-Si bonds after thermal annealing of the layers, leading to a higher effective lifetime, as it reduces the defect absorption of the sub oxides. For n-type FZ material, lifetime values as high as 1890 μs are obtained, resulting in a surface recombination velocity $S_{\text{eff}} < 6.6$ cm/s. Solar cells, prepared with a-SiO_x:H for passivation on both wafer sides, reach a V_{oc} up to 675 mV, so far limited by a relatively low fill factor and high series resistance.

INTRODUCTION

In the research field of crystalline silicon (c-Si) solar cells, electronic surface passivation has been recognized as a crucial step to achieve high conversion efficiencies. The suppression of surface recombination by surface passivation is one of the basic prerequisites to obtain high efficiency solar cells. Thermally grown silicon oxide has shown excellent surface passivation properties, but it implies a high temperature application (~ 1050 °C). Low-temperature processing sequences are based mainly on passivation with silicon-nitride (Si_xN_y:H_z) [1], amorphous silicon films [2], amorphous silicon oxide [3], or amorphous silicon carbide [4] and stacks of those. Focusing on the junction fabrication techniques of a-Si/c-Si solar cells using a low-temperature PECVD technique, passivation of the contact and surface regions of the cell avoiding high-temperature cycling becomes an important issue. Hydrogenated amorphous silicon sub oxides (a-SiO_x:H) represent a material system suitable for this application. In this work, we investigate the applicability of a-SiO_x:H films as passivation layers. For comparison, intrinsic amorphous silicon films with no oxygen content are identically processed.

The film compositions and also the changes in the microscopic structure of the amorphous network upon thermal annealing are studied using Raman spectroscopy and SIMS measurement. To determine the passivation quality of the a-SiO_x:H films, laser-induced microwave-detected photo conductance decay (μ-PCD) provides a contactless measurement of the effective recombination lifetime of free carriers. Solar cells are prepared with amorphous hydrogenated silicon suboxides for passivation

of the crystalline FZ wafers with different thicknesses and are analyzed by light- and dark I-V measurements.

EXPERIMENTAL DETAILS

Figure 1 shows the structure of the heterojunction solar cells prepared. For measuring the lifetime, only a-SiO_x:H layers have been applied, equally treated on both sides of the wafer. The amorphous hydrogenated silicon sub oxides are PECV-deposited by decomposition of silane (SiH₄), hydrogen (H₂) and carbon dioxide (CO₂) at various gas compositions, deposition temperatures and times. The intrinsic a-SiO_x:H layers are deposited at a chamber pressure of 200 mTorr. Initially, the silicon

Fig. 1. Cross section of the heterojunction solar cell.

wafers are cleaned using the standard RCA procedure followed by a dip in fluoric acid (HF) prior deposition. The gas flow rates for SiH₄ and H₂ dilution has been kept constant at 20 sccm, while the CO₂ varied in the range of 0 – 50 sccm. The oxygen content and the resulting optical band gap E_{04} of these films are controlled by varying the CO₂ partial pressure $CO_2/(CO_2+SiH_4)$. For determination of E_{04} and the optical constants by spectroscopic ellipsometry, the films are deposited on top of thermal SiO₂ (1000 Å) onto c-Si wafers. Corning 7059 glass is used for deposition for micro-Raman spectroscopy. For lifetime measurements, 0.8 – 1.2 Ωcm n-type FZ silicon wafers of 300 μm thicknesses are used as substrates; for solar cell applications we used n-type FZ wafer with a resistivity of 0.01 – 0.02 Ωcm. By varying the SiH₄/CO₂ gas flow ratio, different oxygen concentrations can be achieved [5, 6]. All oxygen concentrations quoted in this paper – unless stated differently – refer to the ratio $r_{ox} = [CO_2]/([CO_2]+[SiH_4])$ in the feedstock during deposition in the PECVD setup. The concentration of carbon (C) and other impurities is assumed to be less than 1 at. % for samples investigated in this work.

RESULTS AND DISCUSSION

I. SURFACE PASSIVATION BY A-SiO_x:H FILMS

Investigations on PECV-deposited a-SiO_x:H films have been made measuring the carrier lifetime by the μ-PCD method. This method based on the charge carrier injection in semiconductor by irradiating a spot like area with a laser pulse and determination of the charge carrier concentration vs. time. The charge carrier concentration is estimated by microwave reflection. The relaxation constant is derived from non-equilibrium charge carrier bulk-lifetime. The simplified formula for a homogeneous, defect-free wafer with a spatially uniform carrier lifetime is given by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surf} + \tau_{diff}} . \quad \text{Eq. (1)}$$

Fig. 2. Effective lifetime as a function of oxygen content in the feed stock during decomposition (a) and as a function of deposition temperature (b).

For the calculation of S_{eff} , we assume that both surfaces provide a sufficiently low recombination velocity and have the same values ($S_{\text{eff}} = S_{\text{front}} = S_{\text{back}}$), as well as a symmetric sample structure. The main error in determining S_{eff} arises from the uncertainty in τ_{bulk} . Schmidt and Aberle [7] reported the lowest S_{eff} with 5.5 cm/s for a 1000 Ωcm n-type wafer, passivated with a PECVD SiN_x film. However, the uncertainty of S_{eff} could have been as high as 10 cm/s [8] depending on the value used for τ_{bulk} . Therefore, we calculate S_{eff} for the case that no Shockley-Read-Hall recombination occurs ($\tau_{\text{bulk}} \rightarrow \infty$).

The lifetime had been obtained by mapping the lifetime values on a circular area of 1 cm diameter in 1 mm steps and calculating the average value. Fig. 2 (a) shows our results for effective lifetime and the corresponding surface recombination velocity depending on the oxygen content in the gas flux during deposition. As seen from Fig. 2 (a), we achieve the highest effective lifetimes of 1200 ms for an oxygen content of $r_{\text{ox}} = 20 \text{ at. \%}$ (the deposition temperature has been 350 °C), resulting in a very low $S_{\text{eff}} \sim 8 \text{ cm/s}$. With higher oxygen content in the gas phase, the lifetime decreases. One possible explanation could be that even though we assumed the content of C below 1 %, C increases with increasing oxygen content from the carbon dioxide, resulting in a higher defect density. This will be proven in the following chapter dealing with SIMS measurements.

We found that subsequent annealing of the samples at 250 °C for 1 h in forming gas atmosphere drastically increases the effective lifetime. This might be (i) due to hydrogen saturation of Si dangling bonds at the a- $\text{SiO}_x\text{:H}$ surface, or (ii) due to a change in the microscopic structure of the amorphous network (cf. Raman analysis in the following chapter).

A variation of the deposition temperature (cf. Fig. 2 (b)) with this very $r_{\text{ox}} = 20 \text{ at. \%}$ showed an optimum at a heater temperature of 320 °C, leading to a substrate temperature in our PECVD setup of around 145 °C. A very high effective lifetime ($\tau_{\text{eff}} = 1890 \mu\text{s}$, leading to $S_{\text{eff}} < 6.6 \text{ cm/s}$) has been achieved for samples deposited with an oxygen content of $r_{\text{ox}} = 20 \text{ at. \%}$ and a deposition temperature of 320 °C after subsequent annealing at 250 °C. Thermal annealing at higher temperatures (60 min at 500 °C) leads to a drastic decrease of the effective lifetime for all samples the samples due to the effusion of hydrogen (not shown).

II. COMPOSITIONAL ANALYSIS

Secondary ion mass spectrometry (SIMS) has been carried out to analyze the composition of the a-SiO_x:H films. Explicitly, measurements of films with an oxygen content of $r_{\text{ox}} = 0$ at. %, $r_{\text{ox}} = 20$ at. % and $r_{\text{ox}} = 50$ at. % are compared and depicted in Fig. 3. We found that O is build into the amorphous network; with increasing O content in the feed stock during deposition, SIMS reveals an increasing oxygen content in the network. A higher oxygen content leads also too an increased deposition rate (from 3.0 Å/s up to 3.8 Å/s), indicated by the interface peaks. The pile-ups visible at the interface air/a-SiO_x:H and at the interface a-SiO_x:H/c-Si can be explained as segregation effects. Furthermore, the carbon fraction in the a-SiO_x:H films increases with higher CO₂ content during deposition. This result explains the decreasing effective lifetime with $r_{\text{ox}} = 50$ at. % (shown in Fig. 2 (a)); indicating a higher defect density.

Fig. 3. SIMS measurements of a-SiO_x:H layers deposited with oxygen contents in the feed stock during deposition of $r_{\text{ox}} = 0$ at. % (black lines), $r_{\text{ox}} = 20$ at. % (magenta lines) and $r_{\text{ox}} = 50$ at. % (orange lines).

As shown above (cf. chp. I), subsequent annealing of the samples drastically increases the effective lifetime. This might be (i) due to hydrogen saturation of Si dangling bonds at the a-SiO_x:H surface, or (ii) due to compositional changes in the microscopic structure of the amorphous network. In case of a-Si:H ($r_{\text{ox}} = 0$ at. %), the hydrogen content is roughly 12-14 at. % as reported by Janotta et al. [5, 6]. However, our silicon sub oxides contain a significant higher fraction of hydrogen. The Raman spectra around the 2000 cm⁻¹ band region show typical peaks for Si-H bondings (not shown) for all prepared samples. We thereby assume that the fraction of hydrogen in the films is sufficiently high to cover all dangling bonds and that no additional hydrogen from annealing in forming gas is build up in the amorphous network. Lattice distortions, such as SiO₂ or Si clusters, silicon dangling bonds, molecular hydrogen inclusions, or micro-voids with hydrogen terminated internal surfaces are likely to exist in our a-SiO_x:H samples. Examples are given in the following. In Fig. 4, the Raman spectra for the band region of 250 – 1700 cm⁻¹ - taken exemplarily of the sample with the best effective lifetime results - directly after deposition and after subsequent annealing for 1 h at 250 °C, are presented. Si-(OH)_x bonds appear at peaks at 920 cm⁻¹ and around 1079 cm⁻¹, which agree well with the results shown in [10, 11]. Furthermore, Si-O-Si bonds occur around 820 cm⁻¹ for a-SiO_x:H films, whereas the sample containing no

Fig. 4. Raman spectra of $a\text{-SiO}_x\text{:H}$ films after deposition compared to spectra after post-annealing at 250 °C.

oxygen ($r_{\text{ox}} = 0$ at. %) (not depicted) does not show any compositional changes due to thermal annealing in the microscopic structure. Raman spectra for samples annealed at higher temperatures ($T = 500$ °C for 1 h) exhibit significantly lower Si-(OH) or Si-O-Si peaks for all samples (not shown). Effusion of hydrogen at temperatures above 400 °C might be the reason, as reported by Park et al. [9].

The optical band gaps E_{04} strongly depend on the oxygen content and steadily rise with increasing O from 1.9 eV up to 2.4 eV for 50 at. % O. Thermal annealing at 250 °C does not noticeably influence the band gap, but annealing at higher temperatures (500 °C) leads to a decrease of E_{04} , which can be as well attributed to the effusion of hydrogen.

III. SOLAR CELL RESULTS

It is known that heterojunction solar cells, compared to conventional p-diffused solar cells, feature a lower V_{OC} and fill factor. This appears to be caused by recombination processes throughout the depletion region at the a-Si/c-Si junction. Moreover, mid-gap states exist in the doped a-Si emitter - this possibly increase the leakage current by tunneling process. Light- and dark I-V measurements of our heterojunction solar cells (their structure is given in Fig. 1) has been carried out and are shown in Fig. 5. We found from the analysis of the dark characteristics that we can reduce the backward current density by 2 orders of magnitude when inserting $a\text{-SiO}_x\text{:H}$ films for passivation. Looking at the light characteristics in Fig. 5, the suppression of the backward current density improves the V_{OC} (here: up to 675 mV) and hence the solar cell performance.

However, our thin intrinsic films absorb light but lacks electronic quality – if used in the front side, it absorbs but the thereby generated free carriers are not collected. Therefore it reduces the total short current of the device. Secondly, a high resistivity of our $a\text{-SiO}_x\text{:H}$ hampers the current transport. A decrease of the fill factor presumably is caused by high series resistance and an increased diode ideality factor. Therefore, it is very important to determine the optimum film thickness which is in good agreement with light absorption, electronic quality and passivation quality.

Fig. 5. Light (a) and dark (b) I-V characteristics of solar-cell with different passivation layer thickness of the a-SiO_x:H (structure given in [Fig. 1]). For comparison, a similar solar cell without passivation ($r_{\text{ox}} = 0$ at. %) is given.

CONCLUSIONS

We investigated a-SiO_x:H films deposited in PECVD depending on the oxygen content and the deposition temperature. We found that the post-annealing at 250 °C leads to a generation of Si-(OH) and Si-O-Si bonds. After thermal annealing of those films, we achieved lifetime values on n-type FZ material, passivated by a-SiO_x:H films ($r_{\text{ox}} = 20$ at. %, deposition temperature = 320 °C), as high as 1890 μs ($S_{\text{eff}} < 6.6$ cm/s, note $\tau_{\text{bulk}} \rightarrow \infty$). Solar cells prepared with those a-SiO_x:H films showed V_{oc} up to 675 mV. The suppression of the backward current indicates that a-SiO_x:H efficiently passivates the a-Si/c-Si hetero-interface.

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SIMULATION OF INTERFACE STATES IN a-Si:H/mc-Si HETEROJUNCTION SOLAR CELLS

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ABSTRACT

The impedance, R_s and C_s , of a heterojunction solar cell based on a multicrystalline substrate is measured as a function of frequency. In contrast to the case of conventional monocrystalline base material, an additional signal appears in the $R_s(f)$ and $C_s(f)$ dispersion. The curves are reproduced with an AFORS-HET simulation. A 0.8 nm thick interface layer with a high defect density is introduced for this purpose. An acceptor-type trap with a total density of $1.375 \cdot 10^{20} \text{ cm}^{-3}$, a Gaussian distribution with a center position of $E_t - E_V = 0.6 \text{ eV}$ and a half-width $\Delta E = 0.14 \text{ eV}$, and symmetrical capture cross sections $\sigma_n = \sigma_h = 5 \cdot 10^{-16} \text{ cm}^2$ is found. The width of the parameter window is extremely narrow. The fit data are compared to those of an earlier network analysis.

INTRODUCTION

The characterization of several devices by admittance or solely capacitance measurements dates back to the seventies of the last century [1-3]. A variety of measurement tools and techniques has been developed and a lot of information on the substrates and their defects has been obtained. In the meantime the solar cell becomes of interest due to its increasing economic potential. Thus quite a few publications are found in which capacitive measurements are carried out [4-6]. In this work we deal with a special solar cell, namely a heterojunction based on multicrystalline silicon.

The measured R_s , C_s dispersion curves are analyzed by means of an AFOTS-HET [7] simulation. AFORS-HET is a finite-element code which reproduces all kinds of solar cell characteristics, among them the impedance as a function of frequency. A prerequisite for a successful fit is the proper choice of the trap densities and distributions. However, there is also another approach to these data, namely a network analysis. This approach has been used in an earlier publication [8] and the results will be compared.

EXPERIMENTAL

Block cast boron doped Solsix multicrystalline silicon of 0.5 to 2.0 $\Omega \text{ cm}$ nominal

Fig. 1 - Cross section of the heterojunction solar cell

resistivity is used as starting material. The supplier is Deutsche Solar. According to the Irvin curve, a doping level of $N_A = 7 \cdot 10^{15}$ to $4 \cdot 10^{16} \text{ cm}^{-3}$ is expected. The capacitance simulation requires $N_A = 1 \cdot 10^{16} \text{ cm}^{-3}$. After an RCA cleaning a 10 nm n-type a-Si layer is deposited by PECVD. 80 nm thick indium tin oxide (ITO) is used as an antireflection coating of low lateral resistivity. A Cr-Ag metallization grid on the front side and an Al layer complete the structure (Fig. 1). The final active area of the cell is 1 cm x 1cm. Details of the fabrication process are given in ref. 8. The impedance of the solar cell is measured with an HP 4284 A bridge.

Fig. 2 - Series resistance (left, Fig. 2a) and series capacitance (right, Fig. 2b) of the solar cell as a function of frequency. The full lines reflect the bridge measurements while the scattered curves (squares) are the result of the AFORS-HET simulation.

SIMULATION

AFORS-HET is fed with the layer sequence given by our solar cell fabrication process. The front surface recombination is 10^7 cm/s for electrons and holes. No back side surface field is applied. The work function is fixed to flat band in both cases. The standard trap distributions supplied by AFORS-HET and a doping level $N_D = 1 \cdot 10^{19}$ cm⁻³ are assumed for the a-Si.

AFORS-HET offers an option to introduce interface states. However, it turns out that in most cases convergence problems occur and - even worse - the solution does not vary with varied input data. Thus another approach consists in inserting a thin layer between the a-Si:H and the mc-Si, which contains a large number of bulk states. If the layer is thin enough the integrated bulk states might be considered as surface states [9].

RESULTS

The result of the measurement is reproduced in Fig. 2. The overall tendency of the resistance is a step-like function while the capacitance decreases with $1/f$ as a function of f for low frequencies and stays constant at high frequencies. This is the expected behavior for a junction capacitance, C_j , and its loss, R_j , in series to the wafer resistance, R_w , seen for conventional heterojunction cells [10]. However, a strong hump is visible in both curves. There have been vain attempts to explain the hump by an ad-hoc second time constant (say induced by an unintentional backside junction) so that an explanation by interface states becomes likely. Thus an additional c-Si layer was inserted between the substrate c-Si and the a-Si for the AFORS-HET simulation. A good fit was obtained for an acceptor-type trap with a total density, N_{trtot} , of $1.375 \cdot 10^{20}$ cm⁻³, a Gaussian distribution centered at $E_t - E_V = 0.6$ eV with a half-width $\Delta E = 0.14$ eV, and symmetrical capture cross sections $\sigma_e = \sigma_h = 5 \cdot 10^{-16}$ cm² as seen in the same figure. In Fig. 2a, a contact resistance, R_c , of 0.7Ω is taken into account. This value is obtained from dark and light IV measurements.

In the following we examine the effects of the parameter variation around the above optimum set. Among these, the interface layer bulk trap density, N_{trtot} , the position in the bandgap, the half width of the energetic trap distribution, the electron and hole capture cross

Fig. 3 - Series resistance (left, Fig. 3a) and series capacitance (right, Fig. 3b) of the solar cell as a function of frequency. Variation of the trap energy level.

sections, and the trap type are varied. For all of them, a very narrow fit window is found. In order to avoid overloading, we just show the result of the energy level fitting. In Fig. 3, $E_t - E_V$ runs from 0.5 to 0.7 eV. We have also tested the simulation for side effects such as variation of the substrate thickness and the introduction of a back surface field. No change is seen.

In an earlier paper [8], a network analysis of the sample is done. The following steps are applied: (i) The high frequency resistance is subtracted from the measured series resistance (to remove the wafer and contact resistance), (ii) the remaining impedance is converted into an admittance, (iii) the low frequency conductance is subtracted from the conductance, and the high frequency capacitance is subtracted from the capacitance. – The remaining conductance, G_{Dit} , and capacitance, C_{Dit} , are attributed to the interface states (Fig. 4). These curves are evaluated by means of an interface state continuum model including a slight contribution of statistical fluctuations [11]. This procedure yields a surface state density, D_{it} , of $2.3 \cdot 10^{12} / \text{Vcm}^2$ and a time constant, τ_{it} , of 1.7 ms. Let us compare the two figures with those obtained from AFORS-HET. N_{trtot} is a bulk state density which might be integrated over the thickness, d_{int} , of the interfacial layer yielding a surface state density, N_{ittot} , with $\dim N_{ittot} = 1/\text{cm}^2$. Thus, as a first step, it is confirmed that different N_{trtot} and d_{int} with a constant $N_{trtot} \times d_{int}$ product yield the same AFORS-HET fit (not shown in the figures). So at a first glance all the ‘bulk’ traps of a 5 to 10 Å thick layer can be projected to a single interface forming interface states. The second step would consist in integrating the surface states, $D_{it}(V)$, of Fig. 4 over the total band gap in order to reproduce the same N_{ittot} as above. Unfortunately, the $D_{it}(V)$ distribution cannot be measured with the present tools. If a constant D_{it} is assumed, $N_{ittot} = 2.1 \cdot 10^{12} \text{ cm}^{-2}$ is obtained while $N_{trtot} \times d_{int}$ yields $N_{ittot} = 1.1 \cdot 10^{13} \text{ cm}^{-2}$. A possible conclusion is that not all the bulk states take part in the carrier exchange, i. e., we might have depth dependent carrier cross sections.

In the same way, the time constants can be compared. From the simulation we obtain capture cross sections $\sigma_e = \sigma_h = 5 \cdot 10^{-16} \text{ cm}^2$. If the integrated bulk states can be treated as interface states, the capture cross sections are related to the interface time constants $\tau_{ite,h}$ by

$$\tau_{ite} = 1/(\sigma_e n_s v_{th}) \quad \text{Eq. 1a}$$

$$\tau_{ith} = 1/(\sigma_h p_s v_{th}) \quad \text{Eq. 1b}$$

Fig. 9 - Conduction and capacitance signal of a-Si/c-Si surface states as obtained from the network analysis (from ref. 8)

n_s and p_s are the surface carrier concentrations for electrons and holes, respectively, and v_{th} is their thermal velocity, $v_{th} = 10^7$ cm/s at room temperature. The “surface” electron density within the interfacial layer varies from 9.3 to $6.3 \cdot 10^9$ cm $^{-3}$ and the hole density from $8.1 \cdot 10^9$ to $1.2 \cdot 10^{10}$ cm $^{-3}$ as read in the simulation output. Insertion in Eq. 1 yields $\tau_{ite} = 2.1$ to $3.1 \cdot 10^{-2}$ s and $\tau_{ith} = 2.4$ to $1.7 \cdot 10^{-2}$ s. This results show that the electron and hole transitions are not discernible in the measurement. The reason is identical capture cross sections and carrier densities. In the network analysis we find $\tau_{it} = 1.7$ ms. An explanation for this discrepancy is not yet available.

What is the origin of the interface states? A first hint is obtained from ref. 12, which gathers the energy levels of the most important impurities in (monocrystalline) silicon. The most evident candidates are oxygen and iron, both of energies $E_c - E_t = 0.51$ eV (or $E_t - E_v = 0.61$ eV). The occurrence of these elements in multicrystalline material is proven in many articles [e.g., 13-15]. Other possible contaminations are Ni, Co, Cr, Hf, Mo, W, Au, As, Sb, Ga [16], combinations of these elements with the dopant [pair formation] and with lattice defects. In addition it is shown that multicrystalline silicon displaces many energy levels known from the monocrystalline material or creates new ones. As example oxygen levels $E_t - E_v$ between 0.35 and 0.38 eV (with capture cross sections σ_p between 0.5 and $11.4 \cdot 10^{-17}$ cm 2) are reported in ref. 17. On the other hand, energy levels have been measured, which have not yet been attributed to an impurity or a defect complex [18]. Ref. 19 presents a strong unidentified defect of $E_c - E_t = 0.45$ eV in Baysix (now Solsix) p-type material. This value is not too far from our measured one.

The situation is even more complicated by the fact that the interface can create new energy levels or modify bulk levels. In spite of an intensive search we cannot find a previously published trap, whose data – energy level, capture cross sections - completely coincide with those found by us. Thus a final ascription cannot be given in this state.

CONCLUSION

The impedance of a heterojunction based on a multicrystalline substrate is measured. The simulation program AFORS-HET is used to reproduce the measurements. An appropriate set of input data is found (an interfacial layer with an acceptor-type trap of a total density, N_{trtot} , of $1.375 \cdot 10^{20}$ cm $^{-3}$, a Gaussian distribution centered at $E_t - E_v = 0.6$ eV with a half-width $\Delta E = 0.14$ eV, and symmetrical capture cross sections $\sigma_e = \sigma_h = 5 \cdot 10^{-16}$ cm 2 . From these

data, the total interface state density and time constants are evaluated and compared to a network analysis. They disagree by a factor of five and ten, respectively.

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High-Speed Diagnosis of Multicrystalline Silicon Wafers by Photoluminescence Imaging with HF Immersion

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Abstract

High-speed characterization of non-passivated multicrystalline Si (mc-Si) wafers was demonstrated by photoluminescence (PL) imaging with the wafers immersed in a HF solution. Highly spatially-resolved wafer quality was assessed only within “100 ms” by the present technique. Not only the measurement time was shortened, but also the accurate bulk property was obtained. We also examined the effects of the HF concentration on the surface property, and concluded that 5% HF etching was the most appropriate surface treatment.

1. Introduction

Recently, photovoltaic industry has been expanding greatly, and multicrystalline Si (mc-Si) has become the most dominant materials for solar cells. Although high conversion-efficiency cells have been required, the wafer quality is still poor and has restricted the cell efficiency. For the mc-Si wafers, spatially resolved monitoring of electrical property is essential to improve their quality because there are numerous defects such as grain boundaries and dislocations.

Photoluminescence (PL) imaging has recently been demonstrated to be a rapid and highly spatially-resolved technique for characterizing wafer quality.^[1] Measurement time and spatial resolution of PL imaging are a few thousand times faster and tens of times higher than those of conventional techniques, e.g., microwave photoconductivity decay mapping. Additionally, PL imaging is a contactless measurement and does not require a device structure. Because of these features, it has been expected as an inline tool at any processing stage of the mc-Si solar cells.

In as-received wafers which have no surface-passivation layers, the surface carrier recombination becomes a big problem. The surface recombination not only degrades the PL intensity, i.e., prolongs the measurement time, but also disturbs the accurate measurement of the bulk property. Therefore, restraining the surface recombination is necessary to shorten the measurement time and to examine the bulk property accurately.

Several surface passivation techniques have been reported, such as immersion in HF solution,^[2] iodine/ethanol treatment^[3] and quinhydrone/methanol treatment.^[4] In particular, the surface recombination velocity of the wafers immersed in HF solution is, surprisingly, as low as 0.25 cm/s.^[2] HF etching is generally used in the wafer processes, and the transparent HF solution does not disturb the optical measurement. Taking these advantages into account, we developed a new characterizing technique.^[5] In this paper, we demonstrated the PL imaging of the mc-Si wafers during the HF immersion.

2. Experimental Technique

Figure 1 shows a schematic illustration of the PL imaging with the HF immersion. We used a charge-coupled device (CCD) camera cooled electrically to -70°C for the PL

detection. The CCD sensor was a one mega-pixel Si sensor whose near-infrared (NIR) sensitivity was enhanced. A lens for machine vision applications was mounted on the camera, and high power light-emitting-diode (LED) arrays with a wavelength of 500 nm were applied to an excitation source. The power density of the light excitation was about 100 mW/cm^2 , and the excitation light was illuminated from the same side of the PL signal detection. The NIR light from the LED was cut by IR-cut filters placed in front of the LED arrays. The reflected excitation light was cut off and the spectral component of the band-edge emission from the wafer was extracted by the band-pass filters located between the wafer and the CCD camera, and the PL imaging was performed while the wafer was immersed in the HF solution. To investigate the effect of the HF concentration and the HF etching time on the surface property, we used the 2.5, 5, 10 and 20% HF solution. For this measurement, the light power density was decreased as low as 10 mW/cm^2 , and the excitation light was illuminated only during the data acquisition. All measurements were performed at room temperature.

The mc-Si wafer used for this work was boron doped with a resistivity of $1.1 \text{ } \Omega\text{cm}$, a thickness of $310 \text{ } \mu\text{m}$ and a size of $40 \times 40 \text{ mm}^2$. The slicing damage was etched off by the HNO_3/HF solution. Before the PL measurement, minority carrier lifetime was measured by quasi-steady-state photoconductance technique with a commercial apparatus (Sinton Consulting WCT-100), and we confirmed that the wafer had the lifetime of $32 \text{ } \mu\text{s}$.

In Fig. 2, we show the effect of surface recombination velocity on relationship between the PL intensity and the bulk lifetime, where W is the wafer thickness and S is the surface recombination velocity. The result was calculated with the following condition; the wafer thickness of $200 \text{ } \mu\text{m}$, the resistivity of $1 \text{ } \Omega\text{cm}$ (p-type), the excitation light wavelength of 500 nm and the light intensity of 100 mW/cm^2 . The result indicates that the PL intensity with low S increases two orders of magnitude higher than that with high S , which means that the measurement speed of PL imaging also increases two orders of magnitude. Moreover, the relationship between the PL intensity and the bulk lifetime becomes approximately proportional. With the outstanding passivation ability of the HF immersion, we can characterize the wafer quality more rapidly and accurately.

Fig. 1. Schematic illustration of PL imaging with HF immersion.

Fig. 2. Effect of surface recombination velocity on relationship between PL intensity and bulk lifetime.

3. Results and Discussion

The PL image of the non-passivated mc-Si wafer with and without the HF immersion is shown in Fig. 3 (b) and (c), respectively. For comparison, PL intensity mapping is also shown in Fig. 3 (a). All images were taken from an identical wafer under the same conditions, and they had the same spatial resolution of 100 μm , but the measurement time was greatly different. About 40 min was required to acquire the equivalent image by our PL mapping technique. The PL dark-lines in Fig. 3(a) are the dislocation-related defects, and these regions have extremely low lifetime.^[6] PL imaging without HF immersion was more rapid than the PL mapping. The measurement time was shortened to 60 s, and the defect patterns were also observed. However, this image was noisy and depended on the surface condition. Surprisingly, PL imaging with HF immersion was extremely rapid and clear. We were able to characterize the wafer quality only within 100 ms. We confirmed that the PL intensity with the HF immersion increased two orders of magnitude higher than without the HF immersion. This implied that the surface recombination was dramatically restrained and the PL image primarily reflected the bulk property. These findings show clearly that PL imaging with HF immersion is a powerful tool for characterizing the wafer quality.

Fig. 3. Comparison of rapidity for wafer monitoring. Measurement time of (a) PL mapping, PL imaging (b) without and (c) with HF immersion was 40 min, 60 s and 100 ms, respectively. Identical wafer was examined with a spatial resolution of 100 μm .

We examined the effect of the HF concentration on the surface property as shown in Fig. 4. Averaged PL intensity of the wafer was plotted against the process time, and the intensity gradually increased and reached a maximum value within a few minutes. The intensity of the wafer treated with the 5% HF solution reached maximum more rapidly than the case with the other solution. After the intensity reached maximum, the surface passivation effect continued stably. This means that a few minutes of immersion are sufficient for the passivation.

Fig. 4. Temporal variations of averaged PL intensity from HF-immersed wafer.

The wafer immersed in the 2.5 and 5% HF solutions showed the highest PL intensity, while the intensity in the 10% HF solution was lower, and the 20% HF solution had the lowest PL intensity of all. As the HF concentration increases, the wafer surface becomes rough on an atomic scale.^[7, 8] The degradation of the PL intensity at the high HF concentration can be due to the increase of the recombination center ascribed to the surface roughness.^[9] From the results, we concluded that the 5% HF immersion is the most appropriate surface treatment.

4. Conclusion

In summary, we demonstrated the rapid characterization of the non-passivated mc-Si wafers by the PL imaging with HF immersion. Highly spatially-resolved PL images were acquired within 100 ms. We confirmed that the PL intensity from the HF-immersed wafers increased two orders of magnitude higher than that without the HF immersion. Examination of the effects of the HF concentration on the surface property concluded that the 5% HF immersion was the most appropriate surface treatment and showed that a few minutes of HF immersion are sufficient for the passivation. The present findings showed clearly that PL imaging with HF immersion is a powerful tool for characterizing the accurate bulk property.

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Effect of Surface Passivation on Si Heterojunction and Interdigitated Back Contact Solar Cells

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Abstract

Silicon surface passivation of hydrogenated silicon (Si:H) thin films deposited by RF and DC plasma process was investigated by measuring effective minority carrier lifetime (τ_{eff}) on Si <100> and <111> wafers and correlated with the silicon heterojunction (SHJ) cell performances in front emitter structure and interdigitated back contact (IBC) structure. Excellent surface passivation ($\tau_{\text{eff}} > 1$ msec) and high efficiency front emitter SHJ cells are obtained by both RF and DC plasma deposited intrinsic a-Si:H buffer layer. High efficiency with open circuit voltage (V_{OC}) of 694 mV was achieved on n-type textured Cz wafer using DC plasma deposited buffer layer. High V_{OC} of 683 mV is also achieved in an exploratory IBC heterojunction structure and needs further optimization for improved fill factor.

Introduction

Fabrication of crystalline silicon (c-Si) heterojunction (SHJ) devices by the deposition of wide band gap semiconductors such as amorphous hydrogenated silicon (a-Si:H) are a demonstrated way to fabricate high efficiency c-Si solar cells [1-3]. High efficiency of a-Si:H/c-Si SHJ solar cells is primarily due to increased open circuit voltages (V_{OC}). The increase in V_{OC} is achieved by reduced surface recombination and low emitter saturation currents using a thin intrinsic a-Si:H buffer (i-layer) on both surfaces of c-Si wafer. However, the a-Si:H layer absorbs short wavelength (<600 nm) light and the best passivation is achieved with thicker layers, resulting in greater absorption losses and reduced short circuit currents (J_{SC}) in the front emitter SHJ cells. Formation of heterojunction with both a-Si:H emitter and base contact on the back side in an interdigitated pattern would hence improve the cell blue response and J_{SC} and offer a pathway to realize the full potential of heterojunction devices. Furthermore, a good front surface passivation quality is absolutely necessary for interdigitated back contact (IBC) structure, since the carriers that are generated near the front surface need to diffuse the entire wafer thickness to be collected in the rear.

In this work, we studied the surface passivation quality of a-Si:H i-layers deposited with varying hydrogen dilution on n-type float zone (FZ) Si wafers with two different crystallographic orientation (<100> and <111>) and correlate with the device performances of front emitter SHJ and IBC cells. The SHJ cells were also fabricated on n-type textured Czochralski (Cz) Si wafers, where <100> surface changes to <111> after texturing to realize the benefit of light scattering. Additionally, the a-Si:H layers were deposited by standard 13.56 MHz RF plasma and by DC glow discharge process. Comparison between the two processes elucidates the effect of ion bombardment on Si surface passivation and cell performances during growth of these thin layers.

Experimental

The n-type Si wafers (~300 μm) with resistivity of 1.0 $\Omega\cdot\text{cm}$ for <100> and 2.5 $\Omega\cdot\text{cm}$ for <111> were cleaned for 5 mins in a mixture of $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2$ (4:1) followed by 5 mins rinse in de-ionized water and in 10% HF for 30 sec prior to each Si:H deposition. The Si:H i-layers (10 nm) were deposited on both sides by RF and DC plasma process using a six-chamber large area (30 $\times$ 35 cm^2) deposition system. The substrate temperature, deposition pressure and SiH_4 flow rate were fixed at 200°C, 1250 mTorr and 20 sccm respectively. The primary variable in i-layer process is the H_2 flow rate, which was varied from 0 to 200 sccm and characterized by the dilution ratio $R = \text{H}_2/\text{SiH}_4$. The RF power of 30 W and a DC plasma current of 123 mA were maintained constant. The quality of surface passivation was determined by

measuring effective minority carrier lifetime (τ_{eff}) using photoconductive decay method [4]. Thin layers (10 nm) of p-type a-Si:H emitter followed by 70 nm Indium Tin Oxide (ITO) with metal grids in the front and n-type a-Si:H followed by evaporated Al contact on the rear were deposited to fabricate front emitter SHJ cells. The interdigitated pattern of deposited p- and n-type a-Si:H layers (20 nm) and evaporated Al contacts were created for IBC structure by two step photolithography processing, where the p-region has lateral dimension of 1.2 mm and n-region is 0.5 mm wide. The front surface of IBC cells were passivated by a 20 nm a-Si:H i-layer followed by antireflection (AR) coatings composed of ITO and MgF_2 layers. This surface passivation/AR structure is not ideal for high J_{SC} but provided a means of evaluating the device performance and the utility of the structure as an alternate diagnostic tool to evaluate surface recombination.

Results and Discussions

Figure 1 shows the τ_{eff} as a function of R for i-layers deposited on $\langle 100 \rangle$ and $\langle 111 \rangle$ wafers by DC and RF plasma after annealing the samples at 280°C for 10 mins. It is worth noting that the DC plasma process will have a significantly higher ion bombardment compared to RF in otherwise similar plasma parameters due to higher plasma potential. Three distinct regions can be identified in the variation of τ_{eff} with R (Fig. 1). In region I ($R < 2$), τ_{eff} shows plasma process dependence, namely, DC plasma deposited i-layer at $R = 0$ show lower lifetime ($\sim 500 \mu\text{sec}$) compared to RF plasma deposited i-layers ($> 1 \text{ msec}$) irrespective of the surface orientation. With $R = 0$ at 1250 mTorr, it is likely to have significant polysilane contribution in the film deposition for both DC and RF plasma with comparatively higher in DC due to larger amount of ionic species, resulting in a more defective film in DC process, thereby reduces τ_{eff} . Formation of poly-silane decreases with an increase of R in DC plasma [5] and improves film quality. Hence, τ_{eff} becomes similar for both RF and DC plasma deposited i-layers at $R > 2$ (region II and III in Fig.1), implying little / no deleterious effect of ion damage in DC process on Si surface passivation.

In region III ($R > 4$), however, the measured τ_{eff} exhibits a pronounced Si surface orientation dependence. The values of τ_{eff} sharply decreases to $< 10 \mu\text{sec}$ on $\langle 100 \rangle$ wafers for i-layers deposited with $R > 4$, while on $\langle 111 \rangle$ wafers remains $> 1 \text{ msec}$ even at $R = 10$ for both RF and DC process. It was found out from variable angle spectroscopic ellipsometry (VASE) measurement that i-layer at $R > 4$ on $\langle 100 \rangle$ wafers grow epitaxial or nanocrystalline, while the films remain amorphous on $\langle 111 \rangle$ wafers. Low value of τ_{eff} and loss of surface passivation on $\langle 100 \rangle$ wafers by $R > 4$ i-layers are likely due to the low band gap of epitaxial or nanocrystalline Si layers with larger amount of defects at the interface.

Figure 1: Effective minority carrier lifetime (τ_{eff}) on Si $\langle 100 \rangle$ and $\langle 111 \rangle$ wafers with 10 nm Si:H i-layer deposited on both sides by RF and DC plasma at varying hydrogen dilution (R). The lines are guide to the eyes.

Figure 2: Open circuit voltage (V_{oc}) and fill factor (FF) of SHJ cells on Si $\langle 100 \rangle$ and $\langle 111 \rangle$ wafers with i-layers deposited by RF and DC plasma process at different hydrogen dilution (R).

After completion of lifetime testing of all the samples, they were converted into front emitter SHJ cells by depositing p- and n-type a-Si:H including the ITO and metal contacts. The J_{SC} values were rather similar for all the devices, while the cell efficiency changes with R in i-layers due to changes in V_{OC} and FF. Figure 2 shows the variation of V_{OC} and fill factor (FF) of the cells as a function of R for i-layers deposited on <100> by DC and on both <100> and <111> wafers by RF plasma. Interestingly, the V_{OC} exhibits pronounced wafer orientation dependence in region III ($R = 6$), while FF exhibits only plasma process dependence in region I ($R = 0$). The cell V_{OC} correlates well to the variation of τ_{eff} with R as shown in Fig.1, and decreases to ~ 600 mV for the i-layer deposited with $R = 6$, demonstrating the necessity of high τ_{eff} and good surface passivation quality to achieve high V_{OC} . However, high value of τ_{eff} alone does not insure a high efficiency device because the FF decreases drastically to $< 50\%$ with an “S” shape J-V for the i-layers grown at $R = 0$, despite exhibiting τ_{eff} of > 1 msec in RF process in Fig.1. The poly-silane contribution in the film growth at $R = 0$ forms a defective and presumably wider band gap layer with higher SiH_2 bonding for both processes with an enhanced effect in DC discharge. Such a defective and wide band gap a-Si:H film severely inhibits carrier transport across the i-layer, particularly the hole transport over a large valence band offset in the emitter side and reduces FF. On the other hand, epitaxial / nanocrystalline growth at $R = 6$ narrows the band gap of deposited layer and therefore does not affect hole transport and cell FF, but results in low V_{OC} due to insufficient surface passivation. Consequently, the highest SHJ cell efficiency was obtained for i-layers deposited with $R = 2$.

Table-I summarizes the best device performances on n-type polished FZ <100>, <111> and n-type textured Cz wafers with i-layers deposited by DC and RF processes. Both plasma processes demonstrate SHJ cells with high efficiency and high V_{OC} , therefore, seemingly higher ion bombardment in DC process have neither any effect on surface passivation nor in the cell performance. The SHJ cell efficiency of 18.8% with V_{OC} of 694 mV was achieved on textured Cz wafer due to efficient light scattering and additional MgF_2 AR layer in the front light illuminating surface.

Table-I: Summary of the best front emitter SHJ device performances on n-type polished FZ <100>, <111> and n-type textured Cz wafers with the i-layers deposited by both DC and RF processes.

Wafer	a-Si:H i-layer process	V_{OC} (V)	FF (%)	J_{SC} (mA/cm ²)	Efficiency (%); not independently confirmed
N – FZ<100>	DC	0.686	72.2	32.8	16.2
	RF	0.680	74.1	32.6	16.4
N – FZ<111>	RF	0.689	74.0	33.8	17.2
N – Tex. Cz	DC	0.689	74.0	35.0	17.8
N – Tex. Cz with additional MgF_2 AR coating	DC	0.694	74.4	36.4	18.8

The short wavelength quantum efficiency and hence the cell J_{SC} is expected to increase significantly for the IBC solar cell structure, since it allows independent control for optimum passivation with low reflection / absorption loss in the front illuminating surface and minimization of electrical series resistance in the rear. The IBC structure fabricated on n-type FZ <100> wafers in this work is, however, not optimized in the front surface. Instead, the front surface consists of 20 nm thick R2 a-Si:H i-layer (same total thickness of a-Si:H layer as front emitter SHJ cells) followed by alike AR coatings and thus provide similar optical layers in the front to allow a direct comparison of cell performances with front emitter SHJ cells. The rear side of IBC cells consists of two different structures; (i) interdigitated p- and n-strips without any i-layer [Figure 3(a)] and (ii) 8 nm R2 i-layer over the whole rear surface followed by interdigitated p- and n-strips [Figure 3(b)]. The dimensions of p- and n-strips in the two structures were identical, but width of the gap between p- and n-strip and surface passivation in rear was different. In

case of no i-layer in the rear, about 2 μm gap was not passivated by any amorphous layer, while a wider gap of 50 μm along with the entire rear surface was passivated by i-layer in the second structure.

Figure 3: Schematic cross section of heterojunction cells in IBC structure (a) without i-layer passivation in the rear; (b) with i-layer passivation in the rear; and (c) Illuminated (AM 1.5) J-V for the IBC heterojunction cells, with and without rear i-layer and a front emitter SHJ cells without buffer i-layer.

Figure 3(c) compares the J-V curve under AM 1.5 illumination for the IBC cells with two structures and a front emitter SHJ cell without any i-layer. The figure clearly demonstrate that the V_{OC} and FF are identical for the cells without i-layer passivation in the emitter and contact side for both front emitter SHJ and IBC structure. However, J_{SC} of the IBC cell is $\sim 6 \text{ mA}/\text{cm}^2$ lower than that of front emitter SHJ cell and achieved an independently confirmed efficiency of 11.8% in IBC heterojunction cell. An unpassivated gap between the emitter and contact strips acts as an efficient recombination region for the photogenerated carriers and reduces J_{SC} in IBC structure. Consequently, the IBC cell with the entire rear surface passivated by i-layer exhibits both increased J_{SC} and V_{OC} . The V_{OC} of 683 mV is similar to that of the front emitter SHJ cell on $\langle 100 \rangle$ wafer as shown in Table-I and indicative of good passivation in the emitter and contact strips but has a low FF. Such an “S”-shape J-V suggests existence of carrier transport barrier across i-layers and requires separate optimization of the layer in the IBC structure.

Conclusions

In conclusion, excellent surface passivation ($\tau_{eff} > 1 \text{ msec}$) and high V_{OC} in SHJ cells are achieved by both RF and DC plasma process with hydrogen dilution. Any epitaxial / nanocrystalline growth of i-layer reduces τ_{eff} and cell V_{OC} . The structure of deposited thin Si:H layers strongly depend on the Si substrate orientation. The front emitter SHJ cell efficiency approaching 19% with V_{OC} of 694 mV was achieved on textured Cz wafer using DC plasma deposited i-layer. The exploratory heterojunction cells in IBC structure reveals importance of surface passivation in the rear to achieve high V_{OC} (683 mV) and J_{SC} but demands further optimization of i-layer for improved carrier transport across it and cell FF.

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Progress in diffusion-free back contact solar cell fabricated on S-passivated p-type Si(100) substrate

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ABSTRACT: In this paper, we report our recent results on a back contact solar cell with a diffusion-free p-n junction. This junction is field-induced by the extremely high Schottky barrier of 1.1 eV between low work-function metal Al and S-passivated p-type Si(100) surface. Al silicide is used as ohmic contact finger. This cell is supposed to satisfy a low cost fabrication process.

INTRODUCTION

In most solar cells built on p-type Si, the p-n junction or emitter is formed by P diffusion. The highly doped n^+ region with metal electrode ensures an acceptable contact resistance. However, diffusion process involves a high energy input, and it also complicates the fabrication process for a back contact solar cell. Our recent result indicates that Al on S passivated p-type Si(100) surface produces extremely high Schottky barrier of 1.1 eV (1), which is extracted from a $1/C^2$ -V plot at different frequencies shown in Fig. 1. Figure 2 shows the corresponding low reverse current density for this diode, and the inset is band diagram of a 1.1-eV barrier on p-type Si(100). This result is consistent with low Schottky barrier obtained for titanium on a monolayer Se-passivated n-type Si(100) surface (2). These can be explained by the fact that, passivation of Si(100) surface by Group VI elements terminates dangling bonds (3), and thus significantly reduce the interface states, making an almost ideal barrier height between metal and S- or

Se-passivated Si(100) surface.

1.1 eV Schottky barrier causes degenerate inversion on the Si surface, making this diode behave like a p-n junction diode, i.e., holes are injected from the p-type bulk and electrons from the metal under forward bias. Based on this concept, a diffusion-free back contact solar cell is proposed here. Our focus in this paper is on the cell design and working mechanism and later work will concentrate on the improvement of conversion efficiency.

Figure 1. A $1/C^2$ -V plot at different frequencies for Al/S/p-Si(100) contact to extract Scottky barrier height.

Figure 2. Reverse current density of Al/S/p-Si(100) contact. The inset is band diagram of a 1.1-eV barrier on p-type Si.

CELL PROCESS

Etching and cleaning

The substrate of the cell is single-side polished Czochralski p-type Si(100) with doping concentration of $1 \times 10^{17} \text{ cm}^{-3}$. The area of the cell is $2 \times 2 \text{ cm}^2$ and the thickness around $200 \mu\text{m}$, which should satisfy the minimum requirements of a back contact solar cell. The rough side of the substrate underwent Al gettering step to improve the minority carrier lifetime. The excess Al layer was removed in 20 wt.% NaOH solution, producing a polished surface for later anisotropic etching in 2–3 wt.% NaOH solution plus 10 vol.% isopropanol (4). The sample was subsequently cleaned in 1% diluted HCl followed by 2% HF etch and DI water rinsing. This cleaning process was repeated 5 times to remove surface metal particles.

Coating and contact

Thermally grown $1000 \text{ \AA}$ SiO_2 was performed in oxidation furnace. This layer on textured surface has two purposes. One is as anti-reflection coating to reduce reflectance, and the

other is to reduce surface recombination velocity (SRV). $1000 \text{ \AA}$ SiO_2 on shiny side protects the surface free of contamination from a firing-through step, which results in Al silicide formation as narrow ohmic contact finger. The rest of SiO_2 on shiny side was removed by buffer oxide solution. After this, S passivation was conducted in an aqueous solution of $(\text{NH}_4)_2\text{S}$ (5). The wide finger for junction contact was formed by e-beam evaporation through a shadow mask. Figure 3 shows the cross-section view of the cell structure. The sizes of the wide finger and narrow finger are $1100 \mu\text{m}$ and $600 \mu\text{m}$ respectively. The separation between the wide finger and the narrow finger is $200 \mu\text{m}$.

Figure 3. Cross-section view of the cell structure.

RESULTS

Reflectance

For a back contact solar cell, the front side has no metal covering, which makes it possible the highest light-trapping when the minimum reflectance is obtained. Figure 4 shows the micro-sized pyramids with 100% coverage on Si surface. Anti-reflection coating is either thermally grown SiO_2 or PECVD grown Si_3N_4 . They also serve as passivation layer to reduce SRV. Figure 5 shows the total reflectance of Si

surface after texturing and anti-reflection coating with SiO_2 or Si_3N_4 . The pyramid-textured surface has reflectance about 12%. The minimum reflectance of less than 1% is reached after 100 nm Si_3N_4 coating. Another advantage of Si_3N_4 coating is to improve the bulk materials by hydrogenation, which enhances the average minority carrier diffusion length. Our solar cell uses thermally grown SiO_2 as coating layer because of facility issue.

Figure 4 SEM image of micro-sized pyramids formed by anisotropic etching in 2 wt.% NaOH solution with addition of 10 vol.% isopropanol.

Figure 5 Reflectance of p-type Si(100) surface after texturing and anti-reflection coating with 100 nm SiO_2 or Si_3N_4 .

Conversion efficiency

Figure 6 shows I-V characteristics in the dark and under illumination. The

illumination source is from a ~24 watts lamp. The light intensity on the cell surface is a little lower than AM 1.5, which is roughly calibrated by a same sized standard cell. Under this illumination, the open circuit voltage (V_{oc}) for the cell is 450 mV, and the short circuit current (I_{sc}) is 5.5 mA. Taking the active junction area of 1.66 cm^2 into account, the estimated conversion efficiency is above 1%. This low efficiency is mainly limited by two key factors, surface passivation quality and minority carrier lifetime.

Figure 6. I-V characteristics of diffusion-free back contact solar cell.

1. Passivation quality

It is found that, for some of cells, reverse current density is only $\sim 5 \times 10^{-4} \text{ A/cm}^2$ at -1 V, which corresponds to a low V_{oc} of 300 mV under illumination. With one order of magnitude drop in reverse current density, the V_{oc} is increased to 450 mV. This indicates the importance of low reverse current in cell performance. If the reverse current density can be reduced to $4.5 \times 10^{-7} \text{ A/cm}^2$ like a single diode shown in Fig. 2, it is believed that the efficiency should be significantly increased. However, wet-chemical passivation can not guarantee perfect passivation with

complete Si_3N_4 coverage, and the unpassivated regions will have a low barrier height, corresponding to a high reverse current. Therefore, improvement of passivation quality is a key factor to promote the efficiency.

2. Minority carrier lifetime

High minority carrier lifetime corresponds to a long diffusion length. If this Si substrate under gettering step still possesses a short minority carrier diffusion length less than the substrate thickness of 200 μm , the efficiency will be significantly reduced because the large amount of photo-generated carriers will recombine before they can be collected by the back contacts. So a Si substrate with high minority carrier lifetime is needed for later investigation.

Other factors, such as junction on textured surface, Si_3N_4 passivation on textured surface, and separation between wide finger and narrow finger, etc., may have minor or certain effects on the efficiency. They should be optimized for efficiency improvement.

CONCLUSION

A diffusion-free back contact solar cell is introduced based on field induced p-n junction. Although the cell efficiency is low ($\eta > 1\%$) in current stage, it can be significantly increased with some improvements in process and design.

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Measurement of dislocation distribution in multicrystalline silicon ingots using PVSCAN, a fast optical scanning method

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Abstract:

Dislocation density variation in multicrystalline silicon (mc-Si) ingots was measured using a fast optical scanning system, GT PVSCAN-8000. Spatial distribution and statistical analysis of up to 210mm square mc-Si wafers was acquired in an automated mode with this system. Examples of data for wafers from various positions in the ingot were obtained. Such data can be used to improve and optimize the quality and consistency of mc-Si ingots.

Keywords: multicrystalline, silicon, dislocation density, PVSCAN

1. Introduction:

High dislocation densities have been one of the performance limiting factors of multicrystalline silicon (mc-Si) based solar cells [1-3]. As a typical growth defect, dislocations are generated due to plastic thermal deformation during the crystal growth process. These defects serve as traps or recombination centers for minority carrier charges and also provide precipitation sites for transition metal impurities [4]. The latter behaves as an even stronger minority carrier charge recombination center. Excessive amount of such impurity decorated dislocation tangles cause even shorter minority carrier life time and cannot be passivated, resulting in a fundamental limitation on the conversion efficiency of the solar cells [5, 6].

The industry has adopted many different passivation techniques to reduce impurities in mc-Si wafers. However, research has shown that if the dislocation densities in the mc-Si base material exceeds a certain level ($\sim 10^6$ counts/cm²), passivation techniques are not effective in enhancing minority charge carrier life time [7]. Controlling the dislocation densities below the critical level during the ingot growth stage is very important to produce high efficiency solar cells. Therefore, methods for fast and consistent dislocation density measurements are required to improve the manufacturing processes and product quality.

2. PVSCAN method:

The PVSCAN technology concept was developed at the National Renewable Energy Laboratory (NREL) [8, 9] and shown schematically in Fig.1. In general, the PVSCAN is a laser assisted optical scanning system which can measure multiple material characteristics of

photovoltaic solar cells and wafers. GT Solar Incorporated has obtained an exclusive license of PVSCAN from NREL and developed it into an industry standard instrument, GT-PVSCAN 8000. The specially designed optics and precise XY motion enable full area scanning and mapping of wafers up to 210mm square with a resolution of 25 μ m.

Fig.1. An optical schematic of PVSCAN

In particular, for dislocation density measurements, the laser beam scattered by the etched pits from dislocations is collected and amplified by an optical integrating sphere. Thereby, the intensity of the scattered laser beam increases linearly with the dislocation density on the surface of the etched wafer.

Fig.2. PVSCAN dislocation density mapping and statistical analysis results for sample 11-a

The commercially available system, GT-PVSCAN 8000 incorporates many modern optical, machinery and instrumentation technologies [10]. As a brief summary, the precision and stability of the optics is ensured by an environmentally rigid granite base and gantry structure which is supported by four air shock absorbers installed on a steel bench. A semiconductor grade linear XY table with submicron positioning repeatability is programmed to perform the scan motion. The system is able to scan a typical 156mm square wafer with 200 μ m sampling interval within 10 minutes. A flexible and interactive two-dimensional color map is generated to display both global spatial distribution as well as local details of the dislocation density. The statistical results are also presented in both data and histogram format. Fig.2 shows the interface of the data analysis software. The detailed analysis and high resolution gives the possibility of using GT-PVSCAN 8000 as an off line quality control tool to spot check quality of wafers as well as correlating the quality of wafers selected from different positions within the ingot.

3. Results and discussions

Due to the inhomogeneous thermal conditions during casting or directional solidification of mc-Si ingots, it is of interest to study the dislocation density distribution of wafers from different geometrical locations within the ingot. A better characterization and correlation of dislocation density distribution will help crystal growers to improve their hot zone and process recipes as well as optimize the growth conditions [11]. It can also help to optimize the wafer passivation process during the downstream solar cell manufacturing process [12]. In this study, wafers from selected locations of the ingots were chosen to perform Sopori etching [13] and dislocation density scans. In addition to dislocation density results in fig.2, more wafers were mapped and the data is shown in fig.3 and tabulated in Table I.

Fig.3. Dislocation density maps of selected wafers from mc-Si ingots

As shown by the sample designation in fig. 2, fig.3 and Table I, the first number leading the dash line corresponds to different ingots, the second number indicates the brick position within the ingot, and the letter following the dash line represents the wafer's vertical position inside each brick. In particular, 11-a represents a wafer from one corner brick of ingot 1. 17-a and 17-b are located in the center brick of ingot 1 and they are 6 wafers apart from each other. Similarly, 21-a and 21-b are from one corner brick of ingot 2 and they are 14 wafers apart, and 27-a and 27-b are both from the center brick of ingot 2 and they are 18 wafers apart. Since the dislocation density maps in fig.3 are displayed in small sizes, the mean and mode value of the dislocation density for each wafer is summarized in Table I.

Table I. Dislocation density of wafers from center and corner locations of mc-Si ingots

Ingots	Sample ID	Sample location	Arithmetic Mean	Mode
1	11-a	Corner brick	1.543×10^5	7.075×10^4
	17-a	Center brick	1.383×10^5	5.147×10^4
	17-b	Center brick	1.376×10^5	5.654×10^4
2	21-a	Corner brick	2.191×10^5	1.513×10^5
	21-b	Corner brick	1.984×10^5	1.290×10^5
	27-a	Center brick	1.829×10^5	8.387×10^4
	27-b	Center brick	1.742×10^5	7.540×10^4

Several deductions can be made from Table I. First, wafers from the center brick carry noticeably lower dislocation density than wafers from the corner brick for both ingots. Secondly, within each brick, for both center and corner locations, the adjacent wafers show similar dislocation density levels. In contrast, the wafers show more variation in dislocation density to their vertical position within a brick. In addition, ingots 1 and 2 made at different times also demonstrate different overall dislocation density levels. This indicates that the wafer dislocation density is also influenced by process conditions within each growth cycle. The similarity and difference of the dislocation density mapping data are represented by both average value and statistical data distribution. Such data can be utilized to optimize wafer quality and improve overall consistency.

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Evaluation on uniformity of polycrystalline silicon substrates for solar cells

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INTRODUCTION

Polycrystalline silicon (poly-Si) substrate is widely used for solar cells because the production costs are lower than those for single-crystalline silicon (sc-Si) [1]. However, the energy-conversion efficiency of solar cells fabricated on poly-Si substrates has not been as high as that of sc-Si cells [2-6]. In order to verify the origin of the degradation precisely, we evaluated the uniformity of crystal quality in poly-Si substrates in conjunction with electrical properties. As solar cells essentially consist of p-n junctions, their properties should affect conversion efficiency significantly. Therefore, we fabricated a small p-n diode array on poly-Si substrates and the I-V characteristics were measured for each small diode to evaluate the distribution of electrical properties in the substrate. The crystal qualities were also evaluated in each diode and compared with its electrical characteristics.

EXPERIMENT

We prepared B-doped approximately 50×50 mm poly-Si substrates fabricated with the casting method in the experiment.

Figure 1 show the diode

structure fabricated in this study. Phosphorus was doped by diffusion through a 1×1 mm SiO_2 mask to form the p-n junction. The Al electrode was then deposited and patterned into 1×1 mm square covering a quarter of the P-doped area. Therefore, three quarters of the diode surface was exposed for the evaluation of the crystal quality by non-destructive techniques. There are several parameters that indicate the quality of p-n junctions, such as the ideal factor (n) and reverse bias leakage current. These parameters can be determined by measuring the I-V characteristics of the diode.

Fig1. Structure of p-n diode, (a) layout, and (b) cross-section (A-B)

We measured the I-V characteristics for each p-n diode and defined electrical properties and its variation in the substrate. The crystal quality was evaluated in each diode in conjunction with the diode characteristics, by photoluminescence (PL) and Raman spectroscopy mapping.

RESULTS AND DISCUSS

Figure 2 shows the distribution for ideal factor n of the diodes in the poly-Si substrate. We can recognize that the n value varies between 1.8 and 4, which is much larger than the variations found in diodes on a sc-Si substrate fabricated with the same process simultaneously. The reverse bias leakage current also varied with a similar tendency (Fig. 4), i.e., diodes with a large ideal factor had poor leakage characteristics. Here, we defined leakage current as the current with an applied reverse bias of 1 V.

Fig. 2 Distribution of ideal factor n

Fig. 3 Distribution of leakage current

Figure 4 shows PL macro-mapping image. We found clear differences in PL macro-mapping, i.e., grains including degraded diodes were darker in the mapping, implying lower PL intensities than the others. There was good correlation between p-n diode characteristics and PL intensity.

Optical microscope images of area A, B, C are shown in Fig.5. The diode labeled A showed poor properties with $n = 3.2$ and leakage current of 3.26×10^{-6} A. Corresponding to this poor characteristics, grain boundaries can be observed in the optical microscope image. Although electrical quality was quite different between diode B ($n = 1.86$, leakage current = 6.0×10^{-9}) and C ($n = 3.42$, leakage current = 2.1×10^{-8}), no clear difference was observed in the optical

Fig. 4 PL macro-mapping image of p-n diode array

microscope images without any grain boundary in both cases. Therefore, we can point out that the grain boundaries definitely deteriorated diode characteristics, however, we also found variations in quality even in diodes without any grain boundaries at the p-n junction. Therefore, we evaluated crystalline quality with various techniques to compare these diodes.

Fig. 5 Optical microscope images observed in area A, B, and C

First, PL micro-mapping images were observed for both B and C diodes as shown in Fig.6. The black contrast at the upper left in each image corresponds to Al electrodes, and remaining area is P diffused area. It is clearly observed that the average PL intensity is higher in area B than that in area C. Moreover, several dark lines were observed in the image from diode C. We assume this dark line is some kind of crystal defects, and may affect somehow on the electric characteristic deterioration of the p-n diode.

Fig. 6 PL micro-mapping images at B and C area

Fig. 7 Raman mapping images at A and B area

Next, we measured strain distribution in diodes by using Raman spectroscopy mapping technique, in which Raman shifts proportional to the residual strain in the Si crystal was measured and indicated as a mapping image. Figure 7 shows strain mapping in the diode A, B and C. The strain field was more uniform in diode B than those in diode A and C, which may also imply poor crystal quality and degrade electrical properties.

CONCLUSION

We fabricated a small p-n diode array on poly-Si substrate, and measured the electrical characteristics. The crystal quality was also evaluated in conjunction with the electrical properties by using optical microscope, PL macro and micro mapping, Raman shift mapping. From the evaluation, electrical properties were poor when the diode includes grain boundaries. Moreover, electrical properties were varied even where the diodes do not have any grain boundaries. The difference in PL mapping image and strain uniformity measured by Raman mapping were detected between diodes with different electrical performance.

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Large area EFG (100-cm²) ribbon silicon solar cells with screen-printed contacts

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Abstract

High quality Screen-printed contacts were achieved on large area (100-cm²) EFG ribbon silicon solar cells without forming gas anneal after metal co-firing in the belt furnace. A combination of front Ag paste with medium aggressive glass frit from Heraeus Inc., and optimized co-firing cycle produced 14.6% efficient 100-cm² planar edge-defined film-fed grown (EFG) ribbon silicon cell with low series resistance (0.567 Ω -cm²) and high fill factor of ~78%. A mean fill factor of 0.761 was obtained for twenty EFG ribbon silicon cells for emitters formed at Schott Solar, Inc. A 0.014 standard deviation in the fill factor was attributed to the thickness variation in the EFG ribbon silicon which could lead to nonoptimized contact firing. To improve the efficiency of the screen-printed EFG cells, we used 45- Ω /sq sheet resistance emitters formed with POCl₃. However, because of the high ideality factor we gained only 4-mV in the open circuit voltage with no improvement in the short circuit current density and fill factor. Therefore, we achieved 14.2% efficiency large area screen-printed EFG ribbon silicon solar cell with POCl₃ emitter.

Introduction;

Edge-defined film-fed grown (EFG) ribbon silicon is one of the most promising PV materials to achieve low-cost and high efficiency solar cells. EFG ribbon technology eliminates the kerf loss associated with mechanical sawing and damage etching. Schott Solar, Inc. (Billerica, MA) produces EFG silicon, which is the current leader in production volume of silicon ribbon solar cells [1]. However, like most low-cost multicrystalline silicon materials, the EFG silicon contains high concentrations of impurities and crystalline defects, which degrade the as-grown minority carrier lifetime in EFG silicon to <3 μ s. This lifetime is not enough for high-efficiency cells of >15%. Therefore, it is necessary to improve carrier lifetime during the solar cell fabrication to achieve high-efficiency screen-printed cells on low-cost and defective EFG silicon. The PV industry uses impurity gettering during phosphorus diffusion, Al-doped back surface field formation, and hydrogenation from the amorphous silicon nitride antireflection layer during contact firing, often with varying degree of success.

Screen-printing is a simple, rapid, and cost-effective technique for forming contacts for solar cells. The method of forming the emitter controls the bulk minority carrier lifetime of the cell, the ease of forming the screen-printed contacts and the quality of the p-n junction after contact co-firing. The emitter formation involves phosphorus spray or spin-on followed by drive-in in the IR belt furnace and liquid source (POCl₃) in a conventional tube furnace.

POCl₃ emitters with high sheet resistance and screen-printed contacts have produced efficiency of >16% on 4-cm² EFG ribbon silicon [2]. The major feature of the cell was the processed minority carrier lifetime of 100 μ s, because of SiNx induced hydrogen passivation of bulk defects. In another study, we achieved efficiency of 15.5% 4-cm² screen-printed EFG ribbon

silicon solar cell [3] by using low sheet resistance emitter ($\sim 45\text{-}\Omega/\text{sq}$) formed by POCl_3 and a processed minority carrier lifetime of $80\text{ }\mu\text{s}$. However, only 15.1% and 14.1% efficiencies were obtained, respectively, for 4-cm^2 screen-printed EFG Si cells with emitters formed by IR belt with two-side and one-side coating before drive-in. In this study we investigate large area (100-cm^2) EFG ribbon silicon solar cells with screen-printed contacts using emitters formed by POCl_3 and high volume production at Schott Solar Inc. To eliminate the use of forming gas after the co-firing, we investigated the front silver paste that could produce high fill factor, low ideality factor, low junction leakage current and acceptable fill factor.

Device Fabrication

In this study, cells were fabricated on p-type, $200\text{-}300\text{ }\mu\text{m}$ thick, $3\text{ }\Omega\text{-cm}$ EFG silicon wafers provided by Schott Solar, Inc. Cell fabrication involved (a) emitters diffused at Schott Solar, Inc., on their high volume production line and (b) phosphorus diffusion in a POCl_3 furnace to form a $45\text{ }\Omega/\text{sq}$ emitter. A single-layer SiN_x AR coating was deposited on top of the n^+ -emitter at Schott Solar, Inc. Ag/Al paste (Ferro FX 3398) was screen-printed to form the back stripe and dried at 200°C . This was followed by screen-printed Al (Ferro FX 53-038) on the remaining backside. The front metal grid was then screen-printed on top of SiN_x AR coating. This was followed by contact co-firing in IR belt furnace after profiling to ascertain the wafer peak temperature.

Results and discussion

Model calculations show that to achieve a fill factor of ~ 0.78 , the junction leakage current must be $\leq 1 \times 10^{-8}\text{ A/cm}^2$, series resistance of $\leq 0.6\text{ }\Omega\text{-cm}^2$ shunt resistance of $\geq 1000\text{ }\Omega\text{-cm}^2$. These parameters are determined by a combination of the front Ag paste, emitter sheet resistance (junction depth) and peak firing temperature. The silver particle size and shape (spherical or flakes), the glass frit (aggressive or mild) and additives control the penetration depth of the silver crystallites into silicon. For the multicrystalline wafers, it is important to have a paste with less aggressive glass because of the presence of several orientations with different etching rates. We evaluated several commercial front Ag pastes on EFG Si wafers processed at Schott Solar, Inc. The front Ag paste that showed the most promise with EFG Si wafers was CL80-8729 from Heraeus Inc. (W. Conshohocken, PA).

To optimize the metal co-firing for EFG Si cells, we weighed each wafer after all the metal contacts were screen-printed. We used the middle of the range group of wafers to optimize the peak firing temperature. We then used this optimized value to co-fire twenty wafers of various weights between $5.9\text{--}8.9\text{ g}$. Figures 1-3 show, respectively, the fill factor, efficiency and open circuit voltage distribution for these twenty large area (100-cm^2) screen-printed EFG ribbon silicon cells. Fig. 1 shows a mean fill factor of 0.762 and a standard deviation of only 0.014 for twenty EFG Si solar cells. The fill factor varied from 0.72 to 0.78 because of the varying weight. Variation in the silicon nitride thickness might also have contributed to the fill factor variation. Note: the mean value of the short circuit current density was 30.6 mA/cm^2 and maximum of 31.5-mA/cm^2 .

Figure 1: Fill factor distribution for 20 EFG ribbon silicon cells using CL80-8729 front silver paste from Heraeus Inc and emitters by SCHOTT Solar Inc.

Figure 2: Efficiency distribution for the 20 EFG ribbon silicon solar cells with screen-printed contacts using CL80-8729 paste from Heraeus Inc and SCHOTT Solar Inc., emitters.

In an attempt to improve upon these efficiencies, we explored POCl_3 emitters to take advantage of the two side phosphorus bulk impurity gettering step to improve the bulk minority carrier lifetime in the finished cells. These POCl_3 emitters showed a mean and maximum open circuit voltage of 595 mV and 599 mV, respectively. The maximum short circuit current density, fill factor and efficiency were, respectively, 31.2 mA/cm^2 , 0.764 and 14.2%. The series resistance for all the cells was lower than $1 \text{ } \Omega\text{-cm}^2$. The shunt resistance also was greater than $3000 \text{ } \Omega\text{-cm}^2$ for all the cells. However, the high ideality factor of >1.3 caused the lower fill factor and

therefore lower efficiency than the EFG cells using the SCHOTT Solar Inc., emitters. More work is underway to understand the cause of high n-factor.

Figure 3: Open circuit voltage distribution for 20 EFG ribbon silicon solar cells with screen-printed contacts using CL80-8729 paste from Heraeus Inc and SCHOTT Solar Inc., emitters.

Conclusions

We have achieved high quality contacts on large area (100-cm^2) screen-printed planar EFG ribbon silicon solar cells. We use a combination of emitters diffused at SCHOTT Solar Inc., on their high volume production line, CL80-8729 front Ag paste from Heraeus Inc., and optimized co-firing. A maximum fill factor of 0.776 was produced for the best cell with an efficiency of 14.6%. The open circuit voltage and the short circuit current were only 595 mV and 31.5-mA/cm^2 , respectively. To improve the open circuit voltage and current based on effective gettering of bulk impurity, the POCl_3 emitter was explored. However, this showed a modest 4 mV improvement in the open circuit voltage with lower short circuit current density, fill factor and efficiency. More investigation is thus needed to optimize the diffusion process.

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Impact of Intrinsic Buffer Layer Thickness on the Open-Circuit Voltage in aSi/p-cSi Heterojunction Solar Cells

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Abstract

Heterojunction aSi/p-cSi solar cell simulations were performed to assess the impact of the thickness of the intrinsic buffer layer on open-circuit voltage (V_{OC}). The simulation results indicate that band-bending in the absorbing substrate (which is directly related to the open-circuit voltage) is inversely related to the intrinsic buffer thickness when the hetero-interface defect density is very low. The simulations also show that the only n-aSi/i-aSi/p-cSi heterostructure where an increasing intrinsic buffer thickness results in V_{OC} improvements is one where the quality of the buffer layer improves with increasing thickness.

Introduction

The current high-water benchmark for the aSi/cSi heterostructure is Sanyo's HIT cell, which has achieved high efficiencies of 21% with open-circuit voltages as high as 719mV on a $\sim 100\text{cm}^2$ n-base cSi cell. Most academic research work however, has been focused on the more common p-type substrates with NREL's 711mV and 18.18% on 1cm^2 cells being the highest reported open-circuit voltage and efficiency [2, 4, 7, 8]. One of the stumbling blocks to achieving Sanyo's results on p-type substrates has been optimization of the intrinsic buffer layer that lies between the p-doped crystalline silicon absorbing layer and the n-doped aSi emitter (Figure 1).

Figure 1. Schematic and band-diagram (not to scale) of heterostructure modeled in AFORS-HETv2.0

There is wide agreement in literature that an intrinsic buffer between the crystalline substrate and doped amorphous emitter is necessary for obtaining less defective interfaces since the interface between doped aSi and cSi is more defective than that between i-aSi and cSi [2,4,7]. However, on p-type crystalline substrates, there is disagreement in literature on the *optimum thickness* of the intrinsic buffer and its impact on V_{OC} . Open circuit voltages of over 650mV have been reported on cells with both 5nm and 40nm thick i-aSi buffer layers and there is no experimental consensus on the variation in V_{oc} with buffer thickness. These conflicting experimental results seem to indicate that the buffer layer may have a role that goes beyond simply separating the n-aSi emitter and the p-cSi absorber. In an attempt to clarify these discrepancies, simulations were

used to examine how a buffer layer affects the factors determining V_{oc} . The common equation showing the factors affecting V_{oc} is shown in Equation 1 [11]:

$$V_{OC} = qV_{b2} - kT \ln[(qN_A S_i)/(J_{SC})] \text{ ————— Equation 1}$$

Where V_{b2} is band-bending in the p-cSi base and S_i is the recombination velocity at the aSi/p-cSi interface. The other symbols in Equation 1 have their usual meanings. The simulation results discussed here indicate that, given ideal interfaces, **V_{b2} and thus V_{OC} are functions of the buffer layer thickness**. This relationship does not show up in Equation 1, since it is derived from equations that describe equilibrium in homojunctions.

Modeling Details

AFORS-HET v.2.0 released by the Hahn-Meitner Institut was used to model the 1D structure shown in Figure 1. Table 1 lists the parameters used in modeling each layer.

	p-cSi	aSi
<i>Electron Affinity (eV)</i>	4.03	3.9
<i>Band-gap (eV)</i>	1.12	1.72
<i>N_c/N_v (cm^{-3})</i>	2.8e19/1.04e19	1e20/1e20
<i>Electron/Hole mobility (cm^2/Vs)</i>	1040/412	5/1
<i>Donor Concentration (cm^{-3})</i>	-	1e20 (n^+ -aSi)
<i>Acceptor Concentration (cm^{-3})</i>	1.5e16	0.1 (i-aSi)

Table 1. List of parameters used in modeling the aSi layers and the cSi layer.

The p-type cSi absorber was modeled with a point defect with a density of $1 \times 10^{11} cm^{-3}/eV$ at 0.55eV above the valence band edge. The aSi layers were modeled as having a Gaussian distribution of defect states with the distribution details shown in Figure 2. The p-type cSi/i-aSi interface was modeled as a 1nm thick i-epitaxial layer with a constant defect density at all bandgap energy levels. A ‘perfect’ interface was modeled with the epitaxial layer defect density set to $1 \times 10^{14} cm^{-3}$ since this defect density was low enough to be nearly indistinguishable from a zero defect density interface. This allows us to ignore the effect of a defective c-Si/i-aSi interface and isolate the impact of the buffer layer itself without assuming a zero-recombination interface.

Figure 2. Gaussian distributions used in modeling the defect densities in the (a) i-aSi emitter and (b) n-aSi buffer layers.

Simulation Results and Discussion

Equation 1 shows that the open-circuit voltage is directly proportional to band-bending in the crystalline base. In a homojunction, band-bending across the junction is dictated only by the relative doping concentrations on either side of the junction:

$$V_b \propto \ln(np/n_i^2) \quad \text{—— Equation 2}$$

For an n-aSi/i-aSi/p-cSi heterojunction however, Equation 2 does not provide a complete description of band-bending. Simulations of energy band diagrams and LIV curves show that:

1. Only **total** band-bending (V_b) is a function of the relative doping concentrations
2. The distribution of the total band-bending across the aSi layers and the crystalline absorber vary as a function of the i-aSi buffer thickness.

The plots in Figures 3 illustrate these two points. Figure 3(a) shows that while total band-bending is constant for a given n/p concentration ratio, the distribution of band-bending across the crystalline and the aSi layers (V_{b2} and V_{b1} respectively) depends on the i-aSi buffer layer thickness. Band-bending in the n- and i-aSi layers (V_{b1}) have a roughly linear dependence on the i-aSi buffer thickness while band-bending in the crystalline base has a roughly *inverse-linear* relationship with i-aSi buffer layer thickness. Figure 3(b) shows that V_{oc} also has a roughly *inverse-linear* relationship with i-aSi buffer layer thickness, i.e. as the intrinsic buffer becomes thicker, both V_{b2} and V_{oc} drop which is in agreement with Equation 1.

Figure 3. (a) V_{b2} and V_{b1} dependence on i-aSi buffer layer thickness (b) V_{b2} and V_{oc} dependence on i-aSi buffer layer thickness, as obtained through simulation of n⁺-aSi/i-aSi/p-cSi heterojunction cells. n⁺-aSi doping = $1e20cm^{-3}$; p-cSi doping = $1e15cm^{-3}$.

These simulation results indicate that in aSi/cSi structures with a ‘perfect’ hetero-interface, a thicker buffer layer should reduce V_{oc} . This conflicts with some published experimental data that show V_{oc} increasing with increasing i-aSi thickness, and achieving a maximum value for buffer thicknesses as high as 40nm [7]. However Sanyo’s HIT cells limit the total thickness of the doped and intrinsic aSi layers to 10nm while work at NREL on HWCVD deposited aSi layers on p-type cSi heterojunction cells have also limited the i-aSi layer thickness to 5nm or less [2, 8, 9]. Sanyo and NREL have the highest reported open-circuit voltages on n and p-type substrates

respectively (700mV+) and their results lend experimental support to our simulation results which show that thicker buffer layers are detrimental to high open-circuit voltages. In addition, real-time *in-situ* spectroscopic ellipsometry (SE), Fourier transform infrared spectroscopy (FTIR) and optical second harmonic generation (SHG) measurements during film growth and *ex-situ* measurements after film growth have been used to show that unless the substrate is properly prepared prior to aSi deposition and optimum deposition conditions are used, unintentional growth of a high defect density epitaxial layer followed by a defective i-aSi/i-cSi mixed phase layer will occur, with the layers persisting for tens of nanometers [4, 6, 9, 10]. In such cases, films that are many tens of nanometers thick need to be grown before growth of purely amorphous material occurs. This description of i-aSi growth with gradually improving film quality agrees well with experimental data showing V_{OC} increasing with increasing buffer layer thickness and leveling off (perhaps at the onset of the mixed phase growth) followed by another increase in V_{OC} after several tens of nanometer of film growth (which may mark the onset of purely amorphous film growth) [4, 7].

Simulation results from multiple models incorporating defective interface layers (Figure 4) seem to support the theory that multi-stage growth of the intrinsic buffer is responsible for experimental results that show V_{OC} increasing with buffer thickness. Structure C, which models the multi-stage growth process described above is the *only* one of the modeled structures to show an increase in V_{OC} with increasing buffer layer thickness (Figure 6). Note that the “intrinsic buffer” in these structures can consist of varying thicknesses of both intrinsic epitaxial and intrinsic amorphous layers of varying defect densities. The i-aSi/p-cSi interface defect densities were derived from published experimental data [3].

Figure 4. (a) Structure described in Figure 1; (b) Heterostructure with an epitaxial layer with p-cSi/i-aSi interface defect density = $1e18-1.5e19 \text{ cm}^{-3}$. (c) Heterostructure simulating 20Å epitaxial growth with epi/i-aSi interface defect density = $1e18 \text{ cm}^{-3}$, followed by i-aSi growth of varying quality. The white i-aSi layer, models a purely amorphous film while the grey later models a defective/mixed-phase amorphous layer.

As in the case of the low defect-density/'perfect' hetero-interface structure, Structure B, which incorporates a highly defective epi-layer at aSi/cSi interface, shows an inverse relationship between total buffer thickness and V_{OC} (Figure 5) which lends support to the theory that the sole role of the intrinsic buffer is to separate the crystalline silicon (substrate or epi-layer) from the doped aSi emitter. Once a uniform and purely amorphous intrinsic layer covers the entire substrate, further deposition of intrinsic material will hurt V_{OC} (assuming that subsequent deposition also results in purely amorphous growth). Figure 5 also shows that in a defect free or low defect n-aSi/p-cSi interface, growing the doped aSi emitter directly on the crystalline base gives the highest V_{OC} .

Figure 5. V_{OC} variation with intrinsic buffer thickness for Structure B. The ‘perfect’ n-aSi/p-cSi interface has a defect density of $1e14\text{cm}^{-3}$. The defective n-aSi/p-cSi interface has a defect density of $1e20\text{cm}^{-3}$. For all non-zero buffer layers, the i-aSi/p-cSi epi-interface defect densities are indicated [3].

Structure C attempts to model realistic film growth as it uses an intrinsic buffer layer of gradually increasing quality. The epi-layer thickness and some of the defect densities used were based on spectroscopy measurements and high-resolution TEM cross sections in literature [3, 8, 10]. Figure 6 shows the V_{OC} variation for this structure.

Figure 6. V_{OC} variation with intrinsic buffer thickness for Structure C. The ‘perfect’ n-aSi/p-cSi epi-interface has a defect density of $1e14\text{cm}^{-3}$. In the epitaxial growth phase, the n-aSi/epi-cSi interface defect density is $1e20\text{cm}^{-3}$. Other relevant defect densities are listed in Figure 4.

The initial 20 Å of the buffer models epitaxial growth, with the epi-layer directly contacting the n-aSi emitter (which is why a high interface defect density of $1 \times 10^{20}\text{cm}^{-3}$ is used). The i-aSi layer in Structure C models both mixed-phase growth and purely amorphous growth depending on its thickness. The first 1nm layer of i-aSi has a Gaussian defect density distribution (Figure 2) with peak defect density of $1 \times 10^{20}\text{cm}^{-3}$ and is used to model a highly defective amorphous/mixed-phase layer film contacting the n-aSi emitter. The next 2-3nm of the intrinsic buffer models purely amorphous growth with a lower peak defect density of $2e19\text{cm}^{-3}$. As Figure 6 shows, we see V_{OC} rising with increasing buffer thickness till we have purely amorphous growth. Any

further growth reduces V_{OC} . As mentioned earlier, this was the only structure of the several that were simulated that showed this behavior. This indicates that imperfect multi-stage growth of the intrinsic buffer layer and the resulting high defect density at the interface to the n-aSi emitter is the reason that V_{OC} enhancement with increasing buffer thickness is sometimes observed. It should be noted however that Structure C is an approximation of real amorphous film growth since a real mixed phase film is inhomogeneous in all three dimensions which is a characteristic that cannot be accurately represented in a 1D model.

Conclusions

Based on our simulations, the only role of the buffer layer in aSi/cSi heterojunction solar cells is to provide a cleaner hetero-interface by separating the n-aSi and p-cSi layers. In the ideal case of a perfect hetero-junction, use of an intrinsic buffer is detrimental to the open-circuit voltage. In real devices with defective interfaces, a trade-off is made between a small loss in V_{OC} from the presence of a buffer layer and the large gain in V_{OC} that results from having a far less defective hetero-interface. The simulation results in this work and supporting experimental data from other research groups point to i-aSi buffer layer growth that involves an initial growth phase of highly defective material being the most likely cause of experimental data in literature that show V_{OC} improvements with increasing buffer layer thickness.

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Fabrication and analysis of high efficiency textured String Ribbon silicon solar cells

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Abstract

Solar cell efficiencies as high as 16.8% (4 cm^2) have been achieved on String Ribbon Si at Georgia Tech, using PECVD SiN_x and rapid co-firing of screen-printed contacts to achieve very effective hydrogenation of the bulk defects. Textured String Ribbon is investigated to further improve solar cell efficiencies by combining the merits of the above technologies. Characterization of textured String Ribbon wafers revealed a reduction in weighted reflectance by approximately 2 %. This translates to a potential increase of 1 – 1.5 mA/cm^2 in the J_{sc} and cell efficiencies over 17%. The best cell (4 cm^2) in this study had an efficiency of 16.8% and was mainly limited by defect inhomogeneity identified by LBIC analysis.

Introduction

String Ribbon Si is an inexpensive material for the fabrication of solar cells and shows promise as a cost-effective alternative to single crystal silicon. However owing to thermal gradients during growth and its low-cost crystal growth technique this material has a high density of grain boundaries, dislocations, twins and other physical defects. This added with the presence of metal impurities in the bulk reduces the average as-grown lifetime to 1-10 μs . Effective increase in the bulk lifetime needs to be included in the fabrication process to produce high cell efficiencies. This is achieved in part by the gettering during POCl_3 diffusion and further by SiN_x induced hydrogenation during the contact firing process. The aforementioned techniques were used on 4 cm^2 cells and a peak efficiency of 16.8% was reported earlier on cells with screen-printed contacts[1]. The high efficiency cells used SiN_x as the single layer antireflection coating (SLAR) with no surface texturing.

Texturing has been shown to significantly increase current and improve efficiency by up to 1 % absolute on both single crystalline and multicrystalline Si solar cells[2]. Texturing of crystalline Si has been achieved with the use of acidic and basic solutions[3] as well as reactive ion etching (RIE)[4]. The effect of texturing on String Ribbon Si is studied and its potential for high efficiency low-cost solar cells is discussed in this study. Data from fabricated solar cells as well as reflectance measurements and LBIC analysis are used to support the application and further investigation of textured String Ribbon Si solar cells for low-cost crystalline Si photovoltaics.

Device Fabrication

In this study 2.0 – 3.0 $\Omega \text{ cm}$ boron doped, p-type untextured and textured String Ribbon Si samples, obtained from Evergreen Solar, Inc. (Marlboro, MA) were used. The

thickness of untextured wafers was 300 μm while the textured wafers were 200 μm . After the initial wet chemical cleaning process, n^+ emitter diffusion was performed in a POCl_3 tube furnace to achieve a sheet-resistance of 90 – 100 $\Omega/\square$. A SiN_x SLAR coating with a refractive index of 2.0 and a thickness 800 $\text{\AA}$ was deposited using a low-frequency (50 kHz) plasma-enhanced chemical vapor deposition (PECVD) reactor. The contacts were formed using screen-printing techniques. A commercial Al paste was screen printed on the entire rear surface and a commercial Ag paste was used to form the front grid contacts. Contact firing was performed in a rapid thermal processing (RTP) system (AG associates Heatpulse 610). This enables the simultaneous formation of the Al-doped Si back surface field (Al BSF) and front contacts through the SiN_x while promoting the defect hydrogenation using the hydrogen released from the SiN_x ARC. Several 4 cm^2 cells were fabricated on each String Ribbon wafer and were isolated using a dicing saw and subjected to a forming gas anneal (FGA) before testing and analysis.

Device Characterization and Analysis

Reflectance Measurement

The reflectance measurements and the calculation of weighted reflectance are critical to determining the improvement in the light trapping capacity of these textured wafers. Reflectance measurements were made at each stage of the processing to track the change in weighted reflectance. As can be seen in Fig.2, there was difference of nearly 4% between the planar and textured wafers in their as-grown state it reduced to $\sim 2\%$ after deposition of SiN_x SLAR coating. While this decrease in reflectance is less than that typically observed in single crystalline materials, this represents a substantial potential increase in the current (1-1.5 mA/cm^2) and cell efficiency (0.5% absolute) of String Ribbon cells.

Fig.1. Comparison of reflectance between untextured String Ribbon, textured String Ribbon and textured FZ

Fig.2. Weighted reflectance as calculated at various stages of processing

Solar Cell Results

The average and best cells results from textured String Ribbon Si solar cells are summarized in Table 1. The high V_{oc} values on all these cells indicate an effective hydrogenation from the PECVD SiN_x . The J_{sc} obtained in the textured cells was higher than those obtained on the untextured cells by an average of 1 mA/cm^2 and current densities of over 35.5 mA/cm^2 are the highest reported on String Ribbon Si solar cells with screen printed contacts. In the case of the screen-printed textured wafers, the best efficiency was 16.8 % which is equal to the best on the untextured String Ribbon Si reported earlier[1] and also comparable to untextured screen-printed FZ Si cells. It is proposed that with an improved lifetime and optimized contact firing, the V_{oc} can be improved and the efficiencies can reach values higher than those on untextured String Ribbon.

Table1. Average and Best solar cell performance parameters

	ID	V_{oc} (mV)	J_{sc} (mA/cm ²)	Efficiency (%)	FF	# of cells
Average	Textured String Ribbon	608	35.0	16.0	0.75	22
Best	SR1-3-1	613	35.7	16.8	0.77	

LBIC Measurement

The highest V_{oc} measured on textured cells in this study was 613 mV with an average V_{oc} of 608 mV. While this displays good passivation of defects, the cells in this study show a lower V_{oc} than the best values reported on untextured wafers (631 mV)[1]. To understand this, the best cell was subjected to a light beam induced current (LBIC) mapping. The map of LBIC response of this cell along with the map of the 16.8% untextured cell is shown in Fig. 3. The results indicate that the material inhomogeneity is higher on the textured cell than on the untextured cell with a lower percentage of high LBIC response

regions (≥ 0.60 A/W) on the textured cell indicating regions of low lifetime. Earlier studies have shown that material inhomogeneity can negatively impact cell V_{oc} [5]. This suggests that improved material homogeneity achieved during crystal growth or cell processing of the textured cell can lead to an improvement in V_{oc} and a consequent improvement in cell efficiency above 17%.

Fig.3. Comparison of LBIC maps from untextured and textured String Ribbon

Fig.4.Distribution of LBIC response for untextured and textured String Ribbon

Conclusion

Analysis of reflectance revealed that surface texturing of String Ribbon wafers produced a weighted reflectance that is $\sim 2\%$ lower than the untextured surface in a finished cell. Cell data supported these results with an average J_{sc} 1 mA/cm^2 higher than in untextured cells. However solar cells fabricated in this study reached an efficiency of 16.8%, which equals the previously reported best efficiency due to the presence of material

inhomogeneity. With improved material homogeneity and optimized processing for textured surfaces it is expected that cell efficiencies on textured String Ribbon will soon exceed 17%.

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a-Si/c-Si Heterojunction for Interdigitated Back Contact Solar Cell

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Abstract: Initial experimental and numerical simulation results for interdigitated back contact silicon heterojunction (IBC-SHJ) solar cell, which combines the high voltage potential of heterojunction solar cells while avoiding the absorption losses and allowing high short circuit currents, are reported. Cells without intrinsic buffer layers were fabricated as a proof of concept. The cells with intrinsic buffer layer show open circuit voltage of 683 mV, but with low fill factors, and optimization to reduce this effect is undergoing. Two-dimensional theoretical simulation through software package Sentaurus Device is applied to model the device, where distribution of trap states and thermionic emission were considered for a-Si:H material and a-Si:H/c-Si hetero-interface, respectively. The model results can be correlated to both J-V measurements and LBIC scans. Both experiments and simulation show that the performance of IBC-SHJ solar cell depends on the front surface recombination velocity. Also the model demonstrates that the IBC-SHJ solar cells allow efficiencies in excess of 22%.

1. Introduction

The rapid market growth of silicon (Si) solar cells is driving the development of devices using thinner Si wafers and higher efficiency technologies [1]. An interdigitated back contact silicon heterojunction (IBC-SHJ) solar cell [2], which combines the advantages of both IBC [3] and SHJ [4] techniques, is an attractive device structure for achieving this. IBC-SHJ combines the high voltage potential of heterojunction solar cells while avoiding the absorption losses in these structures and allowing the high short circuit currents of a rear junction back contact solar cell. It also has the advantage of entirely low temperature processing sequence [2]. In this work, initial experimental results for IBC-SHJ cells without and with intrinsic buffer layers are shown. Software package Sentaurus Device is applied to get two-dimensional modeling of IBC-SHJ solar cell. Also the dependence of IBC-SHJ cells to the front surface passivation is discussed both experimentally and theoretically through numerical simulation.

2. Experiments and initial cell results

The schematic of the IBC-SHJ solar cell is shown in Figure 1. The cells were fabricated on 300 μm thick, polished, n-type float-zone silicon wafer with resistivity of 2.5 Ωcm . All a-Si:H layers, intrinsic, p-type and n-type, were deposited in a multi-chamber direct current (DC) plasma enhanced chemical vapor deposition (PECVD) system at 200°C. The front surface was passivated with a 20 nm intrinsic a-Si:H layer followed by AR coatings composed of Indium Tin Oxide (ITO) and MgF_2 , deposited by sputtering and electron beam evaporation respectively. This surface passivation/antireflection structure is not ideal for high J_{SC} but provided a means of evaluating the device performance and the utility of the structure as a diagnostic tool to evaluate surface recombination. At the back of the wafer, the emitter and contacts consist of interdigitated p- and n-type a-Si:H layers respectively at a thickness of 20 nm. A 200 nm thick aluminum deposited by electron beam evaporation is used as a robust contact

for testing. For the case of with back surface intrinsic buffer layer, an 8 nm intrinsic a-Si:H was added to the whole back surface before the deposition of p-/n- type a-Si:H layers. The interdigitated pattern was created by two-step photolithography processing where the p-region has lateral dimension of 1.2 mm and n-region is 0.5 mm wide. The numbers of p-strip and n-strip are fixed at 5 and 4 respectively with a cell area of 1.37 cm². The separation between p- and n-regions is $\sim 2 \mu\text{m}$ for the cell without rear intrinsic buffer layer, which is formed naturally by undercutting during the etching process. While in the cell with rear intrinsic buffer layer, a separation of $\sim 50 \mu\text{m}$ was achieved through masking during photolithography, since the etching process should be avoided to keep the passivation effect of the back surface intrinsic buffer layer.

Figure 2 shows the initial results of J-V curve under AM1.5 illuminations, where the solid curve is the sample without intrinsic buffer layer, and the dashed curve is the one with i-

layer. It can be seen that for the case without i-layer, fill factor (FF) is high (74%) and there is no evidence of shunting between the p- and n-type regions, which demonstrates the robust nature of the process and proves the concept of the structure. For the case of with passivating i-layer, a higher V_{OC} of 683 mV and a larger J_{SC} of 36 mA were obtained, while the FF is low and the JV curve shows “S-shape”. This S-shape JV curve has also been observed in the front junction cell [5] and was resolved through process optimization. Optimizations to reduce this effect in IBC-SHJ solar cell are undergoing.

3. 2D Modeling with Sentaurus Device

To better understand the performance of IBC-SHJ solar cell, numerical simulation of the device is studied through Synopsys device modeling package Sentaurus Device (version Y-2006.06). The structure of IBC-SHJ solar cell used in simulation is similar to Fig.1 except that the front surface AR coatings and the buffer i-layer are replaced by a single passivation layer of SiN_x (70nm). This ideal front surface simplifies the cell structure and it can still simulate the device performance very well with only a little difference in current due to the different anti-reflection effect.

The three governing semiconductor equations, Poisson equations and the electron and hole continuity equations, together with drift-diffusion model [6] in Sentaurus Device were used, and the impurity scattering and carrier-carrier scattering were considered. The Auger and Shockley-Read-Hall recombination were modeled as a function of doping concentration. For the a-Si layers, the critical parameters are the energy distribution of

Figure 1. Schematic picture of the IBC-SHJ structure, where two p-strips and one n-strip are shown. For clarity, the cell thickness is greatly exaggerated.

Figure 2. Illuminated (AM1.5) J-V for IBC-SHJ cells, without (solid curve) and with (dashed curve) back surface buffer i-layer.

the exponential band tails, and the Gaussian distribution of the mid-gap trap states. They were chosen based on Reference [7] and were tuned to fit the properties, dark and light conductivity, of deposited a-Si layers. For c-Si/a-Si interfaces at the back surface, a thermionic emission model was used, in which the distribution function of the interface defect is modeled by two capture cross-sections, one for the holes and one for the electrons. An AM1.5G solar spectrum is used for the optical generation to simulate the current density-voltage (J-V) curve under standard one-sun illumination conditions at an intensity of 100 mW/cm².

4. Effect of front surface passivation

It was noticed that the performance of IBC-SHJ solar cell depends on how the front surface is passivated [2]. Figure 3 shows the reflection corrected internal quantum efficiency (IQE) for the same IBC-SHJ cell characterized at three stages in the process sequence: before anti-reflection coating (ARC), after ARC, and after annealing with ARC. The cell's performance decreases after application of the ARC, but improves after annealing to exceed the initial device performance. The modeling software PC1D was used to fit the IQE curves (dashed lines), and extract the front surface recombination velocity, S , increases from 152 cm/s to 299 cm/s after ARC, while decreasing to 82 cm/s after annealing. This change of front surface recombination causes the different cell performance.

Simulation of IBC-SHJ solar cell with different front surface recombination velocity (S) at SiN_x/c-Si interface was performed and the resulting J-V curves are shown in Figure 4. As seen, both J_{SC} and V_{OC} increase as S decreases, resulting in higher cell efficiency. Since most carriers are generated near the front surface, while the p-n junction is far at back surface, high front S would cause carrier recombination before they reach the back junction. Hence front surface passivation is especially important for IBC-SHJ solar cell. With low front S of 10 cm/s, a value that is achievable and consistent with lifetime measurements of 2.2 milliseconds, the 2D modeling shows that IBC-SHJ cell can attain an efficiency of 22% when back surface is well passivated.

Figure 3. Same sample at three stages show the IBC-SHJ cell performance depends on the front surface recombination velocity (S).

Figure 4. Simulated J-V curve for IBC-SHJ cell with different front surface recombination velocity (S).

To further investigate the device performance, the cell with $S=80$ in Fig.3 was measured using light beam induced current (LBIC) and compared to the theoretical calculations, where the LBIC line scan was simulated using a $50\mu\text{m}$ wide white light beam scanning from left to right on the device. The simulation matches the experimental results well and they are shown in Figure 5. It can be seen that p-region has higher current than n-region, this is because that carriers generated at the p-type strips with the collection junction are more likely to be collected than carriers above the n-type strips, which have to diffuse laterally to a p-type strip. The high degree of correlation between the LBIC measurement and the Sentaurus model further confirms the validity of the determination of the front surface recombination velocity at 80 cm/s in Fig.3.

Figure 5. Comparison of theoretical model and experimental data for a LBIC scan.

5. Conclusions

Initial experimental and numerical simulation results for interdigitated back contact silicon heterojunction (IBC-SHJ) solar cell were presented. IBC-SHJ solar cells without intrinsic buffer layers proved robust nature of the structure. The cells with intrinsic buffer layer have shown V_{OC} of 683 mV and J_{SC} 36 mA , but with low FFs, and optimization to reduce this effect is undergoing. 2D modeling through Sentaurus Device is applied to simulate the device. Both experiments and modeling show that the front surface passivation is very important for IBC-SHJ solar cell. LBIC line scan was simulated and matched with experimental result well. The simulations suggest that by reducing front SRV to 10 cm/s , efficiency of 22% can be achieved for IBC-SHJ solar cell.

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Deep Level Transient Spectroscopy Study of Dislocations in SiGe/Si Heterostructures: The Impact of Fe contamination and Phosphorous Gettering

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ABSTRACT

A SiGe/Si sample containing high density of dislocations were examined by DLTS after Fe contamination and phosphorous gettering. It was found that in the region with 10^7 cm^{-2} dislocations, phosphorous gettering can effectively remove both dissolved and precipitated Fe impurities. Since the 10^9 cm^{-2} dislocations in the adjacent 2 μm thick SiGe layer are effective sinks for self-interstitials, we suggest that self-interstitial injection is not an essential factor for Fe gettering.

INTRODUCTION

Clean dislocations generally exhibit weak electrical activities at room temperatures and are believed to be associated with shallow trap levels. After decorated by impurities, dislocations become strong minority carrier recombination sites and adversely effect device performance. Since extended structural defects are one of the major lifetime limitation factors in mc-Si, and impurity decoration impacts the effectiveness of H-passivation of structural defects, knowledge on the electrical activity of dislocations and dislocation-impurity interactions [1] is important for both silicon solar cell and IC device application. In this paper, we examined Fe decoration and release at dislocations by Deep Level Transient Spectroscopy (DLTS) using a heterostructure SiGe/Si sample which contains misfit dislocations at a well controlled depth.

EXPERIMENTAL

The SiGe/substrate Si heterostructure used in this study was grown by chemical vapor deposition on a lightly doped p-type Si wafer. The structure consists a 25 nm strained-Si / 1.3 μm $\text{Si}_{0.75}\text{Ge}_{0.25}$ / 2 μm $\text{Si}_{1-x}\text{Ge}_x$ graded layer / lightly doped silicon buffer on a Si substrate. SIMS shows that the SiGe/Substrate Si interface is at 3.3 μm , and TEM cross-section image shows a band of dislocations from 1.2 to 3.3 μm . The SiGe layer was non-intentionally doped and SIMS measurements showed that the Boron concentration was below the detection limit, $\sim 2 \times 10^{14} \text{ cm}^{-3}$. The Ge concentration gradient was $\sim 10\%/ \mu\text{m}$ for the graded layer, which gives rise to a misfit dislocation density on the order of 10^9 cm^{-2} . Iron contamination was realized by dipping the sample in an Fe solution [2] (140ml H_2O : 0.6ml NH_4OH (29%): H_2O_2 (32%): 0.1ml Fe spiking solution 1mg Fe/1ml 2% HNO_3) for 5 min, followed by 900°C drive-in annealing in Ar in a vertical furnace, and finally quenching in ethylene glycol. P-diffusion gettering was performed by dipping samples in 10% wt phosphorous acid for 1 min and drying with compressed N_2 , followed by 900°C 40min and 800°C 2h annealing in Ar ambient. Al Schottky diodes were prepared on as-grown and annealed samples by thermal evaporation through shadow mask. For the p-diffused sample, mesa N^+P diodes were prepared by wax covering and chemical etching. Ohmic contacts were produced by rubbing the eutectic Ga-In alloy on the backside of the samples. Fourier-transform DLTS and Capacitance-Voltage measurements were performed on a BioRad DL8000 DLTS system. Fourier coefficient

$b_1 = \frac{2}{T_w} \int_0^{T_w} C(t) \cdot \sin\left(\frac{2\pi \cdot t}{T_w}\right) \cdot dt$ was used in all DLTS plots presented in this article, where T_w the time window for capacitance measurements.

RESULTS AND DISCUSSION

One sample was contaminated by Fe solution and annealed at 900°C for 1min followed by quenching. The sample was characterized by DLTS, see Fig. 1(a)-(c), with different reverse and pulse voltages after 4h and 48h of room temperature storage after quenching. From the 1MHz capacitances, the depletion depth at 1, 2, 4, 8V reverse biases are found to be 3.7, 3.9, 4.4, and 5.3 μm , respectively. The dielectric constant of SiGe alloy was obtained using linear approximation with $\epsilon_{\text{Si}}/\epsilon_0=11.7$ and $\epsilon_{\text{Ge}}/\epsilon_0=16$. The depletion depth calculated from the capacitance is deeper than the filling depth of deep levels by an amount of $\lambda = \sqrt{\frac{2\epsilon_{\text{Si}} \cdot \phi}{q \cdot N}}$, where ϕ is the difference between the deep

level and the Fermi level at the charge neutral region, q the electron charge, N the concentration of net negative charge in the depletion region. Since the epi layer doping is very low, deep levels due to defects are likely the major source regulating the free carrier and net-charge concentrations. Therefore, the probing depth in the SiGe layer cannot be determined because the λ distance cannot be calculated without detailed knowledge on trap concentration and corresponding trap level positions. Qualitatively, the λ distance will increase in the low doping buffer Si and SiGe layers, and smaller voltages will probe shallower regions.

Fig. 1. DLTS spectra measured at 4h and 48h after Fe contamination annealing and quenching. The reverse and pulse voltages are labeled in each figure. Time window $T_W = 20\text{ms}$.

For the Fe-B peak at 55K, the λ distance is 0.3 μm with a $6 \times 10^{14} \text{ cm}^{-3}$ substrate doping. The Fe-B pair concentration was calculated from equation

$$N_T = N_A \cdot \frac{2 \cdot d_0^2}{d_2^2 - d_1^2} \cdot \frac{\Delta C}{C_R} \quad [1]$$

where N_A is the acceptor concentration in the substrate, ΔC is the amplitude of the capacitance transient, C_R the reverse bias capacitance, d_2 and d_1 are the trap filling depth at reverse and pulse reverse bias voltages, and d_0 is the depletion depth at reverse bias. The Fe-B concentrations are listed in Table I. Note that during room temperature storage, the Fe-B concentration increased for 2.5 to $3.4 \times 10^{13} \text{ cm}^{-3}$. The variation across depth is likely reflecting the experimental uncertainty. The DLTS peak at 245 K in Fig 1.(a) is due to interstitial Fe (Fe_i) impurities, which give an energy level at 0.4 eV above the valance band. Calculated from Fig. 2(a)-(b), the concentration of Fe_i at 4 hours after quenching is $1.6 \times 10^{13} \text{ cm}^{-3}$ at depth 3.8 to $4.7 \mu\text{m}$, and $1.1 \times 10^{13} \text{ cm}^{-3}$ at depth 3.3 to $3.8 \mu\text{m}$. Since the strong DLTS band at 210 K in Fig. 1(b) and (c) only appears in Fe contaminated samples, and its amplitude is large in highly dislocated region, it is likely due to Fe precipitates near dislocations. TEM study of this sample shows that many dislocation loops (10^8 cm^{-2}) glided into the Si substrate. Although the Fe_i and Fe-B peaks in figure 1 (b) and (c) do not come from exactly the same depth, they show qualitatively that the disappearance of Fe_i was mainly accompanied by the increase of Fe-B peak, indicating non-effective Fe capture by 10^8 cm^{-2} of dislocations. During room temperature storage, the interstitial Fe impurities either pair with boron, or diffuse to existing Fe precipitates. It is suggested that the strain field due to dislocations is not likely to stably trap Fe_i impurities at room temperatures.

To study the efficiency of phosphorous gettering within highly dislocated regions, one sample contaminated by Fe solution was annealed at 915°C for 10 min, followed by 900°C for 20 min for Fe precipitation, and terminated by quenching. The sample was cut in two half pieces and one piece went through P-diffusion gettering. Figure 2 compares the DLTS spectra acquired from the 900°C , 1 min annealed (clean dislocations), Fe-precipitated, and the P-gettered samples. The reverse and pulse voltages labeled in figure 2 are for the 1 min annealed and Fe-precipitated samples, which have essentially same C-V curves. In order to examine the same depth region, a different set of bias and pulse voltages were determined for the P-gettered sample by noticing the abrupt change of the doping level at SiGe/Si interface.

Fig. 2. DLTS spectra of the SiGe sample after 900°C -1 min annealing, Fe contamination, and P-diffusion gettering. (a) $U_R=8\text{V}$ and $U_p=4\text{V}$ (b) $U_R=2\text{V}$ and $U_p=1\text{V}$. Time window $T_W = 20\text{ms}$.

The trap filling depth of the $8/4\text{V}$ spectra is from 3.8 to $5 \mu\text{m}$, where the dislocation density is approximately $1 \times 10^7 \text{ cm}^{-2}$. Fig. 2(a) shows that 10^7 cm^{-2} of clean dislocations gave no DLTS signals. For the case of $U_R=2\text{V}$ and $U_p=1\text{V}$, the probing depth reached the SiGe graded layer where the

dislocation density is on the order of 10^9 cm^{-2} . Note the weak DLTS signal from the high density clean dislocations. The 210K DLTS band due to Fe precipitates near dislocations is much stronger in the Fe-precipitated sample, compared to the Fe contaminated sample annealed at 900°C for 1min, see Fig. 1. After P-diffusion, the DLTS band at 210K disappeared in the deeper region where the dislocation density is low, and was reduced significantly in amplitude in the highly dislocated region, see Fig. 2. Note that dissolved Fe impurities (Fe-B pairs) were effectively removed by P-diffusion in both low and high dislocation regions. Self-interstitial injection during P-diffusion enhances the gettering of transition metals in substitutional positions. [3] Considering the 10^9 cm^{-2} dislocations in the adjacent 2 μm thick SiGe layer are effective sinks for self-interstitials, our results suggest that self-interstitial injection is not an essential factor for Fe gettering, and Fe impurities are likely to remain in interstitial sites at 900°C . The residual impurities left on dislocations after P-gettering might involve chemical binding at the dislocation core, which requires more energy to break. [4]

While the tail in the low temperature side of the 210K band suggests a distribution of trap energy levels in the bandgap, an Arrhenius plot of good quality was obtained from the 210K DLTS band, see Fig. 3. It was found that the trap has a hole capture cross-section of $2.4 \times 10^{-14} \text{ cm}^2$ and at 0.42 eV above the valance band. The corresponding trap concentration at 3.8~4.7 μm depth is $\sim 2.7 \times 10^{13} \text{ cm}^{-3}$. Khalil et al observed DLTS band of similar shape in Fe precipitated samples. [5] Their DLTS also uses numerical correlation of capacitance transients with a sine function, but with a pulse repetition rate of 17Hz (time window of ~58 ms). Compared with our DLTS results, the DLTS band in Ref [5] appeared at a higher temperature (~245K) even using a larger time window. The shift of the DLTS peak to lower temperature in our SiGe sample is likely due to the fact that the Fe-precipitates are formed at dislocations.

Fig. 3. Arrhenius plot of the 210K DLTS band due to Fe precipitates near dislocations.

In Summary, a SiGe/Si sample containing high density of dislocations were examined by DLTS after Fe contamination and phosphorous gettering. A strong DLTS band at 210K was observed in Fe contaminated sample, and was identified as Fe precipitates near dislocations. After P-diffusion, the DLTS band at 210K disappeared in the deeper region where the dislocation density is 10^7 cm^{-2} , and was reduced significantly in amplitude in the highly dislocated SiGe region. Considering that dislocations are effective sinks for self-interstitials, it is suggested that self-interstitial injection is not an essential factor for effective Fe gettering.

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Photovoltaic Manufacturing Initiative at Georgia Tech – An Update

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Abstract

The Manufacturing Research Center at Georgia Tech is addressing both fundamental and practical issues related to handling and inspection of thin crystalline silicon wafers used in the manufacture of photovoltaic (PV) cells. Work to date has resulted in the development of an instrumented robotic wafer handling test bed, characterization and analysis of wafer deformation and handling stresses when using Bernoulli grippers, measurement and analysis of thin wafer residual stresses, and development of a software framework for real-time monitoring of equipment used in solar cell manufacturing.

1. Introduction

The Manufacturing Research Center (MARC) at Georgia Tech has been addressing photovoltaic manufacturing issues under an NREL grant. The initiative has led to the creation of the Advanced Photovoltaic Manufacturing Laboratory (APVML) to address fundamental and practical issues related to handling and fracture of thin crystalline silicon wafers used in solar cells, measurement of residual and applied stresses due to processing and handling, and the development of factory information software tools for web-based real-time monitoring of equipment used in solar cell manufacturing. The lab is researching new and improved manufacturing techniques to enhance solar cell quality and yield, in order to lower the cost of PV devices. This paper summarizes the major accomplishments of the lab to date in the aforementioned areas.

2. Laboratory Description

The APVML contains the following equipment: i) instrumented robotic wafer handling and transport station with an automated wafer lifting and separation device, ii) a polariscope-based wafer residual stress

measurement system, and iii) computers running factory information systems software that monitor the robotic handling station.

The wafer handling station is equipped with a 4-axis SCARA robot and several wafer gripping devices including Bernoulli and vacuum grippers that are routinely used in the PV industry. The station is also instrumented with thin film force sensors to measure the wafer gripping forces and a laser displacement sensor to measure wafer deformation due to handling. Figure 1 shows a picture of the thin wafer handling test bed. Experimental and modeling studies have been carried out on Bernoulli grippers commonly used for automated handling of silicon wafers/cells in the PV industry. From the measured deformations, stresses induced in the wafer can be evaluated using finite element analysis. Figure 2 shows the measured wafer deformation and the corresponding maximum in-plane principal stress distribution in a 166 μm thick, cast 156mmX156mm polysilicon wafer held in the gripper. The end goal of the thin wafer handling research is to understand wafer breakage mechanisms and to develop new and improved ways for handling thin silicon wafers without breakage.

A critical aspect of preventing wafer breakage is the need for measuring the in-plane residual stresses in the wafer arising from prior process steps. The presence of large tensile residual stresses in the wafer, combined with tensile handling stresses, can lead to premature breakage of the wafer/cell. This project is leveraging prior work on residual stress measurement using infra-red polariscopy funded by NREL. Figure 3 shows a picture of the polariscope-based residual stress measurement system. Recent work has examined the effect of crystallographic orientation on the stress optic coefficient, and in turn the residual stresses. Since poly-silicon wafers have randomly oriented grains, accurate measurement of the residual stress requires that this effect be considered. Figure 4 shows the frequency of different grain orientations in cast wafers determined using X-ray diffraction. Table 1 shows the stress optic coefficients for typical grain orientations.

Georgia Tech continues to develop a software framework for Photovoltaic manufacturing based upon CAMX (Computer Aided Manufacturing using XML) to reduce the costs and complexity of PV manufacturing. CAMX is a set of standards that define XML messages for exchanging data among manufacturing equipment and applications. Originally, CAMX was developed for the electronics manufacturing industry, but now it is being extended to meet the needs of PV. Data produced from PV equipment is being mapped to the original CAMX messages and new messages (data structures) are being developed to accommodate the unique aspects of PV manufacturing.

A powerful feature of CAMX is its ability to transfer XML messages independent of message content. As a result, CAMX applications such as application servers and message brokers do not have to be modified for use in a new industry space.

Currently, Georgia Tech is working with PV tool providers and manufacturers to demonstrate the new message mappings and application web interfaces to display PV specific information. Initially, software wrappers are being used to translate native machine data to CAMX formats. The next step will be to embed software into PV machines tools so they are capable of ‘speaking’ the CAMX protocol natively. Making use of CAMX in PV manufacturing will reduce the costs of PVE products, allow for faster line reconfiguration and speed new installations.

3. Industrial Collaboration

Other important industry-oriented activities in this project include the following: i) survey of PV equipment and cell manufacturers’ R&D needs and priorities, ii) a workshop on PV Manufacturing to discuss industry R&D priorities, iii) new projects on residual stress measurement and handling with PV manufacturers such as Schott Solar, BP Solar, and GE Energy, iv) testing and evaluation projects on thin wafer handling using Bernoulli grippers with PV equipment makers such as MANZ Automation and OTB Solar, and v) discussions with equipment makers on factory information systems.

4. Conclusions

This research program addresses the handling, inspection and real-time web-based monitoring of crystalline silicon wafers used in PV manufacturing. Ultimately, the program aims to improve the quality and yield of thin silicon wafers. The research results are being made available to PV manufacturers.

5. Acknowledgements

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Figure 1. 4-axis wafer handling robot station.

Figure 2. (a) Wafer deformation (mm) for Cast 156 mm x 156 mm mc-Si wafer at 40 litres/min air flow rate, (b) Corresponding maximum in-plane principal stress in wafer.

Figure 3. Polariscope-based residual stress inspection system.

Figure 4. Frequency of grain orientations in cast silicon wafers.

Table 1. Typical result of stress optic coefficients

Orientations (φ)	100	111	111	111	210	211	321	322	421
Pole angle (θ)	20	53	-5	65	-8	31	-100	106	73
Stress optics coefficient($10^{-11} \times \text{Pa}^{-1}$)	2.40	2.54	2.53	2.55	2.08	2.75	1.87	2.35	1.75

Figure 5. Initially, software wrappers are being used to accomplish CAMX communication with PV Manufacturing Equipment (left). The next step is to embed software directly into the machine to accomplish native CAMX communication (right).

Response of *n*-type mc-Si to large variations of gettering and hydrogenation

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Abstract

The minority charge carrier recombination behaviour of *n*-type multicrystalline silicon wafers was systematically studied through microwave detected photoconductance decay, on as-grown samples, on samples submitted to phosphorus diffusion step and on samples after gettering and hydrogenation processes. First, we show that extreme gettering parameters (high temperature, high phosphorous-dosing of the wafer surface, long process) result in a significantly better cleaning of the edge zone of ingots, compared to typical phosphorous emitter diffusion. On the other hand, it results in less cleaning of the bulk silicon matrix, and somewhat more decoration of extended crystal defects. Second, we show that there is much improvement possible by enhanced hydrogenation of the wafer. This improvement applies to extended crystal defects but especially to bulk silicon matrix. Bulk silicon lifetime (in low defect crystals) continues to improve with increasing hydrogenation, in the wafers that we investigated e.g. from values around 150 μ s after typical industrial hydrogenation, to 270 μ s after the highest hydrogenation dose which we investigated.

Introduction

It is well known that the directionally solidified multicrystalline silicon (mc-Si) has become a dominant material in the fast growing photovoltaic market for solar cells because of its cost-effectiveness and excellent electronic properties. Nowadays commercial *p*-type mc-Si based solar cells achieve solar conversion efficiencies in the range of 15–16 % with industrial standard screen printing processes, up to 17 % with improved processes [1] and above 20% with more sophisticated solar cell designs [2–4]. Recently, *n*-type mc-Si has attracted attention as a short term solution to the main current problem for the photovoltaic industry: the silicon supply. A partial solution not yet on the market, is in fact the use of the *n*-doped silicon waste available from the semiconductor industry. Interest in *n*-type silicon is also growing due to the light-induced degradation problems associated with boron doped, oxygenated materials. Several benefits of *n*-type silicon wafers for solar cell applications have been reported recently [5–8], with the realization that *n*-type silicon is potentially more suitable than *p*-type silicon for high-efficiency commercial silicon solar cells. The high lifetimes measured for *n*-type multicrystalline and CZ silicon make innovative solar cells possible. It is important to note, however, that the measured lifetime was found to vary markedly across the surface of the wafer, with lifetimes ten times lower than the maximum values being common [5]. Since a large surface variability of this parameter is detrimental for large area devices, it is then convenient to characterize the effect of any kind of processing, as diffusion, passivation and firing, in terms of lifetime mapping or imaging. Recent solar cell research has focused on material and process requirements for *n*-type solar cells, but some unknowns, concerning the specific role of certain impurities in a boron-free material and that of their interaction with extended defects, still remain. Since it has definitely been proven that in *p*-type mc-Si both the phosphorus diffusion and the contact firing through the silicon nitride improve the overall carrier lifetime and the material quality due to external gettering and bulk passivation respectively [for recent work see e.g. 9–11], we focused our investigations on the effect of phosphorus gettering and hydrogen passivation on bulk lifetime and crystal defects of neighbour *n*-type mc-Si wafers. We characterized the samples by mapping the recombination lifetime using the microwave photoconductance decay technique (μ W-PCD) (Semilab WT2000 [12]).

Experimental and discussion

A batch of neighbouring (12.5x12.5) cm², 0.6 Ω cm, <100>, *n*-type multi-crystalline silicon wafers were wet-chemically saw-damage etched and industrially cleaned. The wafers originated from the bottom of an edge block. The final thickness of the samples was around 250 μ m. The batch was divided in 6 groups as explained in the following table. The G1 group is the reference group, representing the starting material quality. The G2 group simulates the industrial standard phosphorus diffusion / gettering process. The G3 group shows the effect of an extreme phosphorus gettering by POCl₃ diffusion. The G4 group investigates the hydrogen passivation by itself without gettering. In the G5 and G6 groups the wafers are both phosphorus gettering and hydrogenated. Within the G5 group the hydrogenation was fixed and the *pocl* diffusion was varied, in the G6 group the phosphorus gettering was fixed and the hydrogenation process was varied. The last two steps are applied at each group to passivate the surfaces before the bulk lifetime measurement.

Table 1: Processing groups distinctions.

Process Step	G1	G2	G3	G4	G5	G6
in-line diffusion	-	X	-	-	-	-
POCl ₃ diffusion	-	-	X	-	X	X
PSG removal	-	X	X	-	X	X
SiN _x	-	X	-	X	X	X
Firing	-	X	-	X	X	X
SiN _x + doped layer etching	-	X	-	X	X	X
HF dip + SiN _x	X	X	X	X	X	X

Phosphorus gettering

Double side phosphorus diffusion was performed in two different ways. The wafers of the G2 group were received a spray-on P- deposition followed by an in-line P-diffusion, using a Despatch spray-coater system to deposit phosphorus and a Despatch Infra-Red (IR) belt furnace to diffuse the doping impurities through the wafers, resulting in typical industrial in-line diffusion with an emitter with sheet resistance value of 60 Ω/sq [13]. The samples of the G3 group were processed using a Tempress quartz tube furnace [14] at extreme conditions: heavy POCl₃ concentration, high temperature and long process, resulting in a doped layer with sheet resistance value of 10 Ω/sq . The sheet resistance of the doped layers was measured using a four-point probe scanning tool [15]. The samples underwent a HF dip to strip off the SiO₂, and the doped layers were then etched and the wafers were industrially cleaned and subjected to a HF dip prior to the silicon nitride deposition. The SiN_x layers were deposited on both sides of the samples, one side at a time, using a Roth & Rau PECVD system [16]. The samples were then characterized using the μW -PCD lifetime testing techniques [12]. In Figure 1 the sample lifetime maps are showed.

Figure 1: Lifetime maps of effects of gettering. Top: as-grown (left); typical 'industrial in-line diffusion' (60 Ω/sq) (middle); heavy (10 Ω/sq) pocl diffusion (right). Bottom: histogram distribution comparison.

As expected, the average lifetime increases after the P-diffusion process, which induces impurity gettering effects at the external surfaces, but an evident local increase of electrical activity of some grain-boundaries was also observed. Apparently, a redistribution of impurities occurs at the processing temperature and impurities are captured at the deepest sinks. In fact, while the grain-boundaries act as heterogeneous segregation/precipitation sites, some of them will compete with the external surfaces as sinks, partly vanishing the effect of P-gettering. The extreme gettering parameters result in a significantly better cleaning of the edge zone of ingots, compared to typical phosphorous emitter diffusion. On the other hand, it results in less cleaning of the bulk silicon matrix, comparing with the in-line standard diffusion. This indicates, once more, that the effectiveness of the phosphorus gettering is determined by several external parameters such as segregation ratio to gettering layer, dissolution and diffusivity of impurities, etc., as well as by the internal wafer parameters such as

original state and density of the impurities in the silicon. The histogram peak moves to higher lifetime values either with the low temperature and fast diffusion, around 40 μs , or the extreme conditions: high phosphorus concentration, high temperature and slow process, around 60 μs . The 60 Ω/sq emitter results in a less uniform lifetime map compare to the 10 Ω/sq one, but it gives lifetime values greater than 200 μs in some areas.

Hydrogen passivation

To evaluate the individual effect of the hydrogen passivation, the wafers of the G4 group, after the saw damage removal and the industrial cleaning, were received an HF dip just before the double sided silicon nitride deposition [16]. The thickness and the composition of the deposited layers are that used in a standard solar cell line. Then, before the lifetime characterization, the wafers were processed in an IR belt furnace [13], with typical industrial firing step. The Figure 2 shows that, quite surprising given the results (presented later) of hydrogenation in combination with gettering, the hydrogenation process by itself does not result in an improved bulk lifetime. It might be that the diffused hydrogen content is not enough to clean the edges, to improve the bulk and to passivate the crystal defects. It also could be that a redistribution of mobile impurities is happening. Further investigations are needed to understand this.

Figure 2: Lifetime maps of effects of hydrogenation. Left: as-grown. Middle: industrial silicon nitride and firing. Right: histogram distribution comparison.

Phosphorus gettering and hydrogen passivation

It may be possible to still enhance the minority carrier lifetime of the material and, even more important, improve its spatial homogeneity by merging the phosphorus gettering with the hydrogenation process. To investigate the obtained sample lifetime when these two effects are combined we decided to act in the following way. We evaluated the effect of different gettering conditions by varying the phosphorus dose while using a standard industrial hydrogenation process. Then, having fixed the *pocl* diffusion recipe, we varied the hydrogen passivation process by changing the thickness of the deposited silicon nitride layer and modifying the firing step duration.

Effect of variation in gettering after standard hydrogenation

The main driving factors for phosphorus incorporation at given temperature are the percentage of the POCl_3 in the quartz tube and the (oxygen concentration) / (POCl_3 concentration) ratio. We decided to use a quite standard POCl_3 concentration (0.2%) and vary the oxygen dose. Moreover we used three drive-in temperatures and time. The samples of the G5 group, after a saw damage etching and an industrial cleaning, were double side diffused in a quartz tube furnace in three different conditions [14]. After a HF dip to remove the phosphorus silicon glass, we measured the conductivity of the doped layers by a sheet resistance scanning tool [15]. The measured sheet resistance values results in: 50 Ω/sq , 35 Ω/sq and 10 Ω/sq . Then the wafers after a HF dip received an industrial bulk hydrogen passivation, by a double side silicon nitride deposition followed by a typical firing step in an IR belt furnace [16, 13].

Figure 3: Lifetime maps of effects of gettering, evaluated after standard hydrogenation. All wafers POCl_3 diffusion. Top: 50 Ω/sq (left), 35 Ω/sq (middle), 10 Ω/sq (right). Bottom: histogram distribution comparison.

The increase of the phosphorus dose results in: a higher average bulk lifetime value, a more uniform lifetime distribution, and a better edge cleaning effect. On the other hand the maximum obtainable lifetime value is inversely correlated to the doping concentration.

Effect of increased hydrogenation

Figure 4: Lifetime maps after varying hydrogenation. All wafers the same (10 Ω/sq) POCl_3 diffusion. Top: typical 'industrial' hydrogenation (left), 3x thicker nitride, same firing parameters (middle), 3x thicker nitride, 3x slower belt speed used for firing (right). Bottom: histogram distribution comparison.

As it is widely known that the recombination activity of extended crystal defects strongly affects the electrical properties of the material and it is influenced by process-induced contamination, as shown in the previous paragraph, particular care was devoted in trying to passivate them by hydrogenation process. We used the double side [11] silicon nitride layers as source of atomic hydrogen and we diffuse these atoms by a high temperature and fast process using an infrared belt furnace [16, 13]. First, having fixed the 10 Ω/sq poel diffusion recipe, we varied the hydrogen dose by simply depositing a thicker silicon nitride (3 times than standard one) layer, and then we tried to diffuse more hydrogen into the bulk by slowing the firing step time (3 times slower than standard one). So the wafers of the G6 group were processed as that one of the 10 Ω/sq G5 group up to the diffusion, and then were divided in two subgroups, one was processed with thicker SiNx followed by a normal firing, and the other with thicker SiNx and slower firing. The lifetime maps, Figure 4, show that the bulk passivation process is improving by increasing the diffused hydrogen dose. Since this effect is not equally effective in all areas, the homogeneity of the bulk lifetime is decreasing with the hydrogen increasing. Moreover the histogram peak of the sample with thicker SiNx and that received a slower firing is slightly moved to lower lifetime values (this effect can be originated from within the wafer itself).

Conclusion

The extreme phosphorus gettering parameters (high phosphorus concentration, high temperature, long process) result in a significantly better cleaning of the edge zone of ingots, compared to typical phosphorous emitter diffusion. On the other hand, it results in less cleaning of the bulk silicon matrix, and somewhat more decoration of extended crystal defects. Anyway there is much improvement possible by enhanced hydrogenation of the wafer. This improvement applies to extended crystal defects but especially to bulk silicon matrix. Recombination activity of extended crystal defects continues to decrease with increasing hydrogenation. Bulk silicon lifetime (in low defect crystals) also continues to improve, in the wafers that we investigated e.g. from values around 150 μs after typical industrial hydrogenation, to 270 μs after the highest hydrogenation dose which we investigated. On the other hand the lifetime spatial distribution is not improving with hydrogen content. Further investigation of different gettering conditions in combination with extended hydrogenation processes are foreseen as well as a comparison on the effect of the same kind of processes on *p*-type mc-Si wafers.

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Role of the Damage Layer in Bulk and Surface Passivation of Silicon Solar Cells by SiN:H

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ABSTRACT

Deposition of a silicon nitride coating by plasma-enhanced chemical vapor produces a shallow layer of damage beneath the silicon surface. This layer serves as a reservoir of H storage, which is then released during the metallization firing process and diffuses into the bulk of the cell, passivating defects and impurities. We provide experimental evidence of the surface damage and of retention of H in this damaged layer, which supports the theory of H transport across the SiN:H medium and the theory of H trapping-detrapping mechanisms. The SiN:H layer also passivates the surface, but the presence of surface damage can reduce the passivation effect. We present a modified model of surface recombination velocity, which incorporates carrier recombination due to the damaged layer in the space-charge region.

INTRODUCTION

Fabrication of high-performance Si solar cells requires control of both the surface and bulk properties. In particular, it is desirable to have low surface recombination velocity (SRV), as well as low bulk recombination. Hydrogenated silicon nitride (SiN:H) has the unique capability of meeting the required dual passivation. An added advantage of SiN:H is that it is compatible with the fire-through process for self-aligned metallization. The surface-passivation properties of SiN:H are strongly controlled by the positive charge that accumulates at the SiN:H-Si interface. Furthermore, because nitridation is performed in an atomic H ambient, it introduces H into a thin plasma-damaged surface layer [1]. Following the nitride deposition, a Ag-based contact metallization is then screen-printed and fired through the nitride [2]. In this step, the metal penetrates through the nitride to form a low-resistance ohmic contact, while the H diffuses into the bulk of the cell to passivate impurities and defects.

There is considerable information on both the bulk and surface passivation of solar cells by SiN:H. This paper reviews some of the work that is available in the literature. Next, we discuss characteristics of the damage layer and its role in controlling the surface characteristics. This is done by introducing a high carrier recombination zone (corresponding to the damage layer) into an existing model that describes SRV of a Si wafer coated with SiN:H. The results of this model agree very well with the measured results of the injection-level dependence of SRV, as reported in the literature. These results clearly show that the damage layer strongly influences both the

bulk and surface passivation provided by SiN:H. This result emphasizes the need for designing a fire-through process that can heal the damage.

BULK PASSIVATION MEDIATED BY SiN:H FILM AND THE DAMAGE LAYER

According to Sopori *et al.*, deposition of SiN:H by either plasma-enhanced chemical vapor deposition (PECVD) or sputtering [3] produces a shallow, process-induced damaged layer near the surface of the Si wafer. Because the damaged layer has a high solubility of H, a majority of the hydrogen atoms are trapped and “stored” in process-induced traps (PITs) in the surface damaged region during the nitride deposition. In the rapid thermal anneal (RTA) step for metallization firing, H is released from the surface and redistributed into the bulk region. Also, because the concentration of H in the damaged layer is higher than that in the SiN:H layer, some of the H may migrate into the nitride layer. As the H diffuses deep into the Si, it saturates the traps and other defects, and passivates them. At the same time, the damage at the surface is being healed. Eventually, all the traps in the bulk of the Si are filled with H, the surface damage is healed, and the H transport mediated by SiN:H reaches a steady state. Outflow of H across the Si-SiN:H interface eventually stops [3].

Figure 1 is an cross-sectional transmission electron microscopy (XTEM) image showing the existence of surface damage caused by SiN:H deposition. The damaged layer has a very high solubility of H. The typical H concentration in SiN:H layers is in the range of $5\text{--}9 \times 10^{21} \text{ cm}^{-3}$, while the H concentration in the damaged layer exceeds 10^{22} cm^{-3} [4].

Fig. 1. High-resolution cross-sectional TEM of Si-SiN:H interface before firing showing process-induced damage by PECVD SiN:H [1,3].

Fig. 2. SIMS profiles of H before and after firing the PECVD nitride-coated wafer [5].

Figure 2 is a secondary-ion mass spectrometry (SIMS) plot of H in the Si solar cell before and after the standard firing process for solar cell fabrication. The nitride layer was removed prior to SIMS measurements. This figure clearly shows that H has diffused into the Si wafer and that the surface concentration is lower after RTP [5]. The passivation of the bulk upon metallization

firing is a very valuable technique for improving the performance of low-cost, commercial Si solar cells.

SURFACE RECOMBINATION OF A Si WAFER COATED WITH SiN:H

It is well known that high fixed positive charge density Q_f ($\sim 2 \times 10^{12} \text{ cm}^{-2}$) is introduced by the SiN:H layer at the Si surface [6–11], resulting in the formation of a space-charge region (SCR). A SRV model has been developed by Girisch [12] and later adapted by A.G. Aberle *et al.* [8]. We have used this model to calculate injection-level dependence of SRV for SiN:H-coated Si wafers. The modeling results of surface recombination velocity, S_s , as a function of the excess carrier density, Δn , are shown in Fig. 3(a) for n -Si and Fig. 3(b) for p -Si for different fixed positive charge densities and interface state densities. In n -Si, the positively charged insulator attracts majority carriers and repels minority carriers, producing an accumulation layer. In p -Si, a depletion/inversion layer is formed. If other input parameters remain the same, the higher the Q_f , the lower the corresponding S_s . For example, a variation of Q_f from 1×10^{12} to $2 \times 10^{12} \text{ cm}^{-2}$ results in a decreasing S_s by about a factor of 7.

Fig. 3. Calculated dependence of surface recombination velocity (S_s) for (a) n -Si and (b) p -Si surfaces as a function of injection level (Δn) for different fixed positive charge densities and interface state densities, $\sigma_n = 10^{-14} \text{ cm}^{-2}$ and $\sigma_p = 10^{-16} \text{ cm}^{-2}$.

From these figures, we notice the following: (i) The SRV for n -Si is lower than that of p -Si, which is expected because the existence of Q_f causes the minority carriers in n -Si to be repelled from the surface; (ii) In p -Si, a depletion/inversion layer is formed; and (iii) A large Q_f leads to similar behavior of injection-level dependence of S_{eff} , namely, an increase in the SRV at high injection levels. This behavior arises from the fact that a flat-band condition is approached at the high injection levels. It is important to point out that in the above model, the interface between the Si and SiN:H is assumed to have no damage.

Some reported experimental measurements of SRV show that the dependence of SRV on the injection level deviates from those shown in Figs. 3a and 3b [10,11]. Figure 4 shows

experimental data reported by Dauwe *et al.* [11]. It is seen that S_s first decreases with an increase in the injection level and then increases again.

Fig. 4. Measured effective SRV showing dependence on excess carrier density [11].

To reconcile this behavior, we invoke recombination in the damaged region formed by the process-induced defects in the vicinity of the surface. Hence, there is an increased minority-carrier recombination within the damaged layer, which occurs within the SCR. Based on this, one must include recombination in the SCR. A similar conclusion was arrived at by Schmidt [10], but his reasoning did not include the surface damage. However, one can follow his approach to calculate the effect of increased recombination near the damaged surface. Once SCR exists beneath the surface of the wafer, its detailed characteristics are uniquely determined by the shape of the potential barrier. A full derivation of approximate solutions can be found in references [13,14]. We start with the equation

$$\psi(z) = \psi_s \cdot e^{-z/L}, \quad (1)$$

where z is the distance from the surface, and ψ_s is the surface potential at the surface or at one end of SCR ($z = 0$), which can be found by an iterative approach of Shockley-Read-Hall (SRH) formalism [13]. L is the extrinsic Debye length with the definition:

$$L \equiv \sqrt{\frac{k\epsilon_0\epsilon_b KT}{q^2(n_b + p_b)}}, \quad (2)$$

where n_b , p_b denote carrier density of electrons and holes in the bulk, respectively, and ϵ_b is the dielectric constant of the semiconductor.

In the SCR, the carrier densities are functions of the position z :

$$n(z) = n_b e^{\beta\psi}, \quad p(z) = p_b e^{-\beta\psi}. \quad (3)$$

For the definition and parameterization of recombination rate in the SCR, $U_{SCR}(z)$ parameterization, see reference [11]. The recombination velocity in the SCR is calculated by

$$S_{SCR} = \frac{1}{\Delta n} \int_0^L U_{SCR}(z) dz. \quad (4)$$

Hence, the effective SRV is given by

$$S_{eff} = S_s + S_{SCR} . \quad (5)$$

Figure 5 shows the calculated results for S_{eff} as a function of injection level. S_{eff1} (when there is a damage layer) has a more pronounced injection-level dependence compared to S_{eff2} (when there is no damage layer). S_{SCR1} and S_{SCR2} denote the intrinsic recombination in the SCR, with or without damage layer, respectively. S_s is the recombination at the surface. This figure also demonstrates that at low injection level, recombination in the SCR influences the magnitude of S_{eff} , whereas at high injection level, S_{eff} is mostly determined by the recombination at the surface.

Fig. 5. Calculated recombination velocity components S_s and S_{SCR} (dotted lines), and the total S_{eff} (solid lines) at SiN:H-Si interface as a function of injection level. Assumptions:
 p -Si, 1.5 Ωcm ,
 $Q_f = 2 \times 10^{12} \text{ cm}^{-2}$,
 $D_{it1} = 1 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$,
 $D_{it2} = 1 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$,
 $\sigma_n = \sigma_p = 4 \times 10^{-15} \text{ cm}^2$.

After plasma deposition, there is damage beneath the Si surface up to about 20 nm deep [1,3], which agrees well with the calculated L . Note that the major amount of surface damage can be healed by the RTA process, so that the width of the SCR will subsequently be reduced. Therefore, less influence of minority-carrier recombination in the SCR is expected after the firing treatment of Si solar cells.

CONCLUSIONS

The damage layer mediates H transport into bulk Si, but it also affects the recombination at the SiN:H-Si interface by introducing high D_{it} across the SCR. Extended SRH formalism was used to evaluate the recombination effect in the Si-SiN:H interface. Modeling results indicate that at a low injection-level range, carrier recombination in the SCR is the dominant mechanism compared to the S_s . The calculated results seem to agree with the experimental results reported by others. More details of the damage layer or the Si-SiN:H interface need to be developed for a comprehensive understanding of the bulk and surface passivation effects introduced by the PECVD SiN:H layer.

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Application of *PV Optics* to Si Solar Cell Design

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ABSTRACT

PV Optics is versatile and user friendly optical software for designing solar cells and modules. It combines ray and wave optics approaches to analyze multilayer, stratified structures, with planar or non-planar interfaces to determine their reflection, absorption, and transmission characteristics. It is a unique optical package that handles metal optics. Thus, the software can be used to design single and multijunction solar cells and modules. We describe results of *PV Optics* simulation for design of Si solar cells.

INTRODUCTION

Photovoltaic (PV) industry has advanced greatly in the last few years; these advances have led to cost reduction of the commercial PV energy, new materials and new designs for higher efficiency solar cells. High-efficiency solar cell design now includes a number of features such as light trapping, back surface fields, textured and rough interfaces, reflective metallization and multijunction configurations. These features require design tools that can handle a variety of materials and cell configurations such as thick and thin cells, non-planar interfaces, and heavily absorbing layers. Modern high-efficiency silicon (Si) solar cells use fairly complicated optical design, which requires more mature numerical analysis tools [1]. *PV Optics* is software package developed for design and analyses of solar cells and modules. It is applicable to a variety of structures, including thin and thick cells, light trapping structures, and can handle metal optics. It uses a combination of wave and ray optics to include effects of coherence and interference. This paper describes some basic applications of *PV Optics* for Si solar cell design. In particular, *PV Optics* is used to examine the effects of wafer thickness, antireflection (AR) coating thickness, and texture height on the cell performance. One of the important parameters in the cell design is the absorption in the metal; this is particularly true for thin wafers. We will investigate this loss caused by metal absorption in thin cells.

BRIEF DESCRIPTION OF PV OPTICS

Figure 1 illustrates the formalism that is used in *PV Optics*. A beam of unit intensity is incident on the sample of an arbitrary morphology. This beam is split into many beamlets that impinge on the surface. Each beamlet is allowed to propagate, keeping track of its entire path, its

transmission, and absorption until its energy reaches a certain (negligible) value. Maximum achievable current density (MACD) is calculated by adding the total absorbance correspondent to an AM1.5 spectrum [2]. In a multijunction device, the absorbance in each layer is calculated to determine MACD for each junction.

Figure 1. A schematic illustrating the approach in PV Optics.

Figure 2. The graphical main menu for selection of device configuration – (a) selection of device configuration, (b) selection of interface type and material parameters, and (c) selection of semiconductor.

PV Optics starts with a graphical interface with a typical configuration of a module, which includes glass, encapsulation, AR coating, three semiconductor layers, a buffer and a metal, as seen in Figure 2a. The user can modify this configuration and delete the unwanted regions by clicking on that region with the mouse to arrive at the desired device configuration, [3]. For example, Figure 2b shows a configuration for an encapsulated single junction solar cell, and Figure 2c corresponds to a Si cell in air. There is a series of values to be input by the user, or default values used in PV manufacturing [4]. Next, one can go to the page that determines the type of interface (planar or textured), and its characteristics. The AR coating is defined by a two-layer system with parameters (n_1 , k_1 , thickness 1) and (n_2 , k_2 , thickness 2), where n_1 and n_2 are the refractive indexes, and k_1 , k_2 are the extinction coefficients, respectively. The selection of semiconductor offers up to three junction cells and materials such as silicon, amorphous silicon, amorphous silicon top, amorphous silicon middle, amorphous silicon bottom. Additional semiconductor data can be added as requested [4].

After the calculation is finished, *PV Optics* shows a variety of plots, which include (a) reflectance, transmittance, and absorbance of the whole device, (b) absorbance of each active layer, (c) weighted (AM 1.5) absorbance, and (d) distribution of absorbed photon flux.

RESULTS AND DISCUSSION

This section shows a number of output plots from *PV Optics*, which are needed for the design of a solar cell. Figure 3 shows total reflectance, total absorbance, and the metal absorbance of a Si solar cell with the following parameters: wafer thickness = 250 μm , texture height = 1 μm , AR thickness = 750 $\text{\AA}$. The calculated MACD for the cell is about 40 mA/cm^2 . Figures 4 shows dependence of MACD on the thickness of a FTBT cell. As expected, MACD increases with increase in the cell thickness. Figure 5 shows dependence of MACD on the AR coating thickness for a FTBT cell of 250 μm thickness. It is seen that MACD has a peak at a thickness of about 750 $\text{\AA}$.

Figure 3. Calculated reflectance, absorbance, and metal absorption for 250 μm thick Si cell reflectance, transmittance, total semiconductor absorbance, absorbance in metal, and MACD

Figure 4. MACD for FTBT solar cell with a texture height of 1 μm , as a function of Si thickness.

Figure 5. MACD for FTBT solar cell, with a texture height of 1 μm , as a function of AR coating thickness; Si thickness = 250 μm .

The dependence of the metal loss on the cell thickness and the AR coating thickness is shown in Figures 6 and 7, respectively.

Figure 6. Metal Loss for FTBT solar cell with a texture height 1 μm , as a function of Si thickness.

Figure 7. Metal loss for FTBT solar cell with a texture height 1 μm , as a function of AR Coating thickness, Si thickness = 250 μm .

We now consider the effect of encapsulating the cell, whose characteristics are shown in Figure 2. Figure 8 shows the reflectance, absorbance, and the metal absorption for this cell after encapsulation in a module. The reflectance of the encapsulated cell is about 7%. The MACD of the encapsulated cell has dropped to 38.23 mA/cm^2 (from 40.82 mA/cm^2).

Figure 8. Reflectance, total semiconductor absorbance, and absorbance in metal for an encapsulated cell. The cell is 250 μm thick with a two-layer AR coating consisting of 710 $\text{\AA}$ of Si_3N_4 (refractive index = 1.95) on 100 $\text{\AA}$ of SiO_2 (refractive index = 1.45); the texture height is 1 μm .

Another important result generated by PV Optics is the distribution of the absorbed photon flux within the cell, for an AM1.5 incident spectrum. Such a distribution is needed to perform electronic design of the cell by modeling packages such as AMPS [5] or PC1D [6].

We have described only a few examples of the application of PV Optics for the design of Si solar cells and modules. PV Optics is also used in the design of thin film cells such as a-Si, and will also be extended to CIGS- and CdTe-based thin film cells. This software is easy to use and the results for Si and a-Si are very accurate.

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