Development of double-sided silicon strip detectors (DSSD) for a Compton telescope

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Abstract

The low noise double-sided silicon strip detector (DSSD) technology is used to construct a next generation Compton telescope which is required to have both high-energy resolution and high-Compton reconstruction efficiency. In this paper, we present the result of a newly designed stacked DSSD module with high-energy resolution in highly packed mechanical structure. The system is designed to obtain good P-side and N-side noise performance by means of DC-coupled read-out. Since there are no decoupling capacitors in front-end electronics before the read-out ASICs, a high density stacked module with a pitch of 2 mm can be constructed. By using a prototype with four-layer of DSSDs with an area of 2.56 cm × 2.56 cm, we have succeeded to operate the system. The energy resolution at 59.5 keV is measured to be 1.6 keV (FWHM) for the P-side and 2.8 keV (FWHM) for the N-side, respectively. In addition to the DSSD used in the prototype, a 4 cm wide DSSD with a thickness of 300 μm is also developed. With this device, an energy resolution of 1.5 keV (FWHM) was obtained. A method to model the detector energy response to properly handle split events is also discussed.

1. Introduction

The observation of high-energy astrophysical phenomenon utilizing sub-MeV/MeV gamma rays is an attractive result that opens up a new window for studying particle acceleration and nucleon synthesis in the universe. However, the sensitivity is limited because of high background, low efficiency, and the difficulty of imaging utilizing focussing technology. As demonstrated by COMPTEL [1] onboard CGRO (Compton Gamma-Ray Observatory), in the range from ~1 to several tens of MeV, a significant

reduction of background by means of reconstructing Compton scattering is proved to be useful in this difficult spectral band.

Our approach is to apply the concept of Compton telescope in the range of several 10 keV to several 100 keV. In order to extend the capability down to low energy gamma rays, the use of a stack of double-sided silicon strip detectors (DSSD) [2] is very attractive. Taking advantage of significant progress in technology related to Si and CdTe imaging detecors, we are developing a new generation of Compton telescope, the semiconductor Compton telescope (Si/CdTe Compton telescope) [3–8]. Si works as a good scattering medium because the cross-section of Compton scattering becomes larger than that of photo-absorption above 50 keV. In addition, the advantage of Si is its

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relatively small Doppler broadening effect [9] compared with Ge or CdTe [10]. On the other hand, CdTe works very nicely as an absorber thanks to its high atomic number and high density.

The scattering part is very important in the Compton telescope. In order to cover an energy range from several 10 keV, the energy threshold of the detector must be low, because the energy of recoil electrons is almost below 10 keV in this energy band. Furthermore, a high Compton scattering probability is desirable to obtain a high efficiency as a Compton telescope. In the Si/CdTe Compton telescope, we employ a DSSD module that consists of compactly stacked layers of DSSDs (Fig. 1). In order to be hermetically and symmetrically enclosed by absorbers, the scattering part needs to have a compact structure. Also, a symmetrical structure is desirable to reduce possible systematic errors in measurements of linear polarization of gamma rays.

In order to demonstrate the concept of the Si/CdTe Compton telescope, we have developed high-quality DSSD together with a low noise analog ASIC to realize a noise level as low as 1–2 keV (FWHM) [11,12]. As a next step, we work on improving the Compton scattering efficiency. The development of a large volume and high-density DSSD module is a key to achieve the requirements. In addition, the mass of the supporting materials including the read-out electronics should be minimized to reduce the interaction of scattered photons with inactive materials. The improvement of the N-side energy resolution also increases the efficiency. In a previous prototype, an energy resolution of 1.3 keV (FWHM) on the P-side is achieved, while 3.8 keV on the N-side. Thus, an improved N-side resolution makes it possible to determine the position of Compton scattering with high accuracy for smaller energy deposits.

In this paper, we present the results of the new prototype of stacked DSSD module which emphasizes energy resolution and density in Section 2. Next, the results from a 4 cm wide DSSD which improves the Compton scattering efficiency is reported in Section 3. Finally, a detailed DSSD energy response including inter-strip events is discussed in Section 4.

2. Prototype of high density stacked DSSD module

2.1. The new DSSD board

The DSSD used here is the 2.56 cm wide device developed with Hamamatsu Photonics, Japan. See Tajima et al. [12] for the details of this device. The device was produced from an n-type wafer which has resistivity of 5 kΩ cm. The wafer thickness is 300 μm. The N-side has a floating p-implantation between strips to isolate adjacent strips. The strip pitch is 400 μm and the width is 300 μm on each side. The Al electrodes are DC-coupled on each implantation.

A photograph of the newly developed DSSD board is shown in Fig. 2. It consists of one DSSD and two specially designed low noise analog VLSI, VA64TAs, mounted on a small circuit board. The VA64TA is manufactured by IDEAS ASA, Norway in collaboration with us. It has a 64 channel input and can be used for both positive and negative input charges. Combined with the compact design, the support structure is made of plastic instead of Al_2O_3 ceramic. The average thickness of the support in the horizontal direction is $1.4 \, g/cm^2$.

A DC-coupled read-out is employed not only on the P-side but also on the N-side to obtain good energy resolution. To apply reverse voltage, the N-side circuit as a whole is biased by 100 V. The decoupling is performed in the read-out system as described later. Since this system does not need decoupling capacitors in front-end, it becomes possible to shorten the stack pitch to 2 mm from 6 mm in a previous prototype [5,6].

2.2. Four-layer stacked DSSD module

Combining the new DSSD board, a four-layer stack of the DSSD module is constructed. Fig. 3 shows the
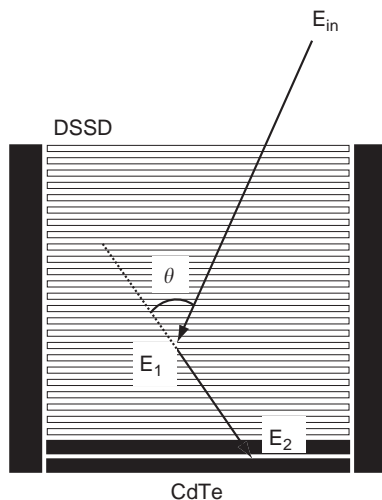

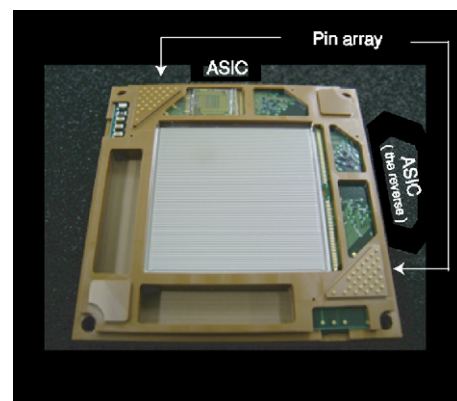Fig. 1. Design of stacked DSSD module with CdTe detectors (absorbers).

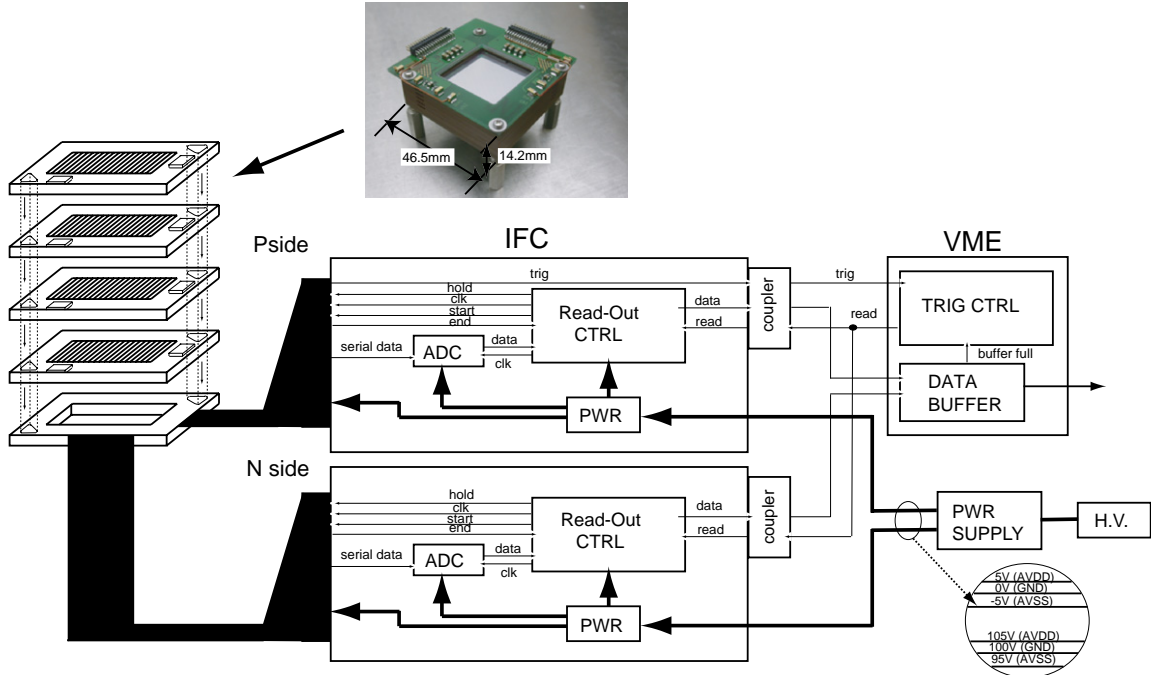Fig. 2. Photograph of a DSSD board.

Fig. 3. Schematic diagram of the four-layer stacked DSSD module.

schematic diagram of the system. Four DSSD boards are daisy-chained via pin arrays and stacked with a 2 mm pitch. Each side has the same read-out board, the Inter Face Card (IFC), which controls the read-out sequence. The IFC interchanges the digital signal with the external system via an ultra fast coupler with 2000 V tolerance, hence we can supply the reverse bias to each DSSD by means of operating two IFCs under voltage gap corresponding to reverse bias. Consequently, we can realize DC-coupled read-out on both sides.

All layers were successfully operated at $-20\,^{\circ}\mathrm{C}$ and a bias of 100 V. In Fig. 4, we present sum spectra of both the P-side and N-side in each layer. The energy resolution at 59.5 keV is obtained to be 1.6 keV (FWHM) in P-side, which is about 0.3 keV larger than the expected value calculated from VA64TA noise performance and the input capacitance of DSSD. The difference is explained by the pitch adapter capacitance between the DSSD and LSI since we observed 1.2 keV (FWHM) for the channels with a short pitch adapter. We are currently fabricating a new LSI with optimized input channel pitch to minimize the length of the pitch adaptor.

In spite of the effect of the pitch adapter capacitance, we recognize an improvement of the N-side energy resolution from 3.8 to 2.8 keV (Fig. 4 right), compared with AC-coupled read-out with RC-bias chip [11] with $R \simeq 4\,\mathrm{G\Omega}$ and $C \simeq 50\,\mathrm{pF}$ in the previous prototype [5,6]. The noise on the N-side is still larger than what was expected from the LSI performance and the total capacitance load. The origin of this "excess noise" is under investigation.

3. A 4 cm wide DSSD

Another way to increase the efficiency is to enlarge the DSSD itself. We have developed a 4 cm wide DSSD for the future stacked DSSD module. Although the preliminary results are already summarized by Nakazawa et al. [13], we here present the detailed performance of the device including energy response. The strip length is 3.84 cm and thus the effective area (active area × thickness) is 2.25 times larger than the 2.56 cm wide DSSD. The strip parameters are the same to these of the 2.56 cm wide DSSD. The thickness is 300 μm, while the strip pitch is 400 μm and the width is 300 μm on both sides.

3.1. Basic characteristics of the device

We measured the leakage current of two selected strips in the P-side using a KEITHLEY 237 multimeter. The $I–V$ curve of the 4 cm DSSD with various temperatures and bias voltages is presented Fig. 5 (left). The leakage current at 100 V bias is 650 pA at $20\,^{\circ}\mathrm{C}$ and 26 pA at $-10\,^{\circ}\mathrm{C}$. These values are about 1.6 times larger than a 2.56 cm wide DSSD, proportional to the size of the device.

A DSSD capacitance has two origins: the body capacitance and the inter strip capacitance. We measured these capacitances using a HP4284A multimeter. The result is shown in Fig. 5 (right). The body capacitance per strip becomes constant at a value of 5 pF above a bias of 70 V. This means that the full depletion voltage is 70 V. However, the N-side inter strip capacitance still decreases even above 70 V and becomes constant around 100 V. This fact
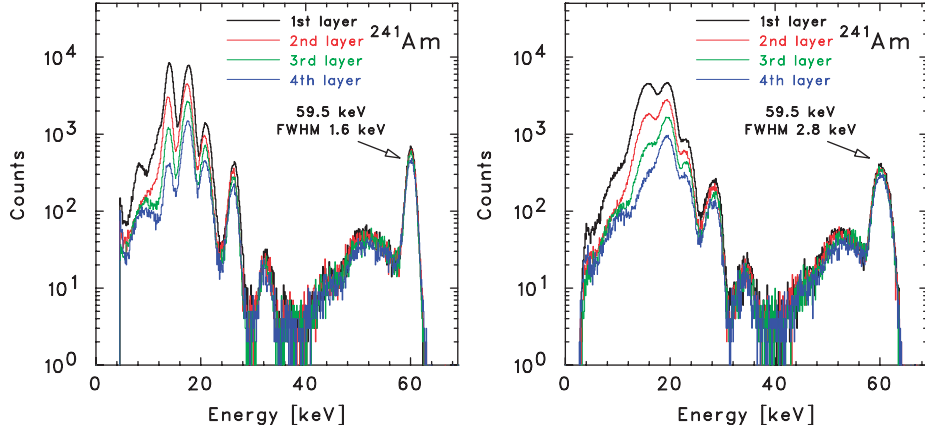
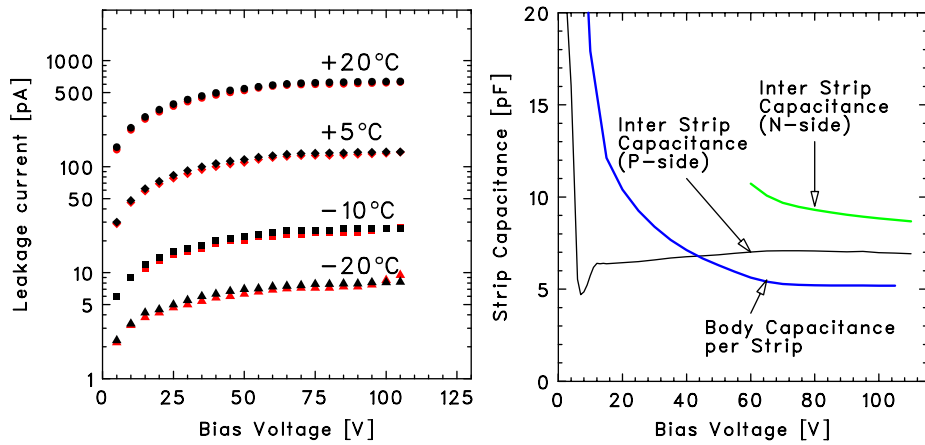Fig. 4. Sum spectra for each layer (left: P-side, right: N-side).

Fig. 5. Measured basic property of 4 cm wide DSSD. *I–V* curve with various temperature (left), *C–V* curve (right).

suggests that actually a 100 V bias is required to make the N-side inter strip fully isolated. Since total input capacitance is a sum of the body capacitance and the inter strip capacitance, we can estimate it as 12.2 and 14.2 pF at the P-side and N-side, respectively.

3.2. Imaging and spectroscopy

We read out the 4 cm wide DSSD using another analog LSI, VA32TA [12]. The 4 cm wide DSSD has a total of 192 channels, so we need 6 VA32TA chips. In this experiment, we apply reverse bias via a RC-bias chip on the N-side.

The DSSD was operated at $-10\,^{\circ}C$ with a 100 V bias. The left panel of Fig. 6 is ^{133}Ba line image integrated in the energy band from 20 to 40 keV. The classic style car mask, made of 0.3 mm thick brass, was mounted 3 mm above the DSSD. The right panel of Fig. 6 is the sum spectra of all 96 strips in the P-side. The energy resolution at 59.5 keV is measured to be 1.5 keV (FWHM). This energy resolution is consistent with the value which is calculated from the VA32TA noise performance and input capacitance.

3.3. Pulse height correlation

We irradiated two adjacent P-side strips (Nos. 73 and 74) with 59.5 keV gamma rays from ^{241}Am. Since the attenuation length is 1.34 cm [14] for 60 keV photons, interactions occur almost uniformly in the 300 μm thickness. Fig. 7 is the distribution of the pulse height correlation. The regions surrounded by rectangles with oblique lines are lower energy lines of ^{241}Am. The distribution shows that our DSSD has roughly 10% split events which share signals between adjacent strips.

The striking feature of the plot is the opposite polarity events which are of unknown origin. This phenomenon is not detected in the same diagram generated for N-side. Because of the threshold of our measurement, we can predict that some events are undetected even though they actually interact in the DSSD. Thus there are "dead events" in the DSSD. The phenomenon is not only observed in a 4 cm wide DSSD but also in a 2.56 cm wide DSSD. The 4 cm DSSD has statistical advantage because of its larger effective area, thus it is suitable for a detailed investigation of energy response.
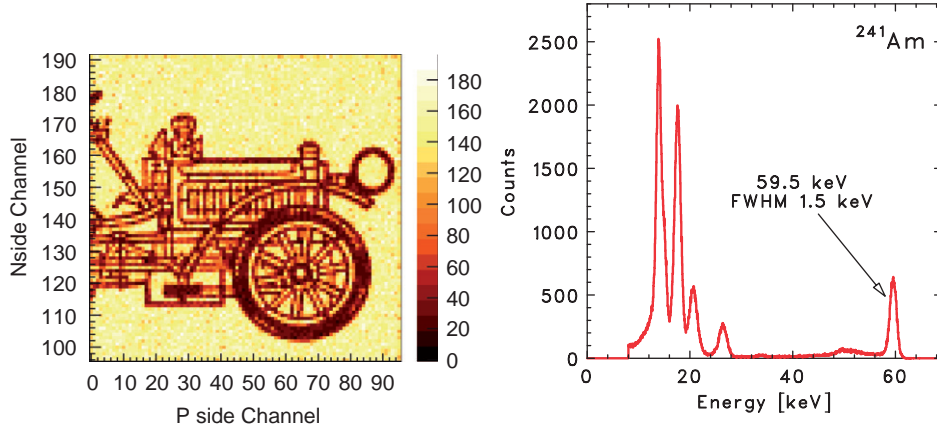
Fig. 6. A shadow image ranging from 20 to 40 keV X-ray irradiated [133]Ba (left), a sum spectrum of P-side irradiated [241]Am (right).
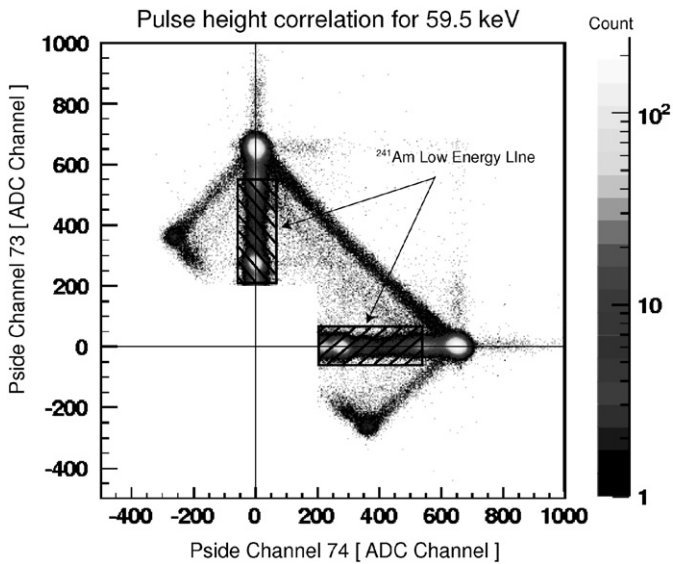

Fig. 7. Pulse height correlation between strip Nos. 73 and 74.

Fig. 8. Internal potential of DSSD under full depletion voltage.

Since the effect will not be negligible in Compton reconstruction, we should identify the origin of these events and evaluate the percentage of the "dead events". In the next section, we discuss these phenomenon, based on two-dimensional device simulator and the assumption of a simple charge induced model.

4. Detailed energy response of DSSD

4.1. Potential simulation

As the first step, the internal potential of the DSSD was calculated using the two-dimensional device simulator VENUS-2D, developed by Fuji Research Institute Corporation, Japan. The geometry is a cross-section perpendicular to the p-strip. We estimate the donor density of n-bulk silicon as 8.3×10^{11} cm^{-3} from our DSSD's resistivity and set p$^+$ and n$^+$ dope density as a typical value 1.0×10^{18} cm^{-3}. Additionally, we set the positive fixed oxide surface charges

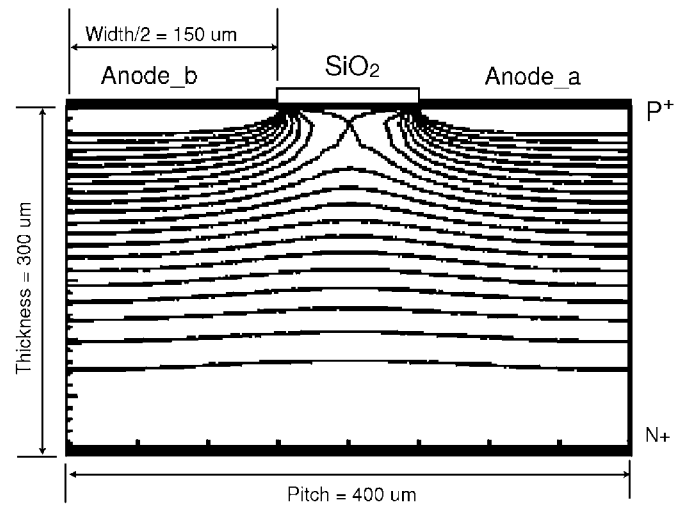in the Si–SiO$_2$ transition region to have a typical value 1.0×10^{12} e/cm^2 [15]. This geometry fully depletes on bias voltage around 60 V, the value of which is consistent with the actual measurements (Section 3.1).

Fig. 8 is a simulated internal potential under full depletion voltage. Positive fixed oxide surface charges induce local minimum potential between the p-strips and in this region electrons are conducted to the center of SiO$_2$ layer, not to N-side. The local minimum potential region extends to about 1500 μm^2 under SiO$_2$ layer.

4.2. Simulated pulse height correlation

Based on the potential simulation, we next calculated the pulse height correlation between the two anodes (Anode_a and Anode_b in Fig. 8) for 59.5 keV photo-absorption events. To estimate the charge collection, we introduce simple assumptions as follows:

(1) Holes and electrons are fully conducted either to electrodes or to the SiO$_2$ layers.

(2) The trajectory of a charge is simply defined by the potential taking no account of initial momentum and thermal diffusion.

(3) Electrons $(-Q)$ conducted to SiO_2 induce the same amount of signal $(+\frac{1}{2}Q)$ to the adjacent strips (Anode_a, Anode_b) (see Yorkston et al. [16] for experimental evidence).

(4) The initial charge cloud size is defined as $C_{init} \simeq 0.0171 \times T_e^{1.75}$ (µm) [17], where, C_{init} is the 2 sigma cloud diameter and T_e is the initial electron kinetic energy. For example, $C_{init} = 21$ µm for 59.5 keV photon absorption.

Fig. 9 is the result of the simulated pulse height correlation. The distribution (Fig. 9 top) is like an oblique rectangle which has the apex $(q, 0)$, $(\frac{1}{2}q, -\frac{1}{2}q)$, $(-\frac{1}{2}q, \frac{1}{2}q)$, $(0, q)$. This corresponds to the experiment (Section 3.3). The reason of forming this distribution is because the amount of charge collection to Anode_a and Anode_b varies according to the point where the initial cloud is generated. We can roughly divide the internal region into eight sections as indicated in Fig. 9 bottom, A–G. All holes move to the nearest strip and all electrons move to N-side in A $(q, 0)$ and G $(0, q)$. All holes move to the nearest strip and electrons are shared between SiO_2 and N-side in B (between $(q, 0)$ and $(\frac{1}{2}q, -\frac{1}{2}q)$) and F (between $(-\frac{1}{2}q, \frac{1}{2}q)$ and $(0, q)$). All holes move to the nearest strip and all electrons move to SiO_2 in C $(\frac{1}{2}q, -\frac{1}{2}q)$ and E $(-\frac{1}{2}q, \frac{1}{2}q)$. Holes are shared between strips and all electrons move to SiO_2 in D (between $(\frac{1}{2}q, -\frac{1}{2}q)$ and

$(-\frac{1}{2}q, \frac{1}{2}q)$). Holes are shared between strips and all electrons move to N-side in H (between $(0, q)$ and $(q, 0)$).

Table 1 shows a comparison of event distributions between experiment (Fig. 7) and simulations (Fig. 9, top). Simulations reproduce the experimental data well. In Section 3.3, we reported on the presence of "dead events". They are shown to originated from the region D (Fig. 9, bottom). In experimental data (Fig. 7), the density of these events is slightly higher than those of the simulation. This is well explained as a contribution of gamma rays below 59.5 keV, such as backscatter events around 48.3 keV (Fig. 7). Although the threshold of measurement and mixed response for different energy photons in the diagram of pulse height correlation make it difficult to measure the probability of "dead events", we predict from simulation that their probability is on the order of 0.1%.

Table 1
Comparison between actual experimental data (Fig. 7) and simulation results (Fig. 9)

Region	Number of events (normalized)	
	Experiment	Simulation
A+G	100	100
H	6.3	4.1
(B+C)+(E+F)	4.5	2.0
D	N/A	0.08

Regions A to H are indicated in Fig. 9. Number of events are normalized to those in the A+G region, which is set to 100.

5. Summary and future prospects

Successful operation of the four-layer stack of a DSSD module with a stack pitch of 2 mm is demonstrated. The DC-coupled read-out is employed on both the P-side and the N-side. The energy resolution of 1.6 keV (FWHM) on P-side and 2.8 keV on N-side is measured for 59.5 keV X-ray at a temperature of $-20\,°C$. The satisfactory performance of the 4 cm wide DSSD which has 2.25 times larger effective area than a 2.56 cm wide DSSD is also demonstrated.

The presence of "dead events" is found from the diagram of pulse height correlation for 59.5 keV incident photons. A two-dimensional device simulation with simple assumptions on charge collection can reproduce the energy response observed in the data well. We conclude from the simulation that the fraction of "dead events" is on the order of 0.1%, originating from the region of the local potential minimum under the SiO_2 layer.

Further approaches for a next revision of the stacked DSSD module include a new circuit board with shorter pitch adapter and an ASIC with an optimized input pitch and on-chip digitizer. As for the detector development, tests of DSSDs with a thickness of 500 µm and size of 4 and 2.56 cm are under progress. We also plan to fabricate a 5.12 cm^2 DSSD with a thickness of 500 µm to achieve 2.5 times larger effective area than a 4 cm wide DSSD
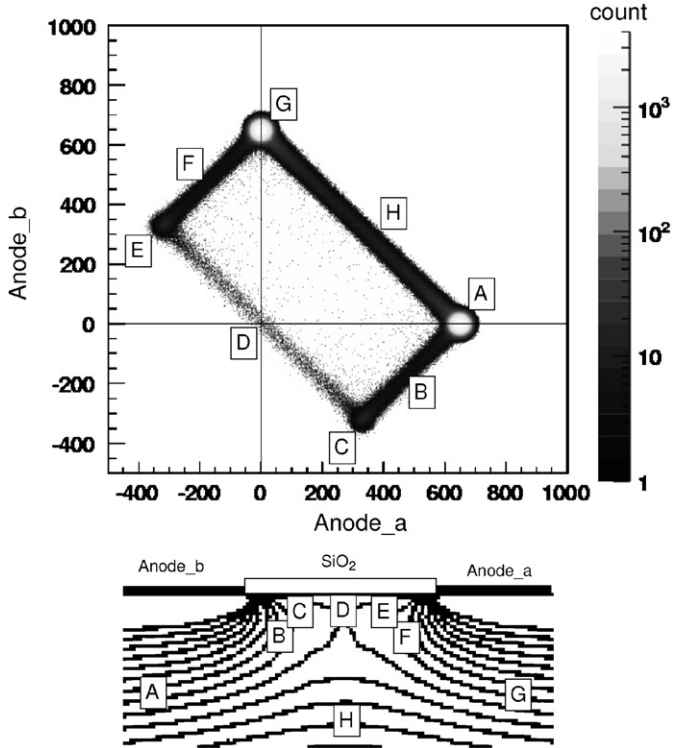

Fig. 9. Simulated pulse height correlation between adjacent strips. According to the region where initial cloud is generated, the distribution becomes oblique rectangle.

with a thickness of 300 μm without increasing the strip capacitance.

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