A Simplified Model for Parameter Estimation and Circuit Analysis of Inductive-Adder Modulator

W. Zhang, W. Eng, C. Pai, J. Sandberg, Y. Tan, Y. Tian

XXX Collider-Accelerator Department XXX

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W. Zhang, W. Eng, C. Pai, J. Sandberg, Y. Tan, Y. Tian
Brookhaven National Laboratory
Upton, NY 11973

Abstract— In this paper, we propose a simplified model for easy estimation of design parameters and quick analysis of inductive adder modulators. Analytical method is used to deduct the simplified circuit model. This model offers an easy way to understand the behavior of the inductive-adder modulator circuits and provides designers a helpful tool to estimate critical parameters such as pulse rise time, system impedance, number of adder stages, etc. Computer simulations demonstrate that parameter estimation based on simplified circuit model is fairly accurate as compared to original circuit. Further more, this approach can be used in early stage of system development to assist the feasibility study of the project and to aid geometry selection and parameter selection of critical components.

I. INTRODUCTION

The demonstration of ARM-II solid-state modulator at LLNL in 1998 opened a new era in pulsed power modulator technology [1]-[3]. This modulator was based on induction voltage adder (IVA) topology. Other systems built on the same principle such as DARHT-II kicker modulator and the prototype AHF kicker modulator further revealed the amazing capabilities of this new technology. Scientists and engineers elsewhere are eager to try to expand this modulator topology to other applications.

However, there is very little literature to help people to understand the parameter range and feasibilities of induction adder modulator in design and development process. During our effort to build a solid-state induction adder modulator, we frequently encountered inquiries of achievable parameters of multi-stack modulator. Primary inquires are voltage or current amplitude, pulse rise time and fall time, pulse duration range, pulse repetition rate, and ability to generate arbitrary pulse waveforms.

In [4] and [5] a single cell circuit model of IVA was given as in Fig. 1. Where, SW is the main switch, C_S is the capacitance of energy storage capacitor, R is the parallel resistor, L_K is core leakage inductance, L_P is primary core inductance, and L_1 and C_1 are the distributed inductance and capacitance of stalk per stack section length.

When the main switch SW is closed, the state space description of single cell circuit is shown in Fig. 2.

Fig. 1. A single cell model of inductive voltage adder.

Fig. 2. State space description of a single cell model of inductive voltage adder with switch closed.

II. THE OUTPUT IMPEDANCE AND TRANSMISSION DELAY TIME ESTIMATIONS

Traditionally, the output impedance has been treated as the stalk impedance [4]-[5]. This condition is true, if transformer primary inductance and leakage inductance are negligible. However, in fast pulse circuit they have to be considered in the design. Reference [5] showed an interesting case of output mismatch to stalk impedance. To analyze output impedance, we use zero-state analysis.

Let us define Z_1 to be the impedance of storage capacitor C_S in parallel of R, and Z_2 to be the summation of Z_1 and leakage inductance L_K. Then, we have the following equations

$$Z_1 = R // \frac{1}{C_S S}$$
$$= \frac{R}{RC_S S + 1} \tag{1}$$

and

$$Z_2 = Z_1 + L_K S$$
$$= \frac{R + L_K S + RC_S L_K S^2}{RC_S S + 1} \tag{2}$$

If we define Z_3 as the impedance of Z_2 in parallel with primary inductance L_P, we have

$$Z_3 = Z_2 // L_P S \tag{3}$$
$$= \frac{1}{\frac{1}{Z_2} + \frac{1}{L_P S}}$$
$$= \frac{(R + L_K S + RC_S L_K S^2) L_P S}{R + (L_K + L_P R) S + (L_P L_K + RC_S L_K) S^2 + RC_S L_P L_K S^3}$$

Further, if Z_4 is defined as the summation of Z_3 and sectional stalk inductance L_1, we can deduct it as

$$Z_4 = Z_3 + L_1 S \tag{4}$$
$$= \frac{(R + L_K S + RC_S L_K S^2) L_P S}{R + (L_K + L_P R) S + (L_P L_K + RC_S L_K) S^2 + RC_S L_P L_K S^3} + L_1 S$$

Consider that the capacitance of storage capacitor has to be large in order to keep voltage constant and be able to provide high repetition rate pulse burst without recharge. In addition, the frequency spectrum of the pulse is usually in the high frequency band for pulsed power or pulsed RF applications. The impedance of C_S at the high frequency range is much larger than the parallel resistor R, and hence R can be ignored. Therefore, we have the following approximation. If $C_S S >> \frac{1}{R}$, then

$$Z_1 = R // \frac{1}{C_S S}$$
$$\approx \frac{1}{C_S S} \tag{5}$$

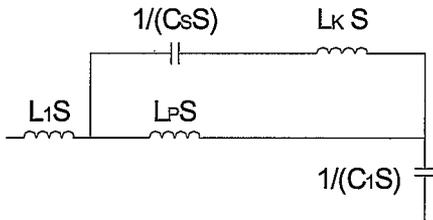Redraw the single cell circuit model in Fig. 2 with resistor R eliminated, it becomes the circuit shown in Fig. 3.

Fig. 3. A single cell model with R eliminated.

Apply (5) into (2) and (3), we have

$$Z_2 = Z_1 + L_K S$$
$$\approx \frac{1}{C_S S} + L_K S$$
$$= \frac{1 + C_S L_K S^2}{C_S S} \tag{6}$$

and

$$Z_3 = Z_2 // L_P S \tag{7}$$
$$\approx \frac{1}{\frac{1 + C_S L_K S^2}{C_S S} + \frac{1}{L_P S}}$$
$$= \frac{L_P S (1 + L_K C_S S^2)}{1 + (L_K + L_P) C_S S^2}$$

Another fact is that the leakage inductance has to be very low comparing to the primary inductance for an efficiently coupled core design. Therefore, if $L_K << L_P$, then

$$Z_3 \approx \frac{L_P S (1 + L_K C_S S^2)}{1 + L_P C_S S^2} \tag{8}$$

At high frequency range the parameters can be chosen to satisfy $L_K C_S S^2 >> 1$ and $L_P C_S S^2 >> 1$. Then the impedance parameters Z3 and Z4 can be simplified as following

$$Z_3 \approx \frac{L_P S (L_K C_S S^2)}{L_P C_S S^2} \tag{9}$$
$$= L_K S$$

and

$$Z_4 = Z_3 + L_1$$
$$\approx L_K S + L_1 S \tag{10}$$
$$= (L_K + L_1) S$$

The circuit in Fig. 3 is reduced to the one shown in Fig. 4.

Fig. 4. A simplified single cell model.

The output impedance is

$$Z = \sqrt{\frac{L_K + L_1}{C_1}} \tag{11}$$

This result shows that the circuit output impedance is larger than the stalk impedance due to the contribution of the leakage inductance. In order to minimize pulse reflections, the output cable and load shall match to the circuit output impedance Z rather then the stalk impedance.

Based on the result of Fig. 4 and (11), an N-stack induction voltage adder is reduced to an N-section transmission line as shown in Fig. 5.
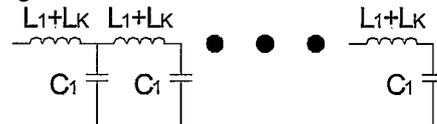

Fig. 5. A simplified inductive adder model.

The impedance of this N-section transmission line is Z as given in (11).

III. ESTIMATION ACCURACY AND EXAMPLE OF OUTPUT IMPEDANCE

To demonstrate the matching effect of output impedance and stalk impedance we use an example. Note that in the following example the stalk is shorted at left end and a matching load resistor is connected to the right end.
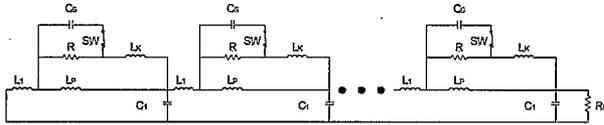
A. Example 1

Fig. 6. A single ended multi-stack inductive adder.

In this example, we investigate the circuit given in [5] a 30-stalk inductive voltage adder. Its parameters are listed in TABLE I.

TABLE I
SIMULATION PARAMETERS

Symbol	Parameter	Quantity
C_S	storage capacitance	24×10^{-6} F
L_P	primary inductance	20.9×10^{-6} H
L_K	leakage inductance	6.5×10^{-9} H
L_l	stalk inductance per stake	20×10^{-9} H
C_l	stalk capacitance	2.6×10^{-12} F
N	number of stakes	30
V_0	initial voltage of C_S	1000 V
R	parallel resistance	50
Z_{STALK}	stalk impedance	50

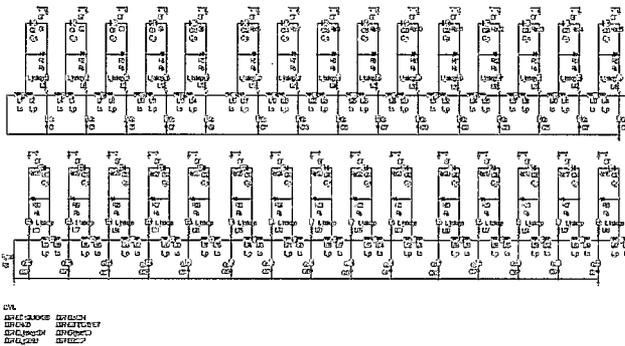The simulation circuit is shown in Fig. 7.

Fig. 7. A 30-stack inductive adder simulation circuit.

Using the impedance estimation formula given in (11) and parameters in Table 1, we have

$$Z = \sqrt{\frac{(20+6.5)e^{-9}}{2.6e^{-12}}} = 100.96 \quad \Omega$$

Here we use a 100 Ω load resistor that is close enough to the estimation impedance in the first simulation.
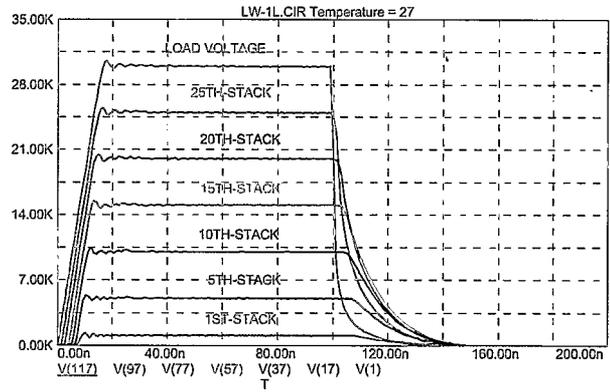

Fig. 8. Voltage pulse waveforms with 100 Ω load impedance.

As a comparison, we used a 50 Ω load resistor that equals the impedance of the stalk in the second case.
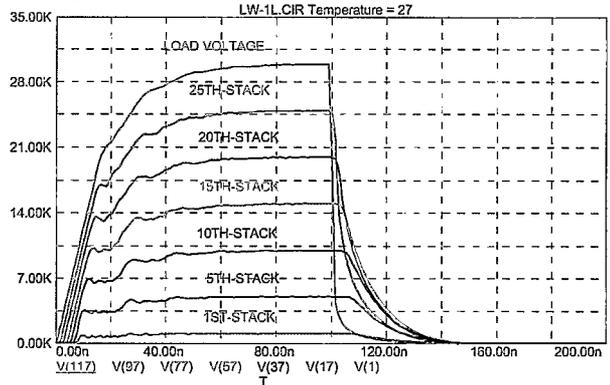

Fig. 9. Voltage pulse waveforms with 50 Ω load impedance.

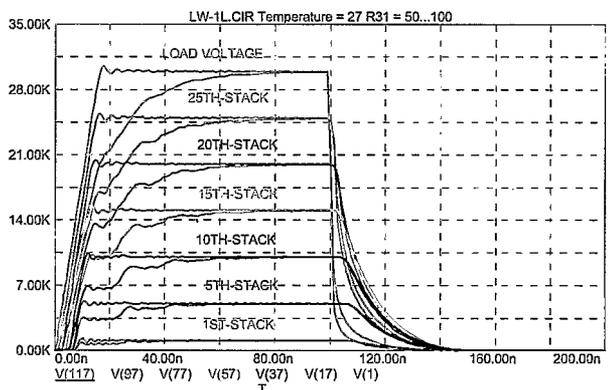The comparison of two simulation results is given in Fig. 10.

Fig. 10. Comparison of voltage pulse waveforms with 100 Ω and 50 Ωload impedances.

It is easy to see that using impedance estimation formula given in this paper produces a clean and sharp pulse waveform at load. This result also validates the merit to reduce stalk impedance [5] in order to match pre-specified load impedance of 50 Ω.

B. Accuracy of estimation

To evaluate the accuracy of the estimation, we wrote a short script in MATLAB®. This script calculates the output impedance of the stalk based on its actual parameters and the estimated output impedance using simplified method at each frequency of interest.

In Fig. 11, the blue trace is the output impedance of the circuit with actual parameters and the red trace is the estimated output impedance using formula in (11).

One can see that over the frequency range of pulse operation, the estimated parameter based on simplified method matches well with the actual output impedance.
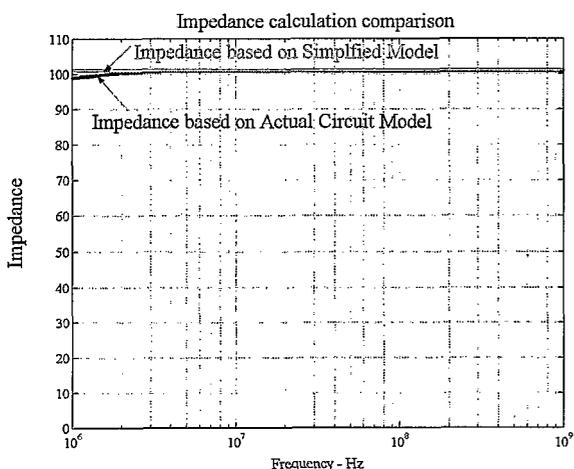

Fig. 11. Comparison of impedance calculation based on actual or simplified circuit model.

IV. ESTIMATION OF PULSE RISE TIME

The output pulse is generated by slightly discharging large storage capacitors of stakes. Each stack cell has a natural resonant frequency of

$$\omega_o = \frac{1}{\sqrt{(L_1 + L_K)C_1}} \qquad (12)$$

and a one-way propagation time as well as the pulse response time of

$$T_C = \sqrt{(L_1 + L_K)C_1} \cdot \qquad (13)$$

The pulses produced by each stack will travel bi-directionally and add up at load. If the inductive voltage adder is terminated at both ends with matched impedance loads, then the pulse rise time of each output pulse is

$$T_{RD} = N\sqrt{(L_K + L_1)C_1} \cdot \qquad (14)$$

A single ended inductive adder with matched impedance load and a short at the far end will have a rise time of

$$T_R = 2N\sqrt{(L_K + L_1)C_1} \cdot \qquad (15)$$

A. An example of pulse rise time estimation

An example can be given. Using parameters given in TABLE I, we have that the output pulse rise time is

$$T_R = 2 \times 30\sqrt{(20 + 6.5)e^{-9} \times 2.6e^{-12}} = 16.9 \ nS$$

We performed a computer simulation of the circuit used in Example 1, and its load voltage pulse rising edge verses time is shown in Fig. 12. The pulse rise time of other stacks are also shown for illustration. Here, all switches are assumed to be ideal and closed simultaneously at 1 nano-second from time zero of simulation.
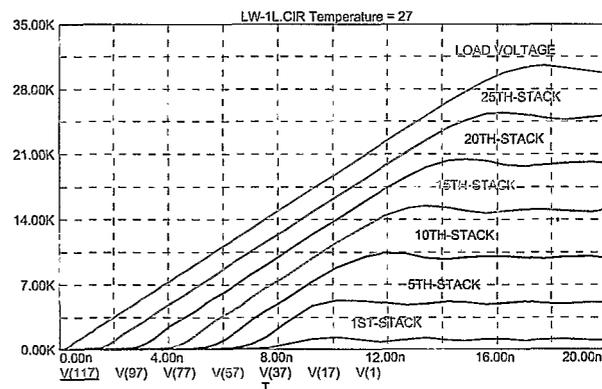

Fig. 12. Voltage pulse rising edge.

The result of load voltage rise time shown in Fig. 12 agrees with the calculation.

V. CONCLUSION

The parameter estimation methods based on simplified circuit models presented in this paper are accurate and easy to use. As inductive voltage adder technology becomes popular, the design tools will be needed to help design and development process. In addition, a simplified model and estimation method will illustrate the design concept to customers in a clear form.

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