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EXPONENTIAL SIGNAL RATE-OF-RISE MEASUREMENT INSTRUMENT

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UNIVERSITY OF CALIFORNIA
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Livermore, California

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Gale Holladay

Ervin Behrin

Donald Campbell

April 6, 1964

Exponential Signal Rate-of-rise Measurement Instrument

Gale Holladay, Ervin Behrin, and Donald Campbell

Lawrence Radiation Laboratory, University of California
Livermore, California

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ABSTRACT

An instrument for detecting the multiplication rate α of an increasing exponential signal of the form $Ee^{\alpha t}$ is described. Accuracies of 5% are obtained for α over the range 10 to 110 generations per microsecond. The input signal is split between attenuator and delay-inverter arms of a bridge network and then recombined by addition in the bridge output. Assuming a constant α input, the bridge output is a function of the attenuation, delay, and instantaneous input amplitude. The electronic circuitry samples and stretches the bridge output when the input signal reaches a fixed voltage level. The resulting output is a known function of α .

INTRODUCTION

The increasing exponential function $e^{\alpha t}$ [$\alpha > 0$] characterizes such natural events as gas discharges, neutron multiplication, and the transistor avalanche phenomenon. This report describes an instrument for measuring the rate of rise, α , of an increasing electrical exponential signal. The exponential rate detector (or alpha bridge) consists of a passive circuit having a discriminator at the input and a voltage sampling circuit at the output (Fig. 1). When one places an increasing potential signal into the rate detector, the output voltage of the passive circuit, at the time when the discriminator fires, relates to the rate of rise of the input exponential signal through known parameters.

The instrument will detect the value of α of a signal having the form $E = Ke^{\alpha t}$ where α is in the range 10 to 110 generations per microsecond. Equipment accuracy is approximately 5% when calibrated with existing exponential signal simulators.

The instrument has an input impedance of 50 Ω and requires a negative 100-V input signal whose α is constant between signal values -20 and -100 V. The unit provides a negative, stretched output pulse having a 15-sec decay time constant so that the pulse magnitude can be easily determined. The magnitude of the output pulse relates to the rate-of-rise of the input signal through a calibration curve. The rate detector provides a +60-V fast rising pulse as a timing reference as well as lock-out and disabling features to protect output information. Four rate detectors and a power supply are constructed in a standard LRL module chassis. Various views of the instrument are given in Figs. 2 through 5.

THEORY OF OPERATION

Block diagrams of the passive bridge network and the electronic circuitry of the instrument are shown in Figs. 1 and 6, respectively.

In the following discussion, delay in the electronic circuitry, attenuation network, or connecting cables, as well as attenuation in the inverter and delay network, will be considered negligible. In general, these are valid assumptions since compensating delays can be added to any parallel path and any attenuation in the inverter and delay network can be considered as part of the attenuation network.

If the input signal is of the form $E_s \exp(\alpha_s t)$, then the signal at the summing junction due to the attenuation network is given by $[E_s \exp(\alpha_s t)]/A$ and the signal due to the inverter delay network is given by $-E_s \exp[\alpha_s(t - t_d)]$.

The total signal at the summing junction for any time t is therefore

$$e_{out} = \frac{E_s}{A} \exp(\alpha_s t) [1 - A \exp(-\alpha_s t_d)]. \quad (1)$$

If we let E_T and t_T represent the voltage and the time when the discriminator fires, then

$$E_T = E_s \exp(\alpha_s t_T) \quad (2)$$

represents the input signal at this moment.

Solving for t_T and substituting this value for t in Eq. (1) gives us the voltage at the output when sampling takes place.

$$e_{out} = \frac{E_T}{A} [1 - A \exp(-\alpha_s t_d)]. \quad (3)$$

If, as a design parameter, we let A and t_d be related by the equation

$$A = \exp(\alpha_0 t_d) \quad (4)$$

where α_0 can be considered as the value to which the unit is "tuned"; then, substituting Eq. (4) into Eq. (3) we obtain for the output voltage

$$E_{out} = \frac{E_T}{A} \left\{ 1 - \exp[(\alpha_0 - \alpha_s)t_d] \right\}. \quad (5)$$

Therefore, the output voltage is a function of known parameters and α_s . The polarity of the signal at the summing junction depends on whether the signal α_s is greater or less than α_0 . A graph of Eq. (5) is shown in Fig. 7.

It should be noted that Eq. (5) becomes linear about the α_0 point. This is shown by restricting the quantity $(\alpha_0 - \alpha_s)t_d$ to be less than or equal to 0.15. With this restriction, the function $1 - \exp[(\alpha_0 - \alpha_s)t_d]$ can be represented to a 1% accuracy by the first term of its Maclaurin expansion.

$$1 - \exp(\alpha_0 - \alpha_s) \approx (\alpha_s - \alpha_0)t_d.$$

The output voltage of the passive network is then given by the linear equation

$$E_{out} = \frac{E_T t_d}{A} (\alpha_s - \alpha_0). \quad (6)$$

PASSIVE NETWORK

The 10-ft length of 50- Ω RG 174/U cable in the input compensates for the circuit delay between discriminator action and sampling (see Fig. 8). Time delay is obtained by the addition of an external 93- Ω RG 194/U cable. Inversion is obtained by a distributed inverter consisting of 10 turns of RG 195/U on a ferrite core terminated by R12. Two 51- Ω , 2-W carbon composition resistors form the attenuation network and summing is obtained by floating the terminated output of the distributed inverter on the attenuation network.

DISCRIMINATOR

The three series diodes, CR1, CR2, and CR3, shown in Fig. 9 are reverse biased to -100 V. The tunnel diode, CR5, is biased in its low voltage state, holding the regenerative trigger circuit Q1 and Q2 off.

The incoming exponential pulse triggers the discriminator when its amplitude overcomes the reverse bias on the series diodes. The additional current supplied by the input pulse switches the tunnel diode to its high voltage state which turns on the regenerative circuit.

The regenerative circuit triggers both the sampling pulse generator and the timing pulse generator through transformer T2. The regenerative circuit also sends a trigger pulse to the delay and disable circuit through C5. Transistors Q1 and Q2 remain conducting, thus locking out the discriminator, until RE1 is energized. The energizing of RE1 removes the regenerative circuit supply voltage and returns CR5 to its low voltage state. A manual reset pushbutton, PB1, is located on the front panel. External resetting may be accomplished by PG9, located on the rear of the module rack. Meter ME1 monitors the discriminator current and serves as a reset indicator.

CR1, CR2, and CR3 are connected in series to lower the input capacitance of the discriminator, and thereby reduce the discriminator rate sensitivity. Resistors R1 and R2 and capacitor C1 comprise a network to further reduce rate sensitivity. Diode CR4 provides protective clamping of all positive signals and all negative signals greater than 120 V.

PULSE GENERATORS

In Fig. 10 the sampling pulse generator Q3 supplies the pulse that samples the output of the passive network. Q3 discharges the charging line composed of L1, L2, C7, C8, and C9 into the 100- Ω attenuation potentiometer R10. The sampling pulse is available for monitoring at PG2, located on the printed circuit board. The attenuation potentiometer R10 is used to adjust the range of the system by regulating the amplitude of the sampling pulse. Transistor Q3 must be selected to avalanche. The sampling pulse characteristics are as follows:

- A. Shape: rectangular
- B. Amplitude: 40 V
- C. Width: 5-10 nsec
- D. Rise and fall times: 2 nsec

The timing pulse generator, Q16, provides a positive, fast rising pulse for external timing. Q16 operates as an avalanche switch to discharge C25 into the 50- Ω timing pulse load. PG4 must be terminated into 50 Ω at all times to maintain calibration accuracy. Transistor Q16 must be selected to

avalanche. Timing pulse characteristics are:

- A. Shape: tail pulse
- B. Amplitude: 60 V
- C. Width: 120 nsec total
- D. Rise time: 3 nsec

SAMPLING CIRCUIT

Point A is initially biased to -10 V by the temperature compensated network composed of R15, R16, and CR10 (Fig. 11).

The leading edge of the sampling pulse drives point A until diodes CR6 and CR7 are forward biased. Point A now assumes the sampling point voltage. The trailing edge of the sampling pulse now reverse biases the diodes, and the voltage at point A decreases the full magnitude of the sampling pulse. Capacitor C11 couples the voltage changes at point A to point B. Upon completion of sampling, the voltage at point B is given by

$$V_S - (V_P + V_B)$$

where V_S is the sampling point voltage, V_P the magnitude of the sampling pulse, and V_B the original bias voltage. Thus, for constant V_P and V_B , the voltage input to the pulse stretcher bears a linear relationship to the sampling point voltage. CR8 and CR9 limit the sampling point voltage to within ± 10 V so that information stored in the pulse stretcher is not affected by signals arriving after the sampling pulse generator fires.

PULSE STRETCHER

The sampled signal at the input to the pulse stretcher has approximately a 20- μ sec decay. The input circuit of the pulse stretcher (Fig. 12) is a White emitter follower, Q4 and Q5. This circuit amplifies the negative sampled signal and drives Q7, a current amplifier. Q7 turns on another current amplifier, Q8, and allows a charge to be placed on the stretching capacitor C16. This negative charge starts to turn off the field effect transistor, Q9, which in turn drives the emitter follower Q11 on, and the output of PG6 becomes negative. Diode CR14 feeds back the output signal to the emitter of Q7. Q7 shuts off when this feedback voltage is the same as its base voltage. This feedback loop makes the gain of the stretcher approximately one. When the input circuit begins to decay, C16 remains charged;

as its discharge path is through the parallel combination of the reverse biased diode CR15 and the high input impedance of the field effect transistor Q9. C16's decay is approximately 15 sec.

With no input to the stretcher, the output is held to approximately -150 mV by the dc feedback loop composed of CR14, the emitter base junction of Q7, CR13, and CR12. This feedback loop is temperature compensated by thermistor R20 and resistors R21 and R22.

Contact RE1-2 resets the pulse stretcher by shorting C16 to ground through a 100-K resistor R28. Ten μ sec after discriminator action, Q6 is turned on by the delay and disable gate generator and disables the pulse stretcher by reverse biasing the emitter base junction of Q8, thus preventing C16 from being further charged.

DELAY AND DISABLING GATE GENERATOR

The function of the delay and disabling gate circuitry of Fig. 13 is to render the pulse stretcher inoperative during the time the output voltage is being read. The operation begins when the discriminator pulse triggers a 10- μ sec single shot multivibrator composed of Q12 and Q13. This 10- μ sec multivibrator delays the disabling action until sampling has been completed. The return of the single shot triggers Q14 and Q15, a 300-msec single shot multivibrator. The 300-msec single shot turns on Q6, the pulse stretcher disabling transistor. After 300 msec, the stretcher returns to its normal condition.

BATTERY POWER SUPPLY

The battery power supply, shown in Fig. 14, consists of six batteries which provide all the voltages necessary to operate four rate detectors. A diode-meter arrangement provides a quick, front panel method of checking battery condition. Battery life is approximately 80 h when operating four rate detectors.

The -100-V bias supply is regulated by zener diode CR5 located in the wireway at the rear of the module rack. This arrangement insures that the critical bias voltage remains independent of battery condition or power supply module used.

AC POWER SUPPLY

The ac power supply module (see Fig. 15) provides all the voltages necessary to operate four rate detectors. All output voltages are zener regulated and decoupled to prevent transient pickup. The ac input is bypassed with feedthrough capacitors to reduce line transients.

The -212, -112, and -100 V supplies are obtained from a full wave voltage doubler. Zener diodes CR3 and CR4 provide the -212 and -112 V outputs. A zener diode in the module rack regulates the -100 V bias supply.

RESULTS AND CONCLUSION

Figure 16 shows a typical rate detector calibration curve. This graph illustrates that the main problem in using the rate detectors for accurate measurements is obtaining accurate calibration signals. The basic limitation within the unit is pulse-to-pulse jitter caused primarily by the sampling pulse generator. This average error is approximately ± 50 mV. The complete schematic of the rate detector is shown in Fig. 17.

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Fig. 1. Simplified block diagram — exponential rate detector.

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Fig. 2. Complete battery operated module rack and ac power supply module.

Fig. 3. Rate detector.

Fig. 4. AC power supply.

Fig. 5. Battery supply.

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Fig. 6. Complete block diagram.

Fig. 7. Graph of the function $E_{out} = \frac{E_T}{A} \left\{ 1 - \exp[(a_0 - a_s)t_d] \right\}$.

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Fig. 8. Passive network.

Fig. 9. Discriminator.

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Fig. 10. Sample pulse generator and timing pulse generator.

Fig. 11. Sampling circuit and waveforms.

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Fig. 13. Delay and disable gate generator.

NOTE:

1. J1 THROUGH J6 ARE TIP JACKS

Fig. 14. Power supply battery.

Fig. 15. Power supply for exponential rate detector.

Fig. 16. Typical laboratory calibration curve.

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