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AN INTERACTIVE GRAPHICS DISPLAY
SYSTEM FOR HYDROLOGIC ANALYSIS

K. M. Busness

December 1970

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AN INTERACTIVE GRAPHICS DISPLAY SYSTEM
FOR HYDROLOGIC ANALYSIS

K. M. Busness

Computers and Control Department
Systems and Electronics Division

December, 1970

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ABSTRACT

A computer controlled interactive graphics display system has been developed to enhance the study of problems related to water resources and pollution control. A Digital Equipment Corporation PDP-9 digital computer serves as the controller for a UNIVAC 1558 display console and an Edwin Industries graphics digitizing table. Supplemental data storage is provided by a Digital Development Corporation fixed-head disc.

TABLE OF CONTENTS

	<u>Page</u>
ABSTRACT.	iii
FIGURES	vii
TABLES	vii
INTRODUCTION	1
SUMMARY SYSTEM DESCRIPTION.	2
DIGITAL COMPUTER	2
GRAPHIC DISPLAY SYSTEM	2
Type 1558 Console.	2
Vector Generation.	5
Character Generation.	10
Display Console Keyboard	12
Display Console Light Pen	12
Display/PDP-9 Interface.	13
DISPLAY REFERENCE DOCUMENTS	19
DISC MEMORY SYSTEM	20
Disc Storage Unit.	20
Disc/PDP-9 Interface.	24
Disc Instructions.	29
DISC REFERENCE DOCUMENTS	31
GRAPHIC DIGITIZING SYSTEM	32
Coordinate Digitizer.	32
Digitizer/PDP-9 Interface	32
DIGITIZER REFERENCE DOCUMENTS.	36
SOFTWARE.	37

AN INTERACTIVE GRAPHICS DISPLAY SYSTEM FOR HYDROLOGIC ANALYSIS

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INTRODUCTION

The study of large and complex ground water flow systems and the development of related mathematical models by classical techniques has been an extremely difficult and time-consuming process. The application of the digital computer to hydrology studies in recent years has vastly improved analytic and predictive capabilities, but still does not efficiently fulfill the scientist-program interaction requirement. Flow system modeling is typically a trial and error process which requires an appreciable degree of data manipulation to effect an accurate solution. Although the computer excels in mathematic capability, relative inefficiencies in data input-output methods have inhibited an effective operator interface.

In an attempt to more closely align the researcher and his tools, a highly interactive data display system has been developed at Pacific Northwest Laboratories. This report describes the various components in the system hardware configuration and explains their operation. Detailed discussion of system software is not included.

SUMMARY

An interactive graphics display system has been developed by interfacing a digital computer, CRT display, coordinate digitizer and disc memory. The system is controlled via a Digital Equipment Corporation PDP-9 digital computer. A UNIVAC Model 1558 CRT Display Console with full graphics capability, keyboard and light pen serves as a peripheral interactive device. Graphical data is converted to digital form for computer-manipulation by means of a coordinate digitizer manufactured by Edwin Industries. Additional data storage capacity is provided by a Digital Development Corporation fixed-head disc.

SYSTEM DESCRIPTION

The interactive graphics display system is shown in Figure 1.

Several additions to the hardware configuration described in this report are planned in the near future. These include a 40 kilobaud data link to a UNIVAC 1108 computer, additional core memory for the PDP-9 digital computer and DECTape magnetic tape transports. Camera equipment will also be used to obtain permanent records of CRT displays.

DIGITAL COMPUTER

The PDP-9 is a general purpose parallel binary computer having a memory configuration of 8192 18-bit words and basic machine cycle time of 1 μ sec. Three standard peripheral devices provide program input/output: a 300 character/second paper tape reader; a 50 character/second paper tape punch; and a KSR-33 teleprinter. The computer mainframe also includes a real-time clock, automatic priority interrupt system, extended arithmetic unit, and direct memory access multiplexer.

GRAPHIC DISPLAY SYSTEM

Type 1558 Console

The salient characteristics of the UNIVAC 1558 Display Console are shown in Table I.

Upon appropriate commands from the digital computer, the console is capable of displaying, on a cathode ray tube screen, absolute and relative long vectors, relative short vectors (0.75 inch or less) and tabular mode character plotting. Two character sizes, 90 degree character rotation, three intensity levels (including blank), and vector texture selection are provided under program control. An alphanumeric keyboard with character and function keys and light pen are available for operator input.

The display medium is a 19 inch diameter cathode ray tube with a usable viewing area of approximately 12 inches horizontally by 12 inches vertically. Data is positioned on this viewing area with respect to a point position matrix square having 1024 addressable points in both X and Y directions. Therefore, a raster unit may be defined as the distance

FIGURE 1. *Interactive Graphics
Display System*

TABLE I. *Summary of UNIVAC 1558 Display Console Characteristics*CRT CHARACTERISTICS:

- A. 12" x 12" VIEWING AREA
- B. 1024 x 1024 POSITION ADDRESSABLE GRID
- C. 0.020" SPOT SIZE
- D. P31 PHOSPHOR

DATA ENTRY:

- A. STANDARD A/N KEYBOARD
- B. 40 FUNCTION KEYS
- C. LIGHT PEN

DRAWING MODES:

- A. LONG VECTOR Absolute or relative to any position
on viewing area. Writing speed (full
screen vector): 32 μ sec
- B. SHORT VECTOR: Relative (up to 63 raster units):
2 μ sec
- C. CHARACTER MODE: Average paint time (after positioning);
5 μ sec. Positioning time: 2 μ sec.
90° rotatable characters
- INTENSITY: 3 programmable levels (including blank)
- VECTOR TEXTURE: Solid, dashed, center line, intensified
end point

INTERFACE:

- A. ESA MODE: 18 bit
- B. DISPLAY COMMANDS: Long vector (2 words), short vector
(1 word), character mode (2 characters/
word)
- C. DISPLAY LIST CONTROL WORDS: JUMP, HALT, FLAG
- D. INTERRUPTS: Light pen, keyboard, view area overflow,
flag

between two horizontal or vertical adjacent points. The position matrix zero reference point is at the lower left corner of the position matrix.

The display console is pictured in Figure 2. A block diagram is shown in Figure 3.

Vector Generation

The 1558 Display has two vector modes; long and short. A line segment may originate at any point on the position matrix and terminate on any other point within the matrix. The time required to blank position the electron beam on the CRT is 16 microseconds maximum, a worst case condition where a full screen movement occurred. The time required to draw a full screen diagonal, assuming the electron beam has already been positioned at the starting point is 32 microseconds, while the time to draw a vector up to 63 raster units long is approximately 2 microseconds. This timing information is measured from the instant at which the input data is available to the deflection system, but accessing of display command words is normally initiated prior to the completion of execution of display commands, providing minimal overhead time for command word accessing.

Long Vector Mode

In long vector mode, the destination of the vector to be drawn is specified (relative mode) relative to its present resting point or is specified (absolute mode) to an absolute position relative to the origin of the position matrix. Two words are required to define this command.

Long Vector Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
f=11		C	B	Z	R	S	<u>+X</u>	ΔX										1ST WORD
		A	I		T	<u>+Y</u>	ΔY										2ND WORD

FIGURE 2. CRT Display Console

FIGURE 3. Display Console Block Diagram

- f (2 bits): Function code 11 denotes "Long Vector" mode.
- Z (1 bit): Z = 0 specifies "relative" vector mode, i.e., beam movement by an amount ΔX , ΔY relative to its present position.
Z = 1 specifies "absolute" vector mode, i.e., beam movement to a point ΔX , ΔY relative to the origin of the position matrix.
- B (1 bit): B = 1 overrides intensity and texture control to produce a blanked beam.
- C (1 bit): C = 1 denotes entry into "tabular" mode following this vector. Also, C = 1 causes resetting of the current "rotate" and "size" control according to the R and S bits.
- R (1 bit): R = 0 specifies that characters are written in the normal horizontal line format.
R = 1 specifies that characters are rotated 90° counter-clockwise with respect to the normal vertical orientation.
- S (1 bit): S = 0 specifies small characters (80 per line).
S = 1 specifies large characters (40 per line).
- +X (1 bit): +X = 0 specifies positive X movement. (Ignored in absolute mode).
+X = 1 specifies negative X movement. (Ignored in absolute mode).
- ΔX (10 bits): The ΔX field specifies the length of the X component of the vector from its present position for Z = 0, and the final X position relative to the origin for Z = 1.
- ΔY (10 bits): This field specifies the same information for Y as ΔX does for X.
- A (1 bit): A = 1 commands resetting of intensity and texture controls with the values of I and T contained in this word. For A = 0, I and T fields are ignored and intensity and texture controls remain unchanged.
- l (2 bits): When A = 1, these two bits define intensity level for this and all following unblanked vectors and all characters, until a subsequent long vector command with A = 1 changes it.

Coding:

I	:	0 0	blank or intensity "off"
		0 1	low intensity
		1 0	high intensity
		1 1	blank or intensity "off"

T (2 bits): When A = 1, these bits define texture for this and all subsequent unblanked vectors until a subsequent long vector command with A = 1 changes it.

Coding:

T : 0 0 solid line (_____)

0 1 dashed line (-----)
50% on, 50% off with the start of the vector drawn

1 0 center line (_____)
40% on, 20% off, 20% on, 20% off with the start of the vector drawn with the long dash

1 1 blank with intensified vector end point

Short Vector

In short vector mode, beam movement is specified relative to its present resting point. The length of vectors in this mode may be from zero to 63 raster units. A short vector is specified by a single command.

Short Vector Word

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

F=10	C	B	<u>+X</u>	ΔX						<u>+Y</u>	ΔY					
------	---	---	-----------	------------	--	--	--	--	--	-----------	------------	--	--	--	--	--

f (2 bits): Function code 10 denotes "short vector" mode.

B (1 bit): B = 1 causes the beam to be blanked for this vector.
B = 0 denotes that the intensity and texture of this vector are as previously specified.

+X (1 bit): +X = 0 specifies positive X movement.
+X = 1 specifies negative X movement.

ΔX (6 bits): The ΔX field specifies the length of the X component of the vector.

+Y (1 bit): +Y = 0 specifies positive Y movement.
+Y = 1 specifies negative Y movement.

ΔY (6 bits): The ΔY field specifies the length of the Y component of the vector.

C (1 bit): C = 1 denotes entry into "Tabular" mode following this vector. Rotate and size control remain as previously set.

Character Generation

The 1558 Display Console contains a character generator, employing a continuous stroke technique with a maximum of eight strokes available for symbol construction.

Two character sizes are available under program control. Large characters, approximately 0.190 x 0.280 inches in size, are written at 40 characters per line with 28 lines required to fill the viewing area. Small characters are written at 80 characters per line with 56 lines required to fill the viewing area. The small characters are approximately 0.095 x 0.140 inches in size. Figure 4 illustrates character display.

A 90° counterclockwise rotation of a character from its normal left to right orientation is available under program control with the point of rotation at the lower left corner of the character. This is also the point of reference of the character on the 1024 by 1024 position matrix, i.e., a character at position (X,Y) will be positioned such that its lower left corner is located at the point (X,Y).

The time required to draw a character, with the electron beam already positioned at the starting point, is dependent upon the number of strokes required to draw the character. This time may be from 2 to 8 microseconds with an average character painting time of 5 microseconds.

Tabular Mode

One word specifies two alphanumeric characters. Character #1 is painted first, followed by beam movement one space right (or one space up if "Rotate" mode is in effect), and then character 2 is painted. The beam then spaces once more in preparation for the characters of the following word. Tabular mode is terminated by the setting of exit bits E_1 and E_2 . Upon exit from this mode, the next word is interpreted as a command word. If the two upper bits of the character code are zero no character will be painted and no spacing will occur. This no-op condition does not affect the exit conditions.

Character Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
E_1	CHAR A								E_2	CHAR B							

E_1 (1 bit): $E_1 = 1$ causes exit from Tabular mode following the painting of character #1.

CHAR A (8 bits): This field specifies the code for character #1.

E_2 (1 bit): $E_2 = 1$ causes exit from Tabular mode following the painting of character #2.

CHAR B (8 bits): This field specifies the code for character #2.

Display Console Keyboard

The keyboard consists of a slightly modified alphanumeric keyboard and a set of function keys (including editing and cursor control keys). All keys are labeled for identification. Upon depression of any key, a unique 7-bit ASCII code is transmitted from the display console to the computer by means of an interrupt. The depression of any key which is not on the alphanumeric portion of the keyboard sends a function bit along with the 7-bit function code. A plastic overlay activates a combination of seven overlay switches and causes, upon depression of the "transmit" switch, a transmit bit and a 7 bit code unique to the particular plastic overlay to be transmitted to the computer. This identifies the overlay and permits applications wherein the function key codes are interpreted differently by the computer stored program for different overlays. The keyboard configuration, character and function codes are shown in Appendix A.

Display Console Light Pen

A light pen is provided to allow construction of displays or modification of existing displays. The light pen is enabled/disabled by means of the previously discussed external function control word. Using the light pen in conjunction with function keys on the console keyboard makes possible a wide range of light pen editing operations; i.e., construction, deleting, moving, calling up new display files, etc. The light pen communicates with the computer by means of an interrupt word.

Display/PDP-9 Interface

A block diagram of the display-computer interface is shown in Figure 5. Two unique data paths are used as display-computer links. The major data interchange utilizes the Direct Memory Access feature (DMA) in the PDP-9. The DMA facility provides an output data path from PDP-9 core memory to the display console which functions on a "cycle stealing" basis. When the display transmits an output data request, the computer operation in progress is suspended for one memory cycle while a word is transmitted from memory to a buffer register within the interface and subsequently to the display for execution. DMA requests have highest precedence in the priority structure of the PDP-9, and are granted within two memory cycles.

The second data path is the normal I/O transfer through the computer I/O bus and Accumulator register. This channel is used to force an instruction word to the display to initialize a display operation or to transmit a display interrupt word into the computer.

Forced Output Mode

Display console operation is normally initiated by forcing a command to the display by means of IOT (Input/Output Transfer) instruction LDBF (Load Display Buffer from AC). See Appendix B for complete IOT listing. The desired first instruction is loaded into the PDP-9 Accumulator. LDBF is next executed to load the word into the interface output data (OD) buffer and subsequently into the display registers. The first word is usually an ESA Jump (Externally Specified Address) instruction which causes the display to emit an output data request (ODR). The ODR functions as a break request signal to the computer DMA. At this time, the DMA and display may function independently from other computer activity, executing a prestored display program.

DMA Output

A break request (ODR) to the DMA results in a word output to the OD buffer. This action generates an output acknowledge pulse which strobes the OD buffer into the display logic for execution. As the instruction execution occurs, the ODR line again activates and the process is repeated.

FIGURE 5. Display Interface Block Diagram

This interchange continues until a special command word or interrupt intercedes.

The display may be cycled within an instruction file by means of the ESA Jump instruction. An ESA Jump at the end of a display file can be used to route the program back to the top of the file or to another file. The implementation of the ESA mode of operation requires the following instruction:

ESA Jump Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
f	0	0	ADDRESS FIELD														

f: f = 01 indicates ESA jump command.

The address field contents replace the current contents of the display ESA register causing the next display instruction to be extracted from the specified address in the digital computer memory.

Interrupt Structure

The utilization of the picture composition and editing features of the console requires a number of interrupt status words to be sent to the computer. Interrupts are sent when a light pen "hit" is detected, a position register overflow condition occurs, a general control flag is received from the computer, or when a key is depressed on the keyboard. The display console is halted until the computer accepts and acknowledges the interrupt data.

Light Pen Interrupt Word

0	1	2	3	4	17
F = 00	0	0	ESA REGISTER		

Upon detecting a light pen "hit," an interrupt is sent to the computer along with the ESA of the element (vector or character) which was being painted at the time of the hit. Bits 2 and 3 indicate the type of element being displayed.

Bits		<u>Mode</u>
2	3	
0	0	Character, C1
0	1	Character, C2
1	0	Long Vector
1	1	Short Vector

Overflow Interrupt Word

0	1	2	3	4	17
F = 10	0	0	ESA REGISTER		

Recognition of the flag bit (F = 1) in a Function Control word causes an External Interrupt with the contents of the ESA register containing the control command word address

Keyboard Interrupt Word

0	1	2	3	4	5	6	7	8	9	17
F = 11	0	0	0	0	0	0	0	KEYBOARD CHARACTER CODE		

Each depression of a keyboard key results in an External Interrupt to the computer along with a nine bit binary code representing that particular key. Bit 9 indicates that a function key has been depressed. Bit 10 indicates that the transmit key has been depressed.

All of the previously discussed interrupts input to the Automatic Priority Interrupt system (API) in the PDP-9. The interrupt (on API level 1) traps the program in progress to memory location 63_8 . Executing the instruction in this location causes the program to enter a subroutine to service the display interrupts. A flag search determines which of the four possible interrupts has occurred, and appropriate action can be taken.

Continuation of display following an interrupt requires that the display receive an interrupt acknowledge (DSIA instruction) from the computer. Following a light pen interrupt, instruction DSLB is additionally required to resume display operation.

Interrupt and DMA activity related to the display *only* can be program controlled. Two IOT instructions, DSEI and DSDI, can be used to enable and

disable *display action*, respectively, while allowing *other* devices *normal access* to DMA and API operations.

Function Control

An additional control word in the display instruction repertoire allows control of various display functions while executing a display program. In addition to providing light pen control, its most useful function is that of providing interrupts during display execution.

Function Control Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
f	H	F	P	D	C	Not Used											

The use of the function control word and the significance of each lettered key position is indicated below:

- f: These two bits are 00 for all operations in the external function control mode.
- H: For H = 1 the display unit ceases to display until another external function is executed from the computer.
For H = 0 the display unit shall continue to operate as specified.
- F: For F = 1 an external interrupt shall be sent to transfer control to the computer.
For F = 0 no external interrupt shall occur.
- P: For P = 1 the D bit shall be examined.
For P = 0 the D bit shall be ignored.
- D: For D = 0 the light pen shall be disabled.
For D = 1 the light pen shall be enabled.
- C: For C = 0 the tabular mode shall not be entered.
For C = 1, the next word executed will be executed in the tabular mode with rotation and size (R and S) as specified by the most recently executed vector mode word that specified these parameters.

Physical Characteristics

Physically, the display interface utilizes printed circuit modules which are inserted into a wire-wrapped connector plane. The modules consist of discrete component type cards, made by Digital Equipment Corporation, which are similar to circuit cards within the PDP-9, and DTL integrated circuit cards developed within PNL. Functional descriptions of the various modules are found in related maintenance documents.

DISPLAY REFERENCE DOCUMENTS

1. UNIVAC 1558 Display Console - Operation Analysis PX5021,
UNIVAC, St. Paul, Minnesota, March 1969.
2. UNIVAC 1558 Display Console - Servicing Data and Adjustments
PX5022, UNIVAC, St. Paul, Minn., March 1969.
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PX5066, UNIVAC, St. Paul, Minn., March 1969.
4. UNIVAC 1558 Display Console - Servicing Diagrams PX5034,
UNIVAC, St. Paul, Minn., May 1969.
5. UNIVAC 1558 Display Console - Schematic Drawings PX5038,
UNIVAC, St. Paul, Minn., October 1969.
6. PDP-9 User Handbook, Digital Equipment Corporation, Maynard,
Mass., January 1968.
7. Digital Logic Handbook, Digital Equipment Corporation, Maynard,
Mass., 1967, 1969.

DISC MEMORY SYSTEMDisc Storage Unit

A Model 14120 Disc Memory Unit supplied by the Digital Development Corporation (see Figure 6) supplements system memory requirements. The disc unit is of highly reliable fixed-head per track design. Read-write heads are pneumatically actuated to an optimum "flying" position. Automatic head retraction occurs when power is removed, assuring that head-disc contact never occurs. Recording surfaces are sealed in a slightly pressurized helium environment to minimize surface contamination and bearing lubricant deterioration. The pressurization system is the only item in the disc unit requiring periodic maintenance.

The principal disc unit characteristics are shown in Table III.

A card rack beneath the disc unit houses the read-write and head addressing electronics supplied by the manufacturer. Manually operated write lockout switches are located on the disc unit front panel assembly. A motor power reset switch is also located on the front panel as are several indicators whose functions are described in Table II.

TABLE II *Disc Indicators*

<u>Indicator</u>	<u>Function</u>
MOTOR POWER ON	Indicates that AC power is applied to the disc unit
ACTUATION PRESSURE LOW	Indicates that head actuation pressure is below nominal
DRUM SPEED LOW	Indicates below nominal operating speed (<3300 RPM).
DRUM TEMP HIGH	Indicates a temperature rise above 150 °F in the sealed drive unit (This condition would also result in removal of motor power)

A block diagram of the disc unit is shown in Figure 7.

FIGURE 6. Disc Storage Unit

TABLE III *Disc Characteristics*

Discs	2
Tracks (Heads)	256 (Non-Contact)
Addressable Sectors	4096
Total Data Words	458,752
Parity	Checksum/Sector
Word Transfer Rate	103 kHz
Run-Speed	3600 RPM
Access Time (Average)	8.5 milliseconds
Write Lockout	128 Tracks
Disc Timing	Bit Clock
	Word Mark
	Sector Mark
	Index Mark
Head Actuation	Pneumatic
Enclosure	Sealed (Helium)
Motor Voltage	115 V., 60 CPS
Start Current	6.8 A.
Run Current	1.1 A.
Operating Temperature	32-105 °F

FIGURE 7. Disc Block Diagram

The disc memory area is organized into sector addressable blocks of 114 words each which may be accessed singly or in multiple strings. The track and sector formats are included in Appendix C. Write lockout may be selected in groups of 8 tracks for up to half of the total storage capacity.

Two status flags are available from the disc unit electronics. A DISC READY line indicates that the disc has reached operating speed and that head actuation pressure is correct. A PERMISSABLE ADDRESS signal advises of an improper address selection when a write operation is attempted on a protected track. The remaining signal lines from the disc unit are read data, write data, write enable and timing.

Disc/PDP-9 Interface

Figure 8 illustrates the functional block diagram of the disc interface.

All data transfers between disc memory and core memory utilize the DMA multiplexer. Variable length data strings of from one word to entire memory capacity are transferred at a 103 kHz word rate.

The interface provides control of data block length, core memory address and disc address functions. Three registers must be initialized prior to a data transfer; a memory counter (MC), a word count (WC) register and disc address register.

Memory Counter

The MC register informs the computer memory address control, through the DMA, which core memory location is to be accessed for a word transfer. This 15-bit register is loaded from the computer accumulator with a word which represents the starting core address. The MC is incremented automatically by a DMA control pulse during each transfer, simplifying sequential operation.

Word Counter

A word count register is initialized from the computer accumulator to contain the 2's complement of the number of words to be transferred.

FIGURE 8. Disc Interface Block Diagram

The WC is also incremented during each transfer. Word count overflow halts disc activity and an interrupt flag indicates completion of the transfer.

Disc Addressing

A third initializing register determines a starting address on disc. Loading the disc address register from the accumulator directly precedes a data transfer, since coincidence between this register and one which is incremented by disc clocking initiates the transfer.

The disc storage area is organized for addressing by track and sector within a track.

Appendix C includes a disc format illustration.

Any one of 256 different tracks and any of 16 sectors within a track may be addressed. Disc unit electronics allows only one track to be active at any given time. However, when the last sector of a track has been accessed and the specified word count has not been satisfied, the track address is automatically incremented to the next consecutive track number.

Data Transfer

Two 18-bit registers provide data buffering and parallel-serial conversion. The Data Buffer (DB) register accepts parallel data from the computer DMA port during write mode and receives data from a shift register (SR) for entry into memory (through DMA) when reading. Data are transferred between the DB and DMA at a 103 kHz word rate and between the SR and disc at a 1.8 MHz bit rate.

All timing for disc/interface exchanges is derived from a timing track which was factory recorded on the disc. Data transfers are synchronized with memory timing to insure that "cycle-stealing" for DMA operations does not destroy current central processor activity.

A four-bit checksum register increments with each data "1-bit." When writing to disc, the checksum register contents are written as the last word in each sector. When reading, the checksum register contents

are compared with the last word in the sector (the checksum written). A parity error results if the two words are not identical.

Control and Timing

Timing signals from the disc timing track are conditioned in the interface to allow a 3-bit delay in all read (disc to core) operations. The delay is required to allow for signal propagation time through the read logic circuitry in the disc.

Numerous control circuits provide for proper sequencing through preamble, data and checksum intervals, selection of read or write modes, data shifting, address incrementing and interrupt detection.

All operations directly related to data transfer depend on the disc timing track for synchronization. Signals derived from the timing track are:

Clock 1 - Bit clock occurs every 540 ns.

Clock 2 - Occurs midway between Clock 1 pulses.

Origin Pulse - One per disc revolution.

Sector Mark - Marks the start of each of 16 sectors per revolution.

Word Mark - Marks the start of each word within a sector.

A diagrammatic description of disc timing is included in the Appendix.

Detailed Operational Theory

Several flow chart diagrams are included in Appendix E. These diagrams illustrate the various sequential operations which occur in the process of effecting a disc transfer. The following steps outline the events which occur in a disc access:

1. Test disc status
2. Load memory counter
3. Load word counter
4. Load disc address and select read/write
5. Address coincidence starts transfer
6. If reading, test checksum for each sector
7. Detect done flag upon completion of transfer.

Read Sequence

Prior to initiation of a disc transfer, the physical status of the disc unit is tested by instruction DKRF (Skip if disc ready). The Memory Counter is loaded from the computer accumulator by DKMA to establish the starting core address. Next, the Word Counter is loaded from the accumulator to set the length of the data block. The computer must be ready to accept data when instruction DKRD (Load disc address from accumulator and read) is issued since the transfer will now be under disc control.

A decode circuit detects coincidence between the address which was selected and a 4-bit Sector Counter which is incremented by disc Sector Mark (SM) timing pulses. A delay circuit prevents accessing an addressed sector at any position other than its entry point. Valid coincidence generates a Read Enable level, enabling the gate on the Preamble Sequence Read (PSR) flip-flop. At this time the read-write head is over the first word in the addressed sector, which is a preamble word containing all 1's. The next disc timing Word Mark (WM) sets PSR which allows C1's (bit timing clock pulses) to shift the first data word into the data Shift Register (SR). Concurrently, all data 1's are being shifted into the CS (Checksum) register.

The next WM ("anded" with C2 clock pulse) generates SR→DB which sends the data word in the SR into the DB (Data Buffer) register. At the same time, a DMA break request is output to the computer. As the next word from the disc is shifting into the SR, the DMA break is granted at which time the MC (Memory Counter) contents are read in to establish the core address, the data word is read into memory, and the MC and WC (Word Counter) are incremented. This process is repeated for the 112 data words (or less) within the sector.

A word sequence counter within the interface is cleared at the start of each sector and is incremented by the WM pulse. The 113th WM (last data word) sets a Chksum 1 flip-flop which allows the next WM to set Chksum Inhibit and halt shifting into the CS register. The following SM pulse initiates a checksum test and subsequently clears the CS register. If the checksum test fails, (i.e., the checksum read differs from that

generated in the CS register) the Chksum Error flip-flop is set. The SM pulse also clears several flip-flops and counters, enabling the sequence to begin anew for the following sector.

Write Sequence

Most of the initializing events in a write operation are identical with those described in the read sequence discussion. The one exception is the disc addressing instruction DKWR (Load disc address and write). This instruction also causes the first DMA break request to be issued, loading the DB with the first data word from memory. Sector coincidence occurs as previously described, but since the R/W flip-flop has been set by instruction DKWR, a Write Enable level conditions the PSW (Preamble Sequence Write) flip-flop. During the first word, PSW is in the reset state, causing all 1's to be written on the disc. The next WM (and C2) generates DB→SR, which transfers the data word from the DB to the SR, and subsequent C1 pulses shift the data in the SR out to the disc. Each time DB→SR occurs, a DMA break request is generated to bring new data into the DB. Concurrent to shifting data to the disc, each 1 bit is shifted into the Checksum register at C2 time.

As in the read sequence, WM 113 sets Chksum 1. The next WM sets Chksum Inhibit and C2 strobes the 4 bits from the Checksum register into the SR to be written as the checksum for the sector. Chksum 1 inhibits DB→SR and the subsequent DMA Break Request.

Termination of a block transfer begins as the WC overflows and sets WC Oflo. The next WM sets Oflo 2, which inhibits SR→DB and DMA Break Requests when reading. During a write operation, Oflo 2 gates off the data to the disc and causes 0's to be written for the remainder of the sector until a checksum word is written. WC Oflo "anded" with Chksum Inhibit also causes a Done flag to be raised during the final checksum interval.

Disc Instructions

Ten IOT instructions have been added to the PDP-9 instruction set for disc control. All instructions require four machine cycles (4 μ sec) for execution. A listing is included in Appendix F.

The two instructions which load the disc address, DKRD and DKWR, also select the use of the API facility for two disc interrupts, Illegal Address and Done. Bit 0 in the disc address word must be set to enable disc API functions. If bit 0 is not set, no API requests will result from *disc* inputs. However, API functions related to *other devices* are not affected. The disc utilizes API level 1, trap address 47₈.

A status test instruction DKRS reads disc status indicator bits into the accumulator in the same manner as the PDP-9 IORS instruction. The status bits indicate that disc API functions are enabled and error conditions as shown in Appendix G.

DISC REFERENCE DOCUMENTS

1. Service Manual for Magnetic Disc Memory System Model No. 14120,
Digital Development Corporation, San Diego, California, 1969.
2. PDP-9 User Handbook, Digital Equipment Corporation, Maynard,
Massachusetts, 1968.
3. Digital Logic Handbook, Digital Equipment Corporation, Maynard
Massachusetts, 1967, 1969.

GRAPHIC DIGITIZING SYSTEM

A coordinate digitizer consisting of a servo-follower table, cursor and related electronics affords the operator a capability to input graphic data identified on a two-dimensional coordinate matrix into the digital computer memory. A block diagram of the system is shown in Figure 9.

Coordinate Digitizer

The digitizing unit was manufactured by Edwin Industries Corporation and is designated Model PF-40. Its major components are a table, which provides the working area and houses a servo-positioning mechanism, and an electronics cabinet which includes the servo-drive electronics and system power supplies. Table IV lists the salient characteristics of the device.

A two-axis positioner driven by servo motors is located within a large adjustable (height and tilt) table which has a working area 36" by 48". An electronic cursor, which is positioned on the table surface, detects an alternating magnetic field. A four-coil sensor beneath the table surface creates an error signal when its X-Y position differs from that of the cursor. The resultant error signal causes the servo-mechanism to move the sensor to a position which nulls the error signal. Thus, the sensor position follows that of the manually positioned cursor.

Two 2-phase shaft encoders are directly driven by the servo-positioning motors to provide position data to the computer interface. The encoder gear ratio is designed to allow detection of a .004" linear movement. Encoder power is supplied by a power supply in the interface.

The only additional output from the digitizer is a switch closure which requests the interface to input coordinate data. Parallel switches are located in the cursor for hand operation and in a foot-operated switch. An additional 16-key keyboard will be interfaced to the system to provide identification and control data.

Digitizer/PDP-9 Interface

A computer interface provides X and Y coordinate buffers and digitize strobe interrupt logic. The interface block diagram is shown in Figure 10.

FIGURE 9. Digitizer Block Diagram

FIGURE 10 . Digitizer Interface Block Diagram

Two 14-bit up-down binary counters increment according to the output of the shaft encoders in the digitizer, with one bit representing a .004 inch lineal measurement. Indicator lamps allow visual examination of the buffer contents. Buffer data are individually read into the PDP-9 accumulator via normal program controlled IOT instructions (See Appendix H).

An interrupt flag is set when a digitize switch closure occurs, resulting in an API level 3 interrupt, assuming the API is enabled. The PDP-9 trap address for the interrupt is memory location 65₈.

Interface construction is of Digital Equipment Corp. R and W series modules.

TABLE IV. *Digitizer Specifications*

Working Area	36" x 48" Adjustable Height Adjustable Tilt
Resolution	0.004"
Static Positioning Accuracy	$\pm 0.004"$
Dynamic Positioning Accuracy	$\pm 0.004"$ @ 1" per sec. $\pm 0.008"$ @ 4" per sec.
Mechanism	Magnetic servo follower
Data Readout	2- $\emptyset$ encoders
Cursor	Cross wire angle view
Digitize Entry	Hand switch on cursor Foot switch

DIGITIZER REFERENCE DOCUMENTS

1. *Instruction Manual for the Edwin Industries Model PF-40 Graphic Coordinate Digitizer*, Edwin Industries Corporation, Silver Spring, Maryland, 1970.
2. *PDP-9 User Handbook*, Digital Equipment Corporation, Maynard, Massachusetts, 1968.
3. *Digital Logic Handbook*, Digital Equipment Corporation, Maynard, Massachusetts, 1967, 1969.

SOFTWARE

As noted throughout previous text, all IOT instructions which have developed for PDP-9 control of the various system devices are listed in following appendices.

A sophisticated multiprogram software system has been developed to provide multi-device (and thus, user) access to the central processor in a shared manner where feasible. A disc operating system affords the operator a virtual immediate access to system and user applications programs otherwise accessed via a paper tape system. Since this report is basically a functional description of the system hardware configuration, only allusion to system software is attempted. For detailed information regarding software development, refer to:

N. B. Smith, Unpublished Data, A Multiprogram Interactive Data Analysis Computer System, Battelle-Northwest, Richland, Washington, October 1970.

L. H. Gerhardstein, Unpublished Data, Disc Operating System, Battelle Northwest, Richland, Washington.

APPENDICES

ERASE TO END OF DISPL	ERASE TO END OF LINE	SOM ▽	' <	✧ >	{ [	}]	Δ □	TRANSMIT
-----------------------------	----------------------------	-------	--------	--------	--------	--------	--------	----------

IN DISP DELETE IN LINE	IN DISPL INSERT IN LINE	TAB	! 1	" 2	# 3	\$ 4	% 5	& 6	, 7	(8	) 9	0 _	=
------------------------------	-------------------------------	-----	--------	--------	--------	---------	--------	--------	--------	--------	--------	--------	---

CURSOR TO HOME	←	Q	W	E	R	T	Y	U	I	Ø	P	:
----------------------	---	---	---	---	---	---	---	---	---	---	---	---

↑
←
→
↓

CHAR ERASE	A	S	D	F	G	H	J	K	L	;	\ ≠
	Z	X	C	V	B	N	M	,	.	? /	RETN

→

FUNCTION
KEYBOARD →

α	β	1	2	3	≥	≤
γ	δ	4	5	6	÷/≡	Λ/∞
η/ε	λ	7	8	9	]	[
π	Σ/σ	+	-	⊗	d	→/←
x	Ω	0	.	÷	√	∫

DISPLAY CONSOLE KEYBOARD CONFIGURATION

APPENDIX A1

HWL-1525

APPENDIX A2

KEYBOARD CHARACTER AND FUNCTION CODES

40 CHAR ERASE	60 0	100 π	120 P	140 ☒	160 χ
41 !	61 1	101 A	121 Q	141 [	161 α
42 "	62 2	102 B	122 R	142 ≤	162 β
43 #	63 3	103 C	123 S	143 ≥	163 γ
44 \$	64 4	104 D	124 T	144 d	164 δ
45 %	65 5	105 E	125 U	145 Σ	165 σ
46 &	66 6	106 F	126 V	145 η	166 ε
47 ,	67 7	107 G	127 W	147 ↖	167 ≠
50 (	70 8	110 H	130 X	150 Λ	170 ~
51)	71 9	111 I	131 Y	151 →	171 ←
52 *	72 :	112 J	132 Z	152 Δ	172 ☐
53 +	73 ;	113 K	133 √	153 ☒	173 >
54 ,	74 ÷	114 L	134 SOM ∇	154 ¢	174 <
55 -	75 =	115 M	135 λ	155 }	175]
56 .	76]	116 N	136 Ω	156 —	176 ≡
57 /	77 ?	117 ∅	137 f	157 {	177 [

APPENDIX B
DISPLAY INSTRUCTIONS

MNEMONIC	CODE	OPERATION
DSLIF	700701	*Skip on no Light Pen flag
DSOF	700721	*Skip on no Overflow flag
DSCF	700741	*Skip on no Command flag
DSKF	700761	*Skip on no Keyboard flag
DSRD	700612	Read display input data into AC
DSIA	700604	Input Acknowledge
DSCI	700644	Clear interrupt flag
DSEI	700702	Enable display interrupts
DSDI	700722	Disable display interrupts
DSLBI	700704	Load display buffer from AC

**Interrupts on API Level 1, Trap Address 63*

APPENDIX C
DISC ADDRESS FORMAT

ADDRESS WORD

RECORDING SURFACE

DISC TIMING FORMAT

APPENDIX D

APPENDIX E

DISC SEQUENCE FLOW CHARTS

READ FLOW	E-2
WRITE FLOW	E-4
DATA READ FLOW	E-6
DATA WRITE FLOW	E-7
PREAMBLE READ FLOW	E-8
PREAMBLE WRITE FLOW	E-10
CHECKSUM READ FLOW	E-11
CHECKSUM WRITE FLOW	E-13
ADDRESS INITIALIZATION FLOW	E-14

READ FLOW

READ FLOW

WRITE FLOW

WRITE FLOW

DATA READ FLOW

DATA WRITE FLOW

PREAMBLE READ FLOW

PREAMBLE READ FLOW

PREAMBLE WRITE FLOW

CHECKSUM READ FLOW

CHECKSUM WRITE FLOW

ADDRESS INITIALIZATION FLOW

APPENDIX F
DISC INSTRUCTIONS

MNEMONIC	CODE	OPERATION
DKRF	707001	Skip if disc ready
DKEF	707021	Skip on no checksum error
DKIA	707041	*Skip on illegal address
DKDF	707061	*Skip if disc done
DKMA	707002	Load Memory Counter from AC
DKWC	707022	Load Word Counter from AC
DKRD	707042	(a)Load disc address from AC & read
DKWR	707062	(a)Load disc address from AC & write
DKCF	707004	Clear disc flags
DKRS	707132	Read disc status into AC

**Interrupts on API level 1, Trap Address 47*

(a)Also enables disc API

APPENDIX G

DISC STATUS WORD

Status test instruction DKRS loads the computer Accumulator with disc status bits as shown.

APPENDIX H

DIGITIZER INSTRUCTIONS

MNEMONIC	CODE	OPERATION
DZRX	707212	Read X position into AC
DZRY	707232	Read Y position into AC
DZCB	707204	Clear X & Y position buffers
DZCF	707224	*Clear input interrupt flag
DZDF	707201	Skip on digitize flag
DZKF	707241	Skip on keyboard flag
DZCKF	707244	Clear keyboard interrupt flag
DZCKB	707264	Clear keyboard buffer

**Interrupt on API level 3, Trap Address 65*

APPENDIX I

API CHANNEL ASSIGNMENTS

<u>DEVICE</u>	<u>PRIORITY LEVEL</u>	<u>TRAP ADDRESS</u>
Software	4	40
Software	5	41
Software	6	42
Software	7	43
DECtape	1	44
Disc	1	47
Paper Tape Rdr.	2	50
Real Time Clock	3	51
Display	1	63
Digitizer	3	65

APPENDIX J

DISPLAY LOGIC DRAWINGS

- 0 Module Locator
- 1 Display Flags & Interrupts
- 2 Display Output I/O
- 3 Display Input I/O
- 4 Display Output Data
- 5 Display Output Data Buffer
- 6 Display I/O Bus
- 7 Display Interface Cables 1
- 8 Display Interface Cables 2

	A	B	C
40	LINE RCVR		
39	LINE RCVR		
38	CON002A (DISC)	CON002A (IO BUS)	
37	PGA400B	PGA400B	
36	ONE SHOT	PGA400B	
35	FFL001A	GAT200A	
34	FFL001A	GAT200A	CON002A (IO TO CP)
33	GAT200A	GAT200A	LCV001A
32	GAT200A	FFL001A	LCV001A
31		FFL001A	LCV001A
30		FFL001A	LCV001A
29	MGA500A	FFL001A	MGA500A
28	PGA400B	LCV001A	LINE RCVR
27	ONE SHOT	LCV001A	LINE RCVR
26	ONE SHOT	CON002A (DMA ADDR)	LINE RCVR
25	ONE SHOT	LCV001A	LINE RCVR
24	GAT200A		LINE RCVR
23	FFL001A	CON002A (DMA DATA)	LINE RCVR
22	FFL001A	LCV001A	CON002A (DISPLAY)
21	FFL001A	LCV001A	CON002A (DISPLAY)
20	MGA500A	LCV001A	ONE SHOT
19	GAT200A	FFL001A	PGA400B
18	GAT200A	FFL001A	PGA400B
17		GAT200A	PGA400B
16		GAT200A	FFL001A
15		FFL001A	FFL001A
14		FFL001A	GAT200A
13		GAT200A	GAT200A
12		GAT200A	GAT200A
11		GAT200A	CON002A (IO OUT)
10		PULL UP R ₁₂	CON002A (AM DATA)
9		PGA400B	
8			
7			
6			
5			
4			
3			
2			
1			

	D	E	F	H
32				
31				
30				
29				
28				
27				
26				
25		R107		
24		R205	W109	
23		R111	W109	
22		R001	W109	
21		R001	W109	
20		R111		
19		R111		
18	CONN (DISC IOTW)	R111	W104	
17	CONN (DISC FLG'A)	R111	W104	
16	CONN (DISPLAY FLG'A)	W603	W104	
15	CONN (DISPLAY IOTW)	R202	R107	
14		R202	R107	R107
13	CONN (DMA CHI ADR)	R123	R111	R107
12	CONN (DMA CHI ADR)	R123	R111	R111
11	CONN (DISPLAY ID)	R123	R001	R111
10	CONN (DISPLAY ID)	R123	R111	R107
9	CONN (IO TO DISC)		R111	R111
8	CONN (IO TO DISC)	W603	R111	
7	CONN (IO TO DISPLAY)	W603	W107	
6	CONN (IO TO DISPLAY)	W603	W107	W107
5	CONN (AM DATA)	W603	IO BUS	IO BUS
4	CONN (AM DATA)	W603		
3		W603		
2		W005		
1	CONN (DATA CHI CONT.)	W010		
	CONN (DMA CHI CONT.)			
	CONN (AM DATA)			
	CONN (AM DATA)			

CLASSIFICATION
<i>None</i>
BY <i>SE Driver 10/15/70</i>

BATTELLE BATTELLE MEMORIAL INSTITUTE P. O. BOX 999, RICHLAND, WASHINGTON 99352 / TELEPHONE 509-942-1111		B	NORTHWEST PACIFIC NORTHWEST LABORATORY
ENGINEER	<i>BURRIS</i>		DATE <i>10/17/70</i>
TITLE	<i>MODULE LOCATOR</i> <i>DISC / DISPLAY</i>		
			SHEET <i>0</i>

REV. NO.		REV. BY DATE		DRAWING STATUS		APPD. BY DATE		FOR		MICRO F.W.D.	
DFTG APPD		DATE		APPD		DATE					
CHECKED				APPD							
DRAWN				ENGR		BUSINESS		4/15/70			
BLDG NO.				INDEX NO.							
SCALE		CLASSIFIED BY		CLASSIFICATION							
		DATE 10/15/70		DATE							
DWG. NO.										SHEET NO.	
										2	
DRAWING TITLE OR INDEX NO.										SHEETS	
U.S. ATOMIC ENERGY COMMISSION RICHLAND OPERATIONS OFFICE										8	
PACIFIC NORTHWEST LABORATORY OPERATED BY BATTTELLE MEMORIAL INSTITUTE											
DISPLAY OUTPUT I/O POP-9/DISPLAY											

INPUT DATA BIT

*** NOTE 1**

**** NOTE 2**

C21 C22 C29 C33 D13 (FA)

17 4 10 7 C22 12 11 C29 5 4 D IDB

16 6 26 25 C22 28 15 C29 9 6 E 1

15 8 46 41 C22 48 21 C29 31 8 H 2 DIA

14 10 62 59 C22 64 25 C29 33 10 K K

13 12 10 7 C23 12 45 C29 39 12 M M

12 14 26 25 C23 28 49 C29 41 14 P P

11 16 46 41 C23 48 57 C29 63 16 S S

10 18 62 59 C23 64 53 C29 67 18 T T

9 20 10 7 C24 12 11 C30 5 20 V V

8 30 26 25 C24 28 15 C30 9 30 D14 D15 D D

7 32 46 41 C24 48 21 C30 31 32 E E

6 34 62 59 C24 64 25 C30 33 34 H H

5 36 10 7 C25 12 45 C30 39 36 K K

4 38 26 25 C25 28 49 C30 41 38 M M

3 40 46 41 C25 48 57 C30 63 40 P P

2 42 62 59 C25 64 53 C30 67 42 S S

1 44 10 7 C26 12 11 C31 5 44 T T

0 46 26 25 C26 28 15 C31 9 46 V V

* NOTE 1 ON ALL LINE RCVR'S WIRE PINS 3, 21, 37, 53 TO PIN 14.
WIRE PINS 19, 35, 51, 69 TO PIN 6 (+10V).
WIRE PINS 13, 31, 47, 65 TO +5V.

** NOTE 2 ON ALL LEVEL CONVERTERS WIRE PINS 17, 55 TO -15V.

						DWG NO.	REV NO.	DRAWING TITLE OR INDEX NO.	
						REFERENCE DRAWINGS			
REV. NO.						U.S. ATOMIC ENERGY COMMISSION RICHLAND OPERATIONS OFFICE			
REV. BY DATE						PACIFIC NORTHWEST LABORATORY OPERATED BY BATTELLE MEMORIAL INSTITUTE			
DRAWING STATUS						DISPLAY I/O INPUT			
APPD. BY DATE FOR MICR F M D						- PDP-9/DISPLAY			
DFTG APPD									
DATE									
CHECKED									
DRAWN									
BLDG NO.									
SCALE									
CLASSIFIED BY									
DATE									
CLASSIFICATION									
SHEET NO.						SHEET			
3						8

	F3	F
IO RUN	D	D
DATA OFLO	E	E
IO OFLO	H	H
IO ADR 3	K	K
4	M	M
5	P	P
6	S	S
7	T	T
8	V	V

[illegible]

INTERFACE TO DISPLAY

FROM	TO	FUNCTION
C20	A3 P1	
46	A	2 ⁰ OUTPUT DATA
42	B	2 ¹
42	C	2 ²
40	D	2 ³
38	K	2 ⁴
36	L	2 ⁵
34	M	2 ⁶
32	N	2 ⁷
30	U	2 ⁸
20	V	2 ⁹
18	W	2 ¹⁰
16	X	2 ¹¹
14	Y	2 ¹²
12	Z	2 ¹³
10	F	2 ¹⁴
8	G	2 ¹⁵
6	M	2 ¹⁶
4	N	2 ¹⁷

FROM	TO	FUNCTION
C20	A3 P1	
54	BT	INPUT ACKNOWLEDGE
56	CK	OUTPUT ACKNOWLEDGE
58	BJ	EXTERNAL FUNCTION ACK
60	CA	CLR

INTERFACE TO DMA

FROM	TO	FUNCTION
D15	DMA C7	
K	K	CH1 ADDR 3
M	M	4
P	P	5
S	S	6
T	T	7
V	V	8

DISPLAY TO INTERFACE

FROM	TO	FUNCTION
A3 P1	C21	
P	46	0 INPUT DATA
Q	44	1
U	42	2
W	40	3
X	38	4
Y	36	5
AD	34	6
AE	32	7
AF	30	8
AH	20	9
AN	18	10
AP	16	11
AR	14	12
AS	12	13
AZ	10	14
BA	8	15
AX	6	16
AY	4	17

FROM	TO	FUNCTION
A3 P1	C21	
BU	58	INPUT DATA RQ
BH	54	OUTPUT DATA RQ
CJ	60	EXTERNAL INTERRUPT
CL	56	SUBROUTINE EXIT

INTERFACE TO DMA

FROM	TO	FUNCTION
D16	DMA C8	
D	D	CH1 ADDR 9
E	E	10
H	H	11
K	K	12
M	M	13
P	P	14
S	S	15
T	T	16
V	V	17

INTRA-INTERFACE

FROM	TO	FUNCTION
C33	D19	
54	D	OUTPUT DATA RQ
56	E	SUBROUTINE EXIT
58	H	INPUT DATA RQ
60	K	EXTERNAL INTERRUPT
62	M	LIGHT PEN FLAG
64	P	OVERFLOW FLAG
66	S	COMMAND FLAG
68	T	KEYBOARD FLAG
70	V	-15 V
D18	C10	
D	54	CH1 DATA READY
E	56	IOT 0704
H	58	IOT 0604
T	68	+10 V.
V	70	+5 V.
K	60	CLR

DMA TO INTERFACE

FROM	TO	FUNCTION
DMA DB	D4	
H	H	CH1 BK RQ
K	K	RQ IN
M	M	ADDR ACC
P	P	DATA ACC
S	S	DATA RQ
T	T	FAST RQ
V	V	FAST CLR

REV. NO.		REV. DATE		DRAWING STATUS		APPD. BY DATE		FOR DATE		MICRO F.M.D.									
DFTG APPD		DATE		APPD		DATE													
CHECKED				APPD															
DRAWN				ENGR		BUSINESS		10/15/70											
BLDG NO.				INDEX NO.															
SCALE		CLASSIFIED BY		CLASSIFICATION															
		AEC/Min		NONE															
		DATE 10/13/70																	
DWG NO.										REV. NO.									
DWG NO.										DRAWING TITLE OR INDEX NO.									
DWG NO.										REFERENCE DRAWINGS									
DWG NO.										U.S. ATOMIC ENERGY COMMISSION									
DWG NO.										RICHLAND OPERATIONS OFFICE									
DWG NO.										PACIFIC NORTHWEST LABORATORY									
DWG NO.										OPERATED BY BATTELLE MEMORIAL INSTITUTE									
DWG NO.										DISPLAY INTERFACE CABLES									
DWG NO.										PDP-9/ DISPLAY									
DWG NO.										SHEET NO.									
DWG NO.										SHEETS									
DWG NO.										7 8									

INTRA-INTERFACE

FROM	TO	FUNCTION
C33	D13	
4	D	IDB INPUT DATA
6	E	1
8	H	2
10	K	3
12	M	4
14	P	5
16	S	6
18	T	7
20	V	8
	<u>D14</u>	
30	D	9
32	E	10
34	H	11
36	K	12
38	M	13
40	P	14
42	S	15
44	T	16
46	V	17

INTRA-INTERFACE

FROM	TO	FUNCTION
D7	C9	
D	4	Ø BIT AM DATA
E	6	1
H	8	2
K	10	3
M	12	4
P	14	5
S	16	6
T	18	7
V	20	8
	<u>D8</u>	
D	30	9
E	32	10
H	34	11
K	36	12
M	38	13
P	40	14
S	42	15
T	44	16
V	46	17

INTRA-INTERFACE

FROM	TO	FUNCTION
D9	C10	
D	4	IDB
E	6	1
H	8	2
K	10	3
M	12	4
P	14	5
S	16	6
T	18	7
V	20	8
	<u>D10</u>	
D	30	9
E	32	10
H	34	11
K	36	12
M	38	13
P	40	14
S	42	15
T	44	16
V	46	17

INTERFACE TO DMA

FROM	TO	FUNCTION
DMA D2	D1	
D	D	AM Ø
E	E	AM1
H	H	AM2
K	K	AM3
M	M	AM4
P	P	AM5
S	S	AM6
T	T	AM7
V	V	AM8

INTERFACE TO DMA

FROM	TO	FUNCTION
DMA D3	D2	
D	D	AM9
E	E	AM10
H	H	AM11
K	K	AM12
M	M	AM13
P	P	AM14
S	S	AM15
T	T	AM16
V	V	AM17

REV. NO.		REV. BY		DATE		DRAWING STATUS		APPD. BY		DATE		FOR		MICROC F.M.D	
DFTG APPD		DATE		APPD		DATE		CHECKED		APPD		DRAWN		ENGR	
BLDG NO.		INDEX NO.		SCALE		LOCATION		DATE		DWG NO.		SHEET NO.		SHEETS	
10/15/70		NONE		10/15/70		NONE		10/15/70		10/15/70		8		8	

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DISPLAY INTERFACE CABLES
PDP-9/ DISPLAY

APPENDIX K

DISC LOGIC DRAWINGS

0	Module Locator
1	Disc I/O - Flags & IOT's
2	Disc I/O - Interrupts
3	Disc I/O - I/O Data & Disc Input
4	Disc I/O - Data to DMA
5	Disc I/O - Flags & DMA Address
6	Control & Timing
7	Preamble Sequence - Word Sequence
8	Disc Address Decode
9	Memory Address Counter
10	Word Count Register
11	Checksum Generator/Decode
12	Data Buffer & Parallel/Serial Converter
13	Disc Cables

	A	B	C
40			
39	LINE RCVR		
38	LINE RCVR		
37	CON002A (DISC)	CON002A (IO BUS)	
36	PGA400B	PGA400B	
35	ONE SHOT	PGA400B	
34	FFL001A	GAT200A	
33	FFL001A	GAT200A	CON002A (IO TO CP)
32	GAT200A	GAT200A	LCV001A
31	GAT200A	FFL001A	LCV001A
30		FFL001A	LCV001A
29		FFL001A	LCV001A
28	MGAS00A	FFL001A	MGAS00A
27	PGA400B	LCV001A	LINE RCVR
26	ONE SHOT	LCV001A	LINE RCVR
25	ONE SHOT	CON002A (DMA ADR)	LINE RCVR
24	ONE SHOT	LCV001A	LINE RCVR
23	GAT200A		LINE RCVR
22	FFL001A	CON002A (DMA DATA)	LINE RCVR
21	FFL001A	LCV001A	CON002A (DISPLAY)
20	FFL001A	LCV001A	CON002A (DISPLAY)
19	MGAS00A	LCV001A	ONE SHOT
18	GAT200A	FFL001A	PGA400B
17	GAT200A	FFL001A	PGA400B
16		GAT200A	PGA400B
15		GAT200A	FFL001A
14		FFL001A	FFL001A
13		FFL001A	GAT200A
12		GAT200A	GAT200A
11		GAT200A	GAT200A
10		GAT200A	CON002A (IO OUT)
9		PULL UP R'L	CON002A (AM DATA)
8		PGA400B	
7			
6			
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4			
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1			

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CLASSIFICATION
None
BY SE Driver 10/15/70

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TITLE <i>MODULE LOCATOR</i>			
<i>DISC/DISPLAY</i>		<i>SHEET 0</i>

NOTE: A3B, A39 — CONNECT PINS 3, 21, 37, 53, 14.

" " 19, 35, 51, 69, 6.

" " 4, 20, 36, 56, 2.

" " 70 TO -15V.; 6 TO +10V.; 13, 31, 47, 65 TO +5V.

REV. NO.		REV. BY	DATE	DRAWING STATUS	APPD. BY	DATE	FOR	MICRO F.M.D.
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DISC I/O		
I/O BUS & DISC INPUT		
PDP-9/DISC INTERFACE		
DWG NO.	SHEET NO.	SHEETS
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		AE Ornel		NONE	
		DATE 10/13/70			
DWG NO.		SHEET NO.		SHEETS	
		4		13	

Disc I/O
DATA TO DMA
PDP-9/DNC INTERFACE

CHØ ADDR BIT 3

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		FLAGS & DMA ADDRESS
		POP-9/DISC INTERFACE
DWG NO.	SHEET NO.	SHEETS
	5	13

NOTES: SIGNAL SOURCE
 WC OFLO(1) B2B-33
 CS INH(1) A21-3
 PWR CLR A27-59

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				CONTROL & TIMING				
				PDP-9/DISC INTERFACE				
DWG NO.		SHEET NO.		SHEETS				
		6		13

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TITLE <i>MEMORY ADDRESS COUNTER (MC)</i>	
<i>POP-9/DISC INTERFACE SHEET 9</i>

REV. NO.		REV. DATE		DRAWING STATUS		APPD. BY		FOR		MICRO	
DFTG APPD		DATE		APPD		DATE		DATE		DATE	
CHECKED		DATE		APPD		DATE		DATE		DATE	
DRAWN		DATE		ENGR		DATE		DATE		DATE	
BLDG NO.		DATE		INDEX NO.		DATE		DATE		DATE	
SCALE		CLASSIFIED BY		CLASSIFICATION		DATE		DATE		DATE	
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WORD COUNT REGISTER (WC)											
PDP-9/DISC INTERFACE											
DWG NO.										SHEET NO.	
NO.										10	
										13

FROM TO FUNCTION

BZZ	DMA C1	CN # DATA
4	D	1
6	E	1
8	H	2
10	K	3
12	M	4
14	P	5
16	S	6
18	T	7
20	V	8

B22	DNA C2	CHG DATA
30	D	9
32	E	10
34	H	11
36	K	12
38	M	13
40	P	14
42	S	15
44	T	16
46	V	17

DATA D4	D3	DATA CONTROL
H	H	CH $\rightarrow$ BK RQ
K	K	RQ IN
M	M	ADDR ACC
P	P	DATA ACC
S	S	DATA RQ
T	T	FAST RQ
V	V	FAST CLR

FROM TO FUNCTION

B25	DMA C3	CHG ADDR
10	K	3
12	M	4
14	P	5
16	S	6
18	T	7
20	V	8

B25	DNA C4	C48 ADDR
30	D	9
32	E	10
34	H	11
36	K	12
38	M	13
40	P	14
42	S	15
44	T	16
46	V	17

From	To	FUNCTION
------	----	----------

DISC 570	A37	
P	4	DATA IN
E	6	ORIGIN P.
W	8	SECTOR P
Y	10	WORD P
A	12	CLOCK 1
C	14	CLOCK 2
DD	16	PERM. ADDR.
FF	18	DISC EBY
M	30	DATA OUT
H	32	WRITE EN
a	54	ADDR 0
c	56	1
e	58	2
A	60	3
R	62	4
n	64	5
r	66	6
t	68	7

<u>FROM</u>	<u>TO</u>	<u>FUNCTION</u>
-------------	-----------	-----------------

B37	D11	IO DATA
4	D	0
6	E	1
8	H	2
10	K	3
12	M	4
14	P	5
16	S	6
18	T	7
20	V	8

B37	D12	IO DATA
30	D	9
32	E	10
34	H	11
36	K	12
38	M	13
40	P	14
42	S	15
44	T	16
46	V	17

FROM	TO	FUNCTION
------	----	----------

B37	D21	
54	D	LOAD MC
56	E	LOAD WC
58	H	READ
60	K	WRITE
62	M	CLEAR
64	P	"
66	S	"
68	T	PWR CLR
70	V	-15 V.

B25	D20	
54	D	CHG DATA RDY
56	E	DATA ACK
58	H	BK RQ
60	K	CHECKSUM ERROR
62	M	DONE FLAG
64	P	ILLEGAL ADDR
66	S	DISC RDY
68	T	RQ IN
70	V	ERROR

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SCALE		CLASSIFIED BY <i>Hedinger</i>		CLASSIFICATION <i>NONE</i>					
		DATE <i>10/15/70</i>							
						DWG NO.	SHEET NO. SHEET		
							<i>13 13</i>		

APPENDIX L

DIGITIZER LOGIC DRAWINGS

- 0 Module Locator
- 1 IO Control
- 2 Position Register
- 3 Indicator Drivers
- 4 I/O Bus

[illegible]

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TITLE <i>MODULE LOCATOR</i> <i>DIGITIZER 1DDP-9</i>	

CLASSIFICATION	NONE
BY	SE Driver 10/15/70

REV. NO.	REV. BY	DRAWING STATUS	APPD. BY	FOR	MICRO F.M.D.																														
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API 3 EN OUT

NOTE: ON ALL CONNECTORS PINS F, J, L, N, R, U ARE GROUND.

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