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AN EIGHT INPUT ADAPTER FOR A CN-1024/211
TIME OF FLIGHT ANALYZER

MASTER

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PHILLIPS
PETROLEUM
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NATIONAL REACTOR TESTING STATION
US ATOMIC ENERGY COMMISSION

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Instrument Development Branch

PHILLIPS
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COMPANY

Atomic Energy Division

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An Eight Input Adapter For a CN-1024/211
Time of Flight Analyzer

R. I. Little and E. P. Elkins

ABSTRACT

A Technical Measurement Corporation Model CN-1024/211 time of flight analyzer was modified for instantaneous external memory control and external variable initial delay using the internal clock source. An external system was designed and constructed. This unit allows splitting the 1024 channel memory into 1, 2, 4 or 8 sections for use with a like number of separate inputs, in addition to some other interesting possibilities. It also contains an initial delay circuit which uses the analyzer's clock for generating up to 65,504 channels of delay in increments of 32 channels. The external circuitry is also applicable to most other analyzer plug-ins and to the older CN-110 analyzer.

An Eight Input Adapter For a CN-1024/211 Time of Flight Analyzer

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An Eight Input Adapter For A CN-1024/211
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1.0 INTRODUCTION

The concept of multichannel time of flight analyzers with multiple grouping in storage, while not particularly new¹ is usually not something incorporated on shelf items because of the tremendous number of practical possibilities which, if included, would make the cost prohibitive.

The more simple setup includes only a single detector and a sample changer, so that for each sample condition a different section of the memory is employed. At lower accumulating rates, this technique might be quite wasteful of time, especially if it is possible to employ a group of detectors, one for each sample condition. Furthermore, by compiling statistical data on all conditions simultaneously the physicist employs the same general input spectrum for all. Indeed, one memory portion is often reserved just to record this spectrum. The number of inputs becomes a function of the experiment and memory limitations in the analyzer. Where the delay generator can provide adequate resolution it is practical to break up a 1024 channel memory into eight sections (octants) of 128 channels each. Under such conditions it would be advantageous to have at least 50 per cent resolution capabilities in delay (64 channel increments) and 25 per cent resolution (32 channel increments) would be desirable.

In solving the problems associated with the design, one first considers the present equipment and its deficiencies, then decides what is possible and practical. Experience, of course, plays an important part in establishing a design philosophy and the objectives. One must then outline the specific changes in the analyzer and create the external equipment. Where prior knowledge indicates that a number of others wish to duplicate the work, step-by-step procedures and parts lists should be included.

2.0 MODIFICATION OF THE CN-1024

2.1 The CN-1024 Before Modification

A Technical Measurement Corporation Model CN-110 analyzer with a Model 211 time of flight plug-in had been used experimentally for pulse routing (up to four inputs) for several years by the Nuclear Physics Branch of Phillips Petroleum Company's Atomic Energy Division at MTR. This provided the groundwork for modification to two CN-1024's, for it was during this period that deficiencies in the system became apparent.

Routing is, in general, accomplished by controlling the N most significant bits of the memory address in a binary system, where 2^N is the desired number of inputs. The CN-110 and its big brother, the CN-1024², can be used for this purpose, with up to four inputs without modification, but only with the following restrictions:

1. The internal delay generator must not be used.
2. Only one group may be used for storage following any given system trigger.

If the physicist can abide by these restrictions, several extremely simple black boxes can be constructed which will provide satisfactory performance without analyzer modification.

In either of these analyzers, the delay generator CARRIES allow superfluous setting of the two most significant address flip-flops into all possible states and the external routing signals only provide SET control, no RESET. Thus, one would find that following a system trigger, practically all his inputs would be stored in the fourth quadrant because as soon as both of the two most significant flip-flops had been set, there would be nothing short of overflow to reset them. Providing a reset only complicates matters by generating superfluous CARRIES, thus creating race problems and an overflow (sometimes) which terminates storage until another system trigger is received.

2.2 The Modification Philosophy

2.2.1 Routing

Considering these rather severe limitations, and all the possible complications which might result from analyzer redesign in the indicated direction, a completely different approach seemed indicated. A number of approaches were evaluated, and after considerable study, one possibility, that of making the memory read from external flip-flops (instead of the three most significant bits of its own address register), led to an even more attractive possibility, that of directly driving or steering, the collectors of those three bits of the address from three mutually exclusive gate pairs as shown basically in Figure 1.

2.2.2 External Delay

Any external delay circuit, in order to provide a substantial improvement, should provide resolution in the order of 25-50 per cent of the minimum number of active time channels, and considerably extend the range. In consideration of the fact that the use of eight inputs was practical, wherein 128 time channels would be available (in each group), resolution of 32 channels would be adequate. Then, because higher order flip-flops in the memory address might become set during initial delay, it must be possible to assure that these, and all other, flip-flops in the address are reset upon the initiation of active timing.

Figure 1
The Basic Steering Circuit
Used for Pulse Routing

2.3 Objectives

Modification of the analyzer was to have accomplished the following objectives:

2.3.1 Operate in a normal manner at all switch settings except those applicable to external use.

2.3.2 Allow complete external control of the three most significant address register flip-flops so that the memory could be divided, externally, into 1, 2, 4 or 8 portions of 102^4 , 512, 256 or 128 channels respectively.

2.3.3 Allow external control of the initial delay period with a resolution of 32 channels, using the internal clock, to 65,504 channels.

2.3.4 Allow readout (display or punchout) of all 102^4 channels regardless of switch settings either on the external package or the analyzer.

2.3.5 Be completely free of the deficiencies discussed in Section 2.1.

2.4 External Equipment Signal Requirements

The following analyzer signals were required by the external equipment in order to accomplish these objectives:

2.4.1 Read-Write Gate

The system trigger initiates this gate when accumulating; it is terminated at the end of the active time. This signal is brought through a complementary emitter follower; it establishes a count mode and conditions the external equipment for external delay, if used.

2.4.2 End of Write Pulse

This pulse follows each read-add one-write sequence. This signal is brought through a complementary emitter follower. An input signal from the external equipment initiates the read-add one-write sequence; the adapter must then gate itself off to prevent spurious changes during the sequence, after which the End of Write pulse terminates, or resets this gate.

2.4.3 External Route

Position nine of the MEMORY LOCATION switch provides this level. This switch position, previously labeled EXT/2, is now called EXT ROUTE. The external equipment must then contain logic to determine whether the analyzer operates as 1, 2, 4 or 8 groups.

2.4.4 External Route and Delay

Position ten of the MEMORY LOCATION switch provides this signal. This switch position, previously labeled EXT/4, is now called EXT ROUTE and DELAY. Routing is identical to EXT ROUTE (2.4.3), and delay is accomplished externally by counting the carry pulses of the 2^4 carry while holding $2^5 - 2^9$ in the address inactive.

2.4.5 2^4 Carry

The set side of the 2^4 address FF provides this signal through a complementary emitter-follower. It drives the external initial delay scaler which then counts in 32 channel increments.

2.5 Internal Changes

In order to provide the required external signals and make the analyzer "system compatible", the following modifications were required. Figure 2 shows the modifications schematically and Appendix 1 provides a simplified step-by-step procedure and parts list.

Figure 2 - CN-1024 Modifications

2.5.1. External Connector

The external connector was changed out to one of larger capacity.

2.5.2 Emitter Follower Card

A card containing the required three complementary emitter followers (2.4.1, 2.4.2, 2.4.5) was constructed and wired into a blank connector in the analyzer.

2.5.3 Two wires from positions nine and ten of the MEMORY LOCATION switch, previously used for overflow control on card 12, were disconnected and fed to the external connector. Paragraphs 2.4.3 and 2.4.4 and 2.5.4 elaborate further.

2.5.4 2⁶ Overflow

A 2⁶ overflow pedestal gate was constructed on a small terminal board which was mounted to the side wall of the chassis near card 12. Lead lengths had to be short between the gate and card 12. It was later discovered that this gate could have been constructed on card 12, using pins J and K, one for the 2⁶ carry signal and the other for

the gate level, which is derived from the external connector. The previous functions of the MEMORY LOCATION switch outputs to pins J and K originally activated the proper overflow carries 2^7 and 2^8 , corresponding to EXT/4 and EXT/2 positions. Since the external package provides selection even greater (effectively EXT/1, EXT/2, EXT/4 and EXT/8), in addition to many possible subsets or permutations, it now takes over these functions by controlling all pedestal gates (2.5.5) when under external control.

2.5.5 Overflow Gate Control Levels

The external connector supplies four pedestal gate levels, 2^6 , 2^7 , 2^8 and 2^9 . The latter three, normally derived from the MEMORY LOCATION switch during internal operation, are essentially floating (internally) during external operation. The external equipment provides drive to all four lines during external operation (only one at a time), 2^6 directly to the newly added pedestal gate, 2^7 - 2^9 in parallel with the MEMORY LOCATION switch.

2.5.6 Address Reset After Delay

The external connector supplies a signal called External Delay which, when grounded, holds the 2^5 address register flip-flop reset, thus preventing 2^4 carries from being counted internally during the external initial delay interval. 2^0 - 2^4 are always reset when the external delay scaler reaches its preset count because this count comes as a result of a 2^4 carry. 2^5 - 2^9 are always reset prior to the system trigger, and External Delay, by holding 2^5 reset, assures that the entire address register starts from reset when the active time scan starts. The diode in this signal line, in the backwiring directly at the 2^5 collector, provides capacitance isolation so that the 2^5 carry operates with minimum loading when External Delay is negative.

2.5.7 Routing and the Address Register

The external connector provides six steering signals, one to each collector of the 2^7 , 2^8 , 2^9 address register flip-flops. A mutually exclusive gate pair in the external equipment drives each flip-flop, overriding all internal carries by holding the appropriate collectors grounded for a substantial portion of the read-add one-write sequence. This forces the externally determined states on the flip-flops so that their complementary sides go negative of their own accord. Diodes, mounted directly on the card connectors in the backwiring, provide capacitance isolation and allow use of different voltage swings or a different logic series in the external package. When control of a particular flip-flop is not required by the external equipment, i.e., 2^7 is not controlled except in EXT/8, then the external control gate pair both rest negative and the diodes both disconnect; this frees the flip-flop to operate in a normal manner. In order to effect this modification it was necessary to remove some of the collector isolation resistors from the original cards and mount them on the connectors in the backwiring in order to obtain direct access to the flip-flop collectors.

2.6 Cabling to the External Equipment

It will be noted that for all analyzer modifications consideration has been given to the problems associated with cable capacitance by use of complementary emitter followers for outgoing signals and isolating diodes on incoming signals where original circuitry switching times might be critical. The external equipment constructed by the Instrument Development Branch employs approximately four feet of interconnecting cable with some wires independently shielded, the shields grounded in accordance with good engineering principles. Probably over ten feet of cable would not impair performance. It should be pointed out, however, that the design of circuitry in the external equipment should give consideration to this factor.

2.7 Detailed Procedure and Parts List

The number of inquiries into previous work done by the Instrument Development Branch in this area indicates that a detailed procedure of the modification might prove useful. Appendix I lists the parts required and a procedure which evolved during the modification of one CN-110 and two CN-1024's. While the procedure only specifically applies to CN-1024's, it may be adapted to the CN-110 by appropriate pin changes and by replacing the Overflow Trigger card (in some cases) with a later one, as used in the CN-1024.

2.8 Operation with Other Plug-Ins

Although the modified analyzers operate primarily with the 211 time-of-flight plug-ins, they perform satisfactorily with 210 plug-ins under internal control. As far as can be determined, the modification should not affect internal operation with any other plug-in currently available. While intended specifically for use with the 211 plug-in, and no attention was paid to its use with other plug-ins during its design, the adapter probably could be employed with other plug-ins.

3.0 DESIGN OF THE EIGHT INPUT ADAPTER

3.1 Selection of Logic Type

Although the selection of a logic type and manufacturer is painfully subjective and somewhat arbitrary, the following factors were considered:

1. Adaptability to the job at hand.
2. Compatibility with Instrument Development fabrication techniques, particularly the use of solderless backwiring.

3. Reliability.
4. Economy.
5. Engineering familiarity. This might be considered in the same breath with all of the above.
6. Spare parts availability.

Diode-transistor NAND logic and pedestal gate circuitry most nearly met the criteria. In balancing cost against speed, it was decided that a nominal 1 MC logic³ could perform the job, although both 200 KC and 5 MC logic can be used in the system interchangeably. Figure 3 shows a functional block diagram of the adapter.

3.2 Interfacing

3.2.1 Inputs

Previous experience in interfacing the A-1 PHS outputs led to a good deal of caution in this area. Inputs from widely spaced amplifiers arrive at insulated BNC connectors from whence they travel on twisted pairs to 3:1 stepdown, non-inverting, terminated pulse transformers (Figures 4 and 5). The secondaries, acting as DC restorers, feed the resultant 15 volt negative pulses through a relay module (103) to NAND gates whose diodes disconnect at -6 volts. The NAND elements not only sharpen the leading edges of the pulses (by amplification and inversion), they provide facility for gating off subsequent pulses while one is being processed by the analyzer. This interface reduces common mode problems and provides excellent signal-to-noise ratio. Where it is desirable to close off the inputs fast without creating race problems in subsequent circuitry, it is necessary that each input trigger its own standard logic pulse so each gate must be followed by its own monostable multivibrator (DM). Flip-flops could also be used.

3.2.2 Outputs

The outputs of the Address Control Gates (Figure 4) which feed the steering diodes in the modified CN-1024 need no interfacing. The diode cathodes tied to the address register flip-flop collectors swing between common and -3 volts; the Address Control Gates (tied to the anodes), by swinging between common and -6 volts (or resting at -6 volts for extended periods), accomplish two desirable effects:

Figure 3
Eight Input Adapter
Block Diagram

Figure 4
Signal Input and Address Modification Logic

1. They provide fast positive transitions and the diode minority carriers and capacity aid in the negative transitions.
2. When static at -6 volts, the minimum of 3 volts diode bias tends to reduce diode capacitance so that the analyzer can work in a normal manner when desired.

Figure 5
Input Signal Isolation Module

3.3 Routing

3.3.1 General

On Figure 4, a monostable multivibrator pulse, when it occurs, sets its code into the Address Flip-Flops, gates the resultant code into the analyzer (through the Signal Input Gate) and, on Figure 5, resets the Store Flip-Flop which in turn gates off subsequent pulses. After the analyzer has processed the pulse it sends back an End of Write pulse which sets the Store Flip-Flop, again enabling the adapter. The logic is so arranged that the input gates open only after a System Trigger (and attendant initial delay, if used), and then only if the analyzer is supposed to be accumulating data (Signal Gate). These gates close immediately after the last active time channel. Since the outputs only follow an input and only last long enough to establish non-ambiguity in the analyzer's 2^7 , 2^8 and 2^9 address flip-flops, the adapter never interferes with display or readout modes in the analyzer.

Figure 6
Control Logic

3.3.2 Manual Routing

If the Jumper Module of Figure 4 contains straight through connections as in Figure 7, the unit functions as a 1, 2, 4 or 8 input adapter, depending on the position of its MEMORY DIVISION switch. However, when the Relay Module of Figure 8 replaces the Jumper Module and the shorting connector P12 is installed, considerably more flexibility can be attained. Figure 9 reveals how this is accomplished. S2 and S3 may be considered as one 3-pole, 17 position switch since when they are used one or the other must always be in the OFF position. S2 selects one octant to which the pulses received at J1 will be routed. Thus for different time intervals or different sample conditions the operator may store pulses from the same source in different octants of the memory. S3 routes a pair of inputs (J1 and J2) into pairs of quadrants or octants or four inputs (J1, J2, J3, J4) into either octants 1, 3, 5 and 7 or 2, 4, 6 and 8.

Constructed on
A BP-30

PPCo-A-5331

Figure 7
Jumper Module

Notes:
All relays shown dc-energized.
Constructed on a BP-30
R's = 100 Ω
CR's = 1N 100
K's = GE # 3S279IG200R8

PPCo-B-5332

Figure 8
Relay Module

3.3.3 Programmed Routing

Obviously, S2 and S3 could be remotely located, since J12 mounts on the rear apron. Moreover, when P12 is replaced by P12A of Figure 10, it is possible to employ up to nine simple contact closures (as from sample changer limit switches) to perform nine different routing combinations automatically. Figure 11 shows the possible combinations and programming requirements in the pin-patch board. Note that without manual intervention the machine must store in octants or quadrants or halves, but never intermixed, because the MEMORY DIVISION switch (S1 of Figure 5) is not duplicated remotely.

3.3.4 Initial Delay

This portion of the logic is called into service only during accumulation and only when the analyzer MODE switch is in the EXT and EXT DLY position (formerly the EXT/4 position). During the initial delay period EXT DLY (Figure 12) holds the 2^5 address flip-flop in the analyzer reset. This prevents 2^4 carries from advancing the address register (which normally acts as a timing scaler).

When reset, all the flip-flops of the Initial Delay Scaler except the least significant return to the zero state; the least significant returns to the one state. This effectively sets up a binary 32. If S5-S14 are OFF, regardless of the position of S4, the first 2^4 carry trips the Initial Delay Preset Gate (after due propagation through two logic elements and a pulse shaper), so that EEID resets the External Delay Flip-Flop (which establishes the overflow carry). EEID also resets the STORE Flip-Flop which, through the Signal Gate, allows storage to begin. The propagation through all the logic (in both the CN-1024 and the adapter)

Figure 9
Signal Control Switching

Figure 10
Remote Signal Control Switching

will cause considerable narrowing of the first time channel, but the narrowing is constant, regardless of channel width, and can be measured if critical (4.2).

If, because of the positions of S5-S14, 2⁴ carry does not trip EEID, the trailing edge of the shaped pulse advances the scaler so that the next carry can examine the gate. Had the scaler been straight binary with the outputs through switches to the gate (so that the gate would have required no inspection pulse), then the propagation, while possibly less, would have been a function of the switch settings (S4-S15), primarily influenced by the lowest number switch in the ON position.

Storage Location	Pin Patch Column						Input Signal Jacks Used
	A	B	C	D	E	F	
1/8							J1
2/8					Δ		J1
3/8				Δ			J1
4/8				X	X		J1
5/8			Δ				J1
6/8			X		X		J1
7/8			X	X			J1
8/8			X	X	X		J1
1/4							J1
2/4					Δ		J1
3/4				Δ			J1
4/4				X	X		J1
1&3/4						Δ	J1&2
2&4/4					X	X	J1&2
1&5/8		Δ					J1&2
2&6/8		X			X		J1&2
3&7/8		X		X			J1&2
4&8/8		X		X	X		J1&2
1,3,5&7/8	Δ						J1,2,3,&4
2,4,6&8/8	X				X		J1,2,3,&4
1/2							J1
2/2					Δ		J1

Δ=Shorting Pins X=Diode Pins PPCo-B-5335

Immediately after the initial delay period EEID triggers a multivibrator (DM on Figure 5)

Figure 11
Remote Signal Control
Programming Chart

PPCo-C-5336

Figure 12
External Delay Counter

which resets the scaler in preparation for the next system trigger. When in the EXT ROUTE and DELAY mode, each subsequent system trigger starts the R/W gate which (Figure 5) triggers EXT ID. This pulse resets the Store Flip-Flop (to inhibit inputs during the delay interval) and sets the External Delay Flip-Flop (enabling 2^4 Carry to be counted).

3.4 Construction

Figures 13 and 14 best show the construction details of the adapter. Table I lists all the major electrical components. The listed power supply, while operating extremely conservatively in this application, was purchased with an eye to future expansion. Figure 15 identifies the system cabling, while Figure 16, 17 and 18 show cable details. Figure 19 shows module location.

Figure 13
Front View
Eight Input Adapter

So called insignificant wiring errors cause most of the checkout problems. No adjustments are required of the logic.

A BL-31 card file can accommodate all the logic and be acquired for less money. However, a BL-33 can house all the logic and an S-029 power supply can provide a more compact and economical arrangement.

Figure 14
Rear View
Eight Input Adapter

In development work, the taper pin connection provides excellent reliability as well as the flexibility necessary for making many modifications and additions. Soldered backwiring can be substituted by employing a BL-32 instead of a BL-33 (or a BL-30 instead of a BL-31). This increases technician time, decreases reliability somewhat, and decreases hardware costs.

Figure 15
Interchassis Cable Diagram

Figure 16
CN-1024 Control Cable

Note-This jumper plug must be installed in J12 during local operation
PPCo-A-5339

Figure 17
Signal Control Jumper Plug

PPCo-A-5340

Figure 18
Remote Signal Control Cable

FILE TYPE BL-33
POWER SUPPLY RP-30
ALL LOGIC HARDWARE AVAILABLE FROM
COMPUTER CONTROL CORP., OLD CONNECTICUT PATH,
FRAMINGTON, MASS

PPCo-B-5341

Figure 19
Logic Module Location

TABLE I

List of Major Components
Eight Input Adapter

<u>Quantity</u>	<u>Part No.</u>	<u>Description</u>	<u>Manufacturer</u>
1	BL-33	Card File	Computer Control Company ³
1	RP-30	Power Supply	" " "
3	BC-30	Binary Counter Pac	" " "
2	DJ-30	Gate Pac	" " "
6	DN-30	Gate Pac	" " "
3	DM-30	Delay MV Pac	" " "
1	FF-30	Flip-Flop Pac	" " "
1	MS-30	Shaper Pac	" " "
2	BP-30	Blank Pac	" " "
1	JL-10	Jumper Set	" " "
8	3S2791G200R8	Relay	General Electric Company
1		9 x 8 Pin Patchboard	Sealelectro
8	H-641	Pulse Transformer	United Transformer Corp.
1	1N3997A	Zener Diode	
16	1N100	Diode	
8		100 Ω , $\frac{1}{2}$ W, 10 Percent Resistor	
2		3-Pole, 9 Position Switch	
1		6-Pole, 4 Position Switch	
1		Taper Pin Insertion Tool	

4.0 SOURCES OF ERROR

4.1 Input Pulse Ambiguity

When two pulses on different inputs arrive closely spaced in time, certain ambiguities may result. If they fall within 10 to 40 nanoseconds of one another (the large variation is quite small in terms of one megacycle logic) and if, for example, one is to be stored in the

first octant and the other in the eight, then theoretically they may be stored in any octant. In actual practice, however, the slight differences in logic element speeds cause preferred octants, and these vary depending upon where the race occurs. Pulses spaced between this ambiguous location region and approximately 200 nanoseconds (again depending upon individual logic element differences) cause a storage in the time of the first pulse but at the group specified by the second. The Input Gates (Figure 4) close after this time, allowing proper storage of pulses spaced greater than 200 nanoseconds (storage of only the first).

If an input pulse, nominally one microsecond wide, is in progress when the Input Gates open (either at the beginning of a time scan or the end of a storage cycle) it will be stored at a time later than it actually arrived; the actual error (a function of pulse width) for an A-1 pulse will be in the order of 0-800 nanoseconds $\pm$ 100 nanoseconds.

Most of the problems associated with input pulse ambiguity may be avoided by proper selection of maximum instantaneous pulse rate. Use of five megacycle logic will reduce the time magnitudes by a factor of two to four.

4.2 Initial Delay Propagation

The propagation times associated with the initial delay system will cause shortening of the first active time channel, by 0.25 to 0.5 microsecond. Most generally the area of interest can be displaced so that the first channel can be neglected. If not, the narrowing effect should be measured by statistical techniques. The propagation time is independent of delay setting; to measure it set in a delay of 32 (or more) channels, and using a pulse generator for a system trigger and a noise source into the A-1, accumulate and record data at 0.25, 0.5, 1.0 and 2.0 microsecond channel widths until good statistics have been acquired. The fraction by which the first channel (perhaps the first two channels at 0.25 microsecond widths) are down below the mean of the others is directly proportional to the propagation delay. Equation (1) expresses the relationship.

$$S = \frac{(C_m - C_1) W}{C_1} \quad (1)$$

where S is the channel one shortening time in microseconds

C_m is the mean acquired count in all channels except channel one

C_1 is the acquired count in channel one

W is the channel width in microseconds

The calculated shortening time for the various channel width settings should agree with one another in width to 25 nanoseconds.

5.0 CONCLUSIONS

Operation of three modified analyzers over a period of six months had revealed no reliability degradation due to the modification. The adapter described herein had, over the same period, operated without failure. Its modules may be used in other systems and replaced without any adjustments. Slower or faster logic can be substituted without wiring changes where either cost or speed become more serious criteria.

6.0 ACKNOWLEDGMENTS

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7.0 BIBLIOGRAPHY

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APPENDIX I

Modifications to CN-1024 Analyzer for External Routing and External Initial Delay Scaling

1.0 List of Materials

- 7 1N281 diodes
- 3 2N440 transistors
- 3 2N1301 transistors
- 6 1K $\frac{1}{4}$ W 5% resistors
- 3 2.2K $\frac{1}{4}$ W 5% resistors
- 1 4.7K $\frac{1}{4}$ W 5% resistor
- 1 10K $\frac{1}{4}$ W 5% resistor
- 1 Small terminal board
- 1 22 pin printed circuit kluge card $4\frac{1}{2}$ " x 5," USECO #13510 or equivalent.
Miscellaneous #26 insulated, stranded wire, spaghetti, solder.
- 1 Gorn GMCT 26 pin connector (bulkhead) and mate (cable). A solder type may be substituted.

2.0 Back Wiring and Chassis Wiring CN-1024

2.1 Remove the wiring from 17A. Replace it with a 2.2K resistor and the cathode of a 1N281 diode. Fasten the wire to the other side of the resistor, using clear spaghetti over the resistor. Solder a two foot length of No. 26 wire to the 1N281 anode, insulate with shrinkable tubing and leave for the time being.

2.2 Repeat the above (2.1) process at 17C.

2.3 Repeat the above (2.1) process at 16T.

2.4 Solder the cathode of a 1N281 to 16N, being careful not to disturb other connections. Solder a two foot length of No. 26 wire to 1N281 anode, insulate with shrinkable tubing and leave unterminated for the time being.

2.5 Repeat 2.4 at 17M.

2.6 Repeat 2.4 at 17N.

2.7 Remove bus wire between 16K and 17K. Repeat 2.4 at 16K.

2.8 Run a wire between 35A and 36A.

2.9 Run a wire between 35M and 36M.

2.10 Remove the wire from 12K. Replace it with the network shown in Figure A1. Locate this network as close to P.C. Socket 12 as possible. Connect the wire which was on 12K to terminal 3 of the network.

2.11 Connect a wire between 36C and 16P.

2.12 Connect a wire between 36E and P6-15.

2.13 Connect 12 Net 1 to 16M.

2.14 Connect a wire between 36J and P6-20.

3.0 Connector Replacement

3.1 Remove P3 (Ext. Mem. Loc.). Marking only the wire from Pin D (Com).

Figure A1
12 Net

3.2 Insulate unused wire ends with shrinkable tubing (four).

3.3 Enlarge the connector cutout to accommodate a 26 pin MRE (Gorn GTC) female bulkhead connector. Install the connector.

3.4 Connect the wire from 3.1 (Com) above to Pin A of the new connector (J3).

3.5 Connect J3C to the Diode Anode at 17N.

3.6 Connect J3D to the Diode Anode at 17C.

3.7 Connect J3E to the Diode Anode at 17M.

3.8 Connect J3F to the Diode Anode at 17A.

3.9 Connect J3H to the Diode Anode at 16N.

3.10 Connect J3J to the Diode Anode at 16T.

3.11 Connect J3K to the Diode Anode at 16K.

3.12 Connect J3L to 12 Net 3.

3.13 Connect J3M to 36D.

3.14 Connect J3P to 12J.

- 3.15 Connect J3R to 12C, 2^9 O.F. gate.
- 3.16 Connect J3S to 12E, 2^8 O.F. gate.
- 3.17 Connect J3T to 12H, 2^7 O.F. gate.
- 3.18 Connect J3U to 12 Net 2, 2^6 O.F. gate.
- 3.19 Connect J3V to 36-K, End of Write pulse.
- 3.20 Connect J3W to 36F, R/W gate.

4.0 Module Changes

4.1 On card 17, jumper or short out the 2.2K resistors loading to Pins A and C.

4.2 On card 16, jumper or short out the 2.2K resistor leading to Pin T, and jumper the collector of Q_2 to Pin K.

4.3 On card 12, remove the 1K resistor leading to Pin K. Jumper Pin K directly to the base of Q_3 . This may be identified by tracing Pins B, D and F each through 100 PF capacitors and 1N281 diodes to a common point (the base of Q_3).

4.4 Build card 36 according to Figure A2.

4.5 On card 12, remove the 1K resistor leading to Pin J.

5.0 Drawing Corrections

5.1 Change the appropriate drawings to reflect all changes.

5.2 On 87859:

5.2.1 S2-4-11 label should be 2nd/4th qtr - to 13V - set 2^8 .

5.2.2 S2-5-11 label should be 2nd half, 3rd/4th qtr - to 13T - set 2^9 .

5.2.3 S2-6-11 label is meaningless.

5.2.4 S2-1-6 label should be Reset 2^9 - to 13W.

Figure A2
Logic Card 36

5.2.5 S2-1-2 label should be to 17K - 2^8 to 2^9 addr carry gate.

5.2.6 S2-2-2 label should be to 17R - 2^7 to 2^8 addr carry gate.

5.2.7 S2-2-5 label should be to reset 2^8 to 13X.

5.2.8 S2-3-2 label should be to 12C - 2^9 O.F. gate.

5.2.9 S2-3-4 label should be to 12E - 2^8 O.F. gate.

5.2.10 S2-3-6 label should be to 12H - 2^7 O.F. gate.

5.2.11 S2-4-10 label should delete P3A.

5.2.12 S2-5-9 label should delete P3B.

5.2.13 S2-6-10 label should delete P3C.

5.3 On B7860, add label at S3-4-2 to read "READOUT."

5.4 On B7870:

5.4.1 Pin B label 2^9 O.F. . . .

5.4.2 Pin D label 2^8 O.F. . . .

5.4.3 Pin F label 2^7 O.F. . . .

5.4.4 Pin J cross out 1/2.

5.5 On B7462-2 Relabel:

5.5.1 Pin R - reset 2^8 .

5.5.2 Pin S - reset 2^9 .

5.5.3 Pin B set 2^7 .

5.5.4 Pin P set 2^9 .

5.5.5 Pin N set 2^8 .

5.5.6 Pin V Quarter (gnd)**

5.5.7 Pin T Half (gnd)**

5.5.8 Pin U Octant (gnd)**

6.0 Switch Label Changes

6.1 Change position 9 of S2 from Ext/2 to EXT RTE.

6.2 Change position 10 of S2 from Ext/4 to EXT RTE and DLY.

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