FOUR-DEEP CHARGE-TIME AND PULSE-WIDTH SCALING DISCRIMINATOR FOR DELAY LINE MWPC's*

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SUMMARY

A discriminator has been developed for digitizing both intercepted total charge and location of electromagnetic shower and particle trajectories in multiwire proportional chambers read by delay lines. Determination of shower trajectory is aided by video signal integration followed by centroid-locating discrimination. Calibrated run-down of the signal integrating capacitor gives the charge information above a given threshold level.

The discriminator is designed to handle up to four shower-induced video signals per event by incorporating steering circuits within the module. Each video signal is examined for time over an adjustable threshold. Video pulses with separation of less than 20 nsec are treated as a single pulse. Counter-logic circuits indicate the number of video signals digitized. These signal processing circuits provide a first level of data sifting which otherwise must be carried out with additional discriminator channels and added complexity in data recognition.

INTRODUCTION

The application of multi-wire proportional chambers (MWPC) as position sensors is well known. A familiar method of readout uses the "amplifier-per-wire" system where each wire of the chamber is connected to an amplifier and logic chain. Output data from this type of system is commonly digital, indicating only whether a particular wire has been "hit". Another method uses the delay line technique[1], where all the wires of a chamber plane are elctrically coupled to a common delay line. The location of a "hit" is determined by measuring the time that the resulting signal takes to reach an end of the delay line. The delay line has the important characteristic of preserving the amplitude of the signal; thus, if the chamber is operating in a proportional mode, the intercepted charge in the chamber by the passage of ionizing particles can be measured.

Another notable characteristic of MWPC delay line readout is the inherent ability of the line to coalesce a cluster of induced signals such as are produced by the passage of electromagnetic showers. The reconstituted output voltage of the delay line then is a signal profile from which the intercepted amount of charge and the location of the shower can be determined.

The application[2] for which this discriminator is developed requires 1) digitizing the charge developed by each of up to four showers per chamber per event and 2) determining the location of each shower. Because of the characteristics listed above, the delay line readout scheme is ideal for this purpose, provided that dead-time effects can be minimized in the manner shown in an associated paper[3].

DISCRIMINATOR OPERATION

The discriminator is essentially composed of two functional sections: the video steering section which includes circuitry to separate the showers, and a section containing four identical charge-to-time converters. Circuit function can be readily followed with the aid of the simplified block diagram in Figure 1. The timing sequence for an event during which for example two showers traversed the chamber is shown in Figure 2. The two video pulses resulting from the two showers are labeled V1 amd V2.

Video Steering Section

The presence of an event is signalled by the Master Trigger. It causes flip-flops FF1 through FF5 to be set into their initial condition: FF1 is set; the others, reset.

The video signals from the delay line first pass through an Inspection Gate. This gate, operated by a signal from the Hazard Inspector[3], is used to gate out signals from the delay line which are unrelated to the event. As pulse V1 exceeds a predetermined threshold, the Time-over-Threshold (TOT) discriminator simultaneously opens video gate G1 and triggers the Integration Period (IP) one-shot.

*Work supported by the National Science Foundation (Grant GP-38611) and the Energy Research and Development Administration.

As pulse V1 re-crosses the threshold on the trailing edge, the TOT discriminator closes video gate G1, resets both the IP one-shot and FF1, and sets FF2 in preparation for pulse V2. Under normal signal conditions, video time-over-threshold will be less than the period of the IP one-shot.

As the second pulse, V2, crosses the threshold of the discriminator, it opens video gate G2 and again triggers the IP one-shot. As pulse V2 re-crosses the threshold on the trailing edge, the discriminator closes video gate G2, resets both FF2 and the IP one-shot, and sets FF3. The process repeats itself for up to four video pulses. The last flip-flop, FF5, indicates an overflow where more than four pulses above threshold levels are received.

The Integration Period one-shot guards against video signals whose time-over-threshold with time in excess of the IP one-shot period will allow the one-shot to time out, thereby setting the appropriate integration overflow flag--OF1 to OF4.

Video Integration and Profile Center-Finding Section

Each charge converter section operates identically as follows.

Integration of the video signal begins immediately upon opening of the video gate. A current proportional to the signal voltage from the video gate output is used to charge an integrating capacitor. The integrated voltage thus developed is applied to the timing discriminator to generate a STOP pulse which is time related to the centroid of the shower induced waveform. A simplified circuit of the timing discriminator is shown in Figure 3a. Figure 3b shows timing relations of typical waveform integration and timing pulse generation. The integrated video signal follows two paths. It is applied to a times 2 attenuator to produce half-height waveform A in Figure 3b. It is also applied to a 400ns delay to produce a delayed unit-height waveform B. If the input video signal is less than 400ns long, waveform A acts to produce a half-height threshold at the comparator; the time of arrival of the half-height of the delayed waveform B is then detected by the comparator. This time is systematically related to the time of arrival of the centroid of the shower pulse at the input to the discriminator.

Video Charge-Time Conversion Method

Generation of the STOP pulse starts the charge-time conversion. The STOP pulse sets Q flip-flop (QFF) which starts a calibrated current source to discharge the integration capacitor. Output of the QFF is brought to the front panel to gate an external scaler. Run-down of the integration capacitor is monitored by a comparator which resets QFF as the capacitor voltage crosses zero baseline. The time interval between set and reset of QFF then represents the relative charge of the video waveform.

Pulse-Width Scaling

Characterization of showers is enhanced with the additional capability to measure the width of the intercepted particles. The width information is generated by the TOT discriminator as previously described.

The output pulse of each video gate is transmitted to start/stop an associated scaler external to the discriminator. The content of each scaler then is systematically related to shower width.

RESULTS

A prototype has been tested using a 14 GeV electron and pion beam and the results met with primary objectives. Inherent charge resolution is 25% predominantly determined from shower electron multiplicity statistics and centroid location is better than 1 mm. Construction of 28 units are being readied to be used in experiments E-192/454 at FERMILAB.

ACKNOWLEDGEMENTS

Thanks are due to members of LBL's Physics Systems Instrumentation Group who had given support to this project, in particular, Stan Olson and Cynthia Whiteside.

REFERENCES

1. Victor Perez Mendez et al., "Electromagnetic Delay Line Readout for Proportional Wire Chambers," preprint UCRL-19858 (June 25, 1970).

2. Stan Olson et al., "A MWPC Instrumentation System with Small Dead-Time and with Provision for Automatic Testing and Calibration," published in these proceedings.

3. D. B. Turner et al., "Delay Line MWPC Hazard Signals Inspector," published in these proceedings.

LEGENDS OF ILLUSTRATIONS

Figure

1. Block Schematic of 4XQT Discriminator

2. Timing Sequence (two TOT event)

3. Waveform Integration and Timing Pulse Generation

BLOCK SCHEMATIC OF 4XQT DISCRIMINATOR

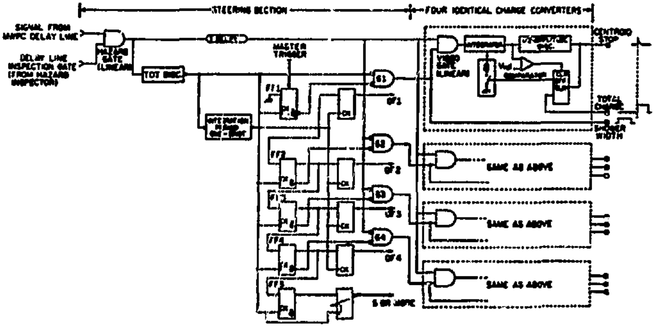


FIGURE 1

4XQT TIMING SEQUENCE (2 TOT EVENTS)

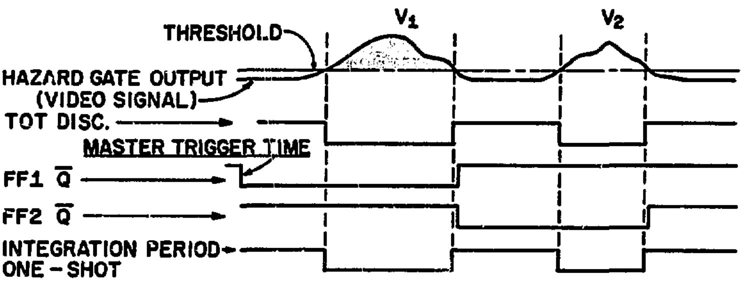
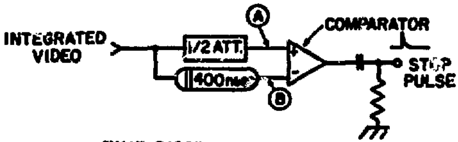


FIGURE 2

WAVEFORM INTEGRATION AND TIMING



TIME DISCRIMINATOR

FIGURE 3(a)

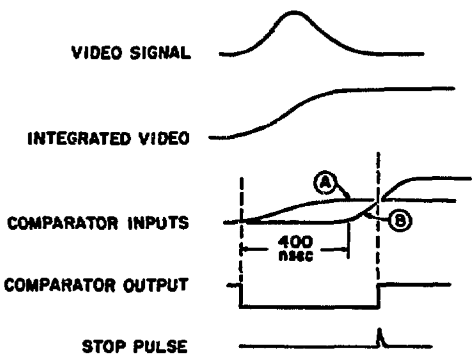


FIGURE 3(b)