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UC-38

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FLOW SOLDERING
AND SUPPORTING
PROCESSES

BDX-613-330

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Project Leader:
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Department 845

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Final Report

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KANSAS CITY DIVISION

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ABSTRACT

An investigation was conducted to evaluate the application of flow-soldering techniques to the fabrication of printed-wiring board assemblies at Bendix Kansas City. Circuit-board design principles, cleaning methods, solderability tests, and lead-forming techniques were reviewed and present board soldering specifications were re-evaluated as supporting activities. Overall results of the project indicate that flow soldering is a suitable process for use on many types of BKC printed circuit-board assemblies, and that use of that method will increase production rates on those assemblies for which it is suited.

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SUMMARY

The history of flow soldering experimentation at Bendix Kansas City goes back about 15 years, when two engineers tried to solder a printed wiring board assembly by dragging it across the surface of a molten solder bath. Many problems were defined as a result of those experiments, but few were solved, and the experiments were discontinued because the need at that time did not justify further expenditures.

No further action was taken until 1962, when two commercial soldering machines were purchased. These machines were used with various degrees of success through 1966. Most of the inconsistent results experienced was probably caused by lack of product designs compatible with the process and the attitude that flow soldering must produce soldering quality that is visually superior to that of equivalent hand-soldered assemblies.

Since commercial soldering machines and associated process control features had been improved since the initial experiments and because it was apparent that flow soldering might offer quality and economic advantages on some assemblies, the subject was reopened as a feasibility study in 1967. The new project encompassed investigation and study of pc-board soldering features such as board layout and path designs, lead material, cleaning methods, tinning, and solderability, which were required to ensure soldering quality at least equal to that attainable by the best hand-soldering processes. When necessary, specific requirements were established to ensure good wave-soldered assemblies. For the less-exacting processes, general guidelines were established to allow designers and process engineers to exercise individual discretion insofar as possible. The flow-soldering portion of the present soldering specification, 9913000, "Soldering of Electrical Connections," was reviewed and revisions were proposed to provide more realistic evaluations of wave-soldered products.

The methods of determining and maintaining solderability, the cleaning methods, the ultrasonic tinning process, the methods of preforming and retaining component leads, and the pc-board layout and path configuration features resulting from this project can be applied beneficially to virtually all pc-board assemblies, regardless of the method of soldering used.

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DISCUSSION

SCOPE AND PURPOSE

The purpose of this project was to review the work which was accomplished during the 5 years since flow-soldering equipment was installed at BKC and to determine an optimum course of action which must be followed if the process of flow soldering is to become practicable at BKC.

To accomplish this purpose, the project was planned on the broadest base imaginable, with the understanding that some solutions would coincide or coexist with others in such a way that the reporting would be combined.

Basically the project covered the following:

- Capability and the setup conditions of flow soldering equipment;
- Condition of the materials to be soldered;
- Design of the assembly to be soldered;
- Method of assembly just prior to soldering;
- Materials used in conjunction with the soldering process;
- Fixturing required for the soldering process; and
- Cleaning of the assembly after soldering.

The scope of this project included investigation of all parameters that involve flow-soldering equipment, processes, and board conditions which could affect a flow-soldered pc-board assembly. Initially, 16 categories of subject matter were considered necessary conditions to be thoroughly explored and ultimately controlled. Some of these categories became so inextricably combined that they have been reported in their combined form for clarity. Definitions of the 12 remaining categories follow.

- Board Cleaning defines the types of soil which must be removed from metallic surfaces so that successful solder joints may be assured. Methods of eliminating contamination were investigated, as well as the effects of different types of contaminants on flow soldering results.

- Board plating is an extension of one phase of board cleaning; however, the variety of processes and methods of application and control make this a legitimate separate subject. Hot-dip plating, electroplating, and methods of plating-thickness control were included in this portion of the investigation. The tendency of different plating materials to resist the formation of oxides was studied also. The latter is an extension of the subject matter in the first category.
- Printed circuit board design principles were thoroughly evaluated. Recommendations are made concerning path and land size, spacing, and the relationships of all factors which have a significant effect on the success of the flow soldering process. A pattern was developed for a pc board which embodied a spectrum of path configurations ranging from the desirable to the impossible. There are many examples in this pattern that show what to avoid. Photographs were taken to show the results of wave soldering upon these design faults.
- Board material, on investigation, was limited to copper laminated to a fiberglass-reinforced epoxy substrate. As long as this material is used, only a few precautions need to be observed. It was not anticipated that the lower quality phenolic substrates would ever be used in Bendix products; therefore, no evaluation of those materials was included. It is known, however, that the more consumer-oriented product manufacturers have successfully combined phenolic pc boards and flow soldering.
- Solderability of boards and of component leads was treated separately because of its importance in hand soldering, as well as in flow soldering. Methods of determining solderability and methods of achieving it were thoroughly investigated. Much of the material in this report has been collected from the work of other manufacturers and from the BKC materials engineering department.
- Lead cleaning and lead composition are necessarily related, so that what were originally conceived as separate subjects are combined in this report. Because component-lead material varies, depending upon the type of path material, the cleaning processes used are reported separately. Both chemical and ultrasonic methods were evaluated in combination with lead tinning. Details of the ultrasonic cleaning process are discussed in the section pertaining to solderability.
- Lead forming and component holding were combined and studied as as one possible method of securing components in place during wave soldering. This was a significant problem in previous attempts to wave solder at BKC. This problem was greatly magnified by the density of components on the pc board and the use of stand-up (Japanese) component mounting required to achieve such density. New developments in industry have

produced possible answers to this problem, and continue to expand the scope of useful solutions. Because of this, what was done on this project may be obsolete or improved upon by the time this report is released.

- Component insertion was treated empirically because the automation of such processing is expensive and generally requires high production to make it economically feasible. The resulting improvement of quality and reduction of inspection time make this subject particularly significant in relation to flow soldering. A reduction of handling of pc board assemblies between component insertion and soldering is most desirable. Such handling has a tendency to change component positioning, which can disrupt subsequent assembly operations on many board assemblies.
- Fluxing of board assemblies before soldering and effective fluxing materials were investigated, with the greatest attention being given to those methods which have been incorporated in present-day flow-soldering equipment. Automated flux application improves the consistency of flux film and helps reduce handling of the assembly before soldering.
- Fixturing may be approached from many different directions without adversely affecting the results of the flow soldering operation. Two basic types were evaluated, the type which locates the assembly in a rigid relationship with the track of the equipment, and the type which allows the assembly to float across the surface of the molten solder.
- Solder wave control and machine setup were combined because of the close relationship of these factors. The exploration of this subject resulted in establishing basic guidelines rather than producing a tabulation of specific control settings. Since the configuration of the assembly being soldered plays such an important part in the machine setup, it is expedient to describe the desirable end results and explain ways to eliminate the undesirable ones. It is at this level that regimentation of the flow-soldering process breaks down and human experience, technique, and integrity take over.
- Cleaning refers to a post-soldering operation designed to remove those materials added to assist soldering, but which are not desirable as part of the finished product. This operation can be automated or not, as desired. There are advantages and disadvantages either way. These and the types of materials to be removed are discussed generally.

The use of ultrasonics in the solder pot is still in experimental stages. Most manufacturers of flow-soldering equipment are reluctant to say more than that they are "looking into the possibilities." One manufacturer incorporated this as an optional feature in 1967, but has not promoted that option. The principal advantage of ultrasonic agitation in the solder pot is that it eliminates or reduces the need for flux, thereby reducing the amount of cleaning required after soldering.

PRIOR WORK

The first experiments with flow soldering at BKC, focused on the basic condition of dragging a printed circuit board assembly across the surface of a pool of molten solder, were begun about 15 years ago. The presence of dross on the surface of the solder and icicles and bridges on the circuitry of the pc board caused that work to be discontinued. Nine years ago, two wave-soldering machines were installed in two electronic assembly areas. Those machines were more sophisticated than those previously used in that a pump was added to form a wave of flowing solder above the natural level of the pool. This solved the problem of dross, but icicles and bridges remained. These machines were used with inconsistent success, and since consistency is necessary to assure product quality, there was no full-scale effort to incorporate this manufacturing process into production.

From 1962 through 1966, attempts were made to incorporate flow soldering into the manufacturing processes of printed circuit board assemblies at BKC. Some of these attempts were successful and some were not. The reports which were written on the results of those efforts show that the problems were correctly diagnosed, but the solutions were either outside of the state-of-the-art at that time or were disallowed by requirements of specifications which were primarily designed for hand soldering.

In 1966 the subject of flow soldering was reopened, and a process engineer¹ with previous experience in the use of this process elsewhere in industry was employed. He began the present development project in 1967. Most of the accomplishments reported herein came about as a result of his efforts and the rapid advancement of flow-soldering-machine design. The remaining problems of icicling and bridging can be brought under control.

It is interesting to note that the machine most recently evaluated by BKC employs the still-pool type of solder bath--the same basic design used in the first BKC experiments 15 years ago.

¹H. M. Garrison, D/845-3

ACTIVITY

Board Cleaning

Due to the nature of BKC's use of its end product, a high degree of cleanliness is required to guard against current leakage, shorts, or changes in circuit characteristics.

There are two basic types of soil to be considered when working with printed circuit boards:

- The metallic oxides which may affect either copper or tin/lead plating will occur only on the circuit path surface; and
- The oils or other similar types of soil contaminants which are the result of exposure to a normally-degraded air mass or to human-body oils from normal handling.

The latter may affect both metallic and substrate surfaces. Some types of oils will accelerate the formation of oxides or other metallic salts on the surface of the circuitry.

The best method of cleaning, of course, is the prevention of contamination. To accomplish this, the air to which the boards are exposed must be cleaned and filtered, persons handling the boards must wear nylon gloves, and the boards must be enclosed in an envelope or wrapping made of some inert material which does not allow the passage of air.

Cellophane and Mylar are the best of the modern plastics for protective purposes. Plastic films which are heat-sealable have a plasticizer in them which will evaporate from the surface of the plastic and redeposit on the surface of the pc board. Heat-sealable plastic bags can be used if the pc board is prewrapped in some inert material. Any paper used for prewrapping must be neutral, particularly concerning the acid and sulphide content of the paper.

The present method of protecting a cleaned pc board is to heat seal the board in a clean plastic bag. However, this method can create a contamination problem caused from the fumes liberated during the sealing operation. A better method would be to fold the bag twice and staple it securely.

Assuming that the boards are not kept clean, there are procedures which can be used to remove soil from their surfaces. Most oils can be removed with some form of solvent such as trichloroethylene, toluene, or alcohol. The most effective method of application is the spray process, which strikes the surface and is blown off taking a portion of the soil with it.

Wiping is adequate, providing a clean absorbent material is used and not reused on a second board surface. Visual evaluation of a wiping material for cleanliness is not sufficient, since many contaminating oils are transparent and cannot be seen.

Final cleaning processes for pc boards that do not have a gold immersion or which are fused in hot oil consists of a vapor-degreasing operation using Freon PCA (MS4611111), a pumice hand scrub, and water rinse. When clean handling procedures are used, these board-cleaning operations are adequate for wave-soldering applications.

Copper oxides and sulphides and tin/lead oxide are common contaminants of pc-board metallic surfaces. They may be formed by exposure to air. Prevention of the formation can be accomplished by excluding the air from contact with the metallic surface. Containers, either flexible or rigid, which can be evacuated and sealed can be used for that purpose. In place of evacuation, it is possible to replace the air in the container with some inert gas which does not readily combine with the metal or form a salt. For most pc-board metal surfaces this can be accomplished with nitrogen or argon.

If oxides or other salts are formed on the metallic surfaces, they must be removed. The flux which is used in the soldering process will do an adequate job if the deposit on the metallic surface is not too heavy. Heavy deposits must be cleaned by dipping in an acid cleaner, which must then be removed by a double rinse in running water and deionized water.

Mechanical cleaning of pc boards with tin/lead plating has been discarded because of the mechanical action which creates solder slivers and rolling of the tin/lead plating over the edge of the copper laminate which leaves a possibility that the plating will break off at a later time.

Another approach to keeping the board clean is the use of a solder-resist-coating silk screened on the board. The silk screening master is designed to cover the board with the resist coating in all areas except those to be soldered. This method eliminates bridging between adjacent paths and reduces the chances of arc-over. Other advantages inherent in this method are: inspection is reduced; less solder is required in the soldering operation; the plating operation is eliminated; and for some conditions, the silk-screened solder-resist serves as a conformal coating.

A solder-resist coating (Lonco's PC535) was silk screened on developmental boards having tin/lead plating over the copper. These boards were soldered with the wave-soldering machine (pot temp 525°F) to check for blistering of the resist coating. Paths 0.030 inch or wider exhibited some blistering,

particularly where two or more paths with 0.030-inch or less spacing gave a large amount of mass in a small area. The blistering was caused by the tin/lead plating becoming molten and increasing in the Y plane, which ruptured the resist coating. This coating was approximately one year old and would not withstand as much heat as a fresh coating.

If the boards are solder leveled to control the thickness of tin/lead plating before application of solder resist, the incidence of blistering or rupturing of the coating is substantially reduced.

Three unplated pc boards were coated with the resist material and soldered with the wave-solder machine at pot temperatures of 500, 480, and 460°F, respectively. The two boards soldered at 500 and 480°F exhibited some blistering, but not to the extent of the tin/lead-plated boards. The board soldered at 460°F did not exhibit any blistering.

All of the solder-resist coated boards were traversed over the solder wave at 2 feet/minute, and were preheated to 240°F before being soldered.

Board Plating

The major purpose of plating on printed circuit boards is to preserve good solderability characteristics. For the plating to combine with the copper, the copper must be free of finger prints, oxides, oils, or any contaminant. Methods of accomplishing this are discussed in the section on board cleaning.

The most common type of plating, the one used at BKC, is electrodeposited tin/lead plating over a copper base material. If the copper surface is clean, this type of plating is satisfactory; however, if the copper was not clean when plated, the plating may look good, but lack good surface combination. There may be residual contaminants between the plating material and the copper. The tin/lead plating can bridge across such imperfections, hiding them from view. Small localized areas will not cause any problem during subsequent reflow or wave soldering. A larger area may appear as a void in the plating, called a dewetted area, when melting of the plating allows the bridge over such contaminants to separate.

Porosity is another problem that may be encountered in electroplating. If the plating is porous, extended storage will allow oxygen to penetrate through the plating and oxidize the surface of the copper. This causes dewetting in subsequent soldering operations.

Plating thickness by the electroplating process can vary from 0.0003 to 0.0035 inch on the paths or pattern with a minimum of 0.0003 inch in the plated-through holes in accordance with Process Standard 9928001. The best soldering results were obtained with a plating thickness of approximately 0.003 inch on the pattern and 0.001 inch through the hole.

Experiments by one of the major manufacturers of wave-soldering equipment has shown that a solder plating is the best method of preserving a clean copper surface on a pc board. The solder plating gave approximately three times the shelf life of any other protection. Expensive packaging was unnecessary. Solder plating required only a visual inspection for wettability, as compared to a solderability test for other types of plating.

Another type of protective solderable surface for copper-clad pc boards is a pure tin hot-dip process. If this method is used, the leads of the components to be assembled to the pc board should also be hot-dip tinned. Having once been thoroughly wetted by molten tin, copper remains perfectly solderable. To solder a hot-dip tinned surface it suffices to apply pure resin dissolved in alcohol as a flux. Even after years of storage, the soldering operation can be performed satisfactorily. The reason for this is that as soon as the heat melts the tin coating any oxidation or corrosion floats off into the molten resin of the flux, leaving the tin surface clean and ready to merge with the molten solder.

Hot-dip tinning tends to fill or close the holes in a pc board. If this occurs, a subsequent operation is needed to reopen the holes by leveling or reflowing the tin plating material. There are machines on the market which combine these two operations and ensure open holes in hot-dip tinned boards. The leveling or reflowing process may also be used to control the quality of solder or tin/lead plating. The results of wave soldering are much improved if there is not an excess of plating material on the pc board. It is possible to control the application of tin or tin/lead plating material by electroplating, rather than by hot dipping.

Mechanical methods of scrubbing the excess material from the board circuitry are frequently used for economic reasons. These methods may cause bridging across the narrow spaces between the circuitry, causing shorts. The material wiped from the path surface often may hang insecurely along the edge of the path. In either case, the material has not been removed from the board, and it usually causes trouble during the wave-soldering operations.

A solder-leveling process which gives far superior results has been developed. The process impinges hot polyethylene glycol at high pressure against the surfaces of the pc board. The heat melts the plating material and the force of the hot polyethylene glycol striking the board removes any excess plating material. The amount of plating material left on the paths can be controlled by the pressure of the spray and the time the board is subjected to the spray. The polyethylene glycol can be easily removed by a water rinse followed by dipping in alcohol to remove the water.

Printed-Circuit-Board-Pattern Design

It has been said, "If a printed circuit board is not designed for soldering, do not attempt to solder it." This is especially true with wave or flow soldering.

To determine adequate design criteria, a printed-circuit-board test pattern was developed. (See Figure 1.) This pattern incorporated many variations of path and land configurations to determine the proper relationship between land widths and spacing, path width and spacing, direction of path layout, and the direction of board travel across the soldering wave. The path-to-spacing pattern varies from a 0.050-inch path with 0.005-inch spacing to a 0.005-inch path with 0.050-inch spacing. Some of the paths and spacings are 0.005 inch each. The direction of path layout varies from perpendicular to in-line with respect to the direction of travel of the board across the solder wave. Holes of varying size were used to determine optimum hole-diameter-to-lead-diameter ratio. This test pattern proved to have an additional bonus ability in evaluating the variable characteristics of any flow-soldering equipment and to establish the optimum settings of these characteristics.

Approximately 50 plated and unplated test-pattern boards were wave soldered on equipment installed at BKC. Additional boards were soldered on the machines of different wave soldering equipment manufacturers.

These boards were evaluated for the presence of bridging, dewetting, balling, excessive solder deposit, and icicling. (See Figure 2, A through F.)

Figure 1. Flow-Soldering Test Pattern

A. Excess Solder at Points

B. Excess Solder on Wide Paths

C. Solder Balls on Narrow Paths

D. Bridging Between Wide Closely-Spaced Paths

E. Bridging Between Narrow Closely-Spaced Paths

F. Dewetting on Wide Paths

Figure 2. Examples of Flow Soldering on Standard Soldering-Test Patterns

Pattern designs which will achieve zero-percent probability of bridging are desirable. When the pattern consists of equal path and space widths in multiples of two or more paths, as sketched below, the width should be a minimum of 0.030 inch for each. If the paths are less than 0.030 inch the space between them should still be 0.030 inch minimum. Paths and spaces of 0.020 inch each have a 20-percent probability of bridging.

If the path width is increased to 0.060 inch, the space between the paths may be reduced to 0.015 inch. For paths of 0.040 -inch width, the minimum space between adjacent paths is 0.020 inch. See the following sketch.

If paths of 0.100-inch width are placed on each side of a set of one to four narrow paths, the path and space width can be reduced to 0.012 inch each as illustrated by the following sketch.

Figure 3 may be used as a guideline to determine the probability of bridging with various path and space sizes.

The holes through which component leads are placed should be nominally 0.012-inch larger in diameter than the diameter of the lead, with a minimum of 0.004 inch and a maximum of 0.028-inch more than the lead diameter. Experiments have shown that a difference of less than 0.004 inch does not permit the solder to flow through the hole and form a fillet on the top side of the board. A larger difference than 0.028 inch causes voids or unfilled holes.

Examples of good and bad pc-board designs are shown in Figure 4. If the good (desirable) designs are used, fewer soldering problems are encountered. Good designs employ paths of constant width, and the outside diameter of the lands should be consistent with the path width. The distance from the edge of the hole in the land to the outside edge of the land should be approximately the same as the width of the adjacent paths. Wide local paths or pads tend

Figure 3. Probability of Bridging, Path Width Versus Spacing

DESIRABLE FORMS	UNDESIRABLE FORMS
<p>AREAS ON EACH SIDE OF DOTTED LINE APPROXIMATELY EQUAL</p>	<p>SOLDER FILLET WILL BE NONSYMMETRICAL</p>
<p>APPROXIMATELY EQUAL</p>	<p>SOLDER WILL FLOW AWAY FROM TERMINAL AREA</p>
<p>UNIFORM PATTERN AROUND HOLE</p>	<p>OUTSIDE SOLDER FILLETS WILL BE NONSYMMETRICAL</p>
<p>UNIFORM PATTERN AROUND HOLE</p>	<p>SOLDER FILLET WILL BE NONSYMMETRICAL</p>
<p>OUTSIDE SOLDER FILLETS WILL BE NONSYMMETRICAL</p>	<p>OUTSIDE SOLDER FILLETS WILL BE NONSYMMETRICAL</p>
<p>SOLDER WILL FLOW TOWARD LARGER TERMINAL AREA</p>	<p>SOLDER WILL FLOW TOWARD LARGER TERMINAL AREA</p>

Figure 4. Representative PC-Board Land Configurations and the Effects Thereof Upon Solder Flow

to drain solder from surrounding paths and solder joints, to the detriment of both. The wide paths collect excessive solder, and the adjoining narrow paths are starved. Lands and paths should have a common center. Off-center lands produce nonsymmetrical solder joints. A TO-18 or TO-46 transistor mounting pattern provides a specific example of this problem. The designer must often bring a conductor to the base pad of the transistor, between the collector and the emitter pads. This does not allow sufficient clearance, and is a contributing cause of bridging. If it is necessary to approach the base pad on the same side of the board that carries the collector and emitter paths, a space width of at least 0.020 inch should be maintained. This will reduce the probability of bridging, regardless of path width. Flattening the sides of the lands slightly, as shown in the sketch below, is not desirable, but is permissible if not flattened excessively.

It is better design practice to reduce the diameter of the lands as much as possible, as shown in the righthand sketch.

The method to be used for supporting the assembly during the soldering operation should be considered at the same time when the distance between adjacent circuit paths is established, during the design and layout of the circuit board. Inadequate clearance between the carrier and the paths may cause skips and/or fillets in the path plating. The feature of the carrier which holds the board may deflect solder away from an adjacent path and cause a short length of the path to be unwetted. On the other hand, the same carrier feature will sometimes trap solder against the board and form a fillet of solder which must be removed later. It may be necessary to provide tabs on the board for mounting on the carrier.

Converging paths of any width which terminate in relatively sharp points (such as those shown in Figure 2) show a strong tendency to collect excess solder at the points.

Wide paths (0.050 inch or greater) show a tendency to collect excess solder regardless of path orientation with respect to the direction of board motion across the wave. (See Figure 2B.)

Balls of solder were formed on most paths narrower than 0.020 inch. (Refer to Figure 2C.) This may be an indication of dewetting of the solder or tin/lead plate or an indication of the difficulty of obtaining solder flow along a narrow path. These conditions were all less extensive on unplated boards if they were run across the solder wave with the board just touching the surface of the wave. Positioning the bottom of the board below the surface of the solder wave proved to be a compromise.

The optimum condition for obtaining paths without an excess of solder did not provide enough board depth to form a fillet of solder where component leads emerged from the top of the board. If the board was run across the wave with its bottom surface more than 0.020-inch below the wave crest there was a possibility that the solder would curl over the trailing edge of the board and flood the top surface. With boards of 0.032-inch thickness, the depth of the board in the wave should be between 0.010 and 0.020 inch. It is presumed that the depth of the board in the solder wave should be proportional to the thickness of the board. In keeping with the test results, a depth of $1/3t$ to $2/3t$ (t = board thickness) is recommended.

The test evaluation indicates that no flow-soldering equipment now on the market is capable of plating the system of paths of the test pattern uniformly, without fault. Indeed, if this were possible, the test pattern should fall short of one of its intended purposes--that of evaluating optimum machine setup.

The results which were obtained by running the test pattern across the machines of different manufacturers indicate that the settings of solder temperature, preheat temperature, and track speed may not be identical for all machines. We suggest, therefore, that each machine be set up using this design or some other standard pattern.

A by-product of this test panel is the evaluation of printed-circuit-board manufacturing. Etching a clean 0.005-inch space between two 0.005-inch paths without undercutting the path excessively is a tremendous challenge to any printed-circuit-board manufacturer.

This test pattern expanded its usefulness from printed circuit board design to wave-soldering equipment and printed-circuit-board manufacturing evaluation.

Board Material

The majority of pc boards manufactured at BKC have a thickness of 0.032 inch and are made from G-10 or FR-45 glass laminate. The trend for new designs at BKC is to use the FR-45 material, which does not warp as easily as the G-10 and measling is seldom experienced.

Although it is possible to flow solder assemblies built on pc boards of 0.032-inch thickness, the probability of poor solder joints caused by warpage is greatly increased. Boards of 0.062-inch thickness decrease this probability substantially. More-substantial or more-confining fixturing is required to offset the tendency of the thin boards to warp. This fixturing usually provides complete support for the edge of the pc board, with numerous hold-down points to restrain the board. Boards of 0.062-inch thickness can frequently be soldered by using a universal fixture with spring fingers which grip opposite sides of the board.

Both G-10 and FR-45 boards were tested, with the G-10 exhibiting some tendencies to measle. The measling is caused by the top layer of the substrate delaminating from the adjacent layer in a few circular spots, which gives the appearance of white measles. The delamination usually occurs if the adhesive is not completely cured between the substrate layers. This deficiency can be cured by placing the boards in an oven set at 250°F for 45 minutes before components are assembled and wave soldered. Two things should be kept in mind if this procedure is followed: If the component mounting holes and potting holes are in the board prior to the added curing, there will be much more exposed edge; and gases which may be caused by the curing will be more easily liberated. Since internal stresses are likely to occur during the process, provision should be made to restrain the boards to prevent warpage. Another possible cause of measling is the lack of adhesive between the layers. There is no way to correct this after the board material is made. Each delaminate unit area, or measle, is about 0.032-inch in diameter. Severe measling would not reduce the laminated area between board layers by more than 10 percent. For this reason, it is felt that this characteristic should not be cause for rejection.

The FR-45 board material, which is defined as type GH by the MIL-Spec, is designed to be a heat resistant material. One of its characteristics is a near-white color, which makes measling almost impossible to see.

The adhesive which is used to bond the copper material to the surface of the substrate does not show any tendency to break down at solder-wave temperatures. This same adhesive has a marginal ability to withstand soldering-iron-tip temperature. For this reason, rework of any pc-board assembly with a soldering iron should be kept to an absolute minimum. Soldering irons which are used on pc-board assemblies should be the type having controlled tip temperature.

Solderability and Lead Tinning

The Materials Engineering Department was requested to develop a solderability test and specification for printed circuit boards. A progress report from the department indicated that five different types of solderability tests were considered. These included an edge-dip test, a special spread test, a standard spread test, and a minimum-wetting-time test. A fifth test being considered is a solder-leveling process which gives a good indication of the solderability of the pc boards. A report describing these tests and the equipment they required may be found in Appendix A.

Preliminary work consisted of comparing the results obtained from the above mentioned tests. Good correlation between the results from the spread test and the minimum-wetting-time test was found. The material used in the test consisted of pc boards, some of which had been solder leveled to produce a thin, 50-microinch coating.

Solderability results from all five tests were compared and evaluated in an attempt to determine which will best serve as a practical and meaningful solderability test for printed circuits (Refer to the report on solder leveling in Appendix B!) A similar evaluation is being conducted by the Components Engineering group, evaluating the solderability of component leads. It appears that a variation of Military Standard 202 can be adopted.

An ultrasonic solder pot² was loaned to BKC to evaluate the ability of that equipment to tin component leads to BKC requirements without use of flux.

Approximately 250 components (tantalum capacitors, diodes, and resistors) with various lead compositions and exterior coatings were tinned by use of different temperatures and ultrasonic-exposure times. Particular emphasis was placed on testing the tantalum capacitors, since previous tinning of a small quantity indicated a problem with this type of component. All the components were checked for electrical characteristics before and after tinning, with no detrimental effects due to ultrasonics observed. (See Appendix C.)

The component leads were dipped into the solder pot, using a mechanism which controlled the immersion and withdrawal rate at 1 inch per second. The mechanism held the lead in the molten solder for 4 seconds. During the dwell time, the ultrasonic generators were triggered, creating cavitation in the molten solder for a predetermined period of dwell time.

² Redford Corporation, Model 1147

The ultrasonic action was continued during the withdrawal of the lead from the solder pot. The ultrasonic-exposure time shown in the accompanying charts indicates the total time the leads were exposed to ultrasonics. The leads were dipped to within approximately 0.016 inch of the body to simulate actual production requirements.

Ultrasonic generators operating at 27 kHz supplied the power to the horizontally-opposed transducers which produced the cavitation action. The optimum distance between the transducers was 0.250-inch clearance on each side of the material being tinned. To eliminate changing the position of the transducers for each size of lead, they were spaced approximately 0.750-inch apart and the input power was varied as required.

Step switches on the control panels of the generators allowed input power variation from 75 to 100 percent, or approximately 150 to 200 watts per generator. Several different power settings were tried, as indicated by the accompanying charts. The tests attempted to determine the minimum power required to obtain a good tinned coating.

The tinned components were inspected by three different individuals and tinned conditions were rated as acceptable or not acceptable. A 5X magnifier was used to inspect the leads per BKC Specification 9913000. The combined results are shown on the accompanying charts in Appendix C. Further testing of lead solderability indicated that all leads were solderable, even those that had been designated as not acceptable.

To test the solderability of the tinned components, randomly-selected component leads were clipped at the body, bent in a U-shape to check both the body end and the free end of the lead, and soldered into plated-through holes of a special pc board, as sketched below.

Sixty components, or 120 joints, were randomly selected, cross-sectioned, and photographed to check for solder adherence to the component leads. Another 16 component leads were cross-sectioned to measure the tin/lead thickness. A third group of 15 component leads was checked for solderability per MIL-STD 202, Method 208.

Review of the photos indicated good solder adherence and good wettability on most of the component leads. A few of the leads had an oxide interface which was probably due to the thin tin/lead coating. This oxide interface was most prevalent on a gold-plated dumet-type lead. It did not prevent wicking up the lead, and there was no difference noted due to time in the ultrasonics or to the temperature of the solder.

The average tin/lead thickness of the sampled leads was 86.3×10^{-6} inch and varied from 62×10^{-6} to 140×10^{-6} inch. Ultrasonic-time and solder-temperature variation did not establish any significant effect on coating thickness. The coating, however, was thinner on gold plated leads.

Solderability was checked by degreasing the leads of the components in trichloroethylene, dipping in Alpha 100-30 flux, and in 63/37 solder at 460°F for 5 seconds. The solder-coat coverage was then observed. If the coating was continuous, without pits or bumps, and had a bright finish, the lead was considered to have good solderability. All of the leads were considered solderable, but the degree of solderability varied from good to fair.

Judging from the electrical and visual tests, the ultrasonic-solder-pot tinning will give a satisfactory coating even on leads that were previously untinnable; i. e., SA1306. It should also be noted that approximately 9 months elapsed between tinning and the solderability testing. The electrical tests definitely proved that the ultrasonics in the solder pot had no detrimental effects on the electronic functions of the components.

Considering all the aspects of tinning and its associated problems, it is recommended that components with Dumet, Kovar, nickel and other leads that are difficult to solder or tin be pretinned with an ultrasonic solder pot.

Another approach tried by a radio manufacturer was a tinning process using pure tin. The tin coating was applied by an electroplating process. This process was superior to a hot-tin dip, since the thickness of the coating on the lead could be more easily controlled. This company prepared component leads by the electroplating process, placing 300 microinches of 100-percent tin on the leads. For comparison, a similar batch of component leads were hot dipped to provide pure tin coatings of 40, 80 and 100 microinches that were typical of conventional solder-bath processes. Another batch of component leads was prepared with a 300-microinch coating of 60/40 tin/lead alloy applied by electroplating.

The solderability results were as predicted. The highest coverage, 100 percent, was provided by the 300-microinch plating of pure tin. The 60/40 tin/lead alloy coating provided a 95-percent coverage. The solder-bath coating provided substantially less coverage.

The reasons for preferring electroplating over hot dipping as a method of applying a coating is that in the hot-dip process the wire is drawn to size and passed through a bath of molten tin or solder. The resulting coating tends to be nonuniform in thickness as it teardrops around the wire before hardening. Also, there are areas on the wire that come in contact with the mandrels of the coating equipment; these areas may not accept the coating.

In the electroplating process, the wire is drawn to size and through a long bath of plating solution, as in any plating operation. The plating thickness is uniform and can be controlled by the length of time the wire is in the solution and the amount of plating current.

The above-mentioned manufacturer further investigated the advantages of electroplated tin coatings by running two batches of 100 wires each. One batch was obtained from an outside source for which the plating and the plating process were not determined. The other batch was known to be electroplated with pure tin. The defect rate with the electroplated coating was 0.5 percent, while the other batch had a defect rate of 1.6 percent. This manufacturer said that more work needs to be done to determine the cost/effectiveness ratio of heavier electroplated tin coatings on component leads; however, the results to date indicate that this is a satisfactory means of achieving near-zero defects from lack of solderability.

Lead Cleaning and Composition

Cleaning of component leads at BKC is not done at the production assembly level; therefore, it is essential to have good solderable component leads when components are drawn from stores for production assemblies.

Composition of the lead material plays an important role in the solderability of component leads. Components with leads made from Dumet, Kovar, or Alloy 52 have caused soldering problems because of the oxidation of the dissimilar metals used in the leads. Those materials are defined as follows.

Dumet: Nickel/iron core with nickel-flashed and gold-plated copper sheath; or Dumet and steel composition with tin and tin/lead coating.

Kovar: 29 percent nickel, 53-percent iron, and 17-percent cobalt composition with gold plate.

Alloy-52: 52-percent nickel and 48-percent iron composition with gold plate.

Two approaches were taken within this work to provide a component lead suitable for production soldering. One method was a cleaning process involving the use of special cleaning materials (Copper Wet 918 or Metex

M-673), soldering flux only, or after degreasing. Several methods were evaluated using these cleaning materials, from which the following recommendations are made.

- Dumet, gold plated: Clean in Alpha Copper Wet 981, dip in Alpha 611 flux, and dip in 600°F solder pot for 5 seconds.
- Dumet and steel, tin or tin/lead dipped: Clean in Metex M-673 solder stripper, dip in Alpha 611 flux, and dip tin in 600°F solder pot for 5 seconds.
- Kovar, nickel, or Alloy-52, gold plated: Vapor degrease with trichloroethylene or Freon TMC solvent, and tin with Alpha 611 flux and 63/37 solder pot. (The recommended cleaning cycle is a dip in boiling solvent, a rinse with the solvent by use of the degreaser wand, and a final rinse as the components come through the vapor zone.)
- Copper, tin/lead dipped: Tin the leads with Alpha 611 flux and 63/37 solder in a 600°F solder pot. (If desired, the leads may be cleaned in the vapor degreaser before tinning, as described above.)

The following is the recommended procedure when using Copper Wet 918 or Metex M-673 cleaners.

1. a. Vapor degrease components in trichloroethylene or Freon TMC.
 - b. Clean by dipping in 100 percent solution of Copper Wet 918 or Metex M-673 as outlined above for 30 seconds. Agitate parts during cleaning.
 - c. Rinse in cold flowing tap water.
 - d. Rinse in cold demineralized water.
 - e. Alcohol dip and air dry.
2. Tin within 24 hours after cleaning, using the flux and the solder pot temperature previously stated.
3. Solvent clean to remove flux residue.

The recommended solder is a 63/37 composition which is readily available and is widely used. Based on past history, leads treated in the above-mentioned steps and obtaining a good tin/lead coating should be usable six months later.

The second tinning method that was investigated employs an ultrasonic soldering pot. That method is described in detail in the Solderability and Lead Tinning section of this report.

Component Holding and Lead Forming

There are several different methods of holding components in the proper positions on the printed circuit boards until they can be wave soldered. One such method that has been used at BKC employed bee's wax, which was applied with the aid of a mold around the periphery of the boards. Molten bee's wax was poured over and around the components and allowed to solidify, thus holding the parts in predetermined positions. The assembly was then passed over the wave-soldering machine, after which the wax was removed by spraying with hot trichloroethylene. That cleaning process removed the wax satisfactorily, but also removed some of the component and board markings.

Special lead-forming techniques were investigated with some of the basic lead configurations shown in Figure 5. Those lead shapes can be formed by use of a lead-forming machine and suitable dies.

Some of these lead configurations were not satisfactory, since they created problems in spacing component leads too close together. They could be used as alternative methods in designs where component density is not too great.

The most promising means of holding a component appears to be a commercially available metal ferrule. This device is somewhat like an eyelet with three prongs retained inside the lead space. Components leads can be pushed through between these prongs to be the desired height. (See Figure 6.)

The design of the connector actually aids the solder to wick through the board and form the desired fillet on top of the board.

A metal ferrule (Figure 6) which will hold the components vertical and at the proper height was obtained from Berg Electronics, Incorporated. The ferrule which was available for a 0.062-inch-thick board was too long for BKC use. Most of our pc boards are 0.032-inch thick. (The company has since produced a 0.032-inch long ferrule which can be used on our boards. A recent evaluation of this shorter ferrule indicates that it will do a satisfactory job if lands are 0.060 inch or more in diameter.)

Boards 0.023-inch thick were sent to Berg for insertion of the 0.062-inch long ferrules. Wires were inserted in the ferrules and soldered with the wave solder machine. The joints were sectioned and photographed (See Figure 7) to check the solder wicking and adherence. Examination of the photograph shows good results in both categories.

Figure 5. Typical Lead-Form Configurations

Figure 6. Berg Electronics Lead-Gripping PC-Board Eyelet

Figure 7. Metallurgical Cross-Section Through Two Griplet Joints

Experiments were pursued at BKC in an attempt to make a similar gripping device an integral part of the pc board. The board was laminated with half-hard copper sheeting. The copper was etched as shown in Figure 8. It was then formed down into the hole in the board substrate. (Figure 9.) The springy fingers of copper held the component lead very much the same as the commercial connector. The design was turned over to D/822 process engineers to devise a method of incorporating this into pc-board manufacturing. An economically feasible process could not be developed before the end of this project.

Component Insertion

Three basically-different pieces of equipment have been evaluated relative to the insertion of a component in the proper location in the pc board.

The first unit was the most sophisticated and the most highly automated of the three. The machine is tape controlled. It moves the pc board in three axes (X, Y, and θ), to bring the proper holes in position to receive the component. The tape also selects the right component and the correct orientation. When these two operations are complete, the machine inserts the component into the board and then progresses to the next component.

The machine as supplied by the manufacturer will only insert axial-lead components in a lay-down position. It is not known at this time if the machine can be remodeled to insert radial-lead components and transistors.

The second tape unit is more simple and more versatile, but less automated. It consists of a tape-controlled group of component compartments which present the components to the operator one at a time according to a pre-determined sequence. At the same time a light image in the form of an arrow projected on the board surface indicates the proper location and orientation for the component, which is then inserted by the operator.

Both of these units are subject to operator error: the first, during the loading operation of the machine; and the second, during the loading of the component compartments and during the insertion operation. Conversely, a well-informed and alert operator, using the second unit, has the opportunity of checking the identity of each component during the insertion operation.

The third type of unit is similar to the second, except that the location for the component and the check of its identity and orientation is accomplished by the operator, who looks through a split optics viewer at a model board and at the board being assembled. The viewer may present either a side-by-side or a superimposed image. This system requires operator verification of the component, its location, and its orientation. Although existing units of this type are manually controlled, it would be possible to add a programmed

Figure 8. Board Land Laminated With Half-Hard Copper to Provide a Lead-Gripping Feature

Top View Above

Board Cross-Sectional View Below

Figure 9. Experimental PC-Board Lead-Gripping Device

presentation of components coupled to a numerically -controlled indexing of the printed circuit board.

There is little decrease in the time required to insert components in a pc board when one of these three systems is used; however, by restricting the operators field of view or directing his attention to a particular location, a great amount of confusion is eliminated, which avoids tiring the operator and improves his reliability. This is of particular importance on pc-board assemblies which have a large number of components and a high component density.

Fluxing

Several types of flux are available for soldering printed circuit assemblies. The mildest flux is a water-base rosin which can be used if the assembly is clean.

The mildly activated flux, consisting of rosin and a mild cleaning agent such as alcohol, is possibly the most common flux used in electronic assemblies. The alcohol can be driven off by applying a moderate amount of heat. The specific gravity of the flux in liquid form is easily controlled and the residue of the flux remaining after soldering is easily removed. The activated flux has some acid-type cleaner which will cause corrosion problems if it is not thoroughly cleaned and removed from the assembly after soldering.

An evaluation was made of seven fully-activated, seven mildly-activated, and three nonactivated fluxes. (See PDR-197, April, 1970, prepared by W. A. Mulholland, which identifies the characteristics of the flux material, its effectiveness, and its effect on the conductors and solder joints of pc-board assemblies.)

Flux may be applied by several different means such as brush, spray, dipping, wave, and foam. The first two methods give uneven coating and there is a good possibility of missing some of the solder joints completely. The wave type applicator gives an even, relatively-heavy, coating, which causes problems in removing the flux residue after soldering. The most effective type of flux applicator, as determined by this PDO, is a foam fluxer. This system uses air forced through a porous stone or a perforated metal tube submerged in a liquid flux. This action creates bubbles and causes foam which is forced up through a chimney over which the pc-assembly is passed. This foaming action breaks down the flux material into minute particles, which allows easier wicking through the holes and places less flux on the bottom of the board. This allows easier cleaning, or possibly no cleaning if the right type of flux is used. Such a flux applicator had been installed on the wave-soldering machine which was in D/60. It has been used and has produced good results. To ensure a supply of clean air for this unit, an air filter and two air regulators with oil traps were installed in the air supply line just before it enters the fluxer.

A vital ingredient of adequate control of the flux foam is proper air pressure. The normal manifold pressure of 80 to 100 psi is reduced to 5 psi and controlled within 1/4 to 1/2 psi.

The second element of control is the solid content of the liquid-flux mixture. This condition is determined by measuring the specific gravity and adding additional solvent when necessary. The specific gravity ranges from 0.852 to 0.921, depending on the material being used, and it is controlled to ± 0.005 on the same scale.

Adequate ventilation should be provided for the foam fluxer to avoid the collection of fumes.

Fixturing

Fixturing for wave soldering may be of two basically different types. The use of one type or the other is completely arbitrary as far as the wave-soldering equipment is concerned. The type used is best determined by the characteristics of the pc-board assembly.

One type of fixturing holds the level of the board assembly in a rigid relationship to the position of the track. This system usually consists of a platen which is designed to carry a particular board assembly and a carrier which is supported by and is pulled along the track. This carrier is usually designed to carry many different platens. The carrier is adjustable to adapt to different platen sizes, but is not adjustable in the vertical distance from the track support surface to the platen position. (See Figure 10.) Adjustments along the vertical direction are made by changing the level of the top of the solder wave by small amounts (± 0.062 inch).

The other type of fixturing floats the board assembly across the solder wave. The board assembly is attached to the platen by strips of spring metal which allow the board to move freely in a vertical direction. This motion is limited by a positive stop against the bottom surface of the board assembly to prevent it from hitting solid portions of the equipment. This stop also controls the depth of the assembly in the foam-fluxer wave. As the board assembly crosses the solder wave it is free to float on the wave surface. The only things that controls the depth of the bottom surface of the pc board in the solder wave are its weight and the area of board surface contacting the solder wave. The second system is more difficult to design, but it eliminates critical control of the solder-wave height. The parameters of board configuration and assembly weight are fixed; therefore, uniformity is improved.

Interboard wiring is usually located around the periphery of the board assembly to provide easy access when board subassemblies are assembled together. On a rigidly mounted platen, contouring the opening where the

Figure 10. Special-Design Board Carrier for the Flow-Soldering Machine

board is mounted, so that the lands which receive interboard wires are masked from contact with the solder, is relatively simple. When floating-mount fixturing is used, this masking function must be accomplished by some other means. This is usually done by applying a coating of solder-resist material which can be removed later with a solvent.

The angle between the direction of solder flow and the plane of the pc-board surface is critical in obtaining a soldered assembly free of icicles and bridging. The rigid mounting presents a uniform angle at all times. Controlling this angle with the flexible mounting requires an adjustment of the vertical position of the end of the spring-metal strips which are fastened to the platen or carrier.

Machine Setup

The wave-soldering machine which was put to use for this process development project consisted of three sections: the fluxer, the preheater, and the solder pot.

It is possible, although inefficient, to flux assemblies for wave soldering with a brush or spray. Both methods are difficult to control and often result in excess flux or unfluxed spots.

The best consistency is obtained by using a wave or foam fluxer as part of the wave soldering line. The wave soldering machine in D/60 had a wave fluxer at the time process development was started. The pump in this fluxer did not give a steady wave nor a wave with a smooth surface. A foam fluxer was purchased to improve the fluxing consistency and to evaluate the foam type of fluxer.

The foam fluxer required a well-regulated supply of low-pressure clean air. The air pressure needed to be controlled from 4.75 to 5.25 psi. To ensure good control and a supply of clean air, two stages of pressure regulation and an air filter were added between the air manifold and the fluxer unit. To set up the fluxer, the air was turned on for a minimum of 30 minutes to assure a uniform flux mixture throughout the tank. A sample of flux was then drawn from the drain tube and checked for specific gravity. If it was too high, thinner was added until the specific gravity fell within tolerance. The adjustment of specific gravity of the flux had to be performed daily.

The air pressure was set to achieve the proper height of the foam wave which would completely wet the bottom of the board without flooding the top surface with flux. The flux from the bottom of the board and in the space between the component lead and the hole surface was driven up through the hole in sufficient quantity to make a good solder joint between the lead and the land on top of the board.

If the temperature of the surface of the board assembly was too near the solidus temperature of the solder at the moment the solder wave left the board, icicling and bridging occurred. There were two sources of heat available to raise the temperature of the board assembly: the preheater, and the solder pot.

The preheater consisted of a bank of infrared lamps set just below and at each side of the bottom surface of the assembly. The heat was reflected upward at an angle of 45° against the bottom of the board. In some equipment, these lamps have been replaced by a hot plate or heating coils set directly below the bottom of the assembly.

The preheating was controlled by two variable factors: heat energy delivered by two banks of infrared lamps, and the speed at which the assembly was passed over these lamps. The heat energy delivered by the lamps was controlled, each bank separately, by a HI-LO switch and a variac which was scaled in dimensionless units from 0 to 100.

The speed of the assembly passing over the heat lamps was the same as that of the conveyor chain and could be adjusted from less than 1 to over 10 feet per minute. Since the conveyor speed did not change throughout the complete wave-soldering operation, it had to be a compromise of the best speed for all operations performed.

See Figures 11 and 12 for graphs which show the relationship of these factors on the equipment in D/60.

Reasonably, the track speed which controlled the length of time which the assembly was subjected to either heat source, was a factor in the control of the board assembly temperature. A second factor was the temperature of the heat source. The solder wave had temperature control capability to 650°F.

Solder-wave temperatures above 500°F contribute to measling. It has not been proven that measling causes a pc board to be nonfunctional, but it is an indication of having been exposed to high temperature. The material which bonds the copper to the pc-board substrate also may be degraded by high temperature. The obvious alternative to the use of excessive temperatures is to reduce the temperature of the source and increase the time of exposure. The best way to accomplish this is to preheat the boards before soldering. Some manufacturers of wave-soldering equipment suggest a preheat temperature of 180 to 225°F.

Two factors which affect the amount of heat required to achieve a desired conductor temperature are the total area of the conductor surface which is exposed to the heat source and the total area of the pc board.

Figure 11. Test-Pattern Board Temperature Versus Variac Setting and Track Speed for High-Temperature Range Switch Position

Figure 12. Test-Pattern Board Temperature Versus Variac Setting and Track Speed for Low-Temperature Range Switch Position

The variables of solder temperature and track speed are relative to the amount of circuitry per square inch of board surface. It is generally safe to assume that a greater circuit density requires more heat. The general direction of paths in relation to the direction of motion of the pc board across the solder pot is significant also. The conductivity of the copper and tin/lead plating on paths running parallel to the direction of motion carries heat back to the trailing end of the board before it reaches the solder wave. Transverse paths do not act in that manner. At present, there is not a sufficient amount of test data to predict a definite machine setting in advance. Until such predictions are possible, it will be normal procedure to run a few boards through the machine and evaluate the results to determine the necessary settings.

Plating on the path and land surfaces may affect the amount of heat energy required to achieve correct board temperature. Heavy tin/lead plating adds mass which must be heated. If the plating surface is bright, it will reflect more heat energy than a copper surface.

There are two types of solder pots in use on automatic soldering machines. The simpler of the two is a pool of molten solder with controls which hold the temperature of the solder to $\pm 5^{\circ}\text{F}$ of the control setting. This solder pot has an indicator that shows when the solder level in the pot is lowered to a predetermined point. At that time, the addition of one pound of solder will restore the original level. The other type of solder pot is basically the same; however, it incorporates a pump which forces the solder upward between two plates or baffles that are set near the center of the pot. The process that employs a pump and baffle plates is called wave soldering. Several variations in the shape of the solder wave are obtainable with machines from different manufacturers, and some machines are designed to provide different wave shapes on the same machine.

Several different baffle plates were made for trial on the flow-soldering machine in Department 60 to study the effects of different wave configurations. Some of these are shown in Figure 13. The first change was to make the angle of the horizontal portion of the baffles separately and infinitely variable. When the baffle that forms the secondary or leaving wave was sloped downward and away from the center of the wave, icicling and bridging increased. This position decreases the angle between the solder-flow direction and the surface of the board, as shown in Figure 14. As the secondary-wave baffle was elevated, the icicling and bridging condition improved to a point where the baffle position was approximately 7-degrees above horizontal. No improvement was apparent above that baffle position. The angle between the solder-flow direction and the board surface at the point where the solder leaves the board became much larger when the baffle was raised above the horizontal position. Raising the secondary baffle caused an undesirable reduction of the wave depth at the point where the solder spilled over the

Single Wave

Dual Wave

Fixed Interchangeable Curved Baffles

Dual Wave

Fixed Angular Baffles

Dual Wave

Adjustable Baffles

Figure 13. Wave Shapes Produced by Four Different Types of Baffles Which Were Made for the Flow-Soldering Machine

Figure 14. Adjustable Baffles Used to Control the Shape of the Solder Wave

baffle (Figure 15). This adjustment caused the top surface of the combined primary and secondary waves to slope, also. To conform the motion of the board to that slope, the track of the machine was adjusted for a 5-degree upward slope from the horizontal plane. (Figure 16.) That change had no apparent effect on icicling and bridging.

The speed of the pump in the solder pot was advanced to increase the depth of the secondary wave; however, this caused ripples in the surface of the solder wave. Further adjustments revealed that the distance between the baffles, relative to the rate of solder flow, was a determining factor in the formation of ripples. Increasing the rate of flow caused ripples to appear in the solder wave, as shown in Figure 17, and caused the height of the wave to pulse at the frequency of pump revolution. Increasing the distance between the baffles reduced both the rippling and the wave pulsing. This test indicated that a dc motor with good speed control was needed to counteract the effects of line-voltage fluctuations upon the solder-pump output. Some of the later wave-soldering machines now employ that method.

Although the shape of the solder wave, as determined by the baffles and the direction of the solder flow as it leaves the surface of the board, affects the formation of icicles and bridges and excess solder buildup on the paths and lands of the pc boards, each equipment manufacturer employs a different wave shape. One provides different baffle systems to allow the user to select the waveform which he considers best suited for a specific type of product. (Figure 18.) Another manufacturer has designed the aperture and baffles in a manner that allows for infinite adjustment of the wave shape. Two manufacturers use a solder pot with two separate chambers, so that two individually-controlled waves can be produced. This nonuniformity of method indicates a lack of agreement among both users and manufacturers of flow-soldering equipment on the optimum wave shape. Development of flow-soldering methods at BKC has not been sufficient to determine the optimum shape of the solder wave.

The design of the flow-soldering equipment that is now available at BKC does not permit consistent, good results on assemblies with the high component densities that many BKC products require. The possibility of updating this equipment has been considered, but was regarded as too costly in view of the limited results which can be assured. However, the present equipment must be replaced if further advances in flow-soldering are anticipated.

Cleaning

Solder flux is used more liberally than any other material on soldered assemblies. Spray application of trichloroethylene is an effective method of removing that flux. Unfortunately, some component and board markings are removed also. If markings must be retained, it may be necessary to apply some type of protective coating over the marking areas before the components are installed on the boards.

Figure 15. Baffles Adjusted for a Flat-Top Solder Wave

Figure 16. Baffles and Track Adjusted to Increase the Departure Angle of the Solder From the Board

Figure 17. Solder-Wave Ripples Caused by Excessive Flow Rate or Insufficient Distance Between the Baffles.

A. Single Cascade Wave

Solder flow is opposed to the direction of board motion. The effective velocity of the board in relation to the solder is thereby increased, with no decrease in the time of board contact with the solder. The lift at each ridge drives the solder through the plated holes to form fillets that bond the leads to the lands on the top of the board.

B. Flat-Top, Bidirectional Wave

This wave shape is typical of that produced by most flow-soldering machines. Because the wave is flat topped, it provides vertical motion only at the center. The board must travel a little deeper into this wave, as compared to the more-complex wave shapes. Removal of excess solder from the board depends principally upon the break-away or departure angle where the solder breaks away from the board surface.

C. Bidirectional Flat-Top Cascade

This wave shape is a composite of those shown in A and B above. It is basically a bidirectional wave; however, each baffle has a ridge that serves to improve the flow of solder through the holes to the top surface of the board.

Figure 18. Wave Shapes Produced by Three Different Fixed Baffle Systems

Another material which always has to be removed is masking material used to keep certain holes on the pc board from being filled during the flow soldering process. This material can usually be removed by stripping it from the board by pulling. Two factors must be considered in the choice of a strippable coating: the effect of any coating residue on subsequent soldering operations, and the requirement of adhesion of some materials (encapsulation or conformal-coating) to the surface previously covered. Silicones may not greatly inhibit the solderability of the surface, but they usually destroy adhesion between the surface and any other material. In addition, silicone residues are extremely difficult to clean from any surface.

Sometimes it may be necessary to use some form of solder resist during the flow soldering process, and to remove it after soldering. This material will usually withstand temperatures up to 500°F, and it is a tough film which will resist handling damage. Of the materials investigated at BKC, a hot trichloroethylene spray is the usual method recommended for removal. This is even more devastating to unprotected markings than a room-temperature spray. In consideration of this, it may be advisable to coat the bottom of the board only, or to use a material which need not be removed. As is the case with unassembled pc boards, it is preferable to avoid contamination as much as possible. After spray cleaning, the assembly should be kept in a dust-free atmosphere and handled only with clean white nylon gloves when handling cannot be avoided.

Soldering Specification 9913000 has been reviewed, and certain exceptions need to be made to some of its requirements. The suggested changes follow.

- Paragraph 3.2.1.2: Mechanical cleaning of scale and oxides from printed circuit boards may cause a solder overhang at the edge of conductors. This condition can be avoided by a solder leveling process which heats the solder to its melting point by spraying it with hot polyethylene glycol under high pressure. The impingement of the hot polyethylene glycol against the liquid solder removes all but a film covering the conducting surfaces. The thickness of this film can be controlled by the pressure and the time of application. The polyethylene glycol is easily removed by a water rinse, and the boards can be dried by an alcohol rinse and evaporation.
- Paragraph 3.2.1.3 seems to be restricted to the tinning of gold-plated leads when hand soldering is being performed. Tinning of gold-plated leads just prior to any type of soldering would be a good way to determine pin solderability. This would also remove most of the gold in a relatively small quantity of solder, which would be easier to replace than the solder in a flow soldering machine.

- Paragraph 3.2.4.2 refers to repair of flow-soldered joints using a hand soldering iron (one application only). The paragraph should be expanded to allow at least two passes across the solder pot, followed by retouching the joint with a soldering iron if necessary. Because the solder-pot temperature is considerably lower than that of the soldering iron, repeated exposure to the molten solder is not degrading to the adhesive holding the conductor material to the epoxy substrate.
- Paragraph 3.3.1.1 describes ideal solder joints for hand soldering. This presumes a hand-held component with an unclined lead. The appearance of joints described in this paragraph cannot apply if a lead connector is used or if the lead is clinched. Sections 1, 6, 7, and 10, should be revised.
- Paragraph 3.3.2.2.1.b dictates that a clinched lead must be against the path. This is unnecessary, and the 0.125-inch limitation for the clinched lead length is too long. The end of the clinched lead should not extend beyond the periphery of the land. The height of the solder joint should not exceed the maximum allowed for unclined leads.
- Paragraph 4.2.2 requires a black-light test to determine the cleanliness of the assembly. This same test is not required of hand-soldered boards, and there is no reason why flow-soldered assemblies should be presumed to be any dirtier than hand-soldered assemblies.

ACCOMPLISHMENTS

The accomplishments of this project may be divided into three basic categories:

- Evaluation of existing procedures and materials and their relationships to the flow-soldering process;
- Adaptation of existing procedures and materials to flow-soldering requirements;
- Establishment of flow-soldering procedures and supporting techniques which were not used at BKC prior to this work; and
- Assimilation of knowledge and development of processes necessary to establish flow-soldering as a production process at BKC.

The supporting activities included development of the following capabilities:

- Methods of cleaning and storage to ensure solderability;
- Principles of pc-board design which should be exercised in board layout and preparation of circuit masters;
- Effective methods of securing components to pc-boards for flow soldering;
- Establishment of guidelines for setup and operation of flow-soldering machines; and
- Use of ultrasonic agitation in lead-tinning to promote solderability and avoid the use of excessive flux.

FUTURE WORK

Having accomplished the objectives outlined above and described in this report, no additional work is planned for the immediate future.

If a decision is made to update or replace the present flow-soldering machines, further work may be necessary to prove in the machines for scheduled production use.

Appendix A

PRINTED WIRING BOARD SOLDERABILITY TESTS

**Excerpted From an Internal Memorandum Report
From B. T. Lampe, D/862 To H. M. Garrison, D/845
June 16, 1970**

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Appendix A

PRINTED WIRING BOARD SOLDERABILITY

INTRODUCTION

A reliable soldering process depends to a large extent on the solderability of the printed wiring board. Solderability is a measure of the ease by which molten solder will wet the conductors on the board. It is important that the printed wiring board have good initial solderability, and that it retain good solderability during storage. A practical test for quantitative measurement of the solderability of printed wiring boards has been needed for a long time. The purpose of this study was to develop a test procedure that would provide a simple and meaningful test for solderability. The study was limited to tin/lead plated printed wiring boards, which is the type most commonly used at BKC.

INVESTIGATION

A good solderability test must give an indication of the solderability of the board after storage, preferably without destroying the board. The test should measure the solderability of both the conductor paths and the plated-through holes. A literature survey was made to determine what work had been done in the area of solderability testing of printed wiring boards. The literature search turned up several tests that had sufficient merit to warrant further investigation. Several of the tests had been used at BKC in the past for other solderability studies. These tests were evaluated for possible application on printed wiring boards.

Edge-Dip Test

This test is probably the most accepted solderability test in the electronic industry today. It can be used for printed wiring boards and component leads. The test procedure is defined by Electronic Industries Association Test Standard RS-178-A¹, by MIL STD 202D, Method 208², and by IPC Test Standard IPC-S-801³. This test is simply a dip test where the part is immersed into a solder pot under controlled conditions and the solderability is determined by visual inspection. The dwell time in the solder, the immersion rate, and the withdrawal rate is controlled through the use of a cam operated dipping device shown in Figure A-1. A rosin-base flux is used and the temperature of the solder is closely controlled. The criteria for acceptable solderability according to this test method is a minimum of 95-percent coverage of the surface being tested by the molten solder. The balance of surface may contain small pin holes, dewetted areas, rough spots, or uncoated base metal, provided such defects are not concentrated in one area.

Figure A-1. Edge-Dip Solderability Tester

A tester similar to that shown in Figure A-1 was built and evaluated for solderability-testing of printed wiring boards. It proved to be a very simple and meaningful test for solderability. However, it does not provide a quantitative measure of solderability, and a visual interpretation of the results is required. In order to be used as a production or inspection test, visual standards are almost a necessity. The test acceptance criteria, as specified by the above standards, are very easy to meet with the quality of tin/lead plated boards used at BKC. For use at BKC, these criteria should be tightened to allow no virtual defects and require 100 percent coverage when viewed at 10X magnification. This would put it in line with BKC accepted quality standards.

The edge-dip solderability test can be either a nondestructive or a destructive test. By dipping only the edge of the printed wiring board into the solder pot, the test board can be salvaged and used later on. More meaningful results can be obtained, however, by cutting up the board and testing a number of the pieces. This test does not provide a good solderability test for plated-through holes.

Solderability-Spread Test

The solderability spread test measures the ability of liquid solder to spread out over a surface. The greater the spread for a given amount of solder the better the wetting, and correspondingly, the better the solderability.

Passel⁴ modified the spread test to give a spread factor which is relatively independent of the quantity of solder. The numerical value of the spread factor can be correlated to solderability. The procedure used in this test is outlined in Appendix B.

Figure A-2 shows a sketch of the solderability spread tester that BKC has used for several years for solderability testing. It has proved to be a very valuable test because it assigns a numerical value to solderability. However, this test is not well suited for printed wiring boards because the insulating epoxy between conductor paths on the boards restricts the flow of the solder. This test is more suited for evaluating the solderability of various base materials or coatings.

Fabish⁵ designed a solderability spread test specifically for printed wiring boards. An apparatus similar to his was built (Figure A-3) and evaluated. In this test, the pwb is placed down on the test fixture (face down) and lowered onto the surface of the molten solder in a solder pot. The solder rises through the holes in the plate and wets the conductors of the board. The area of spread is taken as a measure of solderability. Different-size test fixtures are used for different-size boards.

Figure A-2. BKC Solderability Spread Tester

Figure A-3. Fabish⁵ Solderability Spread Tester

That test proved to be unsatisfactory for a number of reasons. First, it was limited to boards with simple designs and long, wide conductor paths. Secondly, there could be no warpage of the board, because the board had to lay perfectly flat on the test fixture. The test required considerable skill to perform and the results obtained from the test are not very consistent. It is not applicable to plated-through holes.

Minimum-Wetting-Time Test

Unlike the spread test, which is a static test, the minimum-wetting-time test is a dynamic test which measures the time it takes for the solder to wet the sample. The rate of wetting is taken as the measure of solderability. A sketch of the minimum wetting time tester is shown in Figure A-4. The original apparatus was developed by Thwaites^{6, 7} We have used this test with good success in a number of solderability studies. It is a rather simple test and probably the most sensitive of all the solderability tests. Although usually a destructive test, it can be used to test the solderability of plated-through holes as well as conductor paths.

Solder-Globule Test

This solderability test was developed by Tenduis and later modified by Wade and Brown⁸ for determining the solderability of lead wires. It measures the time necessary for a globule of liquid solder to wet around the circumference of a lead wire. It provides a numerical evaluation (wetting time) of solderability. This test works well for printed-wiring-board components, but does not show much promise as a solderability test for the board itself. A modification of this type of test may prove to be useful in evaluating the solderability of plated-through holes.

Solder Leveling

Solder leveling is a recently developed process whereby the tin/lead coating on the printed wiring board is melted and the excess is removed under pressure, producing a smooth, thin coating on the board, 40 to 80 micro-inches in thickness. All excess solder on the conductor paths and in the holes is removed. The process is carried out at approximately 425°F in a neutral, oil-base solution. Since this process melts and reflows the tin/lead, it produces an effect similar to that of actual soldering. Any solderability problems with the board are brought out by the solder-leveling process in the form of nonwetting, or dewetting, of the solder coating. It also provides a check on the composition of the tin/lead coating. A high-lead coating will not be completely melted and removed by this process because of its high melting point. Lead-rich globules will remain on the board after leveling. High-lead (60 percent +) content coatings have a much shorter shelf life than the standard 60 Sn/40 Pb coatings, and can cause solderability problems.

Figure A-4. BKC Minimum Wetting Time Tester

The solder-leveling process provides a solderability test that comes closer to duplicating actual soldering than any of the other tests. Studies (see Appendix B) are underway to further evaluate the solder-leveling process as a potential fabrication process for printed wiring boards.

RESULTS AND CONCLUSIONS

The results of the investigation to develop a simple and meaningful solderability test for tin/lead-coated printed wiring boards is summarized in Table A-1. The results are not too satisfying. No one test or combination of tests will provide a reliable measure of the overall solderability of the printed wiring board. The solderability of both the conductor paths and the plated-through holes has to be measured. The solderability depends upon the solderability of the tin/lead, as well as the base metal (copper). The test should, as nearly as possible, duplicate the actual soldering operation. None of the tests evaluated in this study really did that.

Table A-1. Solderability Tests for Printed Wiring Boards

Solderability Test	Applicable to PWB		Destructive or Nondestructive	Test Results	Comments
	Paths	Holes			
Edge-Dip Test	Yes	Yes	Nondestructive	Visual	Simple test, good for production use, meaningful results.
Spread Test (Standard)	Yes	No	Destructive	Numerical	Unpractical for PWB's
Fabish Spread Test	Yes	No	Destructive	Numerical	PWB must be of simple design, difficult to use.
Minimum-Wetting-Time Test	Yes	Yes	Destructive	Numerical	Sensitive to slight changes in solderability. Elaborate equipment required.
Solder-Globule Test	No	Yes	Destructive	Numerical	Not practical for PWB's
Solder Leveling	Yes	Yes	Nondestructive	Visual	Best potential of all tests; should be investigated further.

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Appendix B

SOLDERABILITY PRODUCED BY SOLDER LEVELING

Excerpted From a Special Report by B. T. Lampe
July 8, 1969

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Appendix B

SOLDERABILITY PRODUCED BY SOLDER LEVELING

INTRODUCTION

The conductors of printed circuit boards are normally coated with tin/lead to enhance solderability. This coating is applied by electroplating or hot-solder dipping. Most of the printed circuits produced at BKC are coated with electroplated tin/lead. Two of the greatest difficulties with tin/lead plating of printed circuits are the control of the tin/lead plating composition and the control of the plating thickness in plated-through holes. Solder dipping offers the advantages of simplicity, good composition control, and enhanced solderability, but thickness control of the coating is a major problem. Solder leveling is a process whereby the tin/lead coating (electroplated or solder-dipped) is melted and the excess is removed from the printed circuit board under pressure, leaving a smooth coating 40 to 80 microinches thick. The heating solution is neutral in pH and is easy to remove after leveling. Solder leveling offers the advantages of producing a level, fused coating, both in the holes and on the circuit paths. It eliminates tin/lead overhang and permits tighter tolerances on the finished printed circuit board. In addition, it provides its own built-in solderability test. Any solderability problems with the printed circuit boards are brought out by the solder leveling process in the form of non-wetting and dewetting of the solder coating. A practical and meaningful solderability test for printed wiring boards has been needed for a long time, and solder leveling appears to offer an effective means of satisfying that need.

Since the tin/lead coating produced by the solder-leveling process is very thin (40 to 80 microinches), it does not offer the oxidation protection of the standard tin/lead coatings of 0.0003 to 0.0009 inch thickness. The purpose of this project was to evaluate the long-term solderability of solder-leveled printed circuit boards under various storage and packaging conditions. Solder-leveled boards tested during this evaluation retained a solderability spread factor rating of more than 80 percent after aging for 9 months.

PROCEDURE

Three types of test panels were used. These 5- by 6-inch panels were plated with tin/lead to a thickness of approximately 1/2 mil and sent to the Cimron Division of Lear Siegler, Inc. in San Diego, California, to be solder leveled in their machine known as the Hydro-Squeegee. Some of the plain panels were hot tin/lead dipped in 63/37 solder prior to leveling.

Three different solderability tests were used. The apparatus used in these tests is shown in Appendix A, Figure A-2. In this test, predetermined quantities of solder and flux are placed on the test coupon (1-1/2 inch dia disc) held by a Teflon support ring. The test coupon is heated to a given temperature above the melting point of the solder and held at that temperature for a given time. The area of the coupon over which the solder spreads can be used as a measure of the solderability; however, a more meaningful parameter is the solderability spread factor, which is independent of the spread area and directly related to the height of the resulting solder spread. It is calculated from the following formula:

$$\text{Spread Factor (Percent)} = \frac{D-H}{D} \times 100,$$

where

D = Diameter of hypothetical sphere having a mass equivalent to that of the standard solder preform and

H = Maximum height of the solder on the test coupon.

The spread-test conditions were as follows.

Test Temperature: $480 \pm 10^{\circ}\text{F}$

Flux: Nonactivated rosin (Alpha 100-30)

Solder: 20 mm³ preforms of 63/37 tin/lead

Time: 5 seconds after start of melting

In this test, the solder preform is melted and allowed to spread on top of the test specimen for 5 seconds. The heat source (solder bath) is then removed and the specimen is allowed to cool. The area of spread is measured with a planimeter, and the height of the solder is measured with a depth gage. Spread factors are determined from the solder heights.

The magnitude of the spread factor is a measure of the solderability of the material being tested. The following scale is generally considered standard for solderability tests.

<u>Spread Factor</u>	<u>Solderability</u>
Up to 60	Very Poor
60 to 70	Poor to Fair
70 to 80	Fair to Good
80 to 90	Good to Very Good
90 and Over	Excellent

The second type of solderability test used in this investigation was the minimum-wetting-time test. This test measures the minimum time necessary for the solder to wet the test specimen. Unlike the spread test, this test measures the rate of wetting. A sketch of the apparatus used is shown in Appendix A. In this test, the specimen is fluxed, placed in the holding clamp, and allowed to pass through the molten-solder bath at a controlled speed. When the specimen enters the solder bath, a timer is activated. It is automatically shut off as the specimen leaves the solder bath. The total time in the bath is measured by the timer and controlled by the speed of the motor. The time in the bath is increased in controlled steps until total wetting is achieved. The minimum time it takes to achieve complete wetting is taken as the minimum wetting time.

The test conditions of the minimum wetting time test were as follows.

Test Temperature: $480 \pm 10^{\circ}\text{F}$ (Solder bath temperature)

Flux: Alpha 100-30 (Nonactivated)

Solder: Solder bath of 63/37 tin/lead composition

The third type of solderability test used on this investigation was a simple solder-dip test defined by MIL-STD-202C, Method 208A. In this test, the specimen is clamped in a mechanical dipping device, dipped into a solder bath at a controlled rate, held for a specified time, and withdrawn at a controlled rate. The specimens are then examined at 10X magnification for completeness of wetting. Solder defects such as pinholes, dewetting, and nonwetting are noted. The test conditions were as follows.

Test Temperature: $480 \pm 10^{\circ}\text{F}$

Solder Bath: 63/37 tin/lead

Dwell Time in Bath: 4 seconds

Flux: Nonactivated rosin (Alpha 100-30)

The test panels were received approximately 7 days after solder leveling. Another 7 days were required to fabricate the panels into test specimens. As a result, it was approximately 14 days before any of the panels were coated or tested for solderability. Prior to coating or testing, the specimens were degreased in trichlorethene. Aging of some of the test specimens was accelerated in a humidity chamber at 100°F and 95 percent relative humidity for 10 days prior to solderability testing. The remainder of the test specimens were natural aged for 9 months in unsealed plastic bags. Some of the parts were coated with a rosin-base protective coating (Alpha Protectocoat 828-10) before aging. A previous evaluation of various types

of rosin-base coatings showed them to be effective in preserving the solderability of copper and solder-coated copper surfaces.

The results of the solderability tests shown in Tables B-1 through B-4 represent the average value of four samples for each test.

DISCUSSION AND RESULTS

Two groups of the tin/lead plated panels exhibited a rough surface finish after solder leveling. There were many pimples on the surface which appeared to be inclusions in the tin/lead coating. The supplier pointed out that this condition indicated an imbalance in the plating bath. Some of the original plated panels were then checked for tin/lead composition and found to have approximately a 45-percent tin/55-percent lead coating, rather than the expected 60-percent tin/40-percent lead. The inclusions were found to be lead-rich areas, the melting point of which exceeded the temperature of the solder-leveling solution; therefore, those areas were not fully melted during the process. Composition control is one of the major problems associated with tin/lead-alloy plating and the solder-leveling process proved to be a good test for the plating composition. The other groups of panels did not exhibit this condition after leveling. The plating on these panels was analyzed and found to be approximately 60/40-tin/lead.

The solderability test data for the tin/lead-plated panels that were not solder dipped prior to solder leveling is shown in Table B-1. Although the original plating was high in lead content (approximately 55 percent), it is assumed that the resulting tin/lead coating after solder dipping was approximately 60/40, since these panels did not exhibit the rough surface texture of the high-lead panels that were not solder dipped.

It is apparent from the test data shown in Tables B-1 through B-3 that there is a measurable loss in solderability after solder leveling. In Table B-1 it can be seen that the solderability spread factor of the solder-leveled panel was approximately 9-percent lower than the as-plated panel after two weeks natural aging. The solderability spread factor of the uncoated solder-leveled panel decreased to 81.1 percent after 9 months natural aging, as compared to a decrease of only 0.9 percent for the as-plated panel. The rosin-base coating appears to be effective in reducing the loss of solderability in solder-leveled samples. The spread factor for the coated samples decreased only 3.7 percent during the 9 months natural aging, as compared to a 8.3-percent decrease for the uncoated samples. The minimum wetting times were all less than 0.15 seconds for the as-plated samples before and after aging, while the solder leveled samples had minimum wetting times ranging from 0.23 to 0.25 seconds. The solderability of the samples, as determined by the MIL-STD-202C dip test ranged from excellent for the

Table B-1. Solderability of Tin/Lead-Dipped Panels After Solder Leveling

Sample	Aging	Spread Area (In ²)	Spread Factor (percent)	Minimum Wetting (seconds)	Dip Test Solderability Rating
1. As Plated, 1/2 mil	Natural, 2 wks	0.455	98.1	0.15*	Excellent
2. As Plated, 1/2 mil	Natural, 9 mo	0.432	97.2	0.15*	Excellent
3. Leveled, Uncoated	Natural, 2 wks	0.130	89.4	0.23	Good
4. Leveled, Uncoated	Accelerated, 10 da.	0.101	86.9	0.25	Fair
5. Leveled, Coated	Accelerated, 10 da.	0.118	86.7	0.25	Good
6. Leveled, Uncoated	Natural, 9 mo.	0.076	81.1	0.25	Good
7. Leveled, Coated	Natural, 9 mo.	0.078	85.7	0.25	Good
*0.15 seconds represents the lower measuring limit of the minimum-wetting-time apparatus.					

Table B-2. Solderability of Tin/Lead Plated* Panels After Solder Leveling

Sample	Aging	Spread Area (In ²)	Spread Factor (percent)	Minimum Wetting (seconds)	Dip Test Solderability Rating
1. As Plated*, 1/2 mil	Natural, 2 wks	0.455	98.1	<0.15	Excellent
2. As Plated, 1/2 mil	Natural, 9 mo	0.432	97.2	<0.15	Excellent
3. Leveled, Unccated	Natural, 2 wks	0.127	89.5	0.22	Good
4. Leveled, Unccated	Accelerated 10 da.	0.077	80.7	0.23	Good
5. Leveled, Coated	Accelerated 10 da.	0.092	83.8	0.24	Good
6. Leveled, Uncoated	Natural, 9 mo.	0.082	83.8	0.24	Good
7. Leveled, Coated	Natural, 9 mo.	0.132	88.6	0.22	Good
*Tin/lead plating composition: 45-percent tin/55-percent lead					

Table B-3. Solderability of Tin/Lead Plated* Printed Circuit Board Specimens After Solder Leveling

Sample	Aging	Spread Area (In ²)	Spread Factor (percent)	Minimum Wetting (seconds)	Dip Test Solderability Rating
1. As Plated*, 1/2 mil	Natural, 2 wks	0.123	86.8	<0.15	Good
2. As Plated, 1/2 mil	Natural, 9 mo	0.128	80.2	<0.15	Good
3. Plated & Fused	Natural, 2 wks	0.246	92.8	<0.15	Good
4. Plated & Fused	Natural, 9 mo	0.151	81.2	<0.15	Good
5. Leveled, Uncoated	Accelerated, 10 da	0.043	61.5	0.20	Poor
6. Leveled, Coated	Accelerated 10 da	0.043	68.3	0.17	Marginal
7. Leveled, Uncoated	Natural, 9 mo	0.027	57.9	0.33	Poor
8. Leveled, Coated	Natural, 9 mo	0.049	66.8	0.20	Marginal
*Tin/lead plating composition: 45-percent tin/55-percent lead					

as-plated samples to only fair and good for the solder-leveled samples. However, all of the solder-leveled samples would have passed the requirements of MIL-STD-202C, i. e., 95-percent coverage, by the new solder coating and no voids exceeding 0.005 inch in diameter. All of the solder-leveled samples exhibited some pitting which appeared to be very small nonwetted areas in the coating.

Table B-2 represents the solderability test data for the plated panels that were not hot-solder dipped prior to leveling. The initial loss in solderability for the high-lead panels was about the same as that for the other panels, except that the loss in solderability during accelerated aging was greater. The rosin-base coating again appeared to be effective in reducing loss of solderability during aging. The data for the as-plated samples used in Table B-1 was used again in Table B-2 as a comparison to the solderability of the solder-leveled samples.

The tin/lead composition of the coating on the as-plated panels was approximately 45-percent tin/55-percent lead. The minimum wetting times and dip-test solderabilities were about the same for these samples as they were for solder-dipped samples, with the solder-dipped samples exhibiting more pitting.

Table B-3 represents the solderability test data from the pc-board samples. In this series of tests, the solderability of the solder-leveled samples can be compared to both as-plated and fused samples. The solderability-spread factor appears to have been suppressed by about 10 percent because of the configuration of the test specimen, since the highest value recorded was only 92.8 percent (plated and fused, 2-week aging). These panels were similar to actual printed circuit boards where the conductor paths are insulated from one another. The flow of the molten solder is restricted by the insulating epoxy, resulting in reduced spread areas and smaller solderability factors. The other solderability tests are not so affected.

The spread factor for the uncoated samples decreased to 57.9 percent after natural aging for 9 months, and to 61.5 percent after 10 days of accelerated aging. The coated samples were better, as usual, but still showed a measurable loss of solderability. The minimum-wetting-time and dip-test results for these samples were worse than the others. Pitting was more pronounced, and most of the uncoated, solder-leveled samples would not have passed the requirements of MIL-STD-202C for acceptable solderability. The as-plated and fused, tin/lead-coated samples also showed a loss of solderability during aging, which was probably a result of high-lead content (55 percent) of the coating.

Table B-4 represents the solderability test data from the third type of panel used in this investigation. This panel was similar to the pc-board panel,

Table B-4. Solderability of Tin/Lead Plated* Unetched Printed Circuit Board Pattern Solder Leveling

Sample	Aging	Spread Area (in ²)	Spread Factor (percent)	Minimum Wetting (seconds)	Dip Test Solderability Rating
1. As Plated*, 1/2 mil	Natural, 2 wks	0.314	94.3	< 0.15	Excellent
2. Leveled, Uncoated	Accelerated, 10 da	0.078	80.6	Not Tested	Good
3. Leveled, Coated	Accelerated, 10 da	0.092	83.8	Not Tested	Good
4. Leveled, Uncoated	Natural, 9 mo	0.076	79.1	Not Tested	Good
5. Leveled, Coated	Natural, 9 mo	0.104	84.8	Not Tested	Good
*Tin/lead plating composition: 60-percent tin/40-percent lead					

except that the copper was not removed from between the tin/lead-plated conductor paths. This allowed the solder to flow more freely between the paths during the spread tests, which probably accounts for the larger spread factors for the solder-leveled samples after aging. However, the bare copper became somewhat passivated by the solder-leveling process, and did not wet as well as might be expected. The nonactivated rosin flux was not strong enough to break down this passivation and allow the molten solder to flow freely between the tin/lead-coated conductor paths. The results however, are comparable to those obtained with the plain tin/lead-coated panels after solder leveling. The dip-test results from these samples were a little better than from the other solder-leveled samples, but pitting was still evident. The composition of the original plating on these panels was approximately 60/40, tin/lead.

CONCLUSIONS AND RECOMMENDATIONS

Four groups of tin/lead-plated panels were solder leveled to produce a fused coating of 40 to 60 microinches and tested for long-term solderability under natural and accelerated storage conditions. When compared to unleveled tin/lead plated boards, the tests of the leveled boards indicated a measureable loss of solderability. The solderability spread factor proved to be the most sensitive indicator of solderability in these tests. The results from the minimum-wetting-time tests and the MIL-STD-202C dip tests substantiated the results from the spread tests, although they were not as conclusive.

The results from the spread tests showed that the solderability spread factor of the solder-leveled panels and decreased approximately 10 percent within two weeks after leveling when compared to a normal as-plated panel. An additional 6 to 9 percent decrease in the spread factor was observed after 9-month storage. The pc-board panels (Table B-3) showed an even larger total decrease in spread factor (approximately 29 percent.) The rosin-base coating proved to be partially effective in preventing the loss in solderability, which was reduced by more than 50 percent by the protective coating. The solderability of the leveled boards did not appear to be affected by the high-lead content of the original tin/lead coating, because the results from the hot-solder dipped samples were not significantly different from the results from the same boards that were not solder dipped prior to leveling.

The results indicate that the greatest loss of solderability with the solder-leveled boards occurs within two weeks after leveling. The additional loss in solderability that occurs with an additional 9-month storage is approximately the same as the loss that occurs within the first two weeks. Apparently, the thin, fused-tin/lead coating or tin/lead/copper-alloy surface oxidizes very rapidly, and behaves like a normal oxide coating in retarding further oxidation. This oxidation may even take place during

the solder-leveling process before it comes in contact with the open atmosphere. How effective the rosin-base coating would be in preventing the initial loss in solderability is another question that needs to be answered. Even with the measurable loss in solderability during storage, the solder-leveled boards would still merit at least a fair-to-good solderability rating, based on the accepted rating scale of spread factors listed earlier in this report. This is about two levels below the excellent-solderability rating merited by the as-plated boards. However, the use of a more activated flux might raise that rating substantially.

This investigation was not designed to be an all-conclusive study of solder leveling and the solderability of thin, fused-tin/lead coatings. Instead, it was designed to study the feasibility of the solder-leveling process for producing solderable printed circuit boards. Based on the results of this investigation, the following conclusions were supported.

- A measurable loss in solderability occurs when solder-leveled boards are exposed to normal storage conditions; however, the boards remain solderable after nine months of normal storage.
- A rosin-base coating is effective in reducing the loss of solderability of solder-leveled boards during storage.
- The solder-leveling process shows promise as a practical and meaningful solderability test for printed circuit boards.
- The biggest loss in solderability with solder-leveled boards occurs within the first two weeks after leveling.

Some important questions remain to be answered before solder leveling can be accepted as a manufacturing process for printed circuit boards. Some of these are as follows.

- How is the solderability of plated-through holes affected by this process? The thickness of the coating at the edge of a hole would probably be less than that on the conductor path.
- How effective would the rosin-base coating be in preserving solderability if applied immediately after solder leveling?
- Is the pitting condition observed on all of the solder-leveled samples used in this investigation characteristic of the process, or is it a result of the original coating or base material?
- Can solder leveling be successfully integrated into the normal productive process of printed circuits? At what point in the overall manufacturing process would it be best to solder level the printed circuit board--

before or after storage? It might be possible to entirely eliminate tin/lead plating of pc-boards by panel-plating the board with copper, followed by a hot-solder dip and solder leveling just prior to assembly. Most solderability problems with printed circuit boards are associated in some way with tin/lead plating. If hot-solder dipping followed by solder leveling would enable pc-board plating to be eliminated, a significant cost savings could be realized. In addition, it would be possible to produce boards with much tighter tolerances.

A more extensive investigation of solder leveling is needed before the above questions can be fully answered. We plan to make a more extensive study of this process in the very near future if a solder leveling machine can be acquired. Solder leveling appears to have potential application at Bendix in the fabrication of printed circuit boards. The small loss in solderability created by solder leveling does not reduce the solderability of the boards below an acceptable level for a good product. Use of 60/40 or 63/37 tin/lead solder and application of a protective coating to the boards immediately after solder leveling is an effective means of retaining solderability during long periods of storage.

Appendix C

PRETINNING IN AN ULTRASONICALLY-AGITATED SOLDER POT

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Appendix C

PRETINNING IN AN ULTRASONICALLY-AGITATED SOLDER POT

The results of pretinning the leads of some of the components listed in Table C-1 in an ultrasonically-agitated solder pot are shown in Tables C-2 through C-6.

Representative samples were chosen for metallurgical cross-sectioning for visual examination, and some were photographed at approximately 25-times magnification for closer inspection (Figures C-1 through C-5). Other samples were chosen for tin/lead-thickness measurements, and others were subjected to solderability tests. The samples selected are identified in the tables.

Some of the heading definitions, terms, and notes used to conserve space in the tables are listed below. Those that are not listed are self explanatory.

TABLE HEADINGS AND NOTES

Generator Setting

Power control setting of the ultrasonic generator (relative)

Ultrasonic Time

Time of lead exposure to ultrasonic cavitation (seconds)

Tinned-Surface Condition

A: Surface acceptable by visual inspection

NA: Surface not acceptable by visual inspection

Positive Symbol (+): Positive lead of polarized components; also used to identify one end of nonpolarized components

Negative Symbol (-): Negative end of polarized components, or opposite end of nonpolarized components

Remarks

- Notes: (1) Cross-sectioned (Figure No. shown, if photographed)
(2) Measured for tin/lead thickness
(3) Fair solderability
(4) Good solderability
(5) Poor solderability

Table C-1. Product Tabulation

SA No.	*	Part No.	Product Spec No.	Lead Composition
659-163	R	357325-00	352092	Dumet Type-D, MIL STD 1276
659-405	R	312868-00	352092	Dumet Type-D, MIL STD 1276
862-29	C	357486-00	353872	Nickel anode, hot tin-dipped cathode, electroplated
862-39	C	358591-00		Alloy-52, MIL STD 7390820 Au plated
862-55	C	359358-00	353872	Alloy-52 anode, nickel cathode, Au plated
862-57	C	359360-00	353872	Nickel or Alloy-52, Au plated
862-59	C	359362-00	353872	Nickel, Au plated
863-21	C	357497-00	353875	Nonferrous metal, hot-tinned, or solder-dipped
866-43	C	359627-00	353878	
866-44	C	359628-00	353878	
866-45	C	359629-00	353878	
866-47	C	359653-00	353878	60% steel, 40% copper, tin-plated
866-49	C	359654-00	353878	
866-50	C	312769-00	353878	
866-51	C	312897-00	353878	
894-139	C	359663-00	354095	Steel, copper-clad and solder-coat
1181	D	355479-00	355479	Dumet, tin-plated
1229-481	R	359719-00	356223	Dumet Type-D, MIL STD 1276
1229-491	R	359794-00	356223	Dumet Type-D, MIL STD 1276
1229-581	R	312873-00	356223	Dumet Type-D, MIL STD 1276
1245	D	356276-00	356276	Dumet, gold or tin plated
1726	T	359401-00		Kovar, Au-plate, 100 ± 50 micro-inch
1729	T	359404-00	359404	Kovar, Au-plate
1745	D	359435-00	359435	Dumet, tin-plate
1749	D	359452-00	359452	Dumet, nickel flash, Au plate
1847	IC	359940-00	359940	Kovar, Au 150 to 250 microinches
1857	D	359966-00	359966	Dumet, tin-plate
1859	D	356480-00	356480	Dumet, 60 microinch nickel and 60 microinch Au plate
1860	D	359969-00	359969	Dumet, tin-plate
MC2350	L	312434-00		
Alloy-52: 52% nickel/48% iron Kovar: 29% nickel/17% cobalt/53% iron				*Component Type R - Resistor C - Capacitor T - Transistor D - Diode IC - Integrated Circuit

Table C-2. SA1306 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Minutes)	Tinned-Surface Condition (See Notes)	Remarks (See Notes)
2	450	5	5	-A +A	(1) (1)
13			4	-A +NA	
40			5	-A +NA	
35			4	-A +NA	
11			3	-A +NA	
32			3	-A +NA	
5			5	-A +A	(2)
16			5	-A +A	
9			3	-A +A	
31			4	-A +A	
38			5	-A +NA	(1) Fig. C-1 (1) Fig. C-1
6			5	-A +NA	
7			3	-NA +NA	(1) (1)
1			3	-NA +NA	
41			5	-A +A	(1) (1)
21			4	-A +NA	
28			5	-A +A	(3) (3)
19			5	-A +A	
10	450	5	4	-A +NA	

*Table Notes are listed on the preceding page.

Table C-2 Continued. SA1306 Tests

Sample No.	Solder Temp. (°F)	Generator Setting	Ultrasonic Time (Minutes)	Tinned-Surface Condition (See Notes)	Remarks (See Notes)
18	450	4	3	-A	(1)
				+A	(1)
30		3	2	-A	
				+NA	
26		4	3	-A	
				+NA	
23		3	2	-A	(1) Fig. C-2
				+NA	(1) Fig. C-2
32		3	2	-A	
				+NA	
42		3	2	-A	
				+NA	
24		4	3	-A	(2)
				+NA	(2)
4		3	2	-A	(1)
				+A	(1)
34		4	3	-A	
				+NA	
8		3	2	-A	
				+NA	
33		4	3	-A	
				+NA	
20	450	4	3	-A	
				+A	
3	450	5	5	-A	(1)
				+A	(1)
12	450	5	5	-A	(1)
	520			+A	(1)
37	450	5	5	-A	
				+NA	
15	450	5	5	-A	(2)
	520			+NA	(2)
39	450	5	5	-A	
	520			+NA	
14	450	5	5	-A	(2)
	520			+A	(2))
27	450	5	5	-A	
	450			+NA	
22	450	5	5	-A	
	520			+NA	
25/29	450	5	5	-A	(3)
	450			+A	(3)

Table C-3. SA1181 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
34	480	5	4	-A	(1)
2				+A	(1)
15				-A	(2)
36				+A	(2)
4				-A	(1)
12	480			+A	(1)
38	530			-A	
11				+A	
27				-A	(2)
21				+A	(2)
16				-A	
43				+A	
8				-A	(1)
40				+NA	(1)
3				-A	(1)
44			4	+A	(1)
1			3	-A	
9				+A	
41				-A	
22				+A	
	530	5	3	-A	
				+A	

Table C-3 Continued. SA1181 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
17	450	3	2	-A	
46				+A	(1)
24				-A	(1)
32				+A	(1)
20				-A	(2)
13		3		+A	(2)
28		4		-A	
39				+A	
31				-A	
14				+A	
0		4	2	-A	
7		5	4	+A	
47				-A	(1)
33				+A	(1)
25				-A	
42	450	5	4	+A	(1) Fig. C-3
6	480	3	3	-A	(1) Fig. C-3
19				+A	
29				-A	(1)
48				+A	(1)
				-NA	(1) Fig. C-4
				+A	(1) Fig. C-4
				-NA	(4)
	480	3	3	+A	(3)

Table C-3 Continued. SA1181 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
30	600	5	3	-A	
				+A	
35				-A	
				+A	
49				-A	(1)
				+A	(1)
26				-A	
				+A	
45				-NA	(1)
				+A	(1)
5				-A	(2)
				+A	(2)
18				-A	(1)
				+A	(1)
10				-A	(4)
				+A	(4)
23				-A	(1)
				+A	(1)
37				-A	
	600	5	3	+A	
*Notes are explained on page C-3.					

Table C-4A. SA659-150 Group 1 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
1	450	3	2	-NA	
2				+NA	
3				-NA	(1)
4				+NA	(1)
5				-NA	
6		3	2	+NA	
7		4	3	-A	
8				+NA	
9				-A	
10				+NA	
11	450			-A	(1)
12	480			+NA	(1)
13				-A	(1)
14				+NA	(1)
15				-NA	
16				+NA	
17		4		-A	(1)
18		5		+NA	(1)
19				-A	(5)
20				+A	(5)
				-A	(1)
				+NA	(1)
				-NA	(2)
				+NA	(2)
	480	5	3	-NA	
				+NA	

Table C-4B. SA659-150 Group 2 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
1	520	3	2	-NA +A	
2				-NA +NA	
3				-NA +NA	
4				-NA +A	(3) (3)
5		3		-NA +A	
6		4		-NA +NA	
7				-NA +NA	
8				-NA +A	
9				-A +NA	
10		4		-NA +NA	
11		5		-NA +A	
12				-A +A	(1) (1)
13				-A +A	(2) (2)
14				-NA +NA	
15			2	-A +NA	
16			3	-A +A	
17				-A +A	
18				-A +A	(1) (1)
19				-A +A	(2) (2)
20	520	5	3	-A +NA	

Table C-4C. SA659-150 Group 3 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
1	540	5	4	-A	
2				+A	
3				-A	
4				+A	
5				-A	(2)
6				+A	(2)
7				-A	(4)
8				+A	(4)
9				-A	(1)
10				+A	(1)
11				-A	(1)
12				+A	
13				-A	
14				+A	
15				-A	
16				+A	
17				-A	
18				+A	
19				-A	
20	540	5	4	+A	

Table C-5. SA862-39 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
0	480	3	2	-A	(1)
1				+A	(1)
2				-A	
3				+NA	
4				-A	
5				+NA	
6				-A	
7				+NA	
8				-A	
9				+NA	
10				-A	(1)
11				+NA	(1)
12				-A	(1)
13				+NA	(1)
14				-A	
15				+NA	
16				-A	(1)
17				+NA	(1)
18				-A	(1)
19	480	3	2	+A	(1) Fig. C-5

Table C-6. SA862-39 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
51	450	4	2	-A	
3				+A	
29				-A	
16				+A	(1)
30				-A	(1)
33				+A	(2)
56				-A	(2)
43				+A	
54				-NA	
25				+NA	
45				-A	
27				+A	
53	450	4		-A	(1)
32	480	3		+A	(1)
4				-A	(1)
19				+NA	(1)
21				-A	(1)
47				+A	(1)
9	480			-A	
7	420			+A	
	420	3	2	-A	
				+A	

Table C-6 Continued. SA862-39 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
11	420	3	2	-A	(1)
				+A	(1)
37				-A	(1)
				+A	(1)
13				-A	(1)
				+A	(1)
62				-A	(2)
				+A	(2)
36				-A	
	420		2	+A	
39	480		4	-A	
				+A	
24				-A	(1)
				+A	(1)
34				-A	(1)
				+A	(1)
55				-A	(1)
				+A	(1)
5				-A	
			4	+A	
26			2	-A	
				+A	
5				-A	
				+A	
14				-A	(1)
				+NA	(1)
6				-A	
				+A	
8				-A	(1)
				+A	(1)
35				+A	(2)
				+A	(2)
52				-A	
				+A	
20				-A	(1)
				+A	(1)
17				-A	
				+A	
49				-A	
	480	3	2	+A	

Table C-6 Continued. SA862-39 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
12	480	3	2	-A	(1)
38				+A	(1)
15				-A	
2				+A	
44				-A	
28				+NA	
40				-A	
61				+A	(1)
72	480			-A	(1)
42	450			+A	
60				-A	(1)
41				+A	(1)
68		3		-A	
23		4		+A	
57				-NA	
1				+A	
3				-A	
63		4		+A	(1)
22		5		-A	(1)
48				+A	
	450	5	2	-A	
				+A	

Table C-6 Continued. SA862-39 Tests

Sample No.	Solder Temp (°F)	Generator Setting	Ultrasonic Time (Seconds)	Tinned-Surface Condition (See Notes)*	Remarks (See Notes)*
73	450	5	2	-A	
				+A	
10				-A	
				+A	
71				-A	
				+A	
64				-A	
				+A	
66				-A	(2)
				+A	(2)
74				-A	
				+A	
75				-A	
				+A	
59				-A	(1)
				+A	(1)
46				-A	(1)
				+A	(1)
69				-A	
				+A	
65				-A	(1)
	450	5	2	+A	(1)

Figure C-1. SA1306-71 Metallurgical Cross-Sections

Figure C-2. SA1306-23 Metallurgical Cross-Sections

Figure C-3. SA1181-33 Metallurgical Cross-Sections

Figure C-4. SA1181-29 Metallurgical Cross-Sections

Figure C-5. SA862-19 Metallurgical Cross-Sections

Appendix D

TEST LABORATORY SUPPORT ACTIVITIES

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Appendix D

TEST LABORATORY SUPPORT ACTIVITIES

This support work was requested to evaluate and to explain the results of a test that was conducted during FY69-2.

In conjunction with an evaluation of equipment which employed ultrasonic energy wave to assist in hot-dip tin/lead plating of component leads, cross-sections of resistors, capacitors, and diodes were selected and the pertinent electrical properties were tabulated by the Bendix Test Laboratory. All of the components tested were within the specified limits of the stipulated properties.

The tested components were returned to Electronic Engineering, where the leads were subjected to immersion in a pool of liquidus 63/37 solder. During the immersion interval, a 4-second burst of ultrasonic energy was directed through the solder and impinged against the side of each perpendicular to the axis of the lead.

The specimens were returned to the Test Laboratory for retesting to determine the effects of ultrasonic exposure on the electrical characteristics of the components. The second tests revealed that 5 tantalum capacitors displayed an increase in dc leakage; all other specimens showed no significant change.

A considerable amount of research was done to determine the reason for the change in the tantalum capacitors. The Military Specification that governs tantalum capacitors was studied, but no new knowledge of the problem was revealed. A query to Mr. C. C. Houtz of Bell Telephone Laboratories brought the suggestion that the cause of the increase in dc leakage might lie in some area other than the application of ultrasonic energy.

Further investigation produced the following possibilities.

- The same equipment was not used to perform the two series of tests.
- The capacitors that were tested were not supplied by a qualified vendor. A tendency for that supplier's capacitors to grade too close the high limit of dc leakage was perhaps the principal reason for failure to meet qualification requirements.
- Surface contamination was suggested as a possible cause of high dc leakage. The high limit is 0.5 microampere for the test voltage used.

A group of tantalum capacitors from a qualified vendor was substituted for the 5 original capacitors, and the tests were rerun. These capacitors, as well as the original units, were subjected to the same time, solder temperature, and ultrasonic agitation variables during the tinning process. Only one variable was changed at any one time.

The tests of the second group of capacitors showed no significant change in dc leakage.

The conclusions reached as a result of components with ultrasonically tinned leads are as follows.

- Application of ultrasonic agitation in the manner that is usual in tinning of leads in a solder pot is not detrimental to the electrical characteristics of resistors, capacitors, or diodes.
- The ultrasonic method of lead tinning is effective on all types of components and lead materials tested. (See the report on lead tinning in Appendix C.)
- Ultrasonic tinning is an acceptable substitute for tinning methods that require liquid flux or other cleaning agents.

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