MASTER

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS
URBANA, ILLINOIS 61801

RECEIVED BY DTIE MAR 17 1970

A HIGH SPEED ANALOG DIVIDER FOR
THE ILLIAC III SCAN SYSTEM*

by

Sergio Franco

LEGAL NOTICE

This report was prepared as an account of Government sponsored work. Neither the United States, nor the Commission, nor any person acting on behalf of the Commission:

A. Makes any warranty or representation, expressed or implied, with respect to the accuracy, completeness, or usefulness of the information contained in this report, or that the use of any information, apparatus, method, or process disclosed in this report may not infringe privately owned rights; or

B. Assumes any liabilities with respect to the use of, or for damages resulting from the use of any information, apparatus, method, or process disclosed in this report.

As used in the above, "person acting on behalf of the Commission" includes any employee or contractor of the Commission, or employee of such contractor, to the extent that such employee or contractor of the Commission, or employee of such contractor prepares, disseminates, or provides access to, any information pursuant to his employment or contract with the Commission, or his employment with such contractor.

File No. 810

October 3, 1969

*Supported by Contract AT(11-1)-1018 with the U.S. Atomic Energy Commission

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

The information contained in the pictures to be processed by the Illiac III computer is converted into digital form by a cathode ray tube flying spot scanner. The light output of the CRT's is likely to be non-uniform from point to point on the screen owing to initial phosphor irregularities, as well as burn out and wear out deteriorations which may occur during the operation. In addition, there may be nonuniformities in the optical system connecting the CRT and the photomultiplier. Thus, there must be some means of distinguishing between PMT signals due to image opacity and PMT signals due to CRT light output variations. In the Illiac III Scan System this is accomplished by using two identical PMT's, one receiving light through the image and the other receiving light through a similar optical path but not through the image. The signal equal to the ratio of the outputs of the two PMT's is then a true measure of the opacity of the image.

The PMT's outputs, after proper amplification and filtering, are normalized to the range +0.020 to +2.0 volts; owing to the image opacity, the output Z of the signal PMT (which receives light through the film) is always smaller than or equal to the output Y of the reference PMT. Since the position of the electron spot on the screen can be updated as frequently as every 0.8 μ s, the circuit performing the analog division between Z and Y must respond with a commensurable speed. Furthermore, this ratio must be accurate within at least 3%, which represents about one half of the LSB of the present 4-bit analog-to-digital converter for the image gray scale encoding.

Among the several ways of accomplishing the division between two analog voltages, the method perhaps most commonly used is that illustrated in Figure 1. The "Multiply" circuit is usually a high speed analog multiplier, based on the transistor variable-transconductance principle; for proper operation, the input V_z must be negative. This approach has the inherent disadvantage that both accuracy and speed are strongly dependent on the magnitude of the divisor, the performance of the

Figure 1 - Analog Divider

circuit becoming worse and worse as the magnitude of V_y decreases¹. For low values of V_y , also the noise of the output signal becomes relevant. For such reasons, this scheme may be employed, at moderate speeds and accuracy, only over modest signal ranges.

The analog divider described herein and shown in Figure 2 forms the ratio V_z/V_y as the antilogarithm of the difference of the logarithms of V_z and V_y . This approach achieves accuracy and speed that are essentially independent of the magnitudes of V_z and V_y over a wider range. In order to illustrate the theory of operation of the circuit, we shall refer to the simplified scheme of Figure 3.

Transistors T_x , T_y and T_z are driven by the corresponding operational amplifiers with collector currents given by V_x/R , V_y/R and V_z/R respectively. For the present we assume that $R_1 = R_2 = R_3 = R_4 = R$. Let $\Delta_v = v^- - v^+$ be the input voltage offset of the op amp which drives T_o , and $\Delta_i = i^- - i^+$ be the input current offset, where i^- and i^+ are the bias currents for the inverting and the non-inverting inputs of the same amplifier. Then the voltages at these inputs are

$$v^- = \frac{V_{Ey} + V_{Eo} - Ri^-}{2}$$

and

$$v^+ = \frac{V_{Ez} + V_{Ex} - Ri^+}{2}$$

1. Arthur Pfaelzer, "What's Wrong With Analog Multiplier Specs", EEE Vol. 17, No. 5., p. 54 (May 1969).

Figure 2 - Analog Divider

Figure 3 - Simplified Diagram of Analog Divider

respectively. The op amp in consideration acts as a regulator and drives T_O in order to keep V_{Eo} such that $v^- = v^+ + \Delta_v$, i.e.

$$V_{Eo} + V_{Ey} = V_{Ex} + V_{Ez} + 2\Delta_v + R\Delta_i. \quad (1)$$

For a high-beta silicon transistor, the relationship between collector current I_c and base-to-emitter voltage drop V_{BE} can be accurately expressed by the equation

$$V_{BE} = A \ln I_c + B,$$

where B is an appropriate quantity which depends on temperature, and $A = kT/q$; k is Boltzmann's constant, T the absolute temperature, and q the electron charge. By inserting the last equation into (1) we obtain

$$A_o \ln I_o + B_o + A_y \ln I_y + B_y = A_x \ln I_x + B_x + A_z \ln I_z + B_z + 2\Delta_v + R\Delta_i. \quad (2)$$

We now introduce the total offset Δ defined by

$$\Delta = 2\Delta_v + R\Delta_i + (B_z - B_y) + (B_x - B_o). \quad (3)$$

Then Equation (2) yields

$$\begin{aligned} \ln I_o &= \frac{1}{A_o} (A_x \ln I_x + A_z \ln I_z + \Delta) \\ &= \frac{1}{A_o} \ln(I_x^{A_x}) + \ln(I_z^{A_z}) - \ln(I_y^{A_y}) + \ln(e^\Delta) \end{aligned}$$

Thus, by exponentiating on both sides, we obtain

$$I_o = \left[e^\Delta (I_x^{A_x}) \frac{(I_z^{A_z})}{(I_y^{A_y})} \right]^{1/A_o}.$$

For a set of randomly chosen transistors of the same type, the A 's are generally close to each other within a few percent. If necessary, one can

sort samples having their A's matched within a smaller percentage², so that the previous equation becomes

$$I_o = \exp(\Delta/A_o) \frac{I_x I_z}{I_y}.$$

Thus our circuit can be used either as a multiplier, with I_x and I_z as inputs and I_y constant, or as a divider, with I_z and I_y as inputs, I_x constant, or as a multiplier and divider simultaneously (three-input device). The input kept constant in the first two modes of operation, apart from the quantity $\exp(\Delta/A_o)$ and possible mismatches between the resistors denoted by R , determines the scale factor of the output I_o .

The transistors used in the present design are Sprague TD101 units, each of which contains a pair of matched transistors which satisfy Equation (1) rather accurately over the operating current ranges (6 to 600 μ A). The reason for choosing the pairs (T_y, T_z) and (T_x, T_o) matched is that of keeping the voltage offsets $(B_z - B_y)$ and $(B_x - B_o)$, appearing in Equation (3) reasonably small and less sensitive to temperature variations than in the case of discrete, unmatched transistors. In this way, the temperature dependence of the total offset Δ and, therefore, of the scale factor $\exp(\Delta/A_o)$, can be sensibly reduced, with the achievement of better accuracies.

In order to examine the temperature drift of the scale factor more closely, we write

$$\frac{\Delta(t)}{A_o(t)} = \frac{\Delta_{25^\circ} + [2(d + D_v) + RD_i]t}{\frac{k298}{q} (1 + t/298)}$$

where t is the temperature in $^\circ$ C referred to room temperature. Room temperature is assumed to be 25° C or 298° K; Δ_{25° is the total initial offset, d is the temperature drift coefficient for the TD101's voltage offset, D_v and D_i are the temperature drift coefficients of Δ_v and Δ_i respectively.

-
2. In Appendix it will be shown that the ratio I_z/I_y can be obtained even in the case of unmatched A's, if appropriate values, different from unity, are chosen for the ratios R_1/R_2 and R_3/R_4 .

From the manufacturer's data sheets we find the following typical, average values:

$$\text{TD101: } |V_{BE\text{left}} - V_{BE\text{right}}| = 2.5 \text{ mv, } d = 6 \text{ } \mu\text{volts}/^{\circ}\text{C.}$$

$$\mu\text{A702C: } \Delta_v = 1.5 \text{ mv, } D_v = 5 \text{ } \mu\text{volts}/^{\circ}\text{C,}$$

$$\Delta_i = 0.5 \text{ } \mu\text{A, } D_i = 4 \text{ nA}/^{\circ}\text{C.}$$

We also have $298k/q \approx 26 \text{ mv}$. Hence, with $R = 3.3K$, and by making the worst case assumption that all the terms in Equation (3) add up constructively, we obtain $\Delta_{25^{\circ}} \approx 10 \text{ mv}$ and

$$\frac{\Delta(t)}{A_o(t)} \approx 0.4 \frac{1 + t/400}{1 + t/300}.$$

The temperature drift coefficient of the scale factor is, therefore,

$$\begin{aligned} \frac{d}{dt} \exp[\Delta(t)/A_o(t)] &= \exp[\Delta(t)/A_o(t)] \frac{d}{dt} \frac{\Delta(t)}{A_o(t)} \\ &\approx \exp(0.4) \cdot 0.4 \frac{\frac{1}{400} (1 + \frac{t}{300}) - \frac{1}{300} (1 + \frac{t}{400})}{(1 + \frac{t}{300})^2} \\ &\approx (1 + 0.4) \cdot 0.4 \cdot (\frac{1}{400} + \frac{1}{300}) \approx \frac{1}{300}. \end{aligned}$$

Thus our calculations lead to a worst case estimate of a drift of about 1% every 3°C , if average components of the types of Figure 2 are used.

Fortunately, temperature tests applied to the analog divider prototype have given results more encouraging than those expected theoretically. Tests have been made for full and for half scale output, and in both cases the drift has been about 2.5% over 20°C , at an average of 1% every 8°C . A possible explanation for this is that the four offsets and relative temperature coefficients of Equation (3) do not add up cumulatively, but rather tend to compensate for each other. This drift figure can be further improved by using units with better temperature control, like the μA726 matched transistor pairs. Indeed, it may be noticed that the scale factor drift is not so strongly dependent on the total initial offset $\Delta_{25^{\circ}}$ as it is on the drift coefficients $2(d + D_v) + D_i$; the latter, therefore, are the most critical quantities to be controlled.

A few remarks about certain features of Figure 2 are appropriate. The whole circuit has been laid out on a single card (1018-318-00). Since the $\mu A702$ are wideband op amps, they inherently tend to be frequency unstable, so that careful filtering of the power supplies at each op amp site is necessary. The RC feedback network of the X, Y, and Z op amps is also used for frequency compensation, owing to the phase shift introduced by the corresponding transistors. In order to have proper division, the transistors have been sorted with $A_x = A_y = A_z = A_o$ within 1%. Hence, also the resistor pairs R15, R16, and R20, R21 ought to be matched with comparable or better accuracy. The output scale factor is set to the prescribed value (4.0 in our application) by adjusting trimpot R5; this adjustment is made at the logarithmic midrange of the inputs, i.e. at $V_z = V_y = 0.2$ volts. The collector current of T4 could be converted back into a voltage signal by feeding it into a potentiometric op amp. Because of the difficulties encountered in the frequency compensation of the $\mu A702$ for this kind of application, the output amplifier is connected in the differential mode. The purpose of R30 and R31 is to shift the signals negatively, so as to comply with the limitations of the input stage of the $\mu A702$ for positive going inputs. R32 is used to adjust the output offset; this is accomplished by temporarily shorting to ground the emitter of T4, and by varying R32 until $V_o = 0$ volts.

Another point to be kept in mind is that the input current and voltage offsets of the X, Y and Z op amps may decrease the accuracy of the divider considerably, when the input signals are in the lower part of their range. In order to discuss this, we refer to Figure 4, and write

Figure 4

$$v^+ = -Ri^+ ,$$

$$v^- = v^+ + \Delta_v ,$$

$$V - v^- = R(i^- + I),$$

so that

$$I = \frac{V}{R} - \left(\Delta_i + \frac{\Delta_v}{R} \right) .$$

Thus, the collector current I may depart from its nominal value V/R by as much as $0.5 + 1.5/3.3 \approx 1 \mu A$; this amount is comparable with the lowest value of I ($6 \mu A$), of which it represents about 15%. Again, these problems can be avoided by using high performance op amps. In our design the $\mu A702$ units have been used because they are the only ones that, at present, combine wide bandwidth with low cost and easy availability.

The d. c. accuracy of the analog divider prototype is exhibited in Table 1. In Figures 5, 6 and 7 the dynamic behavior of the same is shown. It may be noticed that the time required for the output to settle within 3% of its value is better than $1 \mu s$, and is relatively independent of the magnitude of the denominator. This fact is shown especially in Figure 7, where the denominator is varied in the lower part of its range. The noise of the output signal is strongly dependent on the op amp driving T_O , and on the kind of frequency compensation used. In the present application the lead-lag compensation has been used for the sake of speed. In cases where the speed requirements are less demanding, the lag compensation may be used, with the result of a loss in speed but a considerable improvement over the noise.

V_z V_y	0.02	0.05	0.1	0.2	0.5	1	2
2	0.037 -0.003 0.015	0.100 0.000 0.015	0.201 +0.001 0.020	0.404 +0.004 0.020	1.009 +0.009 0.030	2.01 +0.01 0.050	4.01 +0.01 0.070
1	0.078 -0.002 0.015	0.198 -0.002 0.020	0.402 +0.002 0.025	0.813 +0.013 0.030	2.02 +0.02 0.045	4.00 0.00 0.055	
0.5	0.156 -0.004 0.020	0.401 +0.001 0.030	0.810 +0.010 0.040	1.62 +0.02 0.060	4.00 0.00 0.060		
0.2	0.392 -0.008 0.025	1.002 +0.002 0.035	2.01 +0.01 0.050	4.000 0.000 0.060			
0.1	0.786 -0.014 0.040	2.01 +0.01 0.050	3.99 -0.01 0.060				
0.05	1.56 -0.04 0.060	4.02 +0.02 0.070					
0.02	4.05 +0.05 0.130						

Table 1 - D. C. measurements of analog divider accuracy. All entries are in volts. For given values of V_z and V_y , upper entry represents the measured output, middle entry represents the deviation from the theoretical value $(4V_z)/V_y$, and lower entry represents the r.m.s. of the output noise.

Figure 5 - Horizontal: $0.2 \mu\text{s}/\text{div.}$; Vertical: $1 \text{ volt}/\text{div.}$;
 $V_y = 2 \text{ volts}$. Upper trace represents V_z , with
 $0.020 \text{ volts} < V_z < 2 \text{ volts}$. Lower trace represents V_o .

Figure 6 - Horizontal: $0.2 \mu\text{s}/\text{div.}$; Vertical: $0.050 \text{ volts}/\text{div.}$ for
upper trace, $1 \text{ volt}/\text{div.}$ for lower trace; $V_v = 0.150$
volts. Upper trace represents V_z , with $0.020 < V_z < 0.150$
volts. Lower trace represents V_o .

Figure 7 - Horizontal: $0.2 \mu\text{s}/\text{div.}$; Vertical: 0.100 volts for upper trace, 1 volt for lower trace; $V_z = 0.060$ volts. Upper trace represents V_y , $0.060 \text{ volts} \leq V_y \leq 0.300 \text{ volts}$. Lower trace represents V_o .

APPENDIX

The more general treatment of the circuit of Figure 3 for the case $R_1/R_2 = \alpha_i$, $R_3/R_4 = \alpha_o$, with $\alpha_i, \alpha_o \neq 1$, shows that the same circuit may be used to generate not only products or ratios of its inputs, but also rational powers of the same functions. The voltages at the inputs of the amplifier driving T_o are now

$$v^- = \frac{1}{R_3 + R_4} (R_4 V_{Ey} + R_3 V_{Eo} - R_3 R_4 i^-)$$

and

$$v^+ = \frac{1}{R_1 + R_2} (R_2 V_{Ez} + R_1 V_{Ex} - R_1 R_2 i^+)$$

respectively, so that the condition $v^- = v^+ + \Delta_v$ yields

$$\frac{1}{1 + \alpha_o} (\alpha_o V_{Eo} + V_{Ey}) = \frac{1}{1 + \alpha_i} (\alpha_i V_{Ex} + V_{Ez}) + \Delta_v + \frac{R_3 i^-}{1 + \alpha_o} - \frac{R_1 i^+}{1 + \alpha_i}$$

By expressing the emitter voltages in terms of the corresponding collector currents, the last equation leads to

$$\begin{aligned} \frac{1}{1 + \alpha_o} [\alpha_o (A_o \ln I_o + B_o) + A_y \ln I_y + B_y] &= \frac{1}{1 + \alpha_i} [\alpha_i (A_x \ln I_x + B_x) + \\ &A_z \ln I_z + B_z] + \Delta_v + \frac{R_3 i^-}{1 + \alpha_o} - \frac{R_1 i^+}{1 + \alpha_i} \end{aligned}$$

If we now define the total voltage offset δ by

$$\delta = \frac{1 + \alpha_o}{\alpha_o} [\Delta_v + \frac{1}{1 + \alpha_o} (R_3 i^- - \alpha_o B_o - B_y) - \frac{1}{1 + \alpha_i} (R_1 i^+ - \alpha_i B_x - B_z)],$$

then our previous equation yields

$$\ln I_O = \frac{1 + \alpha_O}{1 + \alpha_i} \left[\frac{\alpha_i A_x}{\alpha_O A_O} \ln I_x + \frac{A_z}{\alpha_O A_O} \ln I_z \right] - \frac{A_y}{\alpha_O A_O} \ln I_y + \frac{\delta}{A_O}$$

$$= \ln \left[I_x^{\frac{A_x \alpha_i (1 + \alpha_O)}{A_O \alpha_O (1 + \alpha_i)}} \right] + \ln \left[I_z^{\frac{A_z (1 + \alpha_O)}{A_O \alpha_O (1 + \alpha_i)}} \right] - \ln \left[I_y^{\frac{A_y}{A_O \alpha_O}} \right] + \ln \left[e^{\frac{\delta}{A_O}} \right].$$

Thus, by exponentiating on both sides, we obtain

$$I_O = e^{\frac{\delta}{A_O}} \left(I_x^{\frac{A_x \alpha_i (1 + \alpha_O)}{A_O \alpha_O (1 + \alpha_i)}} \right) \frac{\left(I_z^{\frac{A_z (1 + \alpha_O)}{A_O \alpha_O (1 + \alpha_i)}} \right)}{\left(I_y^{\frac{A_y}{A_O \alpha_O}} \right)}.$$

By properly choosing the values of α_i and α_O , various combinations of rational powers of the inputs can be generated. For example, it is possible to generate the function $(I_z/I_y)^{m/n}$ by choosing

$$A_y/(A_O \alpha_O) = m/n, \text{ i.e. } \alpha_O = (n/m)(A_y/A_O), \text{ and}$$

$$A_z(1 + \alpha_O)/[A_O \alpha_O (1 + \alpha_i)] = m/n, \text{ i.e. } \alpha_i = (n/m)A_z(1/A_O + 1/A_y) - 1.$$

In particular, if one wants to generate the ratio I_z/I_y , the previous conditions lead to the choice

$$\alpha_O = A_y/A_O \text{ and } \alpha_i = A_z(A_O + A_y)/A_O A_y - 1,$$

so that the given ratio may be obtained even in the case of transistors having the A's unmatched.

A general rule to be kept in mind for the purpose of getting

good temperature behavior of the circuit is that, once the values of the α 's have been decided, the other parameters of the circuit (e. g. the current metering resistors R of Figure 3) should be chosen in order to allow the transistors to work over current dynamic ranges as close as possible, so that their voltage offsets can be better controlled.

Acknowledgments

The Author wishes to acknowledge Dr. J. L. Divilbiss for his stimulating discussions. The assistance of Mr. W. A. Miller and Mr. E. Pelg, of the Circuit Layout Department, is also sincerely appreciated.