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M. M. Stephens

J. E. Swansen

L. V. East*

*Canberra Industries, 45 Gracey Ave., Meriden, CT 06450.

los alamos
scientific laboratory
of the University of California
LOS ALAMOS, NEW MEXICO 87545

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SHIFT REGISTER NEUTRON COINCIDENCE MODULE

by

M. M. Stephens, J. E. Swansen, and L. V. East

ABSTRACT

A neutron coincidence module was designed using multistage shift registers to produce the coincidence gates and a crystal controlled oscillator with variable clock outputs to change the gate lengths. The advantage of this system over the conventional, thermal-neutron coincidence gates is a decrease in deadtime by more than an order of magnitude.

I. INTRODUCTION

The classical approach to neutron coincidence counting using moderated thermal-neutron detectors consists of counting multiple neutron events that occur during a time comparable to the neutron slowing-down time of the detector moderator assembly.¹⁻⁴ This is done by opening an electronic gate whenever an event is detected, and counting other events that occur during the gate time as coincidence events. The relatively long gate lengths required, typically 20 μ s to 150 μ s, result in an unacceptably long instrument deadtime since only a single gate is "open" at any one time.

The shift register coincidence circuit described in this report, based on a suggestion by K. Böhnel,^{*} eliminates the long coincidence gate and replaces it with a 64-stage shift register.⁵⁻⁶ Each neutron detected produces a pulse which causes a "one" to be shifted into the shift register. This "one," representing a detected neutron, propagates through the shift register at a selected clock frequency. Coincidences are registered by counting the number of "ones" in the shift register when each neutron is detected. This technique in

effect allows each neutron to start a new gate whose length is determined by the number of stages in the shift register and the frequency of the clock. The instrument described in this report uses five 64-stage shift registers. The first 64-stage shift register is used as the real-plus-accidental gate, the next three are delays; the last register is utilized as the accidental gate.

The deadtime of the shift register coincidence circuit is determined by the period of the clock instead of the total gate length as in the classical coincidence technique. Figure 1 shows a comparison of deadtime at various rates between the shift register coincidence circuit and the conventional type.

The technique used to count the number of pulses present within both the real-plus-accidental and the accidental gates consists of counting a decade scaler up each time a "one" is shifted into the 64-stage shift register, and counting the decade scaler down when the "one" is shifted out of the register.

A decade adder on the output of the up-down scaler keeps a running sum of the pulses within both shift registers each time a new neutron event is detected. The carry-out from the adder is counted in the real-plus-accidental scaler in the readout section of the instrument.

* 1971 visiting scientist at Los Alamos Scientific Laboratory from Kernforschungszentrum, Karlsruhe, Federal Republic of Germany.

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Fig. 1. Comparison of response obtained using a conventional coincidence circuit and the new shift register coincidence circuit in plutonium assay with simulated high background.

The accidental coincidence rate from uncorrected events is measured by using a second gate, delayed in time, but of the same duration as the real gate. The delay is accomplished by three 64-stage shift registers between the real shift register and the accidental shift register. Since all the shift registers operate from a common crystal clock, the gate lengths are exactly equal. The information in the accidental gate is processed in the same manner as the real-plus-accidental gate and may be read out visually or serially to an external device.

II. PHYSICAL DETAILS

The finished instrument, shown in Fig. 2, is constructed in a triple-width N.I.M. unit. The N.I.M.-type construction was selected because of the variety of applications in which the instrument would be used. In most cases the associated instrumentation would also be N.I.M. modules and portable.

In addition to the standard N.I.M. voltages, the coincidence unit must have +5 V from a power supply capable of supplying 3 A. The interior of

Fig. 2. Front view of shift register coincidence module.

the instrument is shown in Fig. 3. A board was designed which holds three wire-wrap cards and attaches to the rails of the N.I.M. unit. There are ten wire-wrap sockets along the top of the board

Fig. 3. Inside view showing wire-wrap boards.

which are used as input/output (I/O) headers between the two boards and the front and rear panels. The bottom board is solidly attached to the rails and contains the circuitry associated with the shift registers and control. The top board is hinged to permit access to the plug-in integrated circuits. This board contains the scalers and associated readout circuitry. Both boards were wire-wrapped on a semiautomatic wire-wrap machine. The I/O connectors for readout, control and test purposes are located on the rear panel shown in Fig. 4.

Figure 5 illustrates the instrument and associated electronics in a stand-alone system used for coincidence counting of 1-gal cans in a 4π well counter.

III. DESCRIPTION OF ELECTRONICS

A simplified block diagram of the shift register and control board is shown in Fig. 6. The gate-length switch, located on the front panel,

Fig. 4. Rear view of shift register coincidence module.

Fig. 5. Coincidence unit in operation with well-counter electronics.

selects the frequency of the system clock. The input from the neutron detector must exceed the discriminator setting before it is shaped and synchronized with the clock in the clocked discriminator (CKD Disc.). There are a number of control conditions that must be met before the CKD Disc. will accept a pulse. The CKD-Disc. pulse is shifted through a switch-selectable number of pre-delay shift register stages before being shifted into the real shift register. A pre-delay is required to compensate for the fact that the amplifier and discriminator exhibit some deadtime at the beginning of the real gate which would produce an error

Fig. 6. Shift register and controls block diagram.

Fig. 7. Shift register and control schematic.

in the number of real-plus-accidental events compared to the number of accidental events.

When an event is shifted into the shift register, it counts a decade scaler in the up direction. Likewise, when an event comes out of the 64-stage shift register, the same scaler is counted down. Thus, the number of events in both the real-plus-accidental and accidental shift registers is known at any given time.

The CKD Disc. strobes the output of the decade scaler into the adder. The contents of the decade scaler thus are added to the previous count before entering the event into the shift register. A timing diagram, lower left in Fig. 6, shows this sequence.

After 3 x 64 stages of delay shift register, the accidental gate processes pulses in the same manner.

The crystal oscillator and dividers at the top of Fig. 7 constitute the shift register clock circuitry. The gate-width switch located on the front panel allows the selection of the appropriate

clock frequency to produce the desired gate length in the 64-stage shift register. The selected clock rate triggers a 100-ns one shot which provides the clock pulses (CK) and $\overline{\text{CK}}$ that are used throughout the instrument for timing purposes. The 0026c, MOS driver converts the +5-V CK to +12-V logic to increase the operating speed of the CMOS shift registers.

The signal input via a connector on the front panel is processed by a 0- to 10-V adjustable discriminator. The discriminator is located on a printed circuit board directly behind the front panel. The output of the discriminator triggers a 0.5- to 2.0- μ s analog delay and shaper, I.C. 243, shown in Fig. 8. The three flip-flops following the shaper have the function of synchronizing the incoming random neutron events with the shift register clock. The output of the shaper sets the first flip-flop, causing the "D" input on the next flip-flop to go high. The next $\overline{\text{CK}}$ pulse sets the second flip-flop which in turn resets the first and sets the third, provided that either of two

Fig. 8. Up-down scaler and adder schematic.

conditions is met at the "D" input of I.C. 133. The two conditions are that the instrument is not in the stop mode and that there is not a nine in the real up-down counter which registers the number of events in the real shift register. These conditions will be discussed later.

The random neutron events are now synchronized with the shift register clock. These pulses are designated CKD Disc. and $\overline{\text{CKD Disc.}}$ and are used for timing purposes throughout the instrument. A timing sequence of these pulses is shown in Fig. 6.

The CKD-Disc. pulses are fed into the data input of the eight-stage pre-delay shift register I.C. 144. The digital pre-delay switch located on the rear panel allows the operator to select from one to eight clock pulses to delay the input before it goes into the real shift register. The switch enables one of the eight inputs of a priority encoder. The coded output of the priority en-

coder "tells" the one-of-eight data selector, I.C. 231, which of the pre-delay shift register outputs has been selected. The selected pulse goes via a MOS driver to the data input of the real-gate shift register.

Each time a pulse enters or exits either the real or the accidental shift register, it is processed by the circuitry in Fig. 8.

A fault indicator on the front panel indicates that one of two possible troubles has occurred. During a measurement, if a nine is recognized in the real up-down scaler, an updating, one-second one shot, I.C. 141, is triggered, energizing the fault light. This indicates the count rate is too high. At the end of a measurement the recognize-zero circuitry checks to see if the real up-down scaler has returned to zero, which should happen if no pulses were missed. These two

problems are also recorded in the fault flip-flop which may be checked by an external device.

The local- and remote-control circuitry is located at the bottom left of Fig. 7. The start, stop, and reset may be performed locally on the front panel or remotely through the rear panel connector.

The circuitry shown in Fig. 8 is identical for both the real and accidental channel. Thus, only one of the circuits will be discussed.

When an event pulse is clocked into the shift register, it also triggers the 100-ns one-shot, I.C. 335. This pulse is synchronized with $\overline{CK}$ and fed to the up input of the decade scaler, I.C. 334. The pulse is also buffered and routed to the rear panel for test purposes. When a pulse is shifted out of the shift register, it is synchronized with $\overline{CK}$ at I.C. 135 and triggers the count down one shot. Thus, the up-down scaler will never try to count in both directions simultaneously.

The contents of both the real and accidental up-down scalars are clocked into a four-bit latch by the CKD Disc. pulse each time a new event is detected. The output of the latch is added to the running sum of the previous events.

The two, four-bit, binary adders, IC 332 and 331, are interconnected to perform a BCD addition. That is, any bit combination above a nine in the top adder is decoded as a carry and adds six to the bottom adder. The timing of the pulses that clock the latches is such that the running sum in the bottom latches is added to the contents of the top latch before the new result is transferred into the bottom latch. The least significant digit is displayed or read out through a four-bit tri-state gate. The carryout from the adder enables a clocked one-shot I.C. 324, which is buffered and drives the 10^1 decade of the display scaler.

A simplified clock diagram of the readout board is shown in Fig. 9. The display oscillator cycles through the 26-digit counter at a 2-kHz rate. The digit lines enable the tri-state output on the decade scalars. Thus, the data from all the devices are put on the four output lines, bit-parallel digit-serial.

In the print mode, the display oscillator is disabled and the digit multiplier is advanced by the external device accepting the data. The

Fig. 9. Readout board block diagram.

pre-set time scaler receives its time pulse from a 120-VAC line. The MCT-2 is a phototransistor optical couple device used to isolate the 120 VAC from the +5-V logic. A gated, Schmitt trigger drives the divider chain for the time pulses.

The pre-set time is thumbwheel-selectable from the front panel. One thumbwheel selects the digit, 0-9; the second thumbwheel selects the power of 10 multiplier. Then the pre-set time is reached, the instrument stops and any external controlling device is alerted.

The real and accidental scalars count the carries of ten from the associated adders while the least significant digit is supplied directly from the adder. The total-event scaler counts the number of pulses that are above the input discriminator threshold setting.

The digits of all the scalars, except the least significant digit, are reset to 15 (all "ones") to facilitate leading zero blanking in the BCD to seven-segment decoder. This is necessitated by the design of the decoder which interprets 15 as a blank. This made it necessary to decode the 15 as a 0 for use by external devices.

The four, one-of-ten CMOS counters at the top of Fig. 10 make up the multiplexing circuitry for display and readout purposes. If the print flip-flop is reset, the display oscillator ripples through the counters at a 2-kHz rate. When the

The 74L85, left center, Fig. 10, compares the setting of the pre-set time thumbwheel switch with the BCD data on the output lines. If it is equal to the time decade selected by the multiplier switch, the pre-set time flip-flop

This instrument extended the range of coincidence counting to high plutonium masses or oxides where high count rate and deadtime were the determining factors in previous conventional-type