DEC 24 1963

BNL 7448

CONF-363-6

FAST ANALOGUE MULTIPLIERS WITH FIELD-EFFECT TRANSISTORS*

V. Radeka**
Brookhaven National Laboratory
Upton, N. Y.

MASTER

Summary

The solution time of analogue multipliers using field-effect transistors is investigated. This time is ultimately limited by the charging time of the field-effect transistor junction. In typical devices suitable for analogue multiplication the charging time is found to be about 10-20 nsec for a multiplication error of less than one percent. A four quadrant pulse amplitude multiplier circuit is described, whose solution time is equal to the field-effect transistor charging time.

Introduction

The principle of analogue multiplication with field-effect transistors, the accuracy and stability considerations, and some basic multiplier schemes have been given previously.¹ This paper deals with speed limits of analogue multipliers as determined by the field-effect transistor.

The field-effect transistor is basically a variable conductance controlled by the reverse bias of the gate-channel junction. Analogue multiplication is based on proportionality of the channel conductance to the gate voltage. The simplest multiplier schemes use two field-effect transistors in a balanced (bridge) configuration. One variable (a voltage) is applied with opposite sign to appropriately biased gates, increasing the conductance of one channel and decreasing the conductance of another one. Another variable is applied as a voltage, or as a current, to the channels. The difference in channel currents is proportional to the product of the two variables, and is given by

$$\Delta I = G_o W_{oo} \beta^{3/2} (x \cdot y) \quad (1)$$

where: G_o , the channel conductance for zero bias $V_{go} + V_{dif} = 0$
 W_{oo} , "saturation" or "pinch-off" potential, i.e. junction barrier potential required to decrease the channel conductance to zero
 $\beta = (V_{dif} + V_{go}) / W_{oo}$, gate bias
 $x = \Delta v_g / \beta W_{oo}$, gate input
 $y = v_d / \beta W_{oo}$, channel input
 V_{dif} , the diffusion potential.

For current input to channels the output can be expressed as

$$\Delta I = \frac{1}{\beta^{1/2} - 1} (x \cdot i_y) \quad (2)$$

where i_y is the current applied to the field-effect transistor pair. Current driving has the advantage that the multiplier output is temperature independent, as the conductance parameter G_o does not appear in (2), and voltage parameters V_{dif} , W_{oo} are independent of temperature over a relatively wide range. The non-linearity is a function of input amplitudes. A suitable set of values x , y and β for a nonlinearity of less than 1 percent, and for symmetrical channel driving with respect to gate, is

$$x_{max} = 1/3, y_{max} = 1/4, \beta = 1/2 \quad (3a)$$

From (1), (2) and (3a)

$$i_{y_{max}} = 2G_o W_{oo} \beta (1 - \beta^{1/2}) \cdot y_{max} \approx \frac{1}{14} G_o W_{oo} \quad (3b)$$

* This work was done under the auspices of the U. S. Atomic Energy Commission

** On leave from Institute Rudjer Boskovic - Zagreb, Yugoslavia

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The minimum solution time can be defined as the time needed to change the conductance of the field-effect transistor to that required by the accuracy of multiplication. As a change in the gate-channel junction charge is necessary to change the channel conductance, the solution time is determined by the junction charging time.

In this paper the charging time is considered in terms of externally measurable field-effect transistor parameters, and with this, the relation between minimum solution time and permissible multiplication error is given.

The minimum solution time can be achieved if the junction charging current does not appear at the multiplier output. A method is presented to prevent this. Thus the solution time can be reduced to the fundamental limits of field-effect transistors. Examples of simple four-quadrant pulse amplitude multipliers are given.

The Field-Effect Transistor Charging Time and Multiplication Accuracy

A planar field-effect transistor with symmetrical geometry is shown in Fig. 1a. The symmetrical geometry is essential for multiplication linearity and, as will be shown later, for fast multiplication. The gate-channel junction is reverse biased and the shaded area shows the depletion region corresponding to the barrier potential $V_{go} + V_{dif}$ = external bias + diffusion potential. If a voltage step Δv is applied between channel terminals and the gate, in addition to V_{go} , the depletion region, and therefore the conducting channel width, adjusts itself to the new value of barrier potential. The charge necessary to change the depletion region width is supplied through the channel. The junction capacitance is distributed along the channel and the channel-junction combination can be considered

as a distributed RC transmission line. In the region of linear multiplication channel conductance is linearly proportional to gate voltage. If $\Delta v(l, t)$ is the potential variation distribution along the channel as a function of time, the channel conductance variation as a function of time is determined by

$$\frac{1}{\Delta g(t)} = \int_{-L}^{+L} \frac{dl}{\Delta g(l, t)} = \frac{-1}{K} \int_{-L}^{+L} \frac{dl}{\Delta v(l, t)} \quad (4)$$

where $K = \frac{1}{2} G_0 / \beta^{\frac{1}{2}} W_{00}$, Δv is positive when in reverse direction.

To determine the potential distribution as a function of time, an RC-line equivalent of the field-effect transistor can be used. Both distributed parameters $R = 1/G$ and C are functions of the gate-channel junction barrier potential. However, if their relative variation is small, they can be considered as constants for the purpose of determining the distribution of a small potential variation. The linear equivalent circuit in Fig. 1b is described by

$$\frac{\partial^2 \Delta v}{\partial u^2} = \frac{\partial \Delta v}{\partial T} \quad (5)$$

where $u = l/2L$ and $T = t / (R_b \cdot C_b)$ are normalized variables for distance and time, $R_b = 1/G_b$ and C_b are total channel resistance and total gate-channel capacitance at a given bias. The potential distribution as a function of time for step-function variation is given by*

$$\frac{\Delta v(u, T)}{\Delta v} = 1 - \frac{4}{\pi} \sum_{n=0}^{\infty} \left[\frac{(-1)^n}{2n+1} e^{-(2n+1)^2 \pi^2 T} \cdot \cos(2n+1)\pi u \right] \quad (6)$$

* General time domain treatment of Eq. (5) known as Fourier-, heat flow-, diffusion equation, etc. is given by Carslaw and Jaeger.²

From (6) the average potential of the line at time T is

$$\frac{\Delta v(T)}{\Delta V} = 1 - \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{1}{(2n+1)^2} e^{-(2n+1)^2 \pi^2 T} \quad (7)$$

This is a rapidly converging series, so that for $T > 1/3\pi^2 \approx 1/30$ only the first exponential term need be used. The potential distribution, i.e. the depletion region width, as it changes with time, is indicated in Fig. 1a. When $\Delta v(1,t)$ asymptotically approaches its limit value ΔV , the channel conductance $\Delta g(T)$, as can be concluded from (4), is determined by the average potential $\Delta v(T)$. As this happens for large T the first exponential term only of Eq. (7) can be used. The relative conductance error - i.e. the multiplication error - is equal to the relative difference from the asymptotic value,

$$\delta_m \approx \frac{8}{\pi^2} e^{-t / \frac{R_b C_b}{\pi^2}} \quad (8)$$

The error of this expression is δ_m^2 for $\delta_m \leq 0.1$, which is the range of interest.

As an example, for a field-effect transistor (2N2608, Siliconix) with $R_b = 1/G_b = 1000$ ohms, $C_b = 15$ pF, $R_b C_b = 15$ nsec, the multiplication error decreases to 0.6 percent at $t \approx \frac{1}{2} R_b C_b = 7.5$ nsec.

The charging current, referring to Fig. 1b and using (6), is calculated as

$$i_t = 2 \cdot \left(-\frac{1}{R} \frac{\partial v}{\partial t} \right)_{l=L} = 2 \cdot \left(\frac{1}{R_b} \cdot \frac{\partial v}{\partial u} \right)_{u=\frac{1}{2}} \quad (9)$$

$$= \frac{8 \cdot \Delta V}{R_b} \sum_{n=0}^{\infty} e^{-(2n+1)^2 \pi^2 T}$$

Higher terms $n \geq 1$, which add up to $i_t \rightarrow \infty$ for $T \rightarrow 0$ due to step function input assumed, vanish rapidly and contribute only about 20 percent of the charge supplied. To test the charging time experimentally the charging current was recorded, Fig. 2, for the field-effect transistor in the example given above. There is no high initial current due to finite rise time of the pulse generator and of the oscilloscope, and due to generator resistance. A somewhat faster decay than would correspond to the time constant $R_b C_b / \pi^2 \approx 1.5$ nsec results possibly from the fact that a fraction of externally measured C_b is concentrated at the channel ends (contacts and lead capacitance). This makes it difficult to estimate apparently small effects of channel end resistance and gate series resistance. The gate voltage variation applied was relatively large as used in multiplication, effecting a change in channel conductance of 1/3 to 1/2. There is no apparent effect of parameter voltage dependence on the transient, possibly due to the fact that the product $R(V) \cdot C(V)$ remains almost constant.

Fast Multiplier Circuit

The fast four quadrant multiplier circuit is shown in Fig. 3. The field-effect transistors are in a bridge configuration with the four-winding transformer, which makes possible compensation of charging currents irrespective of voltage dependent gate-channel junction capacitance. The charging current, equally divided between two channel ends, produces no output. (In the case of an asymmetrical field-effect transistor the difference in charging currents flowing to the channel ends would appear at the multiplier output.) The inevitable difference between charging currents of T_1 and T_2 flows from points 2 and 5 to ground through XF-3, the potential of these points remaining at zero.

(The extreme case would be with only one transistor in the circuit when the whole charging current flows to ground through XF-3 producing no output.) The output current flowing into the low input impedance of current amplifier is equal to the difference ΔI of channel currents for $x \neq 0$, $y \neq 0$. Bias adjustment is provided for conductance balancing of the two transistors, for $x = 0$, $y = y_{\max}$, zero output. In the arrangement shown the channels are driven symmetrically for maximum linearity, and current driving of channels can be used for temperature independence.

In a multiplier circuit the ratio of maximum pulse length to the multiplier solution time (i.e. to the minimum pulse length) is determined mainly by transformer design. Thus in a multiplier which has to process longer pulses, the solution time is solely determined by transformer rise time. A limiting factor in this respect is XF-3 in the current driving mode. A relatively high load resistance of XF-3 (two channels in parallel ≈ 500 ohms) requires high transformer inductance to satisfy the required L/R time constant. High resistance and high inductance result both in an increased rise time. Due to this, to obtain the solution time as determined by the field-effect transistor, a large pulse length to solution time ratio requires voltage driving of XF-3. With this, the output would have a temperature dependence equal to that of the channel conductance. It is about -0.4 percent / $^{\circ}$ C over a relatively wide range and should not be difficult to compensate.

The L/R and rise time requirements of XF-2 are easier to satisfy as it is terminated by the low input impedance (≈ 20 ohms) of the current amplifier.

The component and performance data of two multipliers for two ranges of pulse length to solution time ratio are given, for reasons of different possible applications, obtainable

performance and design criteria. The data (referring to Fig. 3) are given in Table I and corresponding current amplifiers in Fig. 4. Multiplier A is moderately fast for 0.1 - 2 μ sec pulse length and B a fast one for 20 - 100 nsec. For minimum residual signals and aperiodic response, current paths in the layout should be well defined. There should be independent returns for primary of XF-1 and XF-3, a common ground for secondaries of XF-1, XF-3, and a common ground for secondary of XF-2 and current amplifier. Capacitors from points 4, 6 to ground are needed only in case B to balance the stray capacitances of points 1, 3, 4, 6 for $y = y_{\max}$, $x = 0$. Output of multiplier B is shown in Fig. 5.

The field-effect transistors used are Siliconix 2N2608, p-channel, with $W_{00} = 3$ - 4 volts, $1/G_0 \approx 500$ ohms, $R_b C_b = 15$ - 25 nsec at $V_{go} = 1V$. They possess a high channel conductance-to-gate voltage linearity. They also have a high degree of channel symmetry (possibly due to S-shaped planar structure), which is essential with this method of charging current compensation. The asymmetry of a field-effect transistor can be measured in the fast multiplier circuit (B) with points 2, 5 shorted to ground by observing the residual signal for $x = x_{\max}$, $y = 0$ and reversing the channel leads.

Discussion

It is shown that the conductance and multiplication error due to finite charging time of the field-effect transistor decreases as $\exp(-t/\tau)$, with time constant τ equal to about $1/10$ of the product of junction capacitance and channel resistance. This results in minimum solution time of 10 - 20 nsec for typical devices, depending on the accuracy required.

The simple method for compensation of gate-channel junction charging

currents presented here is applicable to ac-coupled multiplier circuits only. However as noted before,¹ the charging currents are compensated in the 4-transistor bridge (using equal transistors), which can be dc-coupled.

The results of the preceding work¹ and this paper show that field-effect transistors make possible analogue multiplication with high speed, reasonable accuracy, and temperature independence.

The pulse amplitude multiplier (A) for pulse length range 0.1-2 μ sec described here is specifically intended for use in $E \cdot \Delta E$ particle identification systems. Simple resistance current adding networks can be used at multiplier and current amplifier inputs for determination of the product $(E+E_0 + K\Delta E) \cdot \Delta E$, with variable coefficients E_0 and K , often required in this application.

Acknowledgements

This paper represents a continuation of the work described by G. L. Miller and myself in Ref. 1. I am indebted to him for that collaboration as it resulted in the ideas presented here. The assistance of John D. White, Jr. from Johns Hopkins University in measurements on field-effect transistors and multiplier circuits is gratefully acknowledged. It is a pleasure to acknowledge many useful discussions with W. A. Higinbotham and R. L. Chase.

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TABLE I
Pulse Amplitude Multiplier Data

Multiplier			A	B
Solution time			0.1 μ sec	20 nsec
Pulse length range			0.1-2 μ sec	20-100 nsec
x - input max.			1.5 volts	1.5 volts
y - input max.			$i_y=0.6\text{mA}$, or 5 volts thru R_1	1.5 volts
Output ΔI max. to current amplifier			$\approx 125 \mu\text{A}$	250 μA
Amplifier output max.			250 mV	125 mV
Residual signal for $x = x_{\text{max}}$, $y = 0$			< 0.3 percent	< 3 percent
Transformers	XF-1,2,3	CORE Electrostatic Shield between Pr. and Sec.	POT S 35/23-3E FERROXCUBE YES	TOROID 208F250-3C FERROXCUBE NO
	XF-1, XF-3 XF-2	Windings (number of turns) Pr. Sec. Pr. Sec.	$\left. \begin{matrix} 30 \\ 2 \times 15 \end{matrix} \right\} \text{No. 30}$ $\left. \begin{matrix} 4 \times 2.5 \\ 10 \end{matrix} \right\} \text{No. 28}$	$\left. \begin{matrix} 4 \\ 2 \times 2 \\ 4 \times 1 \\ 2 \end{matrix} \right\} \text{No. 28}$
Resistors	R_1		8.2 k Ω	30 Ω
	R_2		1 k Ω	51 Ω
	R_3		1 k Ω	100 Ω
	R_4		∞	20 Ω
	R_5		∞	1 k Ω
Field-effect transistors used			2N2608, Siliconix	

Figure Captions

Fig. 1 a) Field-effect transistor (depletion region shown in lower half only)

b) Distributed RC-line equivalent of field-effect transistor

R = channel resistance per unit length

C = junction capacitance per unit length

Fig. 2 Charging current of field-effect transistor.
Reverse bias $V_{go} + V_{dif} = 2V$, $\Delta V = 0.5V$, pulse length 5 nsec. Pulse generator resistance + current measuring resistance ≈ 50 ohms.
horizontal scale: 1 nsec per division
vertical scale: 2 mA per division

Fig. 3 Four-quadrant pulse amplitude multiplier

Fig. 4 Current amplifier

a) for multiplier A, 0.1-2 μ sec

b) for multiplier B, 20-100 nsec

All capacitors should have low inductance.

Fig. 5 Fast multiplier (B) output. Both inputs maximum, pulse length 40 nsec.

horizontal scale: 10 nsec per division

vertical scale: 80 μ A per division

FIG. 1

FIGURE 2

Fig. 3

Fig. 4

FIGURE 5