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Si Pillar Structured Thermal Neutron Detectors: Fabrication Challenges and Performance Expectations

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ABSTRACT

Solid-state thermal neutron detectors are desired to replace ^3He tube tube-based technology for the detection of special nuclear materials. ^3He tubes have some issues with stability, sensitivity to microphonics and very recently, a shortage of ^3He . There are numerous solid-state approaches being investigated that utilize various architectures and material combinations. Our approach is based on the combination of high-aspect-ratio silicon PIN pillars, which are $2\ \mu\text{m}$ wide with a $2\ \mu\text{m}$ separation, arranged in a square matrix, and surrounded by ^{10}B , the neutron converter material. To date, our highest efficiency is $\sim 20\%$ for a pillar height of $26\ \mu\text{m}$. An efficiency of greater than 50% is predicted for our device, while maintaining high gamma rejection and low power operation once adequate device scaling is carried out. Estimated required pillar height to meet this goal is $\sim 50\ \mu\text{m}$. The fabrication challenges related to ^{10}B deposition and etching as well as planarization of the three-dimensional structure is discussed.

Keywords: Thermal neutron detector, pillar, boron-10, helium tube replacements

1. INTRODUCTION

Neutron detectors are required for numerous applications including astronomy, particle physics, homeland security and non-proliferation, amongst others. ^3He has been the workhorse for thermal neutron detectors for the last 50 years; however, it is now in low supply due to increased usage [1]. In addition to the issue with material availability, solid-state thermal neutron detectors have additional advantages over the currently used ^3He gas-based technology in their inherent insensitivity to microphonics, low voltage operation and small device footprint. These recent developments have led to a variety of R&D projects on semiconductor-based thermal neutron detectors. Several different designs of solid-state thermal neutron detectors are currently being investigated [2-6]. Our design is based on a high-aspect-ratio Si PIN diode pillar arrays filled with ^{10}B , which we have coined the "Pillar Detector" [7-16]. Moving from a gas medium to a solid-state material can dramatically reduce the size of the device by increasing the density of the neutron-absorbing material, which is attractive for hand-held applications. A comparison of the primary detector figures-of-merit for our device (after appropriate scaling) and ^3He tubes is shown in Figure 1. This paper includes a review of the Pillar Detector design and the fabrication methods used, along with a discussion of alternate methods and the ultimate performance.

2. NEUTRON CONVERSION MATERIALS

Thermal neutrons have a low probability of interacting with conventional semiconductor materials. An early approach for solid-state thermal neutron detection is to coat a semiconductor material with the thermal neutron absorber/converter material [17]. There are numerous figures-of-merit that need to be evaluated when comparing neutron-sensitive materials, including the energy of the neutron interaction (Q value), the thermal neutron cross-section and the additional energy dispersed during the interaction of neutrons with the material. For instance, in the case of gadolinium, the thermal neutron cross-section is 49,700; however, the reaction byproducts include electrons, x-rays, and gamma-rays, which can impact the noise within the device. Because of this fact, Gd is sometimes not considered optimal for thermal neutron conversion.

A simple way to evaluate neutron-sensitive materials is to look at the probability of interaction, which is a function of the material thickness t , $\eta_{int} = 1 - \exp(-t/mfp)$, where the mean free path (mfp) is calculated by the inverse product of N (the nuclei per volume) and σ (the microscopic cross-section). Candidate solid-state materials for use in thermal neutron detection are shown in Table 1. One approach led by a group of researchers at the University of Nebraska uses semiconducting ^{10}B boron carbide [6]. In contrast to a “bulk” approach, Kansas State University researchers utilize a 3-D structure referred to as silicon “perforation” technology with ^6LiF as the conversion material [2]. However, from Figure 2, it is evident that the highest probability amongst the candidate materials listed is the use of pure ^{10}B .

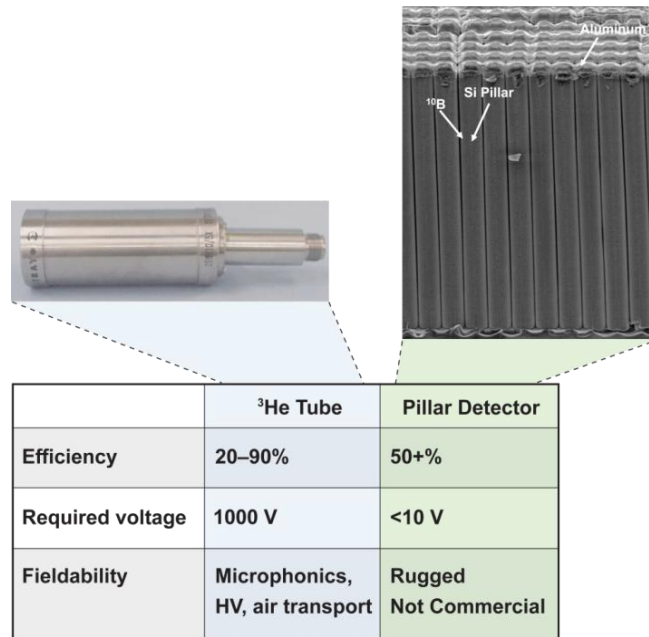


Figure 1. Comparison of the primary detector figures-of-merit for pillar structured thermal neutron detector and ^3He tubes.

Table 1. Candidate solid-state materials for use in thermal neutron detection.

| Material | Mean free path = $1/N\sigma$ [μm] |
|-----------------------------|--|
| Boron | 100 |
| $^{10}\text{Boron}$ | 18 |
| Boron carbide | 119 |
| $^{10}\text{Boron carbide}$ | 24 |
| $^6\text{Lithium}$ | 227 |
| $^6\text{Lithium Fluoride}$ | 172 |

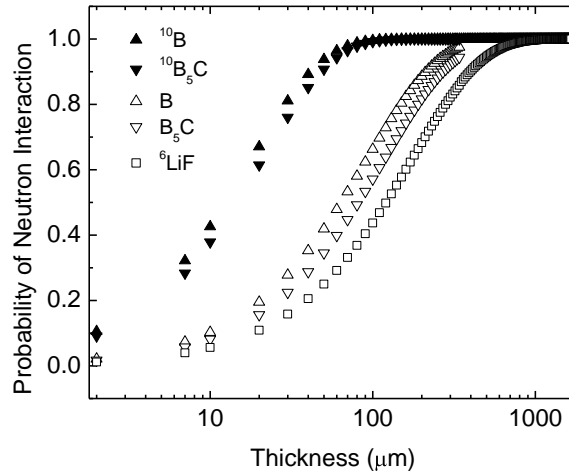


Figure 2. Probability of neutron interaction as a function of thickness of various solid-state neutron conversion materials.

3. PILLAR STRUCTURED THERMAL NEUTRON DETECTOR

Using a three-dimensionally integrated approach, very high detection efficiency is possible because the geometrical constraints on the converter material thickness and the resulting range of the energetic ions are decoupled [11], as shown in Figure 3. First, the thermal neutrons are converted to energetic ions by a material with a high thermal neutron cross-section. ^{10}B is used (its cross-section for thermal neutrons is $\sigma = 3,837$ barns), resulting in the following reaction: $n + ^{10}\text{B} \rightarrow \alpha + ^7\text{Li}$. Here the ^{10}B thickness is defined by the pillar height (etch depth) to absorb the thermal neutrons. About $50 \mu\text{m}$ of ^{10}B is needed to absorb most of a thermal neutron flux. Second, these energetic ions are collected using a semiconductor diode. The pillar pitch of $4 \mu\text{m}$ is defined lithographically to allow a high probability of interaction of the energetic ions with the semiconductor pillar. An efficiency of 20% [32] has been achieved with an array of etched Si pillars with 13:1 aspect ratio ($2 \times 2 \mu\text{m}^2$ pillars with a $26 \mu\text{m}$ height and a separation of $2 \mu\text{m}$) on a planar silicon substrate, arranged in a square matrix. One added benefit of this high-aspect-ratio design is that the so-called “streaming” of neutrons becomes negligible. When the 3-D Pillar Detector is scaled to $50 \mu\text{m}$, a high-efficiency device (>50%) is predicted, with a large neutron to gamma discrimination of 10^5 [10,11].

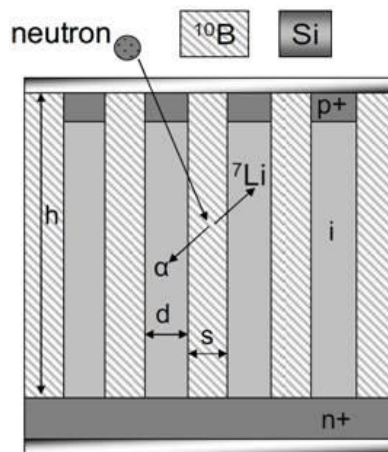


Figure 3. Schematic of a pillar structured thermal neutron detector, h: pillar height ($26 \mu\text{m}$), d: pillar size ($2 \mu\text{m}$), s: pillar separation ($2 \mu\text{m}$).

4. FABRICATION PROCESS AND CHALLENGES

The fabrication approach was developed to be wafer-scale-batch compatible and leverage commercial silicon processing techniques as much as possible. This section outlines an overview of the wafer specifications and processing flow with the subsequent subsections going into detail into specific boron deposition options, boron processing, and large-area fabrication and ongoing challenges. The fabrication process begins by epitaxially growing p+ and i layers on an n+ silicon substrate by chemical vapor deposition; alternatively, the PIN structure can be defined by utilizing float zone silicon with ion implantation. The pillar diameter and spacing are then defined lithographically, followed by plasma etching to create high-aspect-ratio structures utilizing an SF₆-based approach (Figure 4a). A conformal coating of ¹⁰B is then deposited on the pillar array by chemical vapor deposition. The ability to deposit a conformal and uniform coating of ¹⁰B [12] is one of the key steps to the success of the detector (Figure 4b). Next, the “etch-back” is carried out using a Plasmaquest electron cyclotron resonance etching (ECR) [13, 14] to expose the p+ layer for uniform contact formation [15]. Lastly, after the planarization of the sample, aluminum is sputtered onto the structures to fabricate the electrodes (Figure 4c).

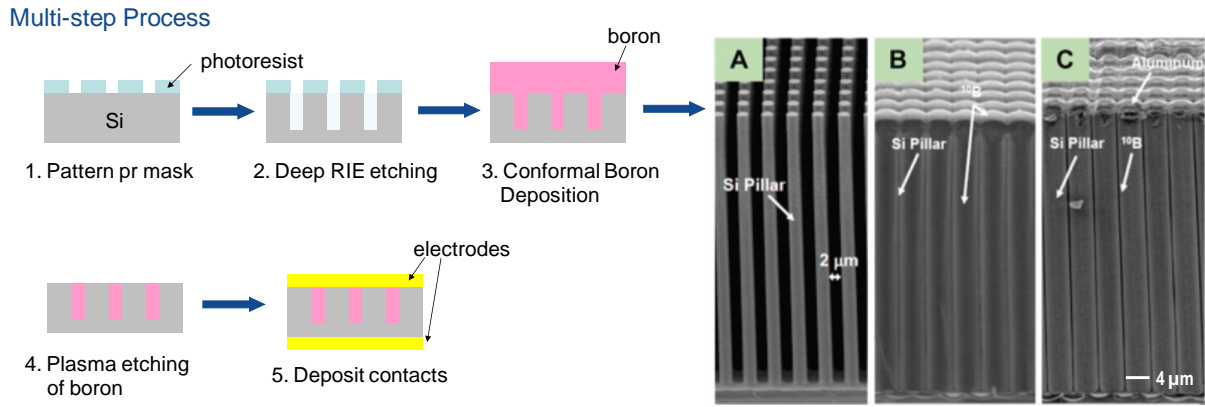


Figure 4. Process flow and SEM images of 50 μm silicon pillars structures: (a) as fabricated by etching, (b) after boron deposition, and (c) after etch-back of excess boron and aluminum evaporation.

4.1 Boron Deposition

Low-pressure chemical vapor deposition (LPCVD) is an attractive process to produce conformal thin films because it has the ability to coat substrate topographies (high-aspect-ratio trenches) uniformly and conformally [12, 18, 19] unachievable by most line-of-sight deposition techniques [20, 21] such as e-beam and thermal evaporation. Growth kinetics data for the pyrolysis of ¹⁰B enriched CVD precursors in different reaction temperature zones is crucial to determine the deposition parameters to conformally coat high-aspect-ratio pillar substrates with ¹⁰B films. For CVD reactions, there are two general types of reactions, as shown in Figure 5: 1) heterogeneous reaction in which the reaction happens preferentially on substrate surfaces and 2) homogeneous reaction in which the reaction occurs between the precursor molecules in the gas phase. For conformal coating, the thermal CVD deposition temperature should be preferentially chosen such that the reaction temperature is high enough to minimize incomplete decomposition of the precursor [22] but low enough to minimize homogeneous precursor decomposition and hence promote film growth on the surfaces, Figure 6. Experimentally, the temperature range to achieve these conditions is 425–475 °C for LPCVD.

The success for the development of a CVD conformal coating process also depends on the choice of a suitable precursor. Possible chemical precursor choices include decaborane, diborane [23], pentaborane, trichloroborazole, trimethoxyborazole, trimethylboron and borazine [24-26]. The empirical equation for the decomposition of decaborane is shown below.



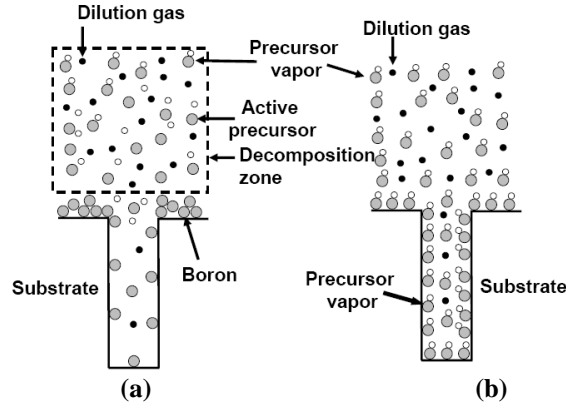


Figure 5. Schematics for (a) heterogeneous reaction and (b) homogeneous reaction during a CVD process.

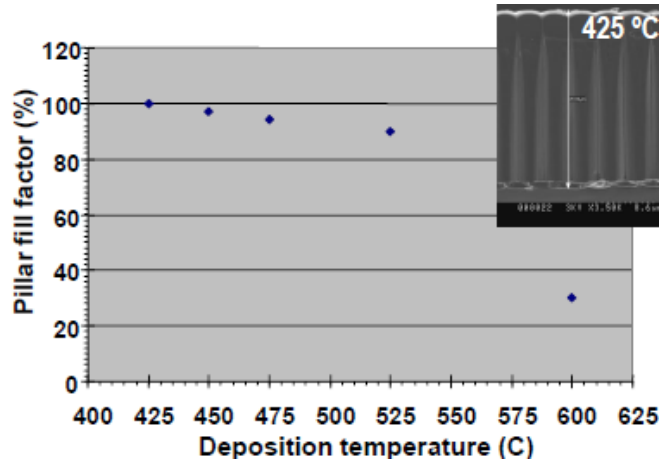


Figure 6. Pillar fill-factor as a function of CVD reaction temperature.

Other approaches for the deposition of ^{10}B films exist, as well. For example, cathodic arc deposition has been examined for the pillar structure [27], with the ability to coat 6 μm tall pillars (3:1 aspect ratio). This technique, however, is limited by formation of voids and sputtering of Si pillars. It appears unsuitable for deposition at higher aspect ratios. Electrophoretic deposition of B films for synthesis of MgB_2 superconductors has also been demonstrated [28].

4.2 Boron Etching

In order to realize the Pillar Detector, it is necessary to develop a controllable, repeatable boron etch process that yields a planar final morphology without damaging the underlying Si pillars. Previous plasma etching of boron has been performed using H-, Cl- and F- based plasmas for cleaning of thermonuclear fusion reactor chambers [29-31]. Rates realized in these processes are extremely low. High-density electron cyclotron resonance (ECR) plasma etching using both CF_4 based and pure SF_6 based plasmas to etch ^{10}B thin films was developed [13]. Fluorine based etches produce the energetically favorable and volatile BF_3 etch product, while the use of Cl_2 based etches would result in the easily dissociated BCl_3 product. The use of an ECR allows for rapid etch rates due to the high ion and radical density as well as the decoupled control of the plasma and RF powers. The use of SF_6 to achieve rapid etch rates with high selectivity to the underlying Si pillars was further examined, with the addition of H_2 and O_2 gases, because Si readily etches in F-based chemistries [14]. The use of O_2 in a ratio of 1:2 $\text{SF}_6:\text{O}_2$ was found to result in rapid removal of ^{10}B , with an etch rate in the range of 0.5–1.2 $\mu\text{m}/\text{min}$, depending on etch parameters. Using this chemistry, there is a negligible etching of the Si pillars, which yields flexibility in etch time duration for device fabrication. Figure 7 shows the pillar tops after (a) over-etching with only SF_6 (poor selectivity) (b) over-etching with 1:2 $\text{SF}_6:\text{O}_2$ and (c) a well-timed etch with 1:2 $\text{SF}_6:\text{O}_2$. It can be observed that for (a) the Si is recessed within the ^{10}B coating, while for (b) the Si protrudes from the surface.

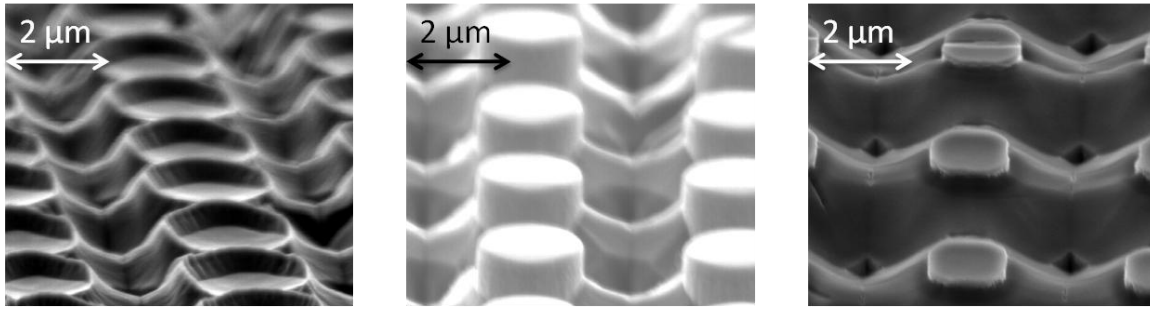
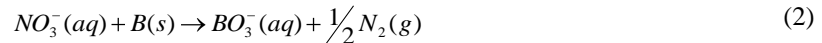


Figure 7. The pillar tops after (a) over-etching with only SF₆ (poor selectivity) (b) over-etching with 1:2 SF₆:O₂ and (c) a well-timed etch with 1:2 SF₆:O₂

In addition to high-density plasma etching, other possibilities exist for ¹⁰B removal. Other typical methods of material removal used in microfabrication include mechanical/chemo-mechanical polishing or lapping and wet etching. In the former, a slurry of liquid (e.g., water) and abrasive (e.g., 3.0 μm Al₂O₃) grit are used to physically remove the material. Chemical assistance may or may not be used. For a three-dimensional structure this approach proves difficult. First, the exceptional hardness of boron (40+ GPa) makes removal difficult. Second, the need to avoid removal of any appreciable amount of silicon would require precise timing and precise uniformity. Lastly, the shear force during the lapping process has been seen to break the high-aspect-ratio pillars. Therefore, it is a less desirable alternative to plasma etching.

In the second case, wet-etching of boron can be accomplished through the use of an oxidation agent, such as nitric acid. It is expected that boron etches in nitric acid at elevated temperature through a two-step process: (1) oxidation and (2) dissolution of the oxide, as shown below:



B₂O₃ is known to have a high solubility in water. The process must take place at elevated temperatures, as boron is known to be resistant to oxidation at room temperature, although this is likely dependent on crystallinity, purity, and porosity, amongst other parameters. Once the reaction begins, it has been observed that it proceeds rapidly. This fact, combined with the inevitable gaps without the 3-D structure, result in removal of the boron from the entire structure and not merely from the top.

4.3 Ongoing challenges

Large-area compatible processing for the Pillar Detectors is required for commercialization. Lithography and deep reactive ion etching for 26 and 50 μm pillars in 4-inch wafer scale (Figure 8a) has been successfully developed. The boron CVD deposition conditions need to be optimized in terms of high fill-factor and boron stress. Optimized boron deposition time and temperature result in large boron fill-factor as well as a flat and uniform boron layer covering on top of pillars as shown in Figure 8b. Non-optimized deposition of boron CVD conditions can produce poor fill-factor and a very thick boron layer on top, which can delaminate to expose pillar tops, which are shown in Figure 8c. Due to the nature of the boron ECR etch as well as the initial film morphology and nonuniformity across the sample, the resulting surface may possess topography on the order of 1–3 μm. Directly metallizing this structure can be problematic and can lead to electrically shorting out the pn junction, if planarization is incomplete [15]. To solve that problem, a planarization process utilizing spin-on polymer fill and lapping back to expose the tops of the pillars was developed. The spin-on polymer (ACCUFLO 2027) was spun on samples followed by high temperature bake at 200 °C repeatedly until the top surface was fully covered by polymer. Chemical mechanical polishing was applied to remove extra polymer with very fine size of alumina abrasive (0.05 μm). A similar process to expose the tops of the pillars can be done by using an oxygen-containing plasma. Figure 8d shows the SEM of planarization. The gaps created by the boron CVD and the ECR etch are completely covered by spin-on polymer, and pillar tops are properly exposed for metallization.

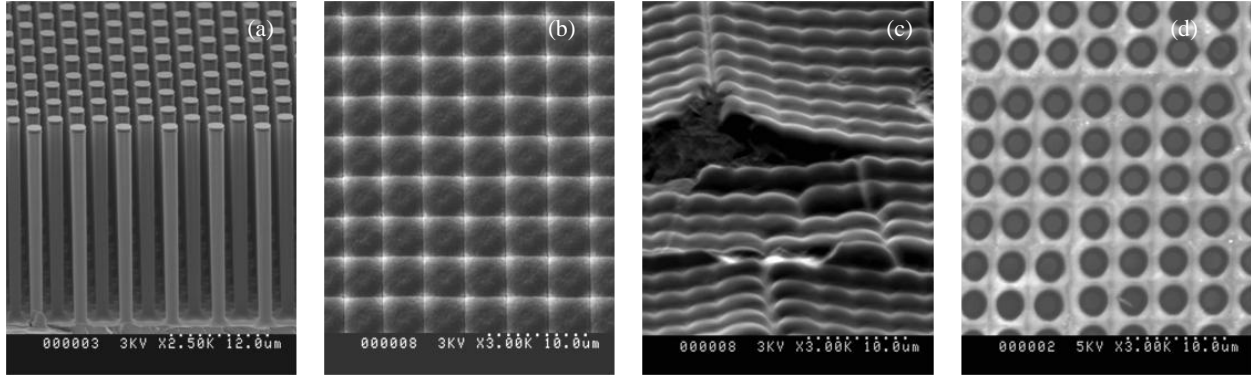


Figure 8. Scanning electron microscopy pictures of fabrication process of high-aspect-ratio pillar etch, 26 μm pillar height, 2 μm pillar width and separation (a), optimized boron CVD (b), non-optimized boron CVD (c), and planarization by spin-on-polymer (d).

4.4 Device performance

Current versus voltage measurement was performed on a detector with 2 μm diameter pillars with 2 μm spacing and 26 μm pillar height (Figure 9a). The Si portion of the detector is based on a layer structure of 3 μm p^+ layer, 22 μm intrinsic layer and n^+ substrate. Low reverse-biased current density of $1.2 \times 10^{-4} \text{ A/cm}^2$ was measured at -3 V. Low leakage current is essential for high sensitivity to neutron events because this contributes to the noise floor of the device. The leakage current is composed of bulk and surface components. The reverse-biased current density of an unetched planar diode structure is on the order of 10^{-7} A/cm^2 , implying that the increase in leakage current is due to surface recombination or stress-induced bandgap narrowing. Further reduction of the leakage current can be achieved by passivating the pillar sidewalls [16]. The intrinsic region has a free carrier concentration of 10^{13} cm^{-3} , which requires -10 V for full depletion. Capacitance versus voltage characteristics were also measured and are shown in Figure 9b. Both leakage current and capacitance can produce background noise. Minimization of background noise requires a careful balancing between both the leakage current and capacitance of the detector, which are proportional and inversely proportional to the square root of the applied voltage respectively.

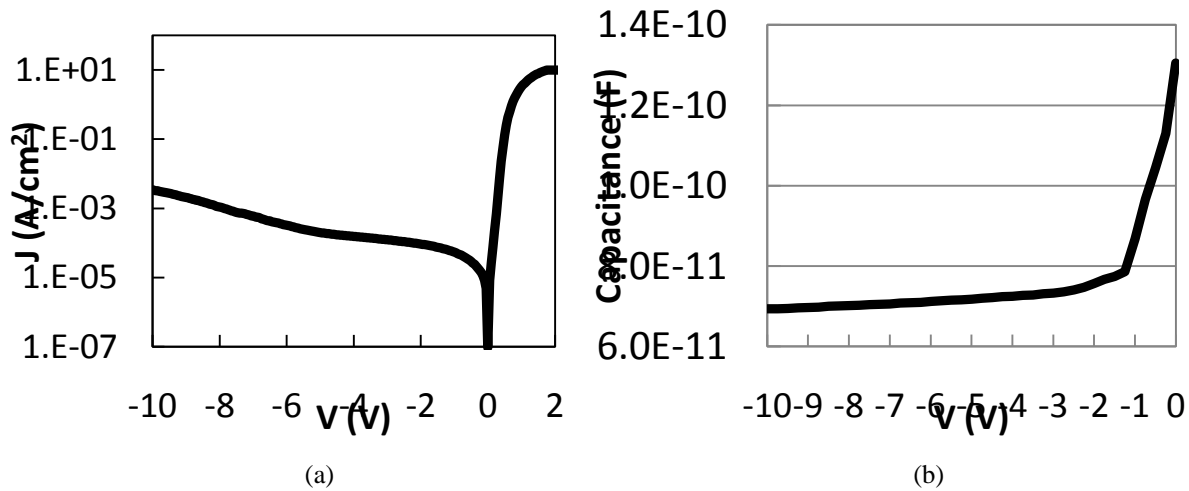


Figure 9. Measured current-voltage (a) and capacitance-voltage (b) characteristics of 26 μm tall Pillar Detector.

Measured neutron and gamma detection spectrum of the pillar structured thermal neutron detector with 26 μm tall pillars and 2 μm pillar width and separation are discussed in this section. The neutron response was measured using a ^{252}Cf fission neutron source with intensity of 2×10^6 neutrons/sec and moderated by 6 inches of polyethylene blocks of to yield thermal neutrons. This measurement was done with rack-mount electronics; the measurement time was 12 hours, with a 0.5 microsecond shaping time. The energy was calibrated with $^{243-244}\text{Cm}$ source, which has an alpha energy peak of 5.5 MeV. Because the neutron source strength decays over time, the calibration structure was re-measured to determine the current thermal neutron source strength using the known standard efficiency of 7.3% [10]. Using this source strength

and the measured neutron counts/min, the efficiency is determined. Specifically, the detection efficiency was determined by integrating all counts above the noise level of 110 keV, which gives a thermal neutron detection efficiency of 20% at -3 V, as shown in Figure 10.

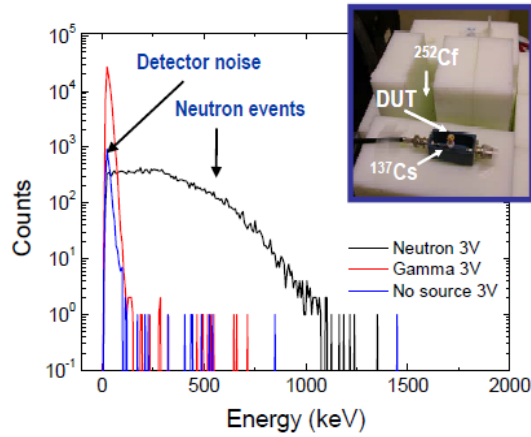


Figure 10. Measured neutron and gamma detection spectrum of the pillar structured thermal neutron detector. The inset shows the test configuration.

The performance of the nine-element detector was determined by measuring both the current-voltage characteristics and thermal neutron response. This is shown in Figure 11 [31]. The neutron measurement was done using a ^{252}Cf source moderated by placing the source within a heavy-water-filled moderating sphere. The detectors were placed 1.5 m from the source. The detectors were measured at 0 V for 3000 s. Integrating the total counts above the background yields 14 counts/($\text{cm}^2 \times \text{sec}$).

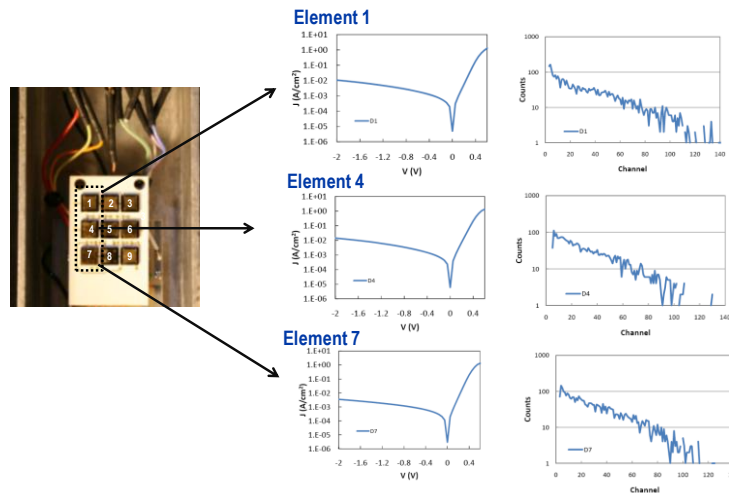


Figure 11. Nine-element detector. Each detector has an active area of 2 mm x 2 mm. Current vs. voltage and thermal neutron response are shown for the first column of the 3 x 3 set.

A nine-channel portable readout chain was built using a custom design based on a well-known topology [33] that includes the charge sensitive preamp, shaping amplifier, low-level discriminator and driver circuit for TTL output. Figure 12 shows a picture of a 3 x 3 array of detectors integrated into the nine-channel readout system and the efficiency of the detectors being used. The fast shaper uses a semigaussian, fourth-order bipolar shape with 250-ns peaking time, which was chosen to minimize the dominant noise component, the noise associated with the detector's dark current. Bipolar shaping poses a penalty to the white (high-frequency) noise components but is more tolerant to the lower frequency components [33] and offers intrinsically better baseline return than unipolar signals, mitigating the need for a baseline restoration circuit. Additional logic gates combine the event detection signals from any of the nine channels to

give an overall detection rate response or a detection rate per-channel. Multiplicity counting can also be easily implemented by external logic. Using an unmoderated isotropic ^{252}Cf source with an activity of 5×10^5 n/s placed 7.5 cm from the nine-element detector with 5 cm of high-density polyethylene above and below, a count rate of 6 cps was obtained. Subsequently, an ASIC was designed to implement the readout functionality with 8 channels in a 4.2×4.2 mm² area. The ASIC implementation combined with the Pillar Detectors is expected to provide a compact, low power, scalable alternative to ^3He tubes for handheld applications.



| <i>Detector</i> | <i>Efficiency</i> |
|-----------------|-------------------|
| 1 | 22 |
| 2 | 23 |
| 3 | 16 |
| 4 | 16 |
| 5 | 20 |
| 6 | 19 |
| 7 | 18 |
| 8 | 20 |
| 9 | 20 |

Figure 12. Nine-channel COTS readout integrated with nine-element Pillar Detector array.

The detection efficiency for a solid-state neutron detector is determined by the counts above the threshold energy divided by the number of incident neutrons. To extrapolate the potential efficiency of the Pillar Detector 3-D numerical simulations were performed [11]. These simulations included MCNP for the neutron histories, SRIM for the energy loss for alpha and ^7Li in both the ^{10}B and Si portions of the detector, along with 3-D finite element TCAD software package (Silvaco’s Atlas) to calculate the transport of the electrons and holes generated by the alpha and ^7Li particles in the Si diode portion of the detector. Figure 13 shows a general trend of how efficiency scales with pillar height and agrees with our experimentally obtained efficiency numbers showing the ability for the Pillar Detector to scale to higher efficiencies.

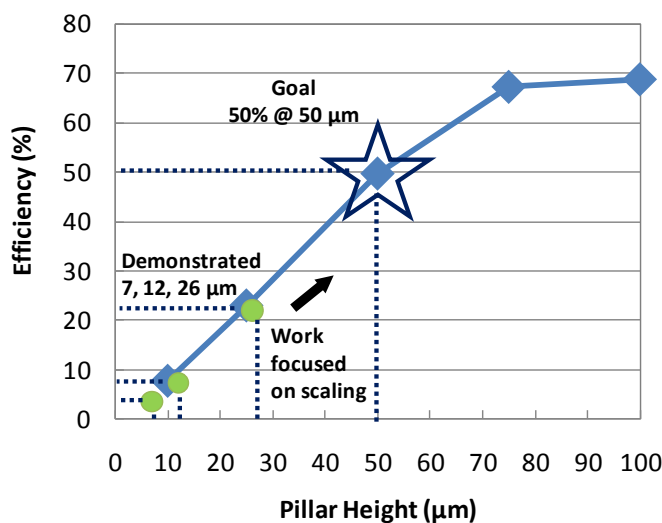


Figure 13. Relationship between thermal neutron efficiency and pillar height (pillar width and separation of 2 μm). The solid line shows the simulated efficiency while the circles show the measured data.

5. CONCLUSION

We have shown that semiconductor-based neutron detectors can be a ^3He replacement for small-form-factor applications. Silicon is an ideal material system for electron/hole collection, and ^{10}B is an ideal neutron conversion material due to its high thermal neutron cross-section and compatibility with silicon foundry processing. The critical process steps for this structure include the deposition and etching of ^{10}B . Chemical vapor deposition has been successfully developed for high-fill-factor conformal coating on high aspect ratio structures while plasma etching of the ^{10}B has been developed using a fluorine- or chlorine-containing mixtures. High-aspect-ratio structures of $2\ \mu\text{m} \times 2\ \mu\text{m}$ pillars, with a $4\ \mu\text{m}$ pitch achieves 20 % thermal neutron detection efficiency, and we have shown how this structure can be scaled to high efficiency. By increasing the pillar height a 50 % efficiency device is possible.

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