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REPORT ON THE LOGICAL DESCRIPTION OF THE SPARK CHAMBER READER

GEORGE SCHWENDER

MASTER

June 1964

BROOKHAVEN NATIONAL LABORATORY
ASSOCIATED UNIVERSITIES, INC.

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**BROOKHAVEN NATIONAL LABORATORY
UPTON, NEW YORK**

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Introduction

The spark chamber reader is an automated system for optically scanning 35 millimeter film used for recording the events produced by a spark chamber experiment. The optics provide a spot of light, 8 microns in diameter. Two scanning positions are incorporated, for a normal and orthogonal scan. The scan is accomplished by having 16 lenses mounted in a rotating wheel; as each lens passes across a cone of light produced by a mercury arc, a light spot is generated that sweeps across the film. The light passes through the film, is then monitored by a photomultiplier tube at each window for the determination of the data points. A data level control is provided to account for different grades and development times of film.

Each frame of film is metered precisely to one window, digitized, and then metered again for the digitization in the second window. The machine is flexible and can produce either a single or double scan, according to the requirement of an experiment.

After metering to a window, the stage carrying the windows is moved at a uniform rate, thereby producing an axis of motion. The movement of the light beam produces the second axis of motion.

When a data point is recognized, both the X and Y addresses are placed in a core memory which transfers, with additional data addressing, onto magnetic tape for processing by the IBM 7094 computer.

The system has the additional facilities for incorporating indicative data, registration of frame and reel number, indications of machine malfunctions or overflows on its data handling capabilities. In addition, the system as a whole embodies a preselection mode of operation.

Preselector

This unit of equipment consists of a film transport, viewing screen, paper punch, frame registration and frame and reel number sensing circuits.

The operator, when viewing the frame, makes the decision as to its usefulness. If the information is useful, a readout of its frame and reel number is recorded on punched paper tape. Upon completion of this operation, throughout the reel of film, the film and punch paper can be mounted on the digitizer. The digitizer then will search for the addresses as called for and digitize only those frames. This entire preselection mode of operation may be omitted and film can be placed directly on the digitizer and have each and every frame digitized.

SECTION I

GENERAL DESCRIPTION

Drawing Number

IH - 258

Purpose:

This report was written to provide a detailed description of the spark chamber reader.

Optical System

The layout of the optical components are shown isometrically in Figure 1. A fixed illuminated pinhole is demagnified by a factor of ten onto the film; motion of the lenses produce the scan line. Sixteen microscope objectives which have large numerical apertures are placed around the circumference of a rotating disk with their optical axis parallel to and 145 millimeters from the axis of the disk. As long as an objective is passing through the cone of light emanating from the pinhole, it focuses a spot of light onto the film.

There are three independent optical channels; two provide for the normal and orthogonal scans of the film. The third channel focuses onto a transmission grating which provides the x-coordinate of the scan by digitizing the position of the disk. A high pressure mercury arc lamp is the source of light for all channels. In each the light is collected and made parallel by a 210 millimeter F 3.5 camera lens. These are followed by a 150 millimeter F 2.3 lens which converges the light onto the pinholes and demagnifies the 300 micron square arc to about 200 microns.

The two scanning positions are located so that the microscope objective has rotated 45° to the edge of the film and in their being perpendicular to each other giving a normal and orthogonal scan.

Y motion is obtained from a precision stage to which

the film is clamped by a vacuum platen. It is digitized by a Ferranti Moire' Fringe Grating System. The combination of the x and y motions produces a cycloidal projectory of the spot on the film.

The start of digitization for a particular scan is a signal produced by the spot which makes the scan. To do this, just before the spot starts onto the film it is interrupted by a 45° silvered prism which deflects the light through a second ten powered microscope objective which remagnifies the spot back up to the original pinhole size. This spot then passes over a slit generating a begin-of-scan pulse. Light intensity is sensed in all channels by ten stage RCA 6199 photo multiplier tubes.

The disk is driven by a belt powered by a synchronous motor at 520 rpm. This then generates one scan line every seven milliseconds with a spot actually scanning for a period of four milliseconds.

Film Transport System

The film transport system which is shown schematically in Figure 2 handles 35 millimeter perforated film. The supply and take-up spools are buffered from the rest of the system by 45 centimeter long vacuum columns. These spools are driven by continuously running motors which are clutched in and out on command from pressure switches on the columns. Between the columns the film is driven by a sprocket drive capstan which in

turn is driven by a reversible motor through an electrical brake-clutch assembly.

The film motion sequence starts when a frame passes through the projector and frame registration marks are sensed by a matrix of photo diodes on the screen. At this time metering of film is commenced through the rotary encoder mounted on the drive capstan shaft. The film is metered to a precise distance, the normal window, where it is clamped to the stage and the normal scan of the frame is begun. When this is completed film is released and advanced to the orthogonal window where once again it is clamped and the stage motor starts the driving of the stage in the reverse direction. Upon completion of the orthogonal digitization, the film is unclamped and the capstan motor returns the film to a position one half of a frame width ahead of the projector. The film is advanced again until the next frame is registered and the process is repeated.

The film travels at two variable independent speeds, in the advance mode its speed is approximately 20 centimeters per second and in the reverse mode its speed is approximately 43 centimeters per second.

Spark Chamber Format

The format for a typical spark chamber photograph is shown in Figure 3. The two squares in the upper right hand corner is the frame registration mark. The coding at the bottom is the frame and film number in a binary coded decimal system.

These are read by the photo diodes on the screen immediately upon sensing frame registration marks. The relative positions of the photo diodes can be adjusted to match any overall magnification.

Photo Multiplier Output

The signals directly at the output of the various photo multipliers are shown by the oscilloscope traces in Figure 4. The parameters for these tracers were as follows:

disk speed 520 rpm

all pinholes 55 microns (this yielded a measured spot size of 7.5 microns and a stage speed of 60 micron per scan)

The x grating used had a 17 micron cycle with the clear and opaque portions approximately equal at 8.5 microns.

The upper left-hand oscilloscope pattern is the x grating signal at two different sweep speeds. The upper shows the entire passage of one spot across the grating. The individual crossings of the grating lines are not visible but this envelope shows a light modulation of about 75%. The shrinkage of light intensity as one moves away to either side of center is caused by the vignetting of the light by the microscope lenses and is not due to defocusing of the light spot. The lower trace is a portion of the upper one with a sweep speed sufficient fast to show the individual crossings. The next photograph down is again the x grating, but with the scans produced by all sixteen objective lenses. These first two patterns were taken with 85%

of the available light removed by a uniform neutral density filter placed over the photo multiplier.

To remove the effect of the vignetting, a non-uniform filter was placed over the photo multiplier to replace the uniform one. This was produced by placing unexposed photographic film over the tube and exposing it to the light from the wheel. With the non-uniform filter in place the x grating signal shown in the lower left of Figure 4 was obtained. In the upper right trace the start-of-scan is shown just below the x grating pulse. The next pattern down, again shows the start-of-scan pulse and above it the output of the photo multiplier behind the film platen when no film is in place. The last pattern was taken with film in place and containing one data point on the scan.

The Data Processing Unit

One function of this unit is to register the begin-of-scan, x and y pulses and data pulses from the photo multiplier tubes, store and then write these coordinates on magnetic tape. Secondly, it commands and supervises all stage control functions such as the movement and clamping of film, starting and stopping of the capstan and stage motors and monitors all safeguard checks of the machine. Thirdly, it provides for the insertion of indicative information, command for the search mode and for preselection of frame and reel numbers that are to be digitized. An abbreviated block diagram of the logic for the data processing unit is given

in Figure 5. Starting at the upper left-hand side of the block diagram the x pulses derived via the picket fence are gated into the x scaler after the begin-of-scan has occurred. During the scan if a data point is detected it will initiate the track centering circuit. This will then gate the contents of the x scaler into the memory register and set the data flip-flop. At the completion of a scan the end-of-scan pulse will then take the contents of the y scaler and deposit this information into the memory register.

Memory Register

The memory register can receive four types of information. The coordinate of the scan (x-scaler), the stage motion (y scaler), indicative information and frame and reel number. Indicative information may be placed upon the tape by a series of switches at the console and will be at the head of all data particular to a file. This information may have any format. The fourth input, frame and reel number, is a bookkeeping function. Upon receipt of either one of the four inputs to the memory register, the interlace is notified of a write command. The interlace will control the function of reading or writing upon the core. The core is a 256 word 18 bit unit.

The Write Cycle

On a write command the interlace circuit receives the initial request. The write-address register will be stepped by

one unit. Then the decoding of the bilateral switches, and the activation of the write driver and bilateral switch will take place. Depending upon the state of the memory register, the inhibit winding will or will not be activated thereby depositing zero or one in the core.

Read Cycle

On the completion of writing 128 words, the write-address register makes a request via the interlace for the initiation of the read-out and also sends a command to the tape control to start the magnetic tape system. The interlace will step the read-address register. This register will be decoded for setting up bilateral switches and the read drivers. It will also produce a strobe for sensing the information in the core and depositing it, via the sense amplifier, to a magnetic core buffer. At this point the core buffer proceeds to place this information, via the tape control circuitry, onto the magnetic tape. This loop will continue until 128 words have been read out of the core. The read-address register will then send a stop command to the tape control unit and inform the interlace circuit. Within the tape control there is provision for the production of a parity character, a longitudinal redundancy check character, end-of-file and end-of-tape. This tape then will have, for a particular frame digitization, many records of 128 words. The file itself will have, within the first record, indicative

information if required; followed by frame and reel number; then the digitization of the normal window immediately followed by the digitization of the orthogonal window, end-of-file and when required the end-of-tape indication.

Track Centering

The data pulse does not appear at the moment the spark is crossed, but instead at some constant distance beyond its center. The method by which the center of the spark is located is explained in Figure 6. An independent track centering scaler is used and when it is full, the overflow pulse causes the data point to be read. It is fed at twice the normal frequency while the spot is transversing the spark, and at four times normal frequency thereafter; thus making the distance from track center to data point independent of spark width. The capacity of the track centering scaler can be adjusted to match the maximum spark width that is expected. Should the spark width exceed the capacity of the scaler, no data is read.

Measuring criteria of the Reader

x count equal to 8.5 microns

size of a spot - 7.5 microns

y count equals 20 microns

tape speed - 60 inches per second

Write cycle time approximately 7 microseconds

All modules were purchased from the Digital Equipment Corporation.

Machine Structure

Figures 7 through 10 give the conformation of the machine. Figure 11 is the first event digitized. Only the normal window position was used with the 45° scan line running generally from lower right to upper left. In figure 12 is shown the face of the cathode ray tube on the 7094 which displayed the event after it had been scanned and transformed from the cycloidal system into the rectangular coordinate system.

The Computer Programs

A program has been written for the IBM 7094 Computer to analyze events obtained from the spark chamber. For example an experiment from a circular spark chamber is now being run to specifically analyze K+P elastic scattering to obtain the differential cross section as a function of scattering angle.

The individual sections of this program do the following:

1. Read a single file from the source magnetic tape.
2. Locate fiducials.
3. Transformation of data into rectangular coordinates.
4. Transformation of orthogonal view data points onto coordinates of the normal view.
5. Sort data in circular sectors.
6. Locate sparks in sectors. Construct tracks from sparks.
7. Reconstruction of the event.
8. The kinematic analysis of particle interaction.

The estimated running time for the above program is approximately 1 second.

SECTION II

DETAIL DESCRIPTION

DATA PROCESSING UNIT

X DATA PULSE

This originates from the photo multiplier that is monitoring the light beam transversing the film during a scan. If the photo multiplier detects a transition from a light area on the film to a dark area, it will start initiating the track centering circuitry. The output of the track centering circuit will produce the "x data pulse" into the data processing unit.

X SCALER PULSE

This set of pulses is generated via the picket fence in association with the light spot.

BEGIN OF SCAN

This pulse is initiated once, previous to entering the area of the film where digitization is to take place.

Y COUNT

This set of pulses originates from the Ferranti system in association with stage movement.

The input pulses to the data processing unit are conditioned on the following:

- no stage error
- digitization allowed
- scan started
- allow Y scaler

Describing the logic now on page 1 of the DPU drawings.

The initiating pulse will be the "BEGIN-A-SCAN." The begin-of-scan originates when the light beam is about to enter either the normal or orthogonol window. If the begin-of-scan is from the normal window, pulse generator S-12 will be fired, if it is originating via the orthogonal window, pulse generator S-13 will be fired. Either one being fired is an input to an AND circuit. Inputs J and K for the normal and inputs N and M for the orthogonal on AND circuit 1-14. The internal logic of the stage control prepares one of these gates to be made. Assuming we are in the process of digitizing the normal window, the K lead of AND circuit 1-14 will be made. Note that the normal/orthogonal flip-flop would have to be in the normal position or the single scan/double scan flip-flop in the single scan mode. Either one of the above would produce the ALLOW on input K of 1-14. The output of 1-14 will fire an inverter 2-18. If we had been using the orthogonal, the N condition of 1-14 would have been made and it would also drive the inverter 2-18. The output of 2-18 which arrives at the AND circuit 2-15, passes on if no stage error has been applied to the machine and the allow digitization condition has been applied. The "BEGIN-A-SCAN" will pass through to set the allow x scaler flip-flop 2-21; in addition it will fire PA 2-14, the output of which examines two AND gates, one of

which will be made depending on which window is being digitized. In the case of the orthogonal, 1-14 T output will be achieved. If it had been a normal, 1-14 W would have been achieved. In the case of the orthogonal window, T output then fires a delay 2-19. Or, in the case of the normal, would have fired delay 2-23. In either case delay 2-20 is fired. Consider a scan for the orthogonal window and 2-19 and 2-20 are fired. Delay 2-19 has a delay of approximately 2.5 milliseconds. This is to delay the setting of flip-flop 2-21 which allows the entry of data. This in essence allows the light to scan the lower section of the frame and not allow data to be received, in effect blanking out that area of the film. This area of the film will contain the frame and reel number. After 2.5 milliseconds, flip-flop 2-21 is set and the allow data condition will be made. Delay 2-20 takes roughly 4 milliseconds before an output is achieved. This allows the scan to transverse the entire window. At the end of this time 1T will reset the allow data flip-flop 2-21 and prevent any additional data from entering. In like manner, if we were considering the normal scan, delay 2-23 would reset flip-flop 2-21 immediately but would, after 1.4 milliseconds, set it on once again, delay 2-20 acts as before, thereby blanking out the upper and lower sections of film.

When the allow x scaler flip-flop and the allow data flip-flop are in the allow states, x data incoming pulses may proceed further. Initially, the allow x scaler flip-flop is set

immediately upon receipt of the begin-of-scan; and via the AND circuit 2-4, the DPU is now conditioned for receipt of the x scaler pulses. At this point we have a frequency doubling circuit consisting of OR circuit 2-10, PA 2-1, delay line 2-6, and inverter 2-9. The final output of the PA will have a frequency that is twice that of the incoming scaler pulse. The x scaler pulses now pass through AND circuit 2-10, inverter 2-9 to the input of the x scaler on page 2.

Consider that a scan is being made and the x scaler input pulses are being registered via the x scaler, and that an x data pulse occurs. It will pass through the AND 2-4, inverter 2-9 PA 3-15 and arrive at the input of the delay 2-11. PA 3-15 will also set the data flip-flop 2-22. The immediate output J of delay 2-11 will set the count of four flip-flop 2-7 and clear the memory register. The setting of the count of four flip-flop will inhibit the x scaler pulses from arriving at the x scaler, thereby allowing static gating of the x scaler to memory register. Its Z output allows, via AND 2-10, the scaler pulses to be applied to PA 2-1. The first pulse arriving would then set the first stage of the count of 4 scaler 2-12 into the one state. The next incoming pulse would then change that flip-flop from 1 to 0 and the carry of that stage would set the second binary bit of the count of four scaler. The next incoming pulse would again set the first bit of the counter, then on the

fourth incoming pulse to the count circuit, this pulse would be allowed to pass through 2-4 AND circuit, inverter 2-9 to pulse generator 3-3. The output of this pulse generator would insert the count of four into the x scaler and reset the count of four flip-flop, thereby allowing the x scaler from the stage to once again single count the x scaler. This all occurs by virtue of receiving an x data pulse. The delayed output of 2-11 approximately 2 microseconds later, produces a pulse that is called X to MR. This pulse will fire PA 3-6, gating the contents of the x scaler into the memory register.

As a result of receiving a data point during a scan, the data flip-flop 2-22 had been set. And before furthering that line of thought, let us regress and follow the Y count chain. Originating from the Ferranti, the Y count is applied to pulse generator 2-13, passing through AND 2-15 conditioned on allow "Y" scan flip-flop 2-22 and no stage error. This pulse then will be applied directly to the Y scaler. It will also be applied to AND condition 3-11 input M.

As described before if during a scan a "X" data pulse occurs it will set the data F/F 2-22 on-placing an allow on 2-15 W and the pulse from delay 2-20 would in turn activate delay 2-16 which would reset the x scaler, counter of four register, track centering and completes the AND condition 2-15X. Delay 2-24 would then initiate the reset memory register, reset the data F/F and command Y to memory register.

X SCALER

This logic may be found on page 2 of the DPU logic. The x scaler pulse from page 1 arrives at the input of pulse amplifier 3-3 and this amplifier then feeds the first stage of a 13 binary bit scaler consisting of flip-flops 3-5, 8, 10, and 12. The x scaler reset pulse arrives from page 1 at the completion of each scan to the OR circuit 3-1 passing on to pulse amplifier 3-6. This pulse will reset all 13 binary bits to the zero state. The count of four arriving from page 1 comes into pulse amplifier 3-6, inverter 2-18 and will come in to the input of the third binary bit of the x scaler.

Y SCALER

All the logic for the Y scaler may be found on page 3. The Y scaler pulse originating from page 1 is applied to pulse amplifier 3-15, the output of which is impressed via inverter 5-9 to the input of the first stage of the Y scaler which is another 13 bit register. Pulse amplifier 4-3 is for resetting the Y scaler to the one state, after which the delayed output of 6-14 counts it by one which clears the Y scaler. The Y to MR pulse arrives at pulse amplifier 4-3 and through the AND gates 4-7 and 4-11, gates the contents of the Y register into the memory register. On both the x and y scaler an engineering display panel gives the visual display of the setting of both scalers.

FRAME REGISTRATION (Drawing page 5)

Upon searching for a frame registration, the capstan motor will be given a start of film forward. This will set flip-flop 6-21 allowing one of the inputs of the AND circuit 6-9 to be made. On receipt of the frame registration, via the stage, the pulse from the AND circuit 6-9 will be applied setting flip-flop 6-15 which sets the post-write-disturb gate 6-17. Also it will initiate delay 6-13. Its immediate output resets the memory register and after a 5 microsecond delay AND circuits 6-17 will be tested. W will be made at this time. This in turn will fire pulse amplifier 6-16 J which gates the contents of the frame number into the memory register. It also checks the condition of the error flip-flop and if set in the error mode will transmit to the memory register an error indication. Delay 6-13 also applies through 6-9 and 6-14 a pulse, frame to MR. This pulse will initiate the writing onto the core memory that which is contained in the memory register. Upon completion of the write cycle, a post-write-disturb pulse will be received via the AND circuit 6-17. This in turn will now set the flip-flop 6-15 and reinitiate delay 6-13. Again requesting the contents of the frame number to be transferred to the memory register. AND circuit 6-17Z output is made at this time and initiates the pulse

amplifiers 6-16 S and V. This in turn takes the second half of the frame number and gates it to the memory register. It also resets the frame number gate flip-flop and the post-write-disturb flip-flop. When the writing cycle is done the post-write-disturb pulse arrives at the AND circuit 6-17 J and at that point is blocked, preventing any additional action of this circuit.

DIGITIZATION AND Y SCALER ALLOW (Drawing page 1)

After the frame and reel number had been read, the film is metered to the normal window, clamped in place, and the stage motion is begun. To insure uniform velocity of the stage a delay is given before digitization is started. The delay is a photo-sensing circuit network that is adjustable via a lead-screw assembly on the stage itself. Therefore only after stage motion has started and is assured of being up to speed is a pulse from the photo-sensing network generated, setting both the Allow Y Scaler 2-22 and the Allow Digitization 2-2 flip-flops via AND gate 4-4, PG 5-8, and inverter 5-9.

FILM NUMBER SEARCH (Drawing page 5)

A push button switch labeled search appears on the console. Depressing this push button and leaving it depressed will move film forward at a fast rate of speed and the least significant bits of the frame number will be displayed on the memory

register allowing the operator to search for a particular frame number to be digitized. Operationally, when one is looking for a particular number, the search button is depressed and, looking at the memory register display, one can see the approach of the desired number. Then the switch is allowed to go to its normal position and the search sequence will then stop on the next frame number. At this point, step by step operation can be achieved by momentarily depressing the search button.

Depressing the search switch on the console will apply a negative voltage level to OR circuit 6-22 which fires pulse generator 6-23. This in turn will go through the AND circuit 6-22 output L. This gives the command to the capstan to go forward at high speed. Film is now in the process of moving. Secondly, flip-flop 6-21 is set to the zero state. In response to the begin-a-frame pulse, 6-9 is activated and the sequence associated with reading the frame number to memory will be initiated except that the request for the frame to memory register pulse will not be allowed at AND circuit 6-9, thereby not requesting write core. Also inhibited is the gating of the first 16 significant bits of the frame number by virtue of not allowing the resetting of the frame number gate flip-flop. The pulse from 6-16 also tests 6-22, and, if allowed, the pulse will be applied to the OR circuit 6-22 F but will not actuate the PG 6-23 as long as the search button is depressed. As the number approaches the

operator would release the search button and then the beginning-of-frame pulse will initiate the generator 6-23. This in turn gives a turn-off-film pulse via 6-22 P output and resets the flip-flop 6-21. Also resetting the pulse-write-disturb gate flip-flop and the frame-number gate flip-flop.

MEMORY REGISTER

This logic may be found on page 4 of the DPU drawings. This register consists of 18 flip-flops, with its associated gating that is comprised of the x scaler, y scaler, frame number, orthogonal or normal indication, indicative data, and error indication. The 18 bit word can be broken up then into the following - word bits 6 through 18 will be used for x and y data. Frame number words will comprise bits 3 through 18. Indicative words will comprise bits 3 through 18. The designation of a normal scan or an orthogonal will appear on the first bit of the word. Error indication will also appear on the first bit of the word. However, this will be significant only on the first word of a file. The differentiation of an x or y data will appear on the second bit of the word and will appear for each and every x or y point that is digitized.

It is necessary that the x, y frame and indicative information be gated into the memory register before going on to the magnetic core. On receipt of any one of these commands the pulse amplifiers 5-6 will be activated. They in turn will clear

out the memory register and after a delayed period, the information, either x, y, etc., will be set into the memory register.

MAGNETIC CORE MEMORY

The logic for the magnetic core memory will be found on pages 6, 7, and 8. A general description may indeed prove useful at this time. In order to write on magnetic core, these features must be fulfilled. An address must be given. The addressing then will be applied to bilateral switches for the selection of the particular core bit to be selected. The read or write mode determines the polarity of the drivers that will set the cores after the address is specified. The next is the writing of a 0 or a 1. In the case of the zero the inhibit driver will be driven. If the intent is to write a one in that bit position, the inhibit driver is not driven. The core associated with this particular machine is a 256 word core - 18 bits per word.

READ WRITE MEMORY ADDRESS REGISTERS

This logic may be found on page number 7. On receipt of the write request initiating from the interlace circuit, delay 8-4 will be activated. Immediately a pulse will be applied to the first bit of the write-address scaler. This scaler consists of 8 binary bits. At the initiation of the delay 8-4 output J

passes through OR circuit 8-2 firing PA 8-3. The output of this pulse amplifier will clear out the 8 bits of the memory-address register. The delayed output terminal E, approximately 2 microseconds later, then does the gating from the write-address scaler into the memory-address register. On the seventh bit of the right-address scaler a carry lead is developed which initiates PA 8-3 going into the AND circuit 8-9 which is carried into the control circuit for the tape transport.

The clearing of this register is done via PA 8-5 and receives the clear command at End-of-Frame via the tape control circuit.

READ ADDRESS SCALER

This scaler consists of 8 binary bits and its mode of operation is identical to the write-address scaler. The carry is again developed on the seventh binary bit indicating 128 or 256 words and in this case the output pulse is called read-carry-stop tape. This in turn is brought into the tape logic control. All three address registers have engineering light displays. As indicated, the memory-address register comprises 8 binary bits. In effect these 8 bits are divided into two groups of four. The first group of four determines the x coordinate of the core plane. The last four bits determine the y coordinate of the core plane. With four binary bits, one can then decode 16 possible conditions -

16 in the x plane and 16 in the y plane. On page 8 this decoding is done via AND circuits 9-5 through 9-12. The outputs pass through negative level amplifiers and then operate the bilateral switches. Again another 16 possible paths apply to the decoding 9-14 through 9-20. They in turn go through negative level amplifiers and pass through the bilateral switches. At this point in the explanation of the core memory, we must interpose the logic for the interlace circuit. This logic will be found on page 6.

INTERLACE

The purpose of the interlace circuit is to assure that all data will be received on the core memory and when the memory has 128 words that a request will be made to the tape transport for the writing of this block of information.

When the reading from the magnetic core to the tape system is in progress, any request for the depositing of new information on the core must be allowed. Therefore in effect the interlace is the distributing point for recording new information on the magnetic core as well as the reading out of core and depositing that information in a block of 128 words on the magnetic tape.

CONSIDERING THE WRITING PROCESS

Four conditions allow for the writing of information; the x data, the y data, indicative, and the frame number. Any one of these four pulses will activate the OR circuit 7-8. The output J then sets the inhibit data flip-flop which in turn will prevent new data from coming in to the DPU circuitry until this request has been disposed of. Inverter 7-6 flips the level and polarity of this pulse and it is applied to two AND circuits. Under the assumption that reading out of the core is not taking place, the pulse will appear on the AND circuit 7-7 output T. PA 7-2 responds to this and initiates a write request, activates delay 7-11 for the resetting of the read-write race flip-flop, sets the read-write flip-flop 7-4 in the write mode, and generates a pulse gate memory register.

Recapping the read-write flip-flop is in the write mode and a gate-memory-register pulse has been generated. This pulse will activate a 2.8 microsecond delay, which is the address-settle time, and can be found on page 4. The output of which hits a delay 5-21 and its output J produces a pulse called gate-bilateral-write and, secondly, if the read-write flip-flop is in the write stage, will pass through a negative AND 4-14, inverters 5-9, and will produce a gate pulse for the memory register which will activate the inhibit drivers depending on the state of the flip-flops in the memory register.

The gate-bilateral-write pulse will then activate, on page 8, the following. First, it will gate the levels for closing one bilateral switch in the x plane and a corresponding closure of one of the sixteen possible codings in the y plane. Second, it will fire the pulse generator 11-10 which initiates an 8/10 microsecond delay 11-1. After the 8/10 microsecond delay firing delay 11-2, which sets the width of the write pulse. The J output is applied to gate 11-3, which is in the write mode, and then to the x-y drivers. The delayed output of 11-2 tests negative AND 11-3 and output P fires delay 11-7. The immediate output J then goes through pulse shaping and level changing and will appear on inverters 11-8 and 11-9. This is the post-write-disturb pulse and is applied to all 18 inhibit drivers. The E output of delay 11-7 completes the write cycle and resets the inhibit-data flip-flop allowing additional information to be fed into the head end of the DPU unit.

THE READ CYCLE

Again going back to the interlace circuit and the read-write-address scalars. During the process of writing on the core we had stepped up the write-address scaler by one for each word written. A carry condition on the seventh bit then indicates the writing of the 128th word in memory. This produces a write-carry pulse that will activate circuitry on pages 6 and 10.

Briefly on page 10 this appears as the command for starting the tape transport and producing the proper inter-record gap. On page 6 this pulse appears at the input of the pulse amplifier 7-12. Output J then sets the flip-flop 7-4 to the one state. This in turn, after the inter-record gap has been produced, will allow the clock generator 7-3 to become activated. The output of the clock generator is now producing a pulse every 83.4 microseconds. In effect producing 200 characters per inch on the tape. The output pulse of 7-3 activates a delay 7-5 and checks the conditions on AND circuit 7-7. If the condition of the tape counter is 00 delay 7-13 will be fired. Immediately its J output will inhibit the gate 7-7 that had been used for the generation of a write request. It does allow the second AND circuit of 7-7 output P to be responsive to any write request. If one appears during the delay time of 7-13 which is approximately 20 microseconds, it will set flip-flop 7-10 which is called the read-write race flip-flop. Now recapping briefly. The initial pulse of the clock had activated delays 7-5, 7-13 and the possible setting of flip-flop 7-10. The first delay 7-5 is approximately 6 microseconds. This delay is for the delaying of a read request in the event that a write has just been made. Secondly, delay 7-13 puts an inhibit on any additional write request as a read is

being activated. During this activate time if a write request has been made, flip flop 7-10 would have been set. At the completion of a read delay 7-13 its delayed output E would test the flip flop 7-10 and if a write request had been made during this 20 microsecond period, it will be reinitiated via PA 7-2.

Following the delayed output of delay 7-5, there is one delay and a negative OR. If the tape counter is at the 00 state, then the output lead H drives PA 7-2 which produces a read request and a pulse-gate-memory register. The read request as outlined before will step the read-address scaler, clear out the memory-address register, and gate the contents of the read-address scaler into the MAR. The gate-memory-register pulse is inhibited via the read/write flip-flop from gating the memory register. However the gate-bilateral pulse does set the desired bilateral gates, hits the x and y driver, and will do the following in the read cycle - at the output of the negative AND 11-3 W inverter 11-4 initiation of the delayed strobe pulse. The delay is manufactured by delay 11-5 and the strobe pulse is applied to the sense amplifiers for gating out the information in the core.

As a result of the read request and the strobe pulse, the core has been read and now deposited on the core buffer, page 9. This buffer consists of an 18 bit buffer. The pulse

called delay set, page 6, then proceeds via positive ANDs 7-15 and will gate the first 6 bits of the 18 in the core buffer to the flip-flops on page 11 associated with the tape control. The pulse also fires the tape character counter and will step this by a unit of one. The next clock pulse which is 83.4 microseconds later will not be able to make an additional read request because the tape character counter is no longer at 00 but the action of resetting the tape buffer, activating delay 7-14 producing delay set and then gating the second set of six character bits from the tape buffer to the tape control circuit will occur. Also the counter will be stepped to the second unit. The next pulse from the clock will again gate out the last 6 bits, 13 through 18, and step the scaler by an additional count. The final gating out of PA 7-16 will reset the tape character counter.

Writing on tape is initiated by the delayed set pulse firing delay 15-4 on page 11. This delay sets the proper parity into flip-flop 15-11 and initiates delay 15-5 which will gate the contents of the magnetic tape buffer to the 7 flip-flops. Now, after three clock pulses, we have written one word on magnetic tape.

On page 9 the logic for the core sense amplifier and the buffer appears. The strobe pulse is connected to the 18 sense amplifiers, and in addition, the sense windings from the core are applied to the sense amplifiers. The strobe then will take the contents being a zero or one from the core and gating it into the sense amplifier core buffer consisting of flip-flops 13-10 through 13-23. The outputs of these flip-flops are gated via the gate buffer in groups of 6 characters at a time to the magnetic tape flip-flops on page 11. The sense amplifiers flip-flops have a visual display.

Tape Control - This logic may be found on page 11 and has been briefly discussed - reading from the core memory to magnetic tape. Going back, upon receipt of the 128 word in the write-command mode a start tape pulse and start IR gap will occur, setting flip-flop 15-1 page 11. This in turn through gates 14-9 and 15-21, will give a forward command to the Potter tape transport which starts the movement of tape. The start tape also sets flip-flop 15-7 for the write command which activates the right amplifiers in the Potter. If the tape transport is at load point as the tape passed over the reflector on the tape, a pulse will be manufactured via PG 14-2 setting flip-flop 14-22.

This in turn with the IR gap pulse will produce a 100 millisecond delay before receiving the gap okay signal as compared to the normal gap requirement of approximately 6 milliseconds produced by delay 15-2. The sense amplifier buffer is gating 6 characters at a time and depositing this information on the tape buffer comprising flip-flops 15-8 through 15-10. The outputs of these flip-flops go into the parity generation circuits, cards 15-6 and 17. If the total number of 'ones' in a tape characted, comprised of 6 bits, is even, the parity circuit will place an allow condition at the input to flip-flop 15-11. The delay set which is activated each time a transmission of 6 bits is made to this buffer will then set the parity flip-flop to the one state. Gating will occur as indicated before into 7 NRZ flip-flops and then directly to the write amplifiers.

Associated with the tape transport system described controls for producing end-of-file, end-of-tape, and LRCC will be found on page 10. The write-carry pulse produced by the write-address scaler enters the OR circuit 14-5 and will test the AND circuit 14-4 and activate delay 14-6. The AND 14-4 is a guard circuit to recognize the attempt to start the tape transport via another write-carry while the tape transport is being stopped. This leg is on the delay 14-8 and is 14 milliseconds in duration

and is initiated via a stop-tape command. If it is in the allow state, we will set flip-flop 14-7 and upon completion of the stop time a request equivalent to the initial write-carry will be made again. Following the delayed output 14-6 a pulse will appear on PA 14-3 providing the tape transport is in a stop condition. This will produce a start-tape command and an initiate of the inter-record gap. Also a path is established for the resetting of flip-flop 14-7 used for the regeneration of a write-carry under the condition that a request to start the magnetic tape had been given while the tape was in the process of stopping. Also it will provide for the setting of the overflow Flip-Flop gate flip-flop 14-13. This flip-flop is reset on each and every stop-tape command. However, if two consecutive write commands are given without being separated by a stop-tape, then 14-13 overflow gate flip-flop prepares for the operation of flip-flops 14-13 and 15-11. Flip-flop 14-13 is the overflow flip-flop and will provide the memory overflow lamp and the setting in of a tape error. The memory dump flip-flop 15-11 in turn provides a path for the manufacture of an overflow dump error set and for the manufacturing of a write-carry command assuring that the memory is entirely clear.

LONGITUDINAL REDUNDANCY CHARACTER CHECK

The completion of a record will produce a stop-tape pulse via the read-address scaler. This in turn fires PA 14-15 on page 10. This PA will apply the stop-tape pulse to three separate locations. One being at coordinate B4 of page 10. Coordinate D8 goes through the OR circuit 14-12 and hits a delay of 330 microseconds. This roughly is 3 characters in duration. The output after the delay will produce a pulse called LRCC and will check through AND circuit 14-16 for the conditions of end-of-file or end-of-tape. If none are present we will then hit delay 14-19, waiting 7.8 milliseconds before the command-stop tape which actually commands the Potter tape transport to physically stop the tape. The LRCC pulse resets all the NRZ flip-flops that are directly connected to the write amplifiers. Thereby producing an even horizontal parity for each of the six character channels and the vertical parity channel.

END OF FILE

The end-of-file pulse is in effect saying that the digitization of the frame has been completed. The y scaler develops an end-of-digitization pulse from page 3 and appearing on page 10, it will go through one of two AND circuits, depending upon the conditions of single or double scan taking place. In any event an output via T or L of inverters 14-9 or 14-16 is

applied to two negative ANDs 14-4 or 14-9. 14-4 will be allowed if the overflow gate flip-flop is set indicating that no writing is taking place. This in turn then will simulate a write-carry and the description of this circuitry has been given. However, the pulse will pass through an OR circuit 14-4 and will be applied through PA 14-3 to set the end-of-file flip-flop 14-10. It would also produce test end-of-tape pulse and end-of-frame pulses. Test end-of-tape appears on page 11 and it will set flip-flop 15-7 to provide a condition for the rewind command when the low tape condition is met. This will be described later. The end-of-frame indication applied to page 6 will set flip-flop 4-7 page 6 allowing for a request to read the last 128 words of the core memory. Upon completion of this readout a stop-tape pulse will then be produced. Delay 14-14 will check two AND circuits and 14-9 output P will be allowed by the condition of the end-of-frame flip-flop ON. This then will provide for the writing of the end-of-file character. However, preceding this the stop-tape will initiate the writing of the LRCC character but the stop-tape command will be blocked at AND circuit 14-16 as a result of the end-of-file flip-flop being on. The PA 14-15 will produce the end-of-file to page 11 and initiate a 5 micro-second delay via delay 14-21. This delay will clear out the read and write-address scalers and also clear out flip-flop 14-22 which inhibits any write or read-carries from being produced

as a result of resetting both scalars. On page 11 the end-of-file pulse will set NRZ flip flops 3, 4, 5, and 6 associated with the conditioning of the write amplifiers. This configuration of writing on 3, 4, 5, and 6 channels is decoded via the IBM tape system as an end-of-frame indication. After a delay of 337 microseconds the flip-flop end-of-file will have been reset and the normal initiation of the stop-tape will occur.

END OF TAPE

End-of-tape will apply an allow on an AND circuit 14-4 input Y. (Page 10) Coincident with an end-of-frame then we will set in addition to the end-of-frame flip-flop the end-of-tape flip-flop. The magnetic core will be in the process of being dumped and in conjunction with the stop-tape pulse, the end-of-file condition will occur and before the stop-tape command is given, we re-enter via delay 14-18 for the manufacturing of a second end-of-file indication. A double end-of-file indication via the tape transport system would indicate an end-of-tape command. The end-of-tape command also precedes to page 11. At that point conditions are met for giving the tape transport system a rewind command.

TRACK CENTERING

The light spot, in making a scan, will traverse the film. Selection as to which window is being scanned at the moment,

the normal or orthogonal, is done in the logic of the stage control and appears on page Zero, AND circuits 2-10. In the case of a normal window, the output T is activated in response to a data point. Output W is activated when scanning the orthogonal window. In either event the incoming data point from the PM tube is a level going in the positive direction. For example, consider the normal window, then the output T would respond to data pulse by producing a positive going pulse at output T. This in turn appears on input K of an inverter 2-9. The output of the inverter appears on input S of pulse generator 1-3. The pulse generator 1-3 is activated on the leading edge of the data point and the pulse generator 1-4 is activated on the trailing edge. Again, if the data pulse arrives, then 1-3 is activated and on the condition from page 1, indicating information is to be received; AND 1-8 is activated and sets flip-flop 1-5, the output of 1-5 applies an allow condition on two AND gates. Considering one negative AND circuit 1-9. Input F has the clock pulse from the x-scaler. This is coming in at a least count of 8.5 microns. It is then doubled through a network and appears at the input of the negative AND at twice the frequency giving a count each 4.3 microns traveled by the light spot. Input H is conditioned in the allow state for all conditions except when the trailing edge pulse generator 1-4 is fired.

Condition J is on a flip-flop that had previously been manually reset or reset at the termination of the preceding data point and therefore output K will be fired. This in turn works its way through an inverter 1-7 and is applied to the first stage of the 8 bit track centering counter. In addition, the pulse also appears on the input N of a negative AND 1-2. This action had occurred on the leading edge of a data pulse. As long as the data pulse is beyond the triggering level of 1-4 the scaler will receive counts via the x-scaler clock. At this point two alternate paths can be followed. 1) If the data pulse is sufficiently long it may be considered to be an unwanted digitization and is to be deleted. For instance, it could be the response when the scan passes into the frame holding area. Under this condition the scaler will fill up on the 256th pulse, making the output z of 1-16 negative and this conditions 2 negative AND circuits 1-2 E and L. On the receipt of the next scaler count pulse, negative AND 1-2 will fire on its output R pass through to fire pulse generating circuit 1-13. This in turn will reset the entire binary scaler and reset flip-flop 1-5. This in effect is the deletion of the incoming data point. On the other hand, if the data pulse falls within the width requirement that had been set up by the experimenter, the trailing edge of the pulse will fire 1-4 before filling of the counter has taken place. This in turn passes through a negative AND and sets flip-flop 1-5

on the input lead W. Setting 1-5 then disables the negative AND 1-9 output K. It does, however, condition 1-9T. This gate becomes active and now the x-scaler pulses will be developed at the output of 1-9V. This in turn is applied to the second bit of the binary scaler and also this pulse tests the condition of the last flip-flop of the scaler via 1-2 H. At this point the data rate in effect is once again doubled. As soon as the scaler receives the overflow condition the next sequential incoming pulse operates 1-2 output K to start the clearing operation as had been explained before. However, another function is performed. Output K, through an inverter, drives a pulse generator that is called data. And this passes to page 1 in data processing unit. Manual reset enters the track centering circuit via 1-15 input V.

STAGE LOGIC DESCRIPTION

Assuming the following, the machine is in its normal reset condition, the tape transport at load point, the stage at the normal window, the stop switches S1 through 8 are in their normal condition, the machine is set for double scan, then the following events will occur upon depressing to start processing switch.

Start Data Processing

Depressing the Start Data Processing switch (page 13) will apply a negative level (-3_v) to a pulse generating unit 3-7 and then to AND circuit located at 3-4. This command will be allowed to pass through this AND circuit under the following conditions:

1. The stage is in its normal condition,
2. The tape is at its load point. (Provision has made, via a switch, that this condition can be ignored),
3. That the stage is not in the thread mode,
4. That the interrupt flip-flop is in the reset condition.

If all four conditions, are met, the command originating via the Start Data Processing switch then resets the stage F/F to the normal state and also proceeds to the preselector and is returned to AND circuit located at 3-14. The AND, 3-14, has two input

level gates, one being associated with the stage condition and the other is film and data safeguard functions. If the stage's, lamps, or vacuum system are not in proper operating condition, the Start-Data Pulse will not continue on. The second level gate is made up of the film clamp and the end-of-tape.

The pulse passes through to two pulse amplifiers located at 1-7.

These then will reset the interrupt flip-flop and produce a negative and positive start pulse and a start-film-forward pulse.

The start-film-forward leads to page 5 of the DPU drawings and will enable the flip-flop to activate the film registration circuit. Upon receipt of film registration, the DPU unit will store the frame number into memory. The frame number will be the first two words of the first record of the file. Pulses start (positive and negative) will do the following on page 14.

1. The start-positive will set the capstan forward flip-flop to the on state and will condition flip-flop 2-24 removing the capstan brake. The start-negative pulse will appear at an OR circuit C1-8 to set the reverse flip-flop and set the fast-slow flip-flop to the slow mode.
2. Now the capstan has these conditions applied to it - clutch on, brake off, and the speed selection. These outputs are passed through a guard circuit C1-12. This guard circuit prevents incompatible commands to be applied to the capstan motor. If the commands as described are applied to C1-12 then

solenoid driver C1-1 will be activated applying a forward signal to the capstan control circuit and solenoid driver C1-1 will be activated applying a capstan clutch signal.

Now referring to the drawing on page 17, the DC capstan controller. Setting the speed flip-flop to the slow position thereby drives solenoid driver 3-24. 3-24 drives the relay associated with the control of the field of the capstan motor. In the slow mode a 250 ohm resistor is placed in series with the field winding, in the fast mode of operation this register is shorted out.

Solenoid driver C1-1 operates the forward relay and CRL relay. Contacts of the forward relay switch the armature of the capstan motor and CRL connects the motor to the directional relays. CRL in operating then operates relay CR2. CR2 in operating connects the motor to the DC line via the motor controller. At this point the capstan motor is turning in the forward direction at slow speed and will continue to do so until commanded differently. The film is now moving through the film transport system. On receipt of a frame registration marking, a pulse will be produced called "frame registration mark" and is applied to pulse generator 3-18, page 14. This in turn will pass through AND 3-12 providing the search flip-flop is not in the search mode, setting the allow meter flip-flop 3-5 to the allow state.

As the film is being driven by the capstan motor, the optisyn, which is connected to the shaft of the capstan motor, is producing a series of pulses, each pulse measuring a distance of .003 inches of film travel. When the allow meter flip-flop was set, the optisyn pulses on 3-21, page 16, were permitted to pass through AND circuit 3-12 to the first stage of the encoder scaler. The encoder scaler has ten bits for measuring the fractional part of a rotation of the Capstan Sprocket Wheel and four additional stages for measuring full turns. Each C3-21 pulse sets the encoder counter up by one, and provides an input to delay circuit 3-1. This delayed pulse is the encoder gate pulse for testing the metering conditions. The decoding circuit that we are interested in at this time is located at 2-9 output "F". The first twelve inputs to this gate are derived from the encoder scaler and can be preset from one experiment to the other. The other conditions that must be met for this gate to be activated are "not in the reverse mode," the normal-orthogonal flip-flop in the normal mode, and the A-B flip-flop in the B mode.

When the film has traveled the preset distance from the frame registration point the encoder gate pulse which is delayed 20 microseconds to allow for the settling time of the encoder scaler, produces an output pulse called "frame-to-normal" at C2-9 at the F collector. This then will pass through the OR circuit C1-17, page 15, and arrive at delay 2-5. Immediately upon arriving

at the delay, the J output will apply a pulse for setting the brake clutch flip-flop 1-15 to the brake side and for setting the forward flip-flop 1-15 to the off side, thereby stopping the capstan motor from feeding additional film. After a delay, to insure the stopping of film, a pulse from 2-5's E output will be produced going through the S1 switch to an inverter 1-21. The output of the inverter will apply a pulse called "Film Clamp On" to the film clamp. This pulse sets the film clamp flip-flop 1-16 to the on state which drives solenoid driver 2-23, thereby applying the power to the clamping device of the stage. The second output of the inverter 1-21 passes through the S2 switch, through an inverter 3-3 to the input of delay 3-6. This delay is to assure that the film clamping has occurred before any further action is initiated. The output of 3-6 delay then applies a pulse that sets the capstan brake clutch flip-flop 1-15 to the off position and resets F/F 2-24. The second output of delay 3-6 passes delay 5-25 through the switch S4 to a pulse amplifier 3-21. With the normal-orthogonal flip-flop in the normal state a pulse will be derived from the H output of the AND circuit 3-20. This pulse will then set the scan normal flip-flop 3-10 to the on side. The output of 3-21 pulse amplifier also goes through inverter 3-3 and sets the stage brake flip-flop 3-11 to the off side. At this point we are attempting to activate the stage motor. Once again the combination of AND circuits 3-19 assures that the brake of the stage motor is removed and only a forward or reverse command

is given before the solenoid drivers that apply power to the motor can take place. At this point the stage is moving, the film is clamped, and digitization is now taking place.

During the process of digitizing, the stage is moving, the Ferranti Reader produces a series of pulses to the Y scaler. At a preset value, depending upon the experiment, decoding will provide a pulse called end-of-frame. This in turn prevents any more digitization of that frame. However, the stage motion is still carrying on. Now as the stage reaches its limit stop, in this case the orthogonal position, a pulse will be produced by 7-24 which sets the normal-orthogonal flip-flop to the orthogonal mode, resets both normal and orthogonal capstan scan F/F's after a 110 MS delay, also provides an input pulse to pulse amplifier 2-17, producing a command pulse to the stage brake flip-flop side which via the guard circuit and solenoid activate the stage brake. The delay output 3-15 appears at the switch S5 and initiates a second delay 3-16. The second path of 3-15 passes through inverter 1-13 to apply the brake on the capstan motor. Delay 3-16 is to assure that the capstan motor brake is applied before the film is unclamped as a result of the delay output 3-16. The second function of the delay output goes through the switch S6 and applied to delay 3-17. This delay is to assure that the film clamp has been removed. Going to the delayed output of 3-17 it will pass through the AND circuit 3-19 provided

that the film clamp condition has been released. The pulse will continue through inverter 2-19 and tests the various gates ON 3-20 outputs W, Z. Of this group only two AND circuits are now in the allow condition. The one associated with 3-20-Z makes provision for setting the orthogonal flip-flop associated with the Z to MR transmissions. 3-14-Z is of more interest at this time and will apply a pulse that will be called "brake-off, forward-on". This will go through OR circuit 1-12, inverter 1-13, to the input of the capstan brake clutch flip-flop setting the clutchside and setting flip-flop 2-24. In addition, the pulse passes through OR circuit 3-12 inverter 2-19 setting the forward flip-flop to the forward side. Once again the conditions are such that we are calling for forward motion of the capstan motor and releasing its associated brake. Guard circuits 1-12 are thereby allowed and the solenoid drivers Cl-1, Cl-11 will become activated as explained in the preceding sections of this description. Film is again moving forward between the normal window to the orthogonal window. During this process the optisyn is upgrading the encoder scaler and when the proper forward motion of the film has occurred an output from the coding chain C2-8 output F which is called "forward-normal to orthogonal" will be produced. This pulse is applied to the OR circuit 1-17 and to the input of delay 2-5. The operation at this point has been explained before with the following exceptions -

The output of pulse amplifier C3-21 instead of applying the pulse to the scan normal flip-flop will now apply the pulse to the scan orthogonal flip-flop 3-10. The stage motor will start and allow the digitization process. At the completion of that scan the end-of-frame pulse appears inhibiting digitization, again the stage is still moving until the stage limit is reached which produces a pulse on PG 3-8 instead of 3-7 as had been explained before. We now set the normal-orthogonal flip-flop 3-5 to the normal state. The action once again is in all respects the same as explained before up to the point where delay 3-17 is activated. 3-17 output, associated with the shutting off of the stage motor, is exactly the same, but the output via inverter 2-19 sensed the conditions on AND circuits 3-20 and 3-14. At this point the gate allowed is 3-20 output W. Output W will go through OR circuit 1-17 producing a pulse called "film-fast reverse-brake-off".

The fast film, "reverse-brake-off pulse" will be applied through OR circuit 1-12 inverter 1-13 to set the brake-clutch flip-flop to the clutch on side, setting the reverse flip-flop C1-16 in the reverse mode and setting the film fast-slow F/F

to the fast condition. Now the clutch is on the capstan, a direction "reverse" in on the capstan motor and the speed mode is fast, thereby activating the capstan through the guard circuits 1-12 and solenoid drivers 1-1 and 1-11 to the capstan motor producing reverse direction at fast speed and the motor will continue until such time that a stop occurs via a metering circuit.

RETRACE DECODING

Decoding circuitry 2-7 output F, when the film has moved in its retraced direction a predetermined value, an output pulse F will appear through OR 1-17 to the input of delay C2-21. Immediately, the output, via the inverter C1-13, will apply the brake on the capstan motor. The pulse will set the AB flip-flop to the B condition. It then is applied via inverter 1-13 to reverse flip-flop setting it to the off state. The delayed output 2-21 goes through the switch S3 and passes through inverter 3-3. The output of which resets the encoder scaler and produces a "recycle pulse". The recycle pulse inhibits additional metering by setting the meter allow flip-flop to the off side. It also appears via the switch S8 to the AND circuit C1-8. Now, providing the interrupt flip-flop has not been set, it will then be passed to inverter C1-13 and appears on OR circuit 3-19 through AND 3-14 to activate the sequence that produced the start of film-forward command.

SINGLE SCAN OPERATION

What had been explained was for the double scan, requirement of the film reader. An option on this machine is single scan. This then acts in the following manner - film moves from registration mark to the normal window, the film is clamped, digitized via the stage and at the completion of that digitization, the film is unclamped and a retrace occurs. On receipt of the next frame registration the film will be passed to the normal window and digitized. Again, at the completion of digitization retrace will occur and metering again will be carried from frame registration to the normal window.

FILM TRANSPORT

As the film goes forward and registration is sensed then the film leaves the frame registration area and passes through the stage comprising the normal and orthogonal window and clamping devices. Leaving the stage the film now proceeds into the second vacuum chamber. This is called the film take-up chamber. This chamber, like the feed chamber, has four limit switches. Upper and lower switches within the limits just described are for control of the feed and take-up brake clutch assembly. Finally the film is spooled via the take-up motor which is controlled via a brake-clutch assembly.

Associated with this system are threading, loading of film operations and the prevention of feeding film when digitization is in process.

THREADING OF FILM

For an operator to thread film a switch must be thrown at the stage itself. Depressing the thread switch will remove the 70 volt supply from all solenoid drivers. In addition a 15 volt supply will be connected to the brakes of both the feed and take-up motors. The operator now is in a position to thread the film through the stage with the assurance that no feeding of film can take place.

LOADING OF FILM

Once the threading operation has been completed the thread switch must be reset before any additional operations can continue. For the loading process the operator now will depress a push button called load film at the stage position. Depressing the load-film switch then appears on an AND circuit 1-8. Providing the vacuum system is on, this pulse will then be passed on to the flip-flop 1-5 removing the brake and applying the clutch to the feed motor. The pulse "load film" then will be applied to actuate the capstan motor forward. In addition the capstan clutch will be applied and the speed selection for the capstan motor will be allowed in the fast mode of operation.

The capstan motor will start removing film from the feed vacuum chamber and the feed motor will be spilling film into the vacuum chamber. This will continue until the sense switch within the vacuum chamber indicates a full vacuum chamber. At that point the sensing element P2 will be operated and remove the clutch from the feed motor and applying the feed brake stopping any additional feeding of film into the feed vacuum chamber. The capstan motor will still be feeding into the take-up chamber. This will continue until the sensing switch in the take-up vacuum chamber P2 is sensed. This in turn will drive the take-up clutch to the activated mode thereby pulling film from the vacuum chamber into the take-up reel. During the process of winding from the take-up chamber, a request for more film is made via P1 in the feed chamber, it will respond by allowing the feed motor to spill film into the feed chamber. Then when the proper balance is made within both chambers this action will immediately come to a halt with film in both chambers.

LIMIT SWITCH OPERATION

If either limit switch in the feed chamber or the lower switch in the take-up chamber is actuated the following sequence will take place -

1. The capstan brake will be applied.
2. The error flip-flop in the DPU unit will be set.
After a time delay via 1-23 flip flop 2-18 will be set. Setting this flip-flop will then operate relay T1 which will drop the 70 volt power supplies from all solenoid drivers. The upper sensing switch in the take-up chamber responds in the same way with the addition that it will actuate the following sequence.
 1. It will remove the film clamp.
 2. It will make the sprocket associated with the capstan go in a floating mode.
 3. It will call for the feed to take place.

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OPTICAL SYSTEM

FIGURE 1

FILM TRANSPORT SYSTEM

FIGURE 2

FIGURE 3

FIGURE 4

FIGURE 5

TRACK CENTERING LOGIC

FIGURE 6

FIGURE 7

FIGURE 8

FIGURE 9

FIGURE 10

FIGURE 11

FIGURE 12