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AN AUTOMATIC LEVEL COMPENSATION SYSTEM FOR LASER INTERFEROMETERS

W. A. Baldauf, Jr.

UNION CARBIDE CORPORATION
NUCLEAR DIVISION
OAK RIDGE Y-12 PLANT

operated for the **ATOMIC ENERGY COMMISSION** *under* **U. S. GOVERNMENT Contract W-7405 eng 26**

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W. A. Baldauf, Jr

This report is based upon a thesis which was presented by the author to the Graduate Council of The University of Tennessee in partial fulfillment of the requirements for the Master of Science degree.

Oak Ridge, Tennessee

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ABSTRACT

A system has been designed which will automatically compensate for signal DC level drift in a laser interferometer system. A prototype of the system has been built and put into an interferometer system where it has proved to be capable of meeting the design requirements.

CONTENTS

SUMMARY

A system has been designed which will automatically compensate for signal DC level drift in a laser interferometer system. A prototype of the system has been built and put into an interferometer system where it has proved to be capable of meeting the design requirements.

INTRODUCTION

Laser interferometers, at present, are being incorporated into machine tool and inspection systems as high-resolution incremental encoders. The use of an interferometer presents several advantages in such systems, namely:

1. Resolution is achieved to a fraction of a wavelength of light (typically 12.5 microinches or less).

2. Accurate linearity, which is affected only by variations in the index of refraction of the light beam path, is now a reality.

3. Compactness and adaptability to a variety of installations is available; consequently, more of the error-producing parts of the machine tool or inspection machine can be included within the position-measuring system.

Of course, with these advantages have come some problems that are peculiar to this type of system. However, many of the problems have been overcome by technology developed in the past few years. Among the improvements are:

1. High-speed counters, which allow machine movements of approximately 600 inches per second with a resolution of 12.5 microinches per count.

2. Low-rise-time photodetectors, which allow machine movements of approximately 90 inches per second when the interference cycle fringe is 12.5 microinches long.

3. Lasers with guaranteed lifetimes of 2,000 hours.

4. Special-purpose computers for converting fringe counts to inches, correcting the fringe length as a function of changes in temperature and barometric pressure, and correcting the fringe length as a function of the workpiece temperature.

But, with all its sophistication, the interferometer has, until recently, required manual adjustment several times a day by an instrument technician. This correction was for the signal DC level which has an effect on the quadrature relationship needed to obtain bidirectional counting. Factors that were compensated by this adjustment were, primarily, power changes in the laser output and drifts in the photodetector, preamplifier, and power supply. Although the importance of these factors may diminish with further advances in technology, automatic compensation for their effects is feasible, as described in this report.

THE AUTOMATIC LEVEL COMPENSATION SYSTEM

BRIEF DESCRIPTION OF INTERFEROMETER APPLICATION AND THEORY

Laser interferometers are used in machine tool and inspection systems to detect movements which are a fraction of the wavelength of the laser light. The helium-neon laser (with a wavelength, λ, of 6328 A or 24.91414 micro-inches) is normally used in this type of application.[1] The smallest increment of movement which a system can detect is a function not only of the wavelength but also of the number of light-path folds and the decoding electronics. Figure 1[2] shows a simple single-folded light-path system. The light from the laser is split into Beams I and II by the beam splitter. Beam I is reflected from the reflector back through the beam splitter to the photodetector; Beam II passes through the beam splitter and is reflected by the cube corner reflector which is attached to a machine axis, and moves with it. The reflected beam (Beam II) returns to the beam splitter and is reflected there to the photo-detector where it is superimposed on Beam I. As Beam II is shifted through one wavelength, the light intensity at the photodetector will vary sinusoidally one cycle. Figure 1 shows the sum of Beams I and II when they are fully re-inforcing each other (maximum intensity) and fully cancelling each other (zero intensity), assuming their intensities are equal.

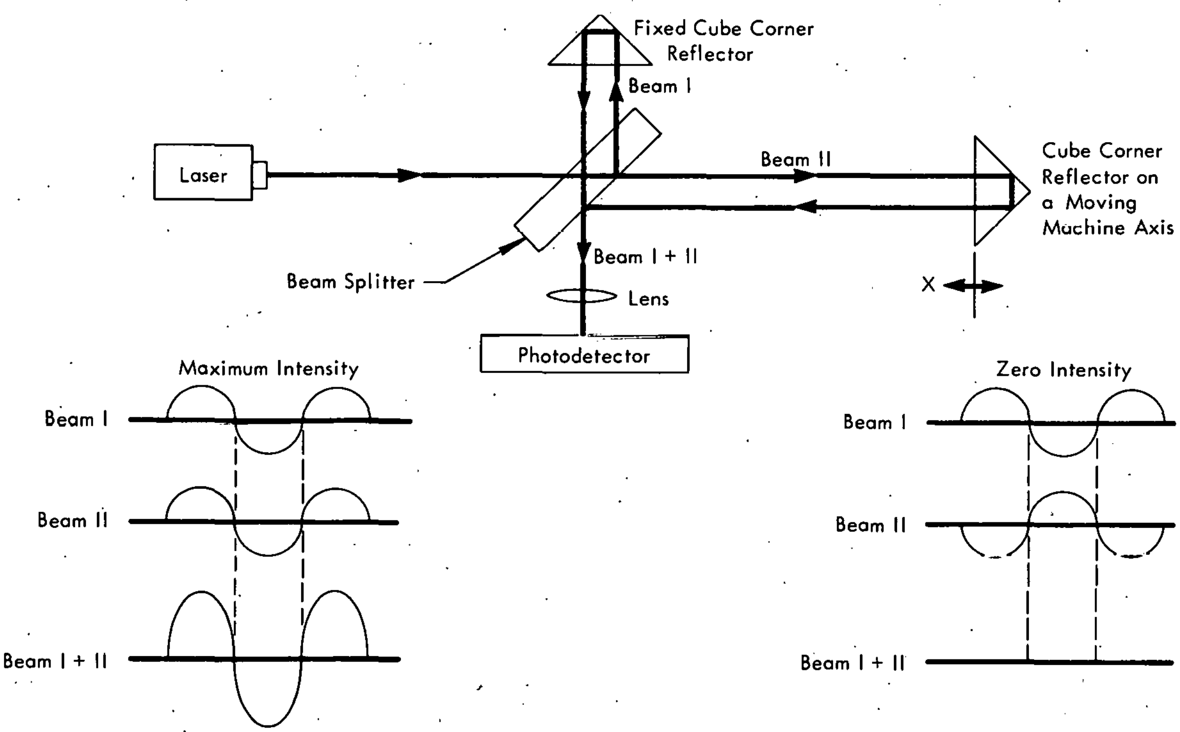


Figure 1. SIMPLE LASER SYSTEM SHOWING THE SUMMATION OF TWO MONOCHROMATIC LIGHT BEAMS TO FORM AN INTERFERENCE SIGNAL.

Generally, each fold in the light path decreases the effective wavelength by a factor of $1/(n + 1)$, where "n" is the number of folds. Thus, the effective wavelength, λ_E, is equal to $\lambda/(n + 1)$ because the length of the light path changes by a value of $\Delta x\ (n + 1)$ for a Δx movement of the machine axis when there are n folds. At the photodetector, the amplitude of the interference signal (Beam I) plus Beam II varies as a function of time, as shown in Figure 2.

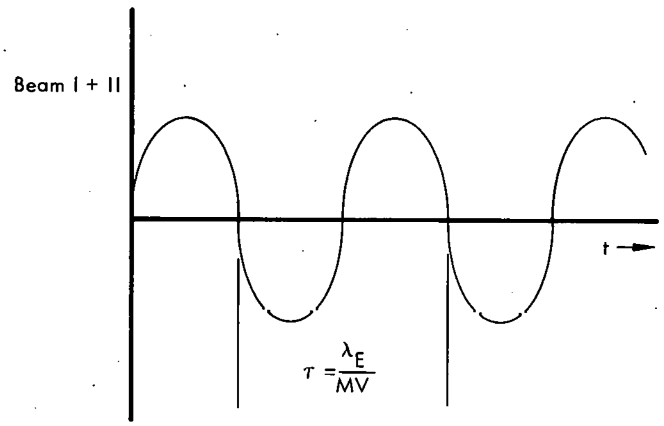


Figure 2. SIGNAL AT THE PHOTODETECTOR WHEN THE MACHINE AXIS VELOCITY EQUALS MV.

In order to get distance information from the simple system shown in Figure 1, the number of cycles of detected light could be counted by counting the zero crossings. However, there is a disadvantage to this. In such a system, the light path could only be decreased or increased monotonically, thereby limiting the system's usefulness. Even if monotonic movement were acceptable, vibrations in the system would probably be unavoidable and would produce extra cycles which would be counted. Consequently, it would appear that the light path had changed more than was actually experienced.

In order to eliminate the disadvantage described, a practical interferometer optical system makes use of the phase-shifting characteristics of the reflective surface of the beam splitter to obtain two interference signals displaced by $\lambda/4$. Such a system is illustrated in Figure 3.[3]

Detection of these two phase-displaced interference signals results in voltage signals which have a quadrature relationship to each other, as indicated in Figure 4. Now, direction of motion as well as distance information can be obtained. Direction is sensed by determining whether Signal B in Figure 4 goes from high to low or low to high when Signal A is in the "high" state.

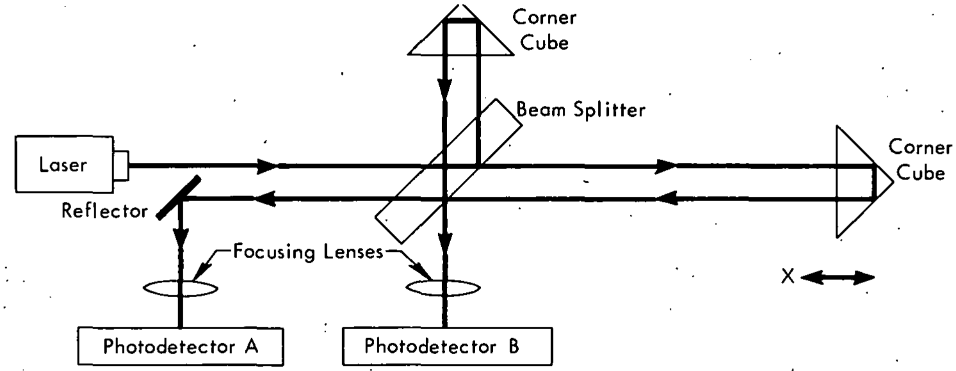


Figure 3. INTERFEROMETER SYSTEM WHICH PRODUCES QUADRATURE INTERFERENCE SIGNALS.

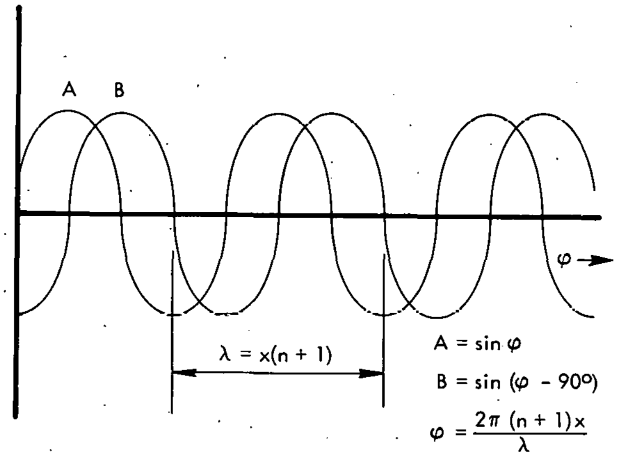


Figure 4. QUADRATURE SIGNALS AT PHOTODETECTORS A AND B AS A FUNCTION OF THE MACHINE AXIS POSITION.

The electronics conventionally used to produce the quadrature signals and sense movement and direction of movements consists of a photodetector (such as a photosensitive semiconductor), a DC-coupled amplifier, a signal-squaring circuit which changes state at the time of a zero crossing (usually a Schmitt trigger), and a direction-sensing logic.(3) These elements are seen in Figure 5. The zero crossings are not necessarily referred to zero volt, but more generally to the center of the hysteresis band of the respective Schmitt trigger. It will be assumed in this report that the hysteresis band is centered about zero volt.

The direction-sensing logic will produce a pulse to count a digital counter up or down at λ_E intervals, or it makes use of one out of the four zero crossings which occur in the λ_E interval. This treatment is the simplest utilization of the information contained in the quadrature signals. More sophisticated

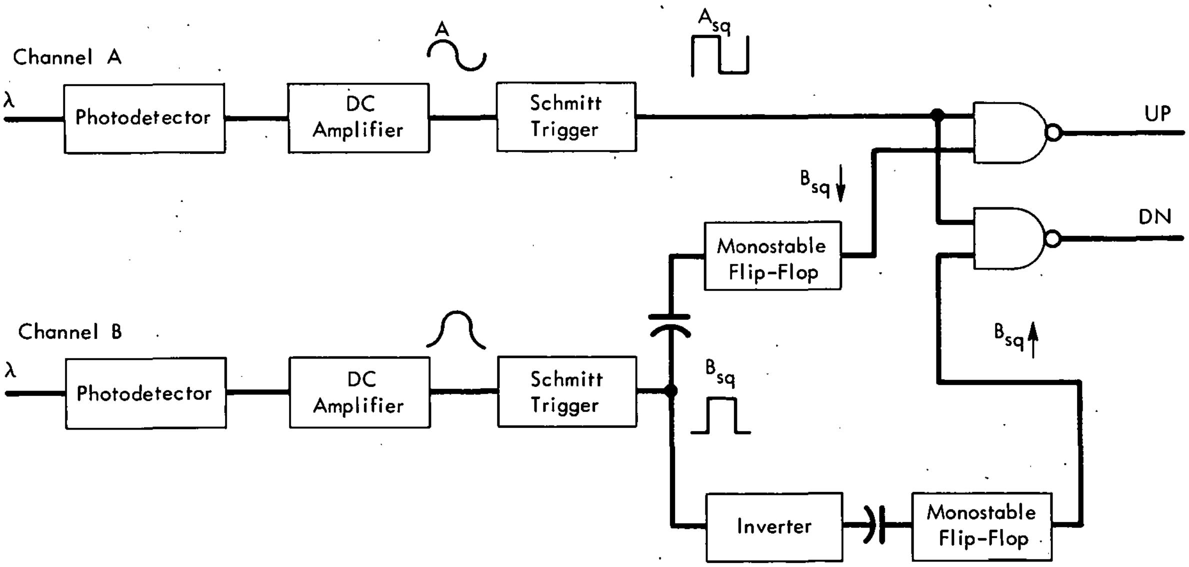


Figure 5. PRINCIPAL COMPONENTS OF THE INTERFEROMETER SYSTEM.

systems which use two or all four of the zero crossings have been designed which produce pulses at 1/2 or 1/4 λ_E intervals. However, for illustrative purposes, the direction-sensing logic shown in Figure 5 is adequate.

SIGNAL DRIFT PROBLEM

The interferometry technique just described depends upon the fact that there is a quadrature relationship between Signals A and B after squaring in their respective Schmitt triggers. The quadrature relationship needed is not absolute but must be good enough so that Signal A is always high when Signal B makes a transition from low to high or high to low at integral λ_E intervals. The desired quadrature relationship will be described as virtual. A loss of the virtual quadrature relationship can produce one of several symptoms:

1. If both squared signals still make transitions but are phase shifted more than 90 degrees from the absolute quadrature, the sense of any movement will be reversed.

2. If Signal A is always high, there appears to be no net movement.

3. If Signal A is always low, there appears to be no movement.

4. If Signal B is always high or always low, there appears to be no movement.

The actual phase relationship of the two signals is primarily a function of their DC levels with respect to their respective Schmitt triggers.

Before operating an interferometer system, the DC level would be manually set to zero volt while monitoring the DC level at the input to the Schmitt trigger. In operation, some drift of the DC level is expected due to laser output intensity changes, misalignment of the optics with respect to the line of actual machine axis travel, and drift in the DC-coupled amplifier. Experience with interferometer systems which have only manual DC level adjustment has shown that frequent periodic adjustments by instrument mechanics using an oscilloscope are necessary to maintain the virtual quadrature relationship. Consequently, a system is desired which will, after a setup adjustment, automatically compensate for DC level drifts caused by any of the factors just listed. It will be referred to herein as the Automatic Level Compensating (ALC) system.

SOLUTION TO THE PROBLEM

In the solution to the problem of maintaining the DC levels by automatic compensation of the DC level drift, one set of constraints and one condition must be considered. The constraint is that the automatic level compensating system must be compatible with an existing system, as defined earlier and further defined in Figure 6, to show the pertinent system parameters. That is, the DC level must be sensed at the input to the Schmitt trigger where the signal source impedance is approximately 20 Ω, the automatic compensating signal (ACS) must be incorporated where the manual adjustment signal voltage with a range of + 1 to + 4 volts is applied (since this point was readily accessible), and the ACS should be capable of bringing the DC level within some tolerable range of the center of the Schmitt trigger hysteresis band. This tolerable range was determined from an analysis which assumed that the two signals were equal in amplitude and in perfect quadrature when their DC levels were equal, that their DC levels drifted equally but in opposite directions, and that their Schmitt triggers had equally wide hysteresis bands.

Let:

$$\text{Signal A} = \sin \frac{2\pi x}{\lambda_E}, \text{ and}$$

$$\text{Signal B} = \sin\left(\frac{2\pi x}{\lambda_E} + 90^\circ\right),$$

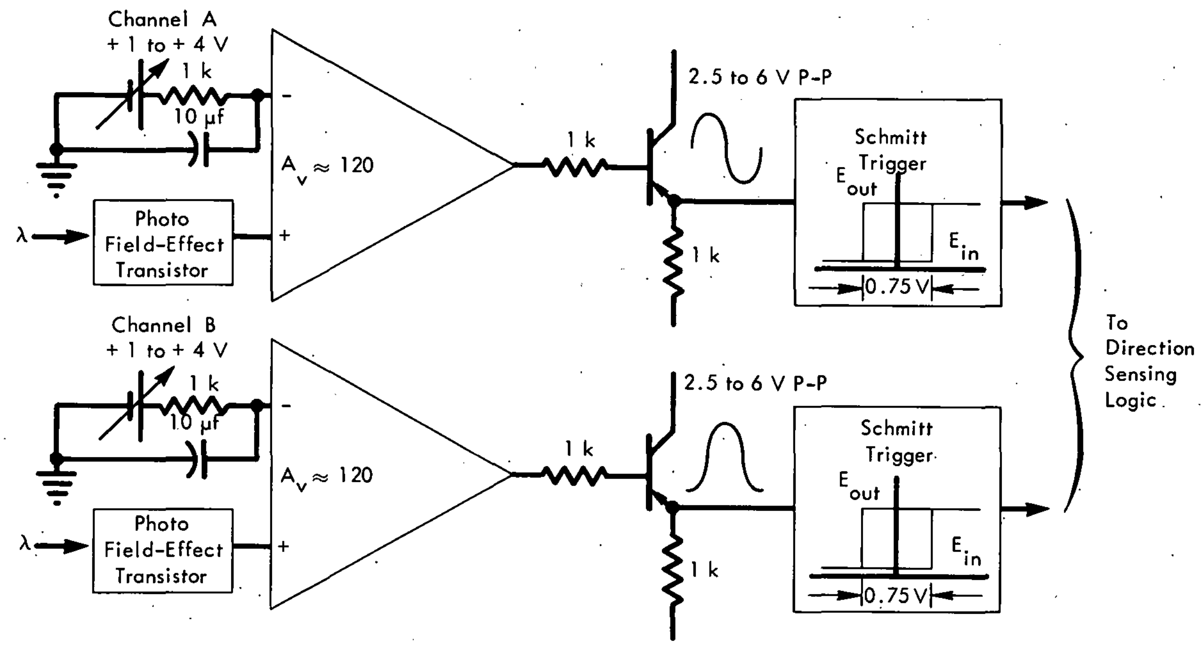


Figure 6. SIMPLIFIED DRAWING OF AN EXISTING INTERFEROMETER SYSTEM ON WHICH THE AUTOMATIC LEVEL COMPENSATING SYSTEM WILL BE USED.

where x is the displacement of the corner cube reflector. An increasing x value, a negative-level drift (-D) for Signal A, and a positive level drift (+D) for Signal B will be assumed. The Schmitt trigger transition point for Signal A is φ_A and for Signal B is φ_B.

Then:

$$\sin \varphi_A - D = 1/2\ H, \text{ and} \qquad (1)$$

$$\sin \varphi_B + D = 1/2\ H, \qquad (2)$$

where:

$\varphi_B = \varphi_A + 90°$,

D represents the drift, and

H the hysteresis width.

An expression for H and D with respect to φ_A can be derived by solving Equations 1 and 2, thus:

$$2D = \sin \varphi_A - \sin (\varphi_A + 90°), \text{ or}$$

$$D = \cos \frac{1}{2} (2 \varphi_A + 90°) \sin \frac{1}{2} (- 90°), \text{ or}$$

$$D = - 0.707 \cos (\varphi_A + 45°).$$

$$H = \sin \varphi_A + \sin (\varphi_A + 90°), \text{ or}$$

$$H = 1.414 \sin (\varphi_A + 45°).$$

For the assumed direction of translation:

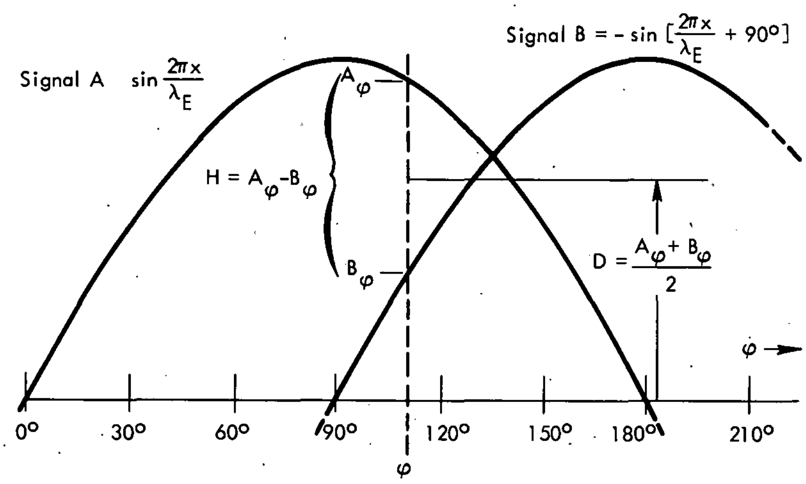
$$n2\pi + 90° \leq \varphi_A \leq n2\pi + 180°.$$

For any φ_A over this range, a maximum D and H which will allow proper operation can be calculated from these expressions.

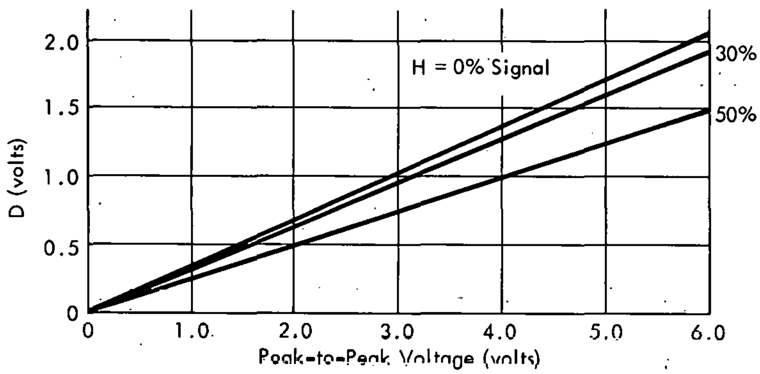
Signal A and inverted Signal B are shown in Figure 7(a) to illustrate a graphical solution of the equations for D and H.

Figure 7(b) presents a plot of the allowable drift as a function of the signal peak-to-peak voltage, V_{p-p}, for several H values expressed as percentages of V_{p-p}. For a 2.5-volt peak-to-peak signal (the smallest normally used in this system), a tolerable level drift of 0.625 volt is read from Figure 7(b).

The condition was that the adjustment was not to be made unless the machine axis was known to be moving. This restriction follows from a consideration of the signal characteristics in the nonmoving case illustrated in Figure 8. In the worst nonmoving case, shown in Figure 8(a), the signal amplitudes would be constant and at least one of the two signals would not be zero. The apparent DC level of one of the channels could be as great as the absolute peak amplitude of its signal. In the best nonmoving case, shown in Figure 8(c), the machine axis would be vibrating due to vibrations transmitted from its mounting pad, or from other moving axes on the machine, and these vibrations would be large enough (many λ_E in amplitude) that the signal average value would essentially be the DC level. Or there could be the in-between case, Figure 8(b), where vibrations would be present but small. Here, the apparent DC level would be somewhere between the actual and one of the peak amplitudes. Vibration frequencies were determined by observation to be 60 or 120 cps and were believed to be caused primarily by rotating synchronous machinery.[4]



(a) Graphical Solution



(b) Allowable Level Drift as a Function of the Signal Peak-to-Peak Amplitude

Figure 7. DRIFT TOLERANCE RELATIONSHIPS.

The cases illustrated in Figure 8(b) and (c) have been observed in existing systems. The case of no vibration, Figure 8(a), has not been observed but could be simulated to some degree by turning off the laser or by obstructing its beam.

With these restraints and conditions in mind, the following design criteria were established for the automatic drift compensation system:

1. The input impedance to the signal monitoring circuit would be 500 Ω or greater.

2. The ACS would be preset within a range of three volts where $+1\text{ V} \leq \text{ACS} \leq +4\text{ V}$.

3. The time constant of the axis "moving" detector would be 1/2 x 1/60 cps, or 8.33 milliseconds or greater.

4. Once "moving" was detected and the DC level was determined to be greater than $|0.3|$ V, a compensating correction would be made.

5. A single correction would not cause the DC level to overshoot the hysteresis band.

6. Corrections would be spaced with adequate time to allow the DC level to respond to one correction before the subsequent one was made.

7. The total range of the ACS would change the DC level by an amount equal to the maximum peak-to-peak signal (6 V), or ± 3 V.

8. Means for an initial setup must be provided.

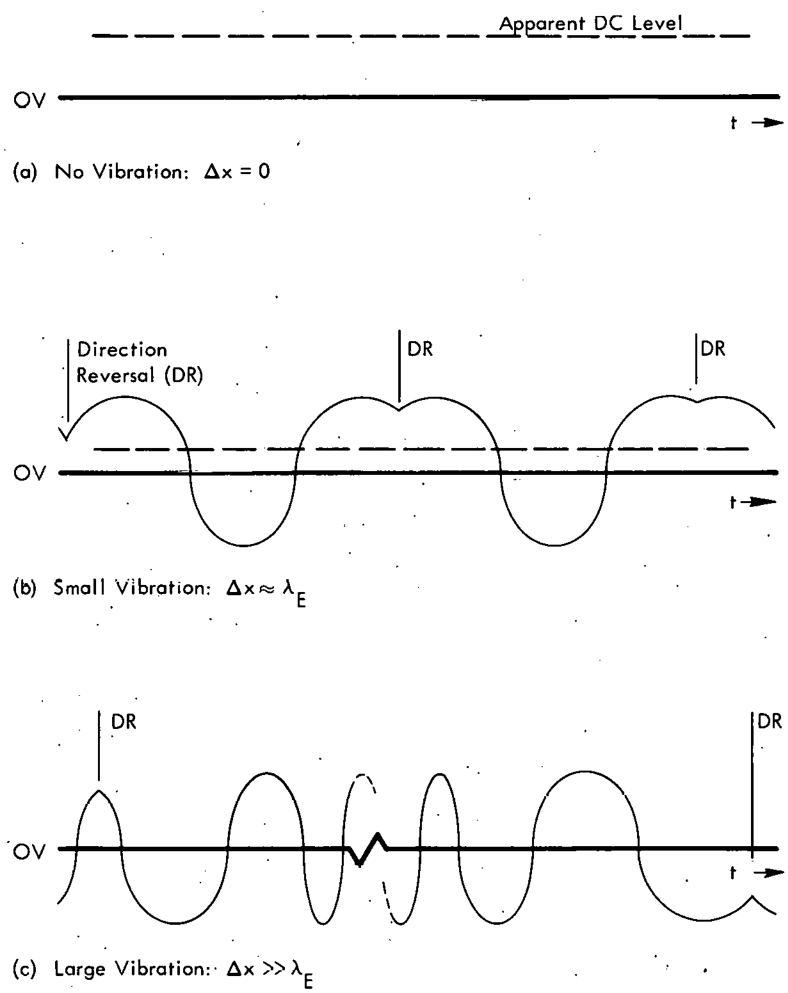


Figure 8. SIGNAL LEVELS FOR THREE NONMOVING CASES.

Figure 9 is a block diagram which is comprised of the existing system, the components of the ALC system which are used by both Channels A and B, and the components which derive the ACS for Channel B (which are duplicated for Channel A but not shown).

Existing Components

The interferometer components and their functions were briefly described earlier and illustrated in Figures 5 and 6. Internally, this system was used intact except that minor circuit adjustments were made in the amplifier output stages and the Schmitt trigger to center the hysteresis band around 0 V to accommodate the ALC system.

Components Used by Both Channels A and B

Moving Detector - The moving detector has for its inputs the up (UP) and down (DN) pulses which also go to the measuring system counters. When the machine axis is moving, there is a predominance of one type of pulse over the other. When the machine axis is not moving but only vibrating, the number of up pulses equals the number of down pulses when measured over several periods of vibration. Therefore, movement can be detected by obtaining a signal proportional to the pulse count difference over a short time period.

A simplified drawing of the moving detector is presented in Figure 10. The logic devices used in the moving detector as well as the other parts of the ALC system are the 5-V TTL devices with 4.5-V logic-level excursions. The monostable flip-flops (MSFF) are needed to broaden the up and down pulses from approximately 300 nanoseconds to 1 millisecond to increase the sensitivity of the moving detectors. The output of the down pulse monostable is a negative pulse which is positively clamped to ground and then goes into the summing filter as a negative signal. The output of the up pulse monostable is a negative pulse which is inverted, is negatively clamped to ground, and then goes into the summing filter as a positive signal. The output of the summing filter goes to two comparators—one responds to a negative voltage which exceeds the negative reference voltage ($-V_R$), the other responds to a positive voltage which exceeds $+V_R$. The comparator outputs are or'ed so that either will provide a moving signal which is used elsewhere in the system. The negative and positive reference voltages chosen were - 0.7 and 0.7 volt, respectively.

The machine velocity threshold, MV_{TH}, which must be exceeded to cause a comparator reference voltage to be exceeded can be calculated from the

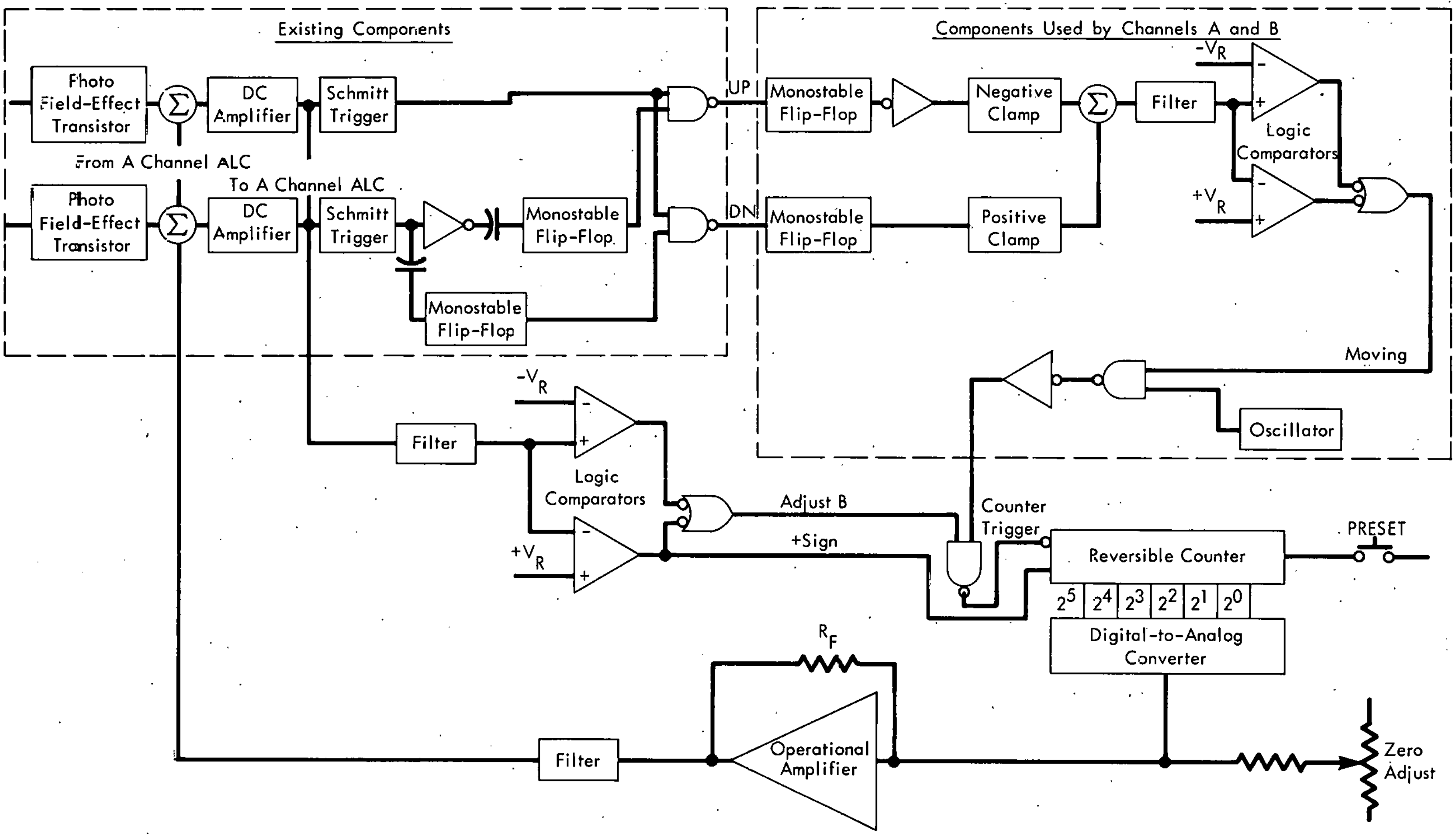
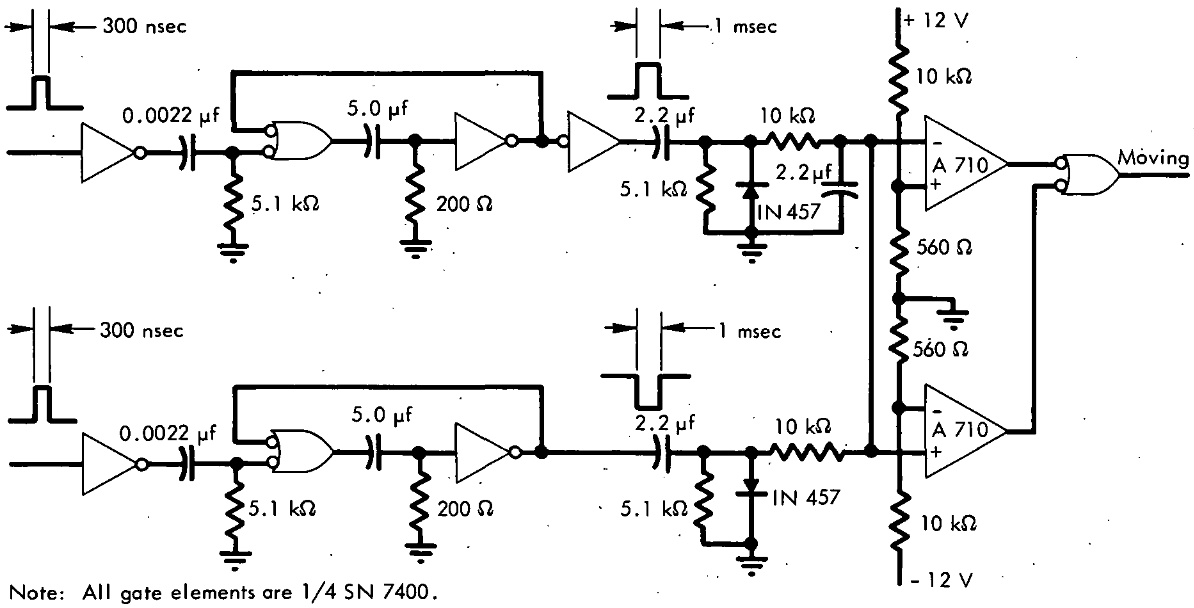


Figure 9. AUTOMATIC LEVEL COMPENSATION SYSTEM.



Note: All gate elements are 1/4 SN 7400.

Figure 10. MOVING DETECTOR.

monostable pulse width, PW, the duty cycle, d, the pulse height, 4.5 V, required to exceed the threshold, and the distance represented by each pulse. The transfer function for the filter is:

$$E_0 = \frac{E_{IN}}{2\left(\frac{RC}{2} S + 1\right)},$$

where:

$$E_{IN} = d \times 4.5\ V.$$

For:

$$E_0 = V_R = 0.7\ V,$$

$$d = \frac{V_R \times 2}{4.5\ V} = 0.312.$$

MV_{TH} can be found from:

$$MV_{TH} = PRF \times \lambda_E, \text{ or}$$

$$MV_{TH} = \frac{d}{PW} \times \lambda_E.$$

Thus:

$$MV_{TH} = \frac{0.312}{1 \text{ msec}} \times 12.5\,\mu\text{in} = 3{,}870\,\mu\text{in/sec} = 0.23 \text{ in/min.}$$

The MV_{TH} arrived at here was thought to be acceptable in most machining and inspection applications. In applications where it is unacceptable, it can easily be changed by changing either V_R or PW. To satisfy Criterion 3, RC/2 must be greater than 8.33 milliseconds. C was chosen to be 2.2 μf and R as 10 kΩ with a resultant time constant of 11 msec. Consequently, a machine velocity equal to MV_{TH} will be detected within approximately 50 msec.

Two modes of operation can be described for the circuit. The first is the axis vibrating mode. In this mode, up and down pulses trigger their respective monostables alternately. A string of up pulses would be followed by a string of down pulses. The string of up pulses would cause the voltage, E_0, to go in a positive direction, the following string of down pulses would cause E_0 to go in a negative direction. The offsetting effects keep E_0 below the threshold of each of the comparators.

In the moving mode, almost all (if not all) the monostable trigger pulses would be either up or down. E_0 would increase or decrease accordingly. If the axis was moving at 0.23 in/min or faster, the appropriate comparator's output would go to zero volt after a time determined by the actual axis velocity, which would be between 4 and 50 milliseconds. A zero-volt output from one of the comparators would produce the moving signal at the output of the nor gate.

Oscillator - A single oscillator is used to provide trigger pulses which are qualified by the moving signal. A simplified diagram of the oscillator is given in Figure 11. The time constant for each of the RC networks coupling the two inverter stages is approximately 75 milliseconds. Consequently, each half cycle of the output is approximately 75 milliseconds long so that the frequency of oscillation is approximately 7 hertz. The oscillator output, $CLOCK_1$, is and'ed with the moving signal to produce the $CLOCK_2$ signal, so $CLOCK_2$ is only present when MV_{TH} is exceeded.

The clock period must be greater than the system response time. This condition is one that is necessary to satisfy Criterion 5. The 150-msec clock

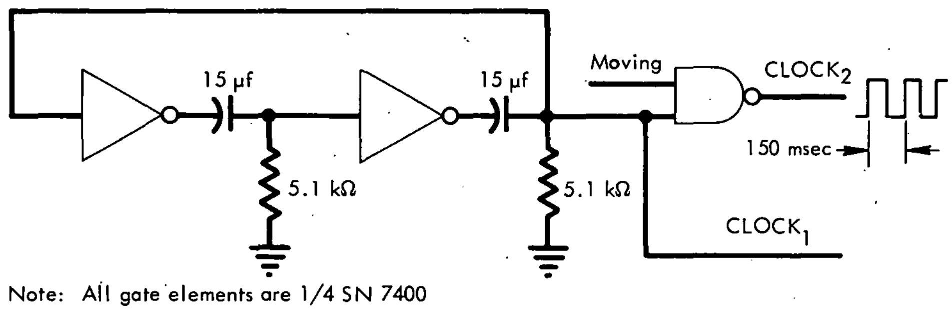


Figure 11. OSCILLATOR.

period does satisfy the criterion, as will be seen from an analysis of the system response time which is presented later.

Components which Derive the ACS for a Signal Channel

There is one set of these components for each channel. Channel B will be referred to in this description.

Signal DC Level Sensor - A simplified drawing of the signal DC level sensor is seen in Figure 12. The input signal to this circuit is obtained from the amplifier output and is the same signal that switches the Schmitt trigger. Generally, the signal is comprised of a DC voltage, which is to be kept within

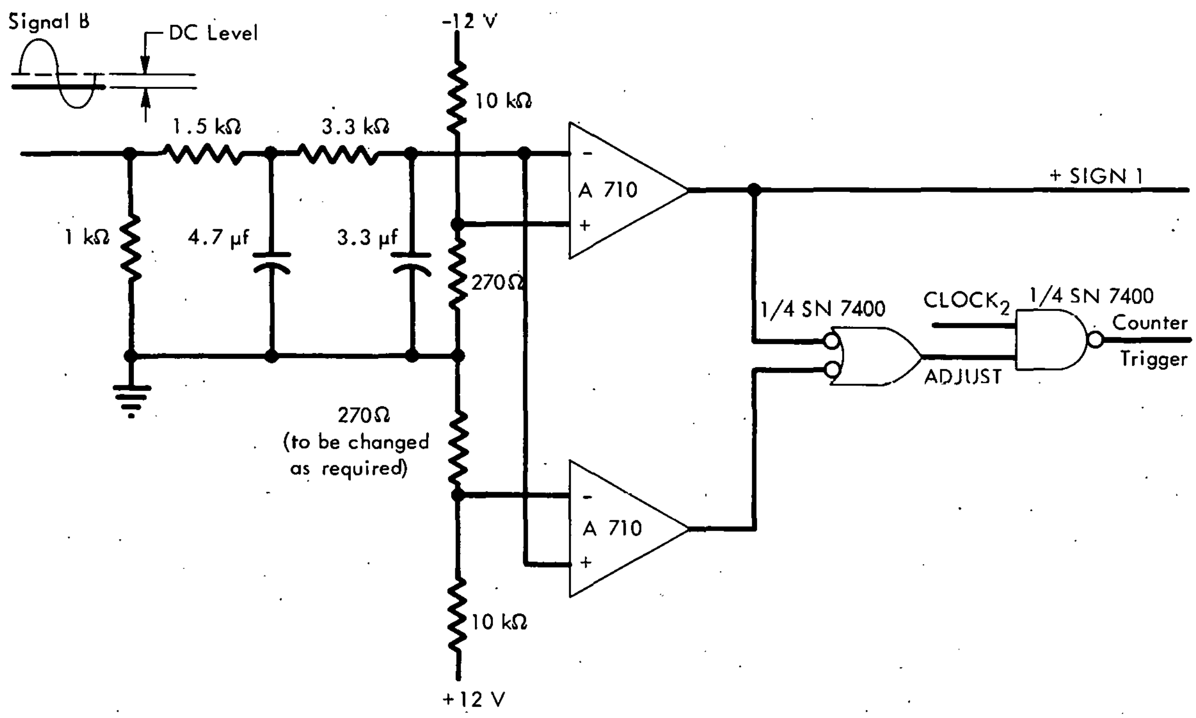


Figure 12. DC LEVEL SENSOR.

the limits defined in Criterion 4, and one of the quadrature signals, of which the frequency is a function of the machine velocity. The peak-to-peak amplitude is adjusted to be in the range of 2.5 - 6.0 volts. The output impedance of the signal source is approximately 20 ohms.

The input signal goes through a low-pass filter to attenuate the quadrature signal. The filter was designed with the following considerations in mind:

1. Provide an acceptably low attenuation of the DC level.

2. Provide little loading of the signal source per Criterion 1.

3. Provide a minimum phase shift of the signal.

4. Attenuate the quadrature signal at 40 decibels or more.

The comparator input bias current is specified by the manufacturer to be a maximum of 15 microamperes at a logic threshold at 70° F. When the negative reference voltage is approached, this amount of current is flowing through the filter. When the voltage is more positive than the negative reference, the amount of current flowing through the filter is greater than 15 μamps (but unspecified by the manufacturer), causing a larger voltage drop. A negative reference voltage and filter voltage drop was chosen to meet Criterion 4, and the positive reference voltage required would be determined experimentally.

A negative reference of -0.32 volt was chosen and the filter DC resistance was set at 4.8 kΩ. Consequently, a negative level less than - 0.32 V + (4.8 kΩ x 15 x 10^{-6} amp) V = - 0.248 volt will cause the negative comparator to change state.

The series input resistance was made 1.5 kΩ to provide an AC load of no greater than about 1.3 percent of the source resistance and negligible phase shift of the signal at the source, thereby satisfying the second and third considerations.

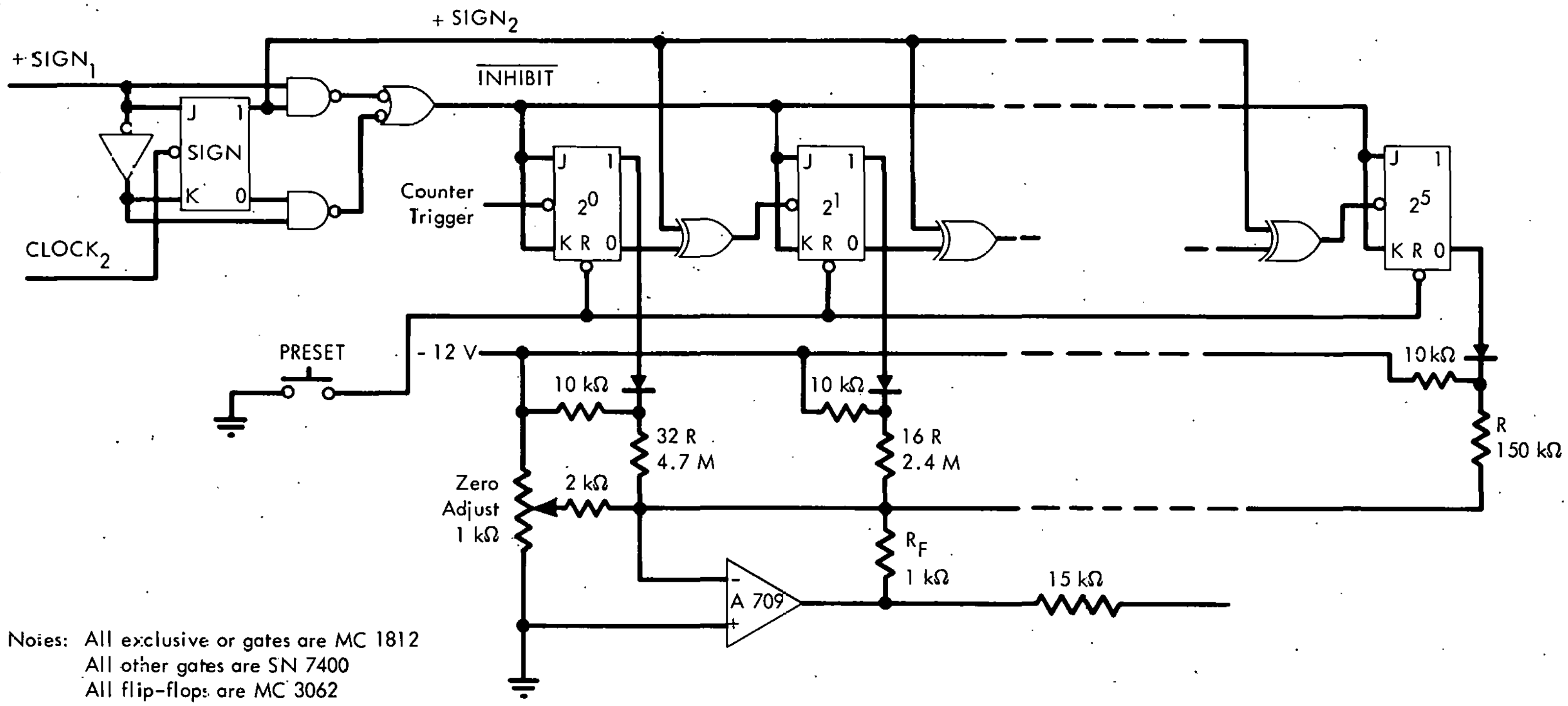
The component values, as shown in Figure 12, gave poles at 8.5 and 39 hertz. This range results in an attenuation of 49 decibels for an input signal of 312 hertz, which satisfies the fourth consideration.

The comparator outputs are normally in a Logic "1" state. They are nor'ed together so that if one of the reference voltages is exceeded, an ADJUST signal is generated at the nor gate output. The ADJUST signal is and'ed with the $CLOCK_2$ signal which is present when moving has been detected. The and'ed output is the COUNTER TRIGGER which will cause the counter to count up or down depending on the state of the + $SIGN_2$ signal. The +$SIGN_2$ signal is derived from the +$SIGN_1$, which is taken from the output of the negative level comparator. Both +$SIGN_1$ and +$SIGN_2$ will normally be in a Logic "1" state and the counter will count up when triggered. When the reference voltage of the negative level comparator is exceeded, +$SIGN_1$ will go to Logic "0" causing the counter to count down when triggered.

Counter and Digital-to-Analog Converter - When the moving signal qualifies $CLOCK_1$ and ADJUST further qualifies it to form the COUNTER TRIGGER for one of the channels, a level compensation adjustment is made.

The Counter used is a six-bit reversible ripple counter with sign control for count direction and an inhibit control which prevents spurious count changes during the sign change. To satisfy Criterion 5, each count could represent no more than a 0.75-volt DC level change, but this will be reduced to 0.5 volt or less to be compatible with the DC Level Sensor deadband. To satisfy Criterion 7, a total change of six volts must be possible. A four-bit counter would have satisfied these requirements, but six bits was chosen since the cost in components was small and increased resolution resulted. The outputs of the Counter flip-flops provide weighted currents to a current summing junction at the input of an operational amplifier which produces an output voltage proportional to the sum of the input currents to the summing junction. This part of the system is shown in Figure 13. The truth table for a reversible counter is given in Table 1. It will be noted that when counting up, if 2^m goes from Logic "1" to Logic "0" then 2^{m+1} changes state. When counting down, if 2^m goes from Logic "0" to Logic "1", then 2^{m+1} changes state. The Counter employed in this system is an economical one component wise, which makes use of these relationships and generates a trigger pulse to the m + 1 flip-flop by using a sign signal and the reset output of the m flip-flop. When the m reset output goes to the same logic state as the sign signal, the exclusive or gate goes from Logic "1" to Logic "0", which triggers the m + 1 J-K flip-flop and makes it change state. Consequently, the count-up sign must be Logic "1" and the count-down sign Logic "0".

The propagation delay of each of the six Counter stages is no greater than 98 nanoseconds so that the worst case (change of Counter state) is accomplished in 588 nanoseconds or less. This short time interval simplifies the filtering of spurious output voltages caused by transient states of the Counter since a relatively wide low-pass filter can be used, keeping the response time small and the component sizes small.



Notes: All exclusive or gates are MC 1812
All other gates are SN 7400
All flip-flops are MC 3062

Figure 13. COUNTER AND DIGITAL-TO-ANALOG CONVERTER.

Table 1

REVERSIBLE COUNTER TRUTH TABLE

t_nUP	2^5	2^4	2^3	2^2	2^1	2^0	t_nDN
0	0	0	0	0	0	0	64
1	0	0	0	0	0	1	63
2	0	0	0	0	1	0	62
3	0	0	0	0	1	1	61
4	0	0	0	1	0	0	60
5	0	0	0	1	0	1	59
6	0	0	0	1	1	0	58
7	0	0	0	1	1	1	57
8	0	0	1	0	0	0	56
9	0	0	1	0	0	1	55
.							.
.							.
.							.
.							.
59	1	1	1	0	1	1	5
60	1	1	1	1	0	0	4
61	1	1	1	1	0	1	3
62	1	1	1	1	1	0	2
63	1	1	1	1	1	1	1
64	0	0	0	0	0	0	0

During sign changes, the Counter must be inhibited to prevent a spurious change of state. To accomplish this, $+SIGN_1$ and the $+SIGN_2$ output of the SIGN flip-flop are applied to a nand gate. If $+SIGN_1$ is not the same logic state as $+SIGN_2$ (the output of the SIGN flip-flop), an inhibit signal is generated which stays in effect until $CLOCK_2$ triggers a change of state of the SIGN flip-flop. The J-K flip-flops can only count when the J and K inputs are Logic "1"; therefore, an $\overline{\text{INHIBIT}}$ signal is used and goes to all J and K inputs of the Counter.

The Counter set and reset outputs are the voltage sources for the weighted currents to the current summing point. Since the Logic "0" state does not give zero volt, but instead about 0.4 volt, the Counter set and reset outputs are clamped to approximately zero volt by the resistor-germanium diode networks shown in Figure 13.

With 2^6 Counter states to satisfy Criterion 7, each step could represent a DC level change of $(6V/2^6) = 0.094$ volt. To compute the operational amplifier gain, the following relationship was used:

$$0.094\ \text{V} = A_v \times 4.5\ \text{V} \times \frac{R_F}{32R},$$

where:

$A_V = 120,$

R_F represents the feedback resistor,

$32R$ the resistance for the least significant bit, and

$\frac{R_F}{32R}$ the voltage amplification of the least significant bit.

Letting:

$$R_F = 1\ \text{k}\Omega,$$

and solving for 32R:

$$32R = \frac{120 \times 4.5\ \text{V} \times 1 \times 10^3\ \Omega}{0.094\ \text{V}} = 5.75 \times 10^6\ \Omega.$$

It was desirable to use available standard resistors so that $32R = 4.7 \times 10^3$ kΩ was used. Therefore, $R \approx 150$ kΩ.

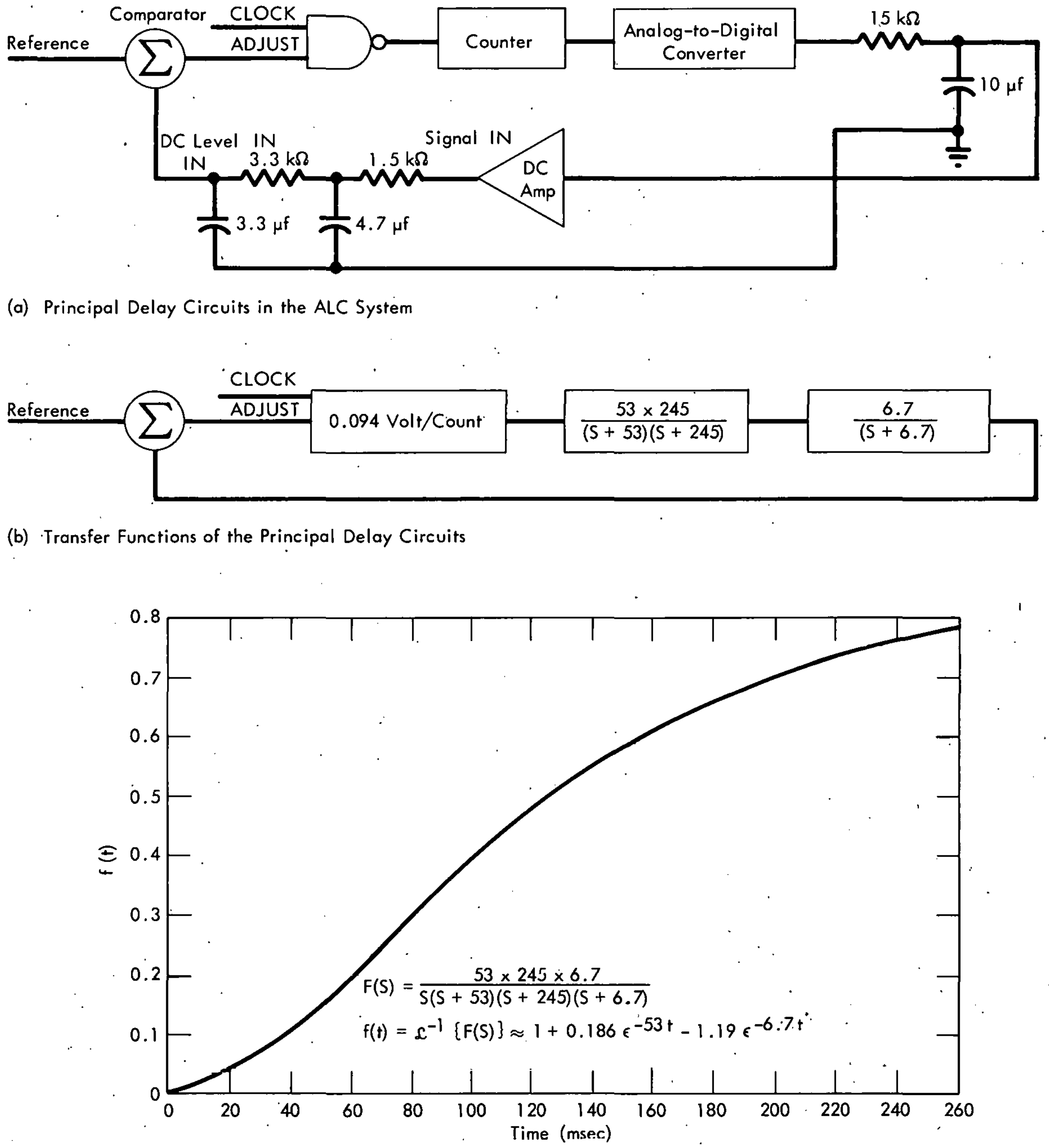
The output of the operational amplifier was filtered to eliminate spurious ACS voltage changes caused by transient states of the counter. The filter time constant was 150 msec, attenuating the amplitude of the worst Counter transient, which would last for no longer than 588 nanosec as stated above, by the factor 3.9×10^{-6}. Expressed in terms of a DC level change, ΔDCL, this value would mean a transient change of:

$$4.5\text{ V} \times \frac{1\text{ k}\Omega}{150\text{ k}\Omega/2} \times 120 \times 3.9 \times 10^{-6}\text{, or}$$

$$\Delta\text{DCL} = 28.0 \times 10^{-6}\text{ V.}$$

<u>System Response Time</u> - The principal system time delays are due to the output filter of the Digital-to-Analog (D/A) Converter which is used to suppress Counter transients and the input filter of the DC Level Sensor which attenuates the AC portion of the signal and passes the DC component. These filter circuits have been previously described individually and now will be considered together to determine the system response time. The system response time will determine the maximum clock rate that can be used. If the clock period is equal to or greater than the system response time, then Criterion 6 will be satisfied. Figure 14(a) shows the filter circuit components in a simplified loop schematic drawing. Figure 14(b) defines the loop in transfer function form. The response to a step function was found by plotting the inverse Laplace transform of the transfer function. The response is shown in Figure 14(c). The composite time constant will be defined as the time to make a 63 percent response, a value of 180 msec. Although a clock period equal to the response time defined in this manner could result in one and only one clock count beyond the minimum number required to return the DC level to within the range of the ± 0.30 volt established in Criterion 4, the 0.30-volt range would not be overshot since each step is only 0.094 volt, nominally. The clock frequency of 7.0 hertz, as told earlier, can therefore be safely used.

The ALC is first set up by presetting the Counter to its midrange by pushing a "preset" button for Channel B. All flip-flops are reset by this action. In order to make this the mid-range condition, the current output of the most significant flip-flop is taken from its reset output and all other current outputs from the set side of their respective flip-flops. While the Counter is in the preset condition (this can be maintained by keeping the preset button depressed or by disconnecting the up and down pulses to the moving detector),



(a) Principal Delay Circuits in the ALC System

(b) Transfer Functions of the Principal Delay Circuits

(c) Step Response Curve

Figure 14. AUTOMATIC LEVEL COMPENSATION SYSTEM TIME RESPONSE.

a manual bias adjustment is made to set the signal DC level at zero volt. The system is then put into the automatic mode by releasing the preset button or reactivating the moving detector.

PERFORMANCE OF THE AUTOMATIC LEVEL COMPENSATION SYSTEM

An ALC system was built essentially as described in the preceding section. The circuits were built using TTL integrated circuit (IC) logic elements, except for the DTL exclusive or gates, and linear IC operational amplifiers and comparators. The system was packaged on a 7 by 10-inch printed circuit board.

An initial checkout of the system, as part of the level control loop for an interferometer amplifier, revealed the need for some detail changes, but the system block diagram remained as previously described. With the changes haywired, the system met all the performance criteria described previously except that Criterion 6 was not checked when using the calculated clock frequency. In order to make the functioning of the system more easily observed during troubleshooting, the clock was slowed to about two pulses per second. At this frequency, Criterion 6 was satisfied; however, it is desirable to make corrections at the fastest possible rate without an overshoot so that necessary adjustments can be made during short moving periods. After the circuit board was revised to incorporate corrections outlined in the next paragraph, the interferometer system was no longer available to be used for checking the accuracy of the calculated optimum clock frequency.

The changes made on the reworked printed circuit board were:

Change 1: The pulse widths of the monostable multivibrators were increased from 1 to 2 milliseconds.

Reason: The pulse height going into the clamp circuits was approximately 3 volts instead of the anticipated 4.5 volts. In addition, the forward drop across the diode caused the clamp reference to be approximately - 0.5 volt instead of 0 volt. The effectiveness of the 3-volt input pulses was, therefore, decreased. The new pulse width requirement was computed as follows:

$$2 \times V_R = d \times \Delta V_E,$$

where:

ΔV_E represents the effective pulse height $= V_1 \dfrac{PW}{\tau} - V_2 \dfrac{\tau - PW}{\tau}$, and

V_R = 0.6 volt (reduced from the 0.7 volt originally used).

In the equation for ΔV_E,

τ represents the period (3.2 msec),

V_1 = 3 volts, and

V_2 = 0.5 volt.

Therefore:

$$1.2 = \frac{PW}{\tau}\left[V_1 \frac{PW}{\tau} - V_2 \frac{\tau - PW}{\tau}\right], \text{ or}$$

$$PW = 2.097 \text{ milliseconds.}$$

Change 2: A low-pass filter was put into the counter inhibit circuit to delay the removal of the $\overline{\text{INHIBIT}}$ signal after a SIGN change.

Reason: There was an apparent race between the $\overline{\text{INHIBIT}}$ and SIGN signals at the change of SIGN. This race was usually won by the $\overline{\text{INHIBIT}}$ signal, probably due to the fact that the switching time of the DTL exclusive or gate was approximately four times that of the inhibit circuit TTL gates.

Change 3: The input filters to the DC level sensors were changed by increasing the resistance values and decreasing the capacitance values while retaining approximately the same time constants.

Reason: To accommodate available nonpolarized capacitors suitable for use on a printed circuit board.

The DC voltage drop across the filter was found to be no greater than 50 millivolts when the total series resistance was approximately 10 kΩ. Since the drop was so small, the positive reference, which was to be experimentally determined, was set equal in magnitude and opposite in sign to the negative reference.

CONCLUSIONS

The Automatic Level Compensation System described here satisfactorily performed in a closed-loop interferometer amplifier application. It was able to detect motion of the machine axis and, when the DC level of the amplifier was outside the desired range, automatically makes a compensating correction.

No spurious level changes were observed when the two conditions stated above were not simultaneously true. The optimum correction rate was analytically determined but not verified because of the unavailability of an interferometer system with which to do this.

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(a) Operated by Union Carbide's Nuclear Division for the US Atomic Energy Commission.