Final Scientific/Technical Report

**Development of Production PVD-AlN Buffer Layer System and Processes to Reduce Epitaxy
Costs and Increase LED Efficiency**

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3. Executive Summary

The DOE has set aggressive goals for solid state lighting (SSL) adoption, which require manufacturing and quality improvements for virtually all process steps leading to an LED luminaire product. The goals pertinent to this proposed project are to reduce the cost and improve the quality of the epitaxial growth processes used to build LED structures. The objectives outlined in this proposal focus on achieving cost reduction and performance improvements over state-of-the-art, using technologies that are low in cost and amenable to high efficiency manufacturing.[1] The objectives of the outlined proposal focus on cost reductions in epitaxial growth by reducing epitaxy layer thickness and hetero-epitaxial strain, and by enabling the use of larger, less expensive silicon substrates and would be accomplished through the introduction of a high productivity reactive sputtering system and an effective sputtered aluminum-nitride (AlN) buffer/nucleation layer process. Success of the proposed project could enable efficient adoption of GaN on-silicon (GaN/Si) epitaxial technology on 150mm silicon substrates.[2] The reduction in epitaxy cost per cm^2 using 150mm GaN-on-Si technology derives from (1) a reduction in cost of ownership and increase in throughput for the buffer deposition process via the elimination of MOCVD buffer layers and other throughput and CoO enhancements, (2) improvement in brightness through reductions in defect density, (3) reduction in substrate cost through the replacement of sapphire with silicon, and (4) reduction in non-ESD yield loss through reductions in wafer bow and temperature variation. The adoption of 150mm GaN/Si processing will also facilitate significant cost reductions in subsequent wafer fabrication manufacturing costs.

There were three phases to this project. These three phases overlap in order to aggressively facilitate a commercially available production GaN/Si capability. In Phase I of the project, the repeatability of the performance was analyzed and improvements implemented to the Veeco PVD-AlN prototype system to establish a specification and baseline PVD-AlN films on sapphire and in parallel the evaluation of PVD AlN on silicon substrates began. In Phase II of the project a Beta tool based on a scaled-up process module capable of depositing uniform films on batches of 4" or 6" diameter substrates in a production worthy operation was developed and qualified. In Phase III, the means to increase the throughput of the PVD-AlN system was evaluated and focused primarily on minimizing the impact of the substrate heating and cooling times that dominated the overall cycle time.

4. Comparison of Actual Accomplishments with Goals and Objectives

In Table 1, the project plan for the two year program has been summarized. All major tasks were completed with 70% on-time or ahead of schedule. The early tasks (2-5) were focused on the initial goal to deposit the PVD AlN buffer layer on sapphire substrates to provide a reference for the GaN on Si development, prove hardware performance, and evaluate LED performance with the PVD films compared to the nucleation and buffer pre-layers of low temperature MOCVD-GaN (LT-GaN) that manufacturers have developed.

The AlN films were characterized for film NU, crystal quality and surface morphology/microstructure. GaN was subsequently grown on the AlN templates.

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Table 1: Task Project Plan

	Tasks	Original EST DOC	Actual DOC	Current Status	Comment
1	Project Management Plan	9/26/2011	9/26/2011	Done	Completed on schedule
2	Prototype System Development	11/1/2011	12/15/2011	Done	Completed 6 weeks behind original plan
2.1	Baseline AIN/GaN on sapphire	11/1/2011	12/15/2011	Done	Completed 6 weeks behind original plan
2.2	Baseline AIN on Si	5/1/2012	4/15/2012	Done	Baseline established 2 weeks ahead of original plan - Film quality not yet at target
3	Thermal MGMT Redesign	11/15/2011	10/1/2011	Done	Completed 6 weeks ahead of original plan
3	In-situ PC	11/15/2011	1/15/2012	Done	Ex-situ PC successfully established 8 weeks behind original plan
3.1	Design Report	11/15/2011	12/15/2011	Done	Completed 4 weeks behind original plan
3.2	Native Oxide Removal	2/1/2012	1/15/2012	Done	Native Oxide removal by ex-situ PC established baseline 2 weeks ahead of original plan
4	Demo and spec Finalization for Prototype	1/15/2012	2/15/2012	Done	Completed 4 weeks behind original plan
4.1	Prototype Demo Capability	1/15/2012	2/15/2012	Done	Completed 4 weeks behind original plan
4.2	Baseline GaN on AIN/Si	5/1/2012	4/1/2012	Done	Baseline established 4 weeks ahead of original plan - Film quality not yet at target
5	Silicon Substrate Evaluation with Kyma	5/1/2012	9/28/2012	Done	Completed on on schedule (revised plan)
6	Design of the Beta Tool	11/31/2011	10/31/2011	Done	Completed 4 weeks ahead of original plan
7	Hardware Procurement of the Beta Tool	1/31/2012	12/31/2011	Done	Completed 4 weeks ahead of original plan
8	Assembly and Test of Beta Tool	6/1/2012	4/27/2012	Done	Completed 5 weeks ahead of original plan
9	Qualification of the Beta System	8/1/2012	7/9/2012	Done	Completed 3 weeks ahead of original plan
9.1	Baseline AIN/ Si Beta process	8/31/2012	8/31/2012	Done	Completed on schedule
	AIN/ Si Beta process (Improved film quality)	8/31/2012	9/14/2013	Done	XRD film quality was improved in 2013 with addition of new h/w
9.2	Baseline GaN on AIN/Si process	8/31/2012	8/31/2012	Done	Completed on schedule
	GaN on AIN/Si process (Improved film quality)	8/31/2012	9/6/2013	Done	No GaN film cracking or Si meltback confirmed in 2013
10	Throughput Enhancement Evaluation	11/1/2012	12/15/2012	Done	Completed 6 weeks behind original plan
11	Manufacturability	9/14/2013	9/6/2013	Done	Completed 1 week ahead of schedule
12	Throughput Improvement Study Design	8/29/2013	9/14/2013	Done	Completed two weeks behind original plan

MOCVD GaN recovery and film quality was compared to GaN grown without a PVD buffer/nucleation layer. A summary of the key film metrics, goals and results are shown in Table 2; Veeco met all technical targets. In Figure 1, we have described the technique used to estimate defect density from XRD. With a FWHM of 1250s^{-1} for the off axis (103) peak, a maximum edge dislocation density of $9 \times 10^9 \text{ cm}^{-2}$ was calculated and from the FWHM of the (002) peak of 380 s^{-1} a screw dislocation density of $3 \times 10^8 \text{ cm}^{-2}$ was estimated. Surface roughness from 0.3-0.5nm was typically obtained as observed in the AFM image in Figure 2. Although high quality GaN was deposited on PVD AIN, manufacture of rudimentary LED devices never demonstrated higher brightness when compared against the standard LT GaN buffer layer process (Table 3). Substrate bow using the sputtered AIN buffer layer proved to be difficult to reduce and could not be controlled with PVD process. Wafer bow as a function of MOCVD growth on PVD and LT GaN nucleation layers is shown in Figure 3.

The remaining tasks covered Phases II and III, the major focus of the project. Tables 4 and 5 summarize the key program accomplishments from the high productivity reactive AIN system. In the following report, we will detail the steps Veeco took to develop this hardware and process and finally conclude with the status of the program.

Table 2: Film Properties of PVD AIN (GaN) on Sapphire

Parameters	Units	AlN		GaN	
		Result	Target	Result	Target
WiW, NU	1 σ , %	<4	<5	<3	<5
WtW		<6	<8	<10	<10
Film Quality	002 ω , arcsec	~350	<400	<200	<350
	102 ω , arcsec	~3000	----	~200	<500
Defect Density (from XRD)	Screw, cm ⁻²	----	----	<5 x10 ⁸	<5 x10 ⁸
AFM Roughness	RMS, nm	0.3-0.5	<2	~0.3	<2
Epitaxial Growth	----	Yes	Yes	Yes	Yes

Figure 1: AlN Defect Density Estimation from XRD

Figure 2: Surface Roughness of 50nm AlN Film on Sapphire

Table 3: LED Device Benefit

Parameter	Result	Target
Improved Crystallinity	~180 arcsec	<200 arcsec
Defect Reduction	$2 \times 10^8 / \text{cm}^2$	Mid $10^8 / \text{cm}^2$
Brightness	~equal to	5% improvement

Figure 3: Sapphire Substrate Wafer Curvature vs. MOCVD GaN Growth Step

Table 4: Film Properties of PVD AIN (GaN) on Si

Parameters	Units	Initial Config. (Single Cathode)				Final Config. (Dual Cathode)			
		AlN		GaN		AlN		GaN	
Substrate: Si		Result	Target	Result	Target	Result	Target	Result	Target
WiW, NU	1σ, %	<4	<5	<3	<5	<4	<5	<3	<5
WtW		<6	<8	<10	<10	<3	<8	<8	<10
Film Quality	002ω, arcsec	~2500	<1500	<600	<350	~1800	<1500	~480	<350
	102ω, arcsec	~3300	<1500	<700	<500	~2600	<1500	~680	<500
Defect Density (from TEM)	Screw, cm ⁻²	NA	NA	~3 x10 ⁸	<5 x10 ⁸	NA	NA	~3 x10 ⁸	<5 x10 ⁸
AFM Roughness	RMS, nm	0.3-0.8	<2	~0.3	<2	0.3-0.8	<2	~0.3	<2
Defectivity	Qualitative	High	10x imp	NA	NA	≥10x imp	10x imp	NA	NA
Melt back	Qualitative	NA	NA	Yes	No	NA	NA	No	No
Epitaxial Growth	----	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 5: Film Hardware and Manufacturability Summary

Parameter	Units	Result	Target
Throughput	wph	11-12	>12
Target Life	kWh	*700	>875
Shield Life	kWh	400	>250
Particle Defect	Mechanical @ >0.2μm	320	<1000
	In-film @ >0.2μm	900	<1000

**Target life expected to exceed 900kWh*

5. Project Activity Summary

Prototype System Development

In order to mitigate risk to the program, certain hardware concepts needed to be evaluated and their risks retired quickly. Veeco assembled a prototype PVD AIN module based on Veeco's MOCVD CVD system in order to demonstrate the feasibility of a PVD buffer for MOCVD GaN growth. In Figure 4 a picture of the system is shown. Using the CVD system as the basis for the PVD prototype allowed Veeco to reuse the essential high temperature components that would be necessary to deposit an epitaxial like PVD film. The system still needed to be modified to accommodate a sputtering target and improved vacuum

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performance. A base vacuum in the 10^{-8} Torr range was needed for high quality AlN. The prototype tool was an ideal test vehicle to prove out initial concepts and to demonstrate the baseline PVD process performance before committing to the high productivity system build.

Figure 4: Prototype PVD AlN Test stand

As previously mentioned, it was important to be able to physically deposit the AlN at high deposition temperatures in order to promote the epitaxial growth on the substrate. As an additional requirement, the sputtered material would need to be guided (flux control) for optimal deposition uniformity and directionality. A water cooled lid, chimney and high temperature shutter concept was initially evaluated for these purposes.

Epitaxial growth on a variety of substrates was successfully demonstrated in the prototype test stand and the key concepts were designed into the beta production system. High resolution TEM's and Selected Area Diffraction Patterns (SADP) are shown in the following figure (Figure 5) confirming that the PVD AlN was grown epitaxially on both sapphire and silicon.

Figure 5: High Resolution TEM and SADP of PVD AlN on Various Substrates

This initial investigation also revealed some notable deficiencies in the prototype system that would need to be addressed in the following design. For manufacturability and throughput the deposition area / rate would need to be increased. The size of the sputtering target would be increased from 4" circular design to an approximately 11" triangular design to incorporate a delta type magnetron configuration for a larger deposition radius capable of coating multiple substrates. Process improvements would also be necessary to improve the buffer layer and subsequent GaN deposition. The latter would prove to be the most challenging aspect of the project and will be discussed later.

Beta System Development

The Beta system design began in late 2011 and final testing was not completed until the end of April of the following year. Veeco again reused the essential high temperature components from their MOCVD systems for the Beta system. The front end and the transport module are essentially the same as Veeco's K465 MOCVD system. The Beta system could accommodate up to three carriers (one in load lock and two in the handler) to improve steady state throughput. The expectation was that there would be a carrier completing cool down in handler, one in process and one outgassing in the load lock in high volume production. The system is configurable for up to two process chambers (C-2 configuration) although this first system was only configured as a C-1. The front end, handler, and entire system are shown in Figure 6.

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The process chamber was specifically designed for high temperature deposition of sputtered films. Equipped with both a turbo pump and a cryo pump, a system base of $<3 \times 10^{-8}$ Torr can be achieved at room temperatures and base pressures of $<3 \times 10^{-7}$ Torr can be maintained at elevated temperatures above 700C. With completion of the acceptance testing the new system was successfully transferred from Engineering to Process development to transition the initial sputter process developed on the prototype system to the Beta system, scale it up for batch processing, and optimize it to meet the specifications and targets set for the program. Process and hardware optimization would actually continue until the end of the program in September 2013.

GaN on Si Process Optimization: Closed Loop Voltage Control

Optimization of the PVD AlN buffer layer Ar/ N₂ ratio at temperatures close to 900C proved to be challenging. The process window for optimal stoichiometry of the initial deposition layer or “barrier layer” is critical to avoid or minimize AlN –Si interface silicide formation (high Ar/ N₂ ratio) and nitridation - amorphous interlayer formation (low Ar/ N₂ ratio). Veeco investigated the initial deposition and interface for several months before we were able to develop a repeatable and robust process.

The initial growth studies revealed that direct growth of AlN films (without the barrier layer – low Ar/ N₂) in poison mode (of hysteresis curve) on Si would lead to the significant nitridation of the Si-AlN interface and consequently a poorer quality interface leading to the deposition of poorer quality AlN epilayer. This was evident in the TEM micrograph and the EDS spectrum of the interface in Figures 7a) and b). In the EDS spectrum, the Al signal lags N spectra around the interface region, confirming the formation of Silicon-nitride phase. On the other hand, deposition of metallic rich film (metal mode of hysteresis) – high Ar/N₂, as a barrier layer, yielded high-quality AlN (Figure 8a) in some areas combined with spots of Al silicide (clustering) as a result of Al and Si interaction and formation of poor morphology (Figure 8b). Hence, the barrier layer growth conditions had to be in an optimal range to enable the formation of homogenous and stoichiometric AlN phase with limited reactivity to Si. Under optimum conditions the deposited AlN films led produced smooth epilayers with good microstructure as evidenced in Figures 9 a) and b).

Figure 6: Beta High Productivity PVD AlN System Including Front End (LFA and Load lock) and Handler

Figure 7: a) Cross section TEM micrograph of AlN deposited without barrier layer – low Ar/ N2 ratio. b) EDS spectrum of the corresponding interface

Figure 8: a) Cross section TEM micrograph of AlN deposited with heterogeneous Al rich barrier layer. b) AFM image for the corresponding film

Figure 9 (a) Cross section TEM micrograph of AlN deposited with optimized homogeneous Al rich barrier layer. (b) AFM image for the corresponding film

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Films deposited under these conditions involved working in an extremely unstable region of the hysteresis curve of the reactively sputtered Al target (Figure 10). This could not be achieved without using closed loop voltage control [3, 4]. With this control, the reactive gas flow rate could be adjusted to maintain a target voltage, advantageous for operating sputtering processes in the transition mode (in between a metallic and poison target mode).

Figure 10: Closed Voltage Loop Control

GaN on Si Process Optimization: Dual Magnetron

Although the closed loop voltage control provided the necessary control of the Ar/N₂ film stoichiometry to be able to effectively deposit metal rich films, minimizing Si surface nitridation, the process was prone to a higher level of micro-arcing as the deposition time increased. The arc frequency increased by 10X over films deposited with the target operating in a poison mode of the hysteresis curve; the voltage control mode was therefore only used for the barrier layer to enable the growth of the best quality films. The inability to operate in voltage controlled mode for the entire AlN process lead to the next set of complications and the need for further hardware optimization. Repeated switching back and forth between transition and poison mode necessitated shuttering and reconditioning the target for each mode. The defect levels increased and subsequent GaN processing resulted in poorer quality films. In Figure 11, an example of a highly defective GaN growth is shown in an optical image with 50X magnification.

Figure 11: Optical Image of GaN on PVD AlN Buffer deposited in Closed Loop Voltage Control

Alternatively, if a second magnetron was employed, two individual processes could be controlled during the transition layer (barrier layer to epi AlN layer) minimizing micro-arcs and provide better control over the entire buffer layer process. Additionally, the constant need for shuttering the target would be reduced as less target conditioning would be needed. The time spent reconditioning the target directly related to the throughput so it would be improved with the addition of the second magnetron. Lastly, another magnetron could provide more flexibility to deposit alternate more exotic bilayers structures for stress control prior to the GaN growth (potentially eliminating the MOCVD stress layers now currently in use). With the dual magnetron, PVD AlN smooth epitaxial layers could be manufactured with good microstructure and low defectivity. There was one remaining step in the buffer layer growth that needed to be addressed before these layers could be reliably deposited in high volumes and it was the silicon surface pre-treatment or pre-clean. In Figure 12, several optical images trace the defect propagation from the native Si surface to the subsequent PVD AlN surface.

Veeco evaluated both in-situ thermal pre-clean [5-23] and the option for remote plasma pre-clean [24] as well as ex-situ wet pre-clean techniques. After extensive testing and evaluation, wet chemical etching of the silicon surface proved to be the simplest and most robust method remove the native oxide and prepare the Si surface for epitaxial growth. The equipment used for Si surface preparation is shown in Figure 13 and included a wet bench, an automated spin rinse dry, and of course a monitored DI water supply. After implementing a standard wet clean procedure [25, 26], defect free AlN films could be deposited. GaN epilayers were subsequently deposited with no evidence of melt back (Figure 14).

GaN on Si Process Optimization: GaN Growth

The results from the MOCVD GaN growth on the optimized PVD buffer layer will be discussed in this section of the report. For reference and a basis of comparison, GaN epilayers grown on MOCVD AlN templates were run concurrently with the PVD templates. Our MOCVD division in Somerset, NJ provided tool time and supporting analysis for the GaN deposition runs. XRD and AFM were again used to assess crystal quality and surface microstructure. The XRF spectra in Figure 15 were representative of typical GaN layers deposited using the AlN buffer layers. The XRD film quality was very similar with no significant difference in the symmetric line broadening from the (002) peak with either buffer layer. The line broadening from the (102) peak is slightly worse for the PVD AlN buffer samples and was consistently observed throughout the program.

Figure 12: Defect Propagation from Initial Surface to Buffer Layer

Figure 13: Veeco Ex-situ Wet Clean Surface Preparation for Si; GaN on Si Program

Figure 14: Optical Micrographs comparing GaN Epilayer Quality on PVD AIN

Figure 15: Representative XRD Spectra of GaN Epilayers on AIN Templates

Figure 16: Representative AFM images of GaN Epilayers on AIN Templates

Figure 17: TEM of GaN on PVD AlN; Dislocation Defects Identified

AFM and TEM measurements confirmed smooth GaN epilayers could be deposited using the PVD AlN templates. Less than 0.3nm surface roughness (Figure 16) was measured by AFM comparable to the roughness measured using MOCVD AlN as a buffer layer. The AFM surface morphology was also indicative of low defect coalesced GaN layers. The program target of $<5 \times 10^8 / \text{cm}^2$ defect density was achieved using the PVD buffer layers. TEM analysis (Figure 17) indicated that the screw dislocation density was $<3 \times 10^8 / \text{cm}^2$ (associated with symmetric line broadening from 002 peak). Edge dislocation density was slightly higher, approximately $\sim 3.5 \times 10^8 / \text{cm}^2$ (associated with asymmetric line broadening from 102 peak), consistent with the XRD film measurements previously discussed. In the end the PVD buffer layers failed to produce GaN epilayers with substantially better film quality than MOCVD AlN layers as Veeco had expected.

Beta System Manufacturability: AlN Buffer Layer Process Repeatability

The Wafer to Wafer (WTW) and Run to Run (RTR) thickness and film quality with the optimized process was evaluated over several runs with varying numbers of wafers in each run (from 2-9 samples / run). Thickness repeatability as measured optically and film quality was measured by XRD (002, 105, 102 peaks). The deviation was calculated as a Range/Mean, R/M. WTW variation was $\leq 2\%$ for thickness and film quality. RTR thickness variation was much tighter at $\leq 0.5\%$. Film quality varied from 1%-2%, with the repeatability in (002) 1%. The

process repeatability significantly exceeded expectations and was strong positive indicator for performance expected in high volume production.

Beta System Manufacturability: Throughput Improvement

Throughput improvements were necessary to meet the program objectives with a 25% increase in throughput from 9 wafers / hr. to 12 wafers / hr. Several modifications were made to the system to reduce overhead and process time. Final throughput was estimated based on calculations with the hardware modifications that were made. The process steps were shown in Figure 18. Comparing the graphs, it can be seen that overhead (heating and cooling) is the most significant contributor to the overall process time and throughput.

Figure 18: Process Time Calculation

An investigation of the Loadlock pump down times revealed that outgassing from the wafer carrier significantly impacted time to base. In particular the quality of the SiC coating that was applied to the graphite carrier was found to directly relate to the outgassing performance. In Figure 19, the pump down performance from a standard carrier completely coated with SiC was compared against one with the coating partially removed from the surface (Modified Carrier). Base vacuum (10^{-6} Torr levels) was achieved in $< 20min$ for the partially coated carrier as compared to the fully coated carrier which was still in the 10^{-2} Torr range for the same time period. As previously discussed, the PVD is sensitive to the process chamber base vacuum and excessive outgassing of material in this environment would be detrimental to the epilayer process. Reaching high vacuum in the initial pump down from atmosphere was critical for quicker process starts.

Figure 19: Loadlock Pumpdown Performance

The transfer module was originally configured with a metal transfer end-effector with a temperature transfer limit of 350C. By using a ceramic end-effector already employed in some of Veeco's MOCVD systems, the transfer temperature could be increased by ~50C; a lot could be effectively transferred to the central handler's wait station 10 minutes faster and allow for the next lot to be transitioned to process. The remaining cool down could be performed in the central handler at elevated pressures as noted in the graph on the right in Figure 18.

Beta System Manufacturability: Bilayer Stress and Strain Control

As previously mentioned in the section that discussed the dual magnetron, another advantage of the second deposition source was the capability to deposit bilayers or multilayer structures for stress and strain control. SiC was chosen as a good first candidate for a bilayer with AlN due to its compatibility with Si. A SiC/AlN buffer layer was deposited onto a silicon substrate after Veeco's standard substrate surface pretreatment and compared to the standard PVD AlN buffer layer. The film stress was tuned from a tensile stress state of 300 MPa (AlN only) to a compressive film stress state of ~50 MPa (SiC/AlN) with the SiC layer directly deposited onto Si (first layer). TEM microscopy (Figure 20a) confirmed an epitaxial relationship between SiC and AlN, however, the direct deposition of the SiC on Si did lead to void formation in the substrate and twinning defects (Figure 20b) in the films. This phenomenon known as the Kirkendall effect would be minimized with a non-stoichiometric SiC target. [27, 28]

Figure 20: TEM and SADP of SiC/AlN Bilayer

6. Products Developed

a. Publications

Below is a list of the publications / posters that were presented under the DOE program. They have previously been distributed to Brian Dotson, Veeco's program manager.

- SSL MFG R&D Workshop, June 13-14, 2012, San Jose, CA
 - “Development of Production PVD-AlN Buffer Layer System and Processes to Reduce Epitaxy Costs and Increase LED Efficiency (EE0005064)”
- International Workshop on Nitride Semiconductors, October 14-19, 2012 Sapporo, Japan
 - “Development of PVD-AlN Buffer Process for GaN-on-Si High Power LED”
- 2013 International Conference on Compound Semiconductor Manufacturing Technology, May 13-16, 2013, New Orleans, LA
 - “Development of PVD-AlN Buffer Process for GaN-on-Si”
- MRS Proceedings, Volume 1492, 2013,

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- Microstructure of epitaxial AlN layers on sapphire substrates deposited by physical vapor deposition
- SSL MFG R&D Workshop, June 5-6, 2013, Boston, MA
 - “Development of Production PVD-AlN Buffer Layer System and Processes to Reduce Epitaxy Costs and Increase LED Efficiency”

c. Networks and collaborations fostered

Veeco collaborated with Kyma Technologies, Inc. in the early phases of the program. With their assistance, the feasibility for in-situ H₂ pre-clean in a PVD sputtering system was confirmed. In addition, Kyma also provided a comprehensive library background for GaN on Si development which provided Veeco the ability to research history and background developments with ease, thereby accelerating the program objectives. The reports Kyma generated were provided as addenda to the final technical report. Addendum I contained the reference library Kyma assembled for Veeco and in Addendum II, the Kyma final report was included.

d. Technologies/Techniques

DOE support enabled Veeco to design, develop, and manufacture their first high temperature, high productivity PVD platform capable of depositing epilayer films. Several other technologies and in particular piezoelectric applications could benefit from the hardware and processes developed in this program.

8. Concluding Remarks

In conclusion, Veeco successfully developed a high temperature PVD AlN buffer system capable of depositing epitaxial quality films to meet the DOE program goals and objectives. Although GaN epilayers could be deposited onto the PVD templates with film quality similar to that achieved using MOCVD AlN buffer layers, Veeco could not achieve the breakthrough performance they were seeking in order to advance the GaN on Si technology. Although the performance benefits using the PVD buffer layer could not be realized, the cost of ownership using PVD buffer layers and/or potentially stress and strain control using PVD multilayers could still be advantageous for the industry.

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