BNWL-1498
UC-32

THE FFTF HYBRID COMPUTER SYSTEM

K. M. Busness

September 1970

AEC RESEARCH &
DEVELOPMENT REPORT

RECEIVED
OCT 15 1970
ROBERT K. SHARP

BNWL-1498

BATTELLE

NORTHWEST

BATTELLE MEMORIAL INSTITUTE PACIFIC NORTHWEST LABORATORIES
3000 STEVENS DRIVE, P. O. BOX 999, RICHLAND, WASHINGTON 99352

LEGAL NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Atomic Energy Commission, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

PACIFIC NORTHWEST LABORATORY

RICHLAND, WASHINGTON

operated by

BATTELLE MEMORIAL INSTITUTE

for the

UNITED STATES ATOMIC ENERGY COMMISSION UNDER CONTRACT AT(45-1)-1830

BNWL-1498

UC-32, Mathematics
and Computers

THE FFTF HYBRID COMPUTER SYSTEM

K. M. Busness

Computers and Control Department
Systems and Electronics Division

September 1970

FIRST UNRESTRICTED
DISTRIBUTION MADE

OCT 14 '70

BATTELLE MEMORIAL INSTITUTE
PACIFIC NORTHWEST LABORATORIES
RICHLAND, WASHINGTON 99352

Printed in the United States of America
Available from
Clearinghouse for Federal Scientific and Technical Information
National Bureau of Standards, U.S. Department of Commerce
Springfield, Virginia 22151
Price: Printed Copy \$3.00; Microfiche \$0.65

ABSTRACT

A hybrid computer system has been developed to augment the simulation studies and design effort for the Fast Flux Test Facility. A Digital Equipment Corporation PDP-9 digital computer and Applied Dynamics/Four analog computer were interfaced by means of high speed analog-to-digital and digital-to-analog conversion equipment. A control interface was developed to provide digital control of analog/hybrid functions.

TABLE OF CONTENTS

	<u>Page</u>
ABSTRACT	.iii
LIST OF FIGURES	vi
INTRODUCTION	1
SUMMARY	1
SYSTEM DESCRIPTION	3
Digital Computer	3
Input/Output	3
Peripheral Devices	5
Modifications	5
Analog Computer	7
Data Interface	7
Analog-to-Digital Conversion	7
Digital-to-Analog Conversion	11
Control Interface	11
Analog Addressing	14
Mode Control	14
Servo Pot Setting	15
Digital Coefficient Units	15
Logic Control and Sense Lines	16
Software	16
Analog-to-Digital Conversion	16
Random Addressing	16
Repetitive and Sequential Modes	17

	<u>Page</u>
Digital-to-Analog Conversion	18
Analog Address and Control	18
Interrupts	18
Data Channel	18
Real-Time Clock	20
Automatic Priority Interrupt	20
Program Interrupt	20
REFERENCE DOCUMENTS	22
APPENDIX A APPLIED DYNAMICS/FOUR EQUIPMENT COMPLEMENT	
APPENDIX B IOT INSTRUCTION FORMAT	
APPENDIX C HYBRID INSTRUCTIONS	
APPENDIX D DATA CONVERSION ROUTINES	
APPENDIX E A/D AND D/A BINARY-TO-VOLTAGE CONVERSION	
APPENDIX F DATA TRUNK LINE ASSIGNMENTS	
APPENDIX G HYBRID CONTROL ROUTINES	
APPENDIX H SERVO POT COEFFICIENT TABLE	
APPENDIX I DCU COEFFICIENT TABLE	
APPENDIX J INTERRUPT SERVICE ROUTINES	
APPENDIX K API CHANNEL ASSIGNMENTS	
APPENDIX L HYBRID INTERFACE LOGIC DRAWINGS	

LIST OF FIGURES

	<u>Page</u>
1. FFTF Hybrid Computer System	2
2. PDP-9 Digital Computer	4
3. Applied Dynamics/Four Analog Computer.	6
4. Data Interface	8
5. A/D Converter Functional Block Diagram	9
6. D/A Converter Functional Block Diagram	12
7. Hybrid Interface Block Diagram	13
8. A/D Conversion Timing.	19
B PDP-9 IOT Instruction Format	B-1

INTRODUCTION

The relative merits of digital and analog computers in the realm of scientific calculation are well known. Digital computers have the ability to perform complex logic operations and precision arithmetic calculations. Speed and the capability to provide a direct analogy to a dynamic situation are attributes of the analog computer. It follows that the advantages of both types of machines are realized in a hybrid computer configuration which enables engineering simulations in real time and even 1000 times faster than real time.

The Pacific Northwest Laboratory (PNL) has been involved in hybrid computing activities since the construction of PNL Hybrid #1 in 1967. Diverse problems were being solved in such areas as N-Reactor Simulation, Fast Flux Test Facility (FFTF) Dynamics and Core Design, and biological simulations. It soon became apparent that the demand for hybrid computer engineering support was exceeding capability. The answer to the expanded requirements pointed to acquisition of a second hybrid system.

This document describes the hybrid computer system which has been developed for use in simulation of the FFTF reactor process and control system. The hybrid computer will also be used to evaluate direct digital control concepts for the FFTF. The discussion which follows will present a general description of the major components in the system and will discuss the operation of the interface which was developed to link these components.

SUMMARY

The Hybrid Computing System consists of an Applied Dynamics/Four analog computer, a Digital Equipment Corporation PDP-9 digital computer, Adage Inc. digital-to-analog and analog-to-digital high-speed conversion equipment, and the interface circuitry required to enact address and control functions.

The Adage conversion linkage provides bidirectional data flow by means of a 24 channel multiplexer, analog-to-digital converter, distributor, and 24 digital-to-analog converters.

Analog addressing, mode selection, potentiometer setting and coefficient reading are performed by the digital computer. Sixteen lines in each direction

Figure 1. FFTF Hybrid Computer System

between the digital computer and digital logic system in the analog computer provide sensing and control of programmed logic operations.

The hybrid system is shown in Figure 1.

SYSTEM DESCRIPTION

DIGITAL COMPUTER

The PDP-9 (see Figure 2) is a general purpose parallel binary computer with 8192 18-bit directly addressable core memory locations and an additional 8192 words of indirectly addressable core memory. Hardware capability includes 60 Hz and 5 kHz real time clocks, extended arithmetic option, 32 channels of automatic priority interrupt, 4 data channels and a direct memory access channel. Machine cycle time is 1 μ sec. Fixed point arithmetic operations execute addition in 2 μ sec, multiplication in 11 μ sec average, and division in 12 μ sec average time.

Input/Output

Data transfer between the PDP-9 and peripheral units is accomplished by means of a bidirectional "party-line" input/output (IO) bus. Standard program-controlled data transfers occur between the peripheral device and accumulator in the digital computer. Control pulses from the digital computer are issued via the memory buffer to a decoding selector in the device. External status inputs to the digital computer flag the Skip, Program Interrupt, Automatic Priority Interrupt, and Data Channel facilities. Data and control transfers to and from the IO bus are enacted by input/output transfer instructions (IOT's). Six bits of the IOT instruction are assigned to device selection, three are used to select three input/output pulses (IOP's), and four may be used to determine sub-device selection. The IOT instruction format is shown in Appendix B.

The data channel facility enables block transfers to and from core memory with high-speed peripheral devices on a cycle-stealing basis. Processor-granted breaks allow data transfers through the memory buffer without modifying any of the other active registers employed by the program in progress.

Figure 2. PDP-9 Digital Computer

Peripheral Devices

A Model KSR 35 teletype unit serves as the principal operator-computer interface device. Circuit modifications permit automatic tabulation and form feed operations. Keyboard and teleprinter flags use the Skip and Program Interrupt facilities.

Two TU55 DECTape transports provide block-format magnetic tape storage. Data may be read or written bidirectionally at a rate of 5000 words per second. A standard format tape stores 576 blocks of 256 words each. The DECTape units communicate with core via the data channel facility.

A 300 character per second photoelectric paper tape reader provides data input in either alphanumeric or binary modes. A paper tape punch outputs at a rate of 50 characters per second. The paper tape system utilizes fan-fold tape.

Additional IO devices interfaced to the digital computer include a line printer and cathode-ray-tube color display. A memory protect option and multi-teletype system will also be installed to permit foreground/background programming. A 500 K word fixed head disc is being interfaced to augment memory capacity.

Modifications

The PDP-9 IO structure has been modified to provide two more levels of sub-device selection in addition to the two sub-device selection bits in the standard configuration. This modification allows more efficient use of device selectors in multi-addressing schemes, such as those used in addressing the several multiplexer and D/A channels in the hybrid data conversion equipment. Compatibility with the methods used in PNL Hybrid 1 is also advantageous from a user viewpoint. The sub-device selection scheme is illustrated in Appendix B.

The PDP-9 IO Section has also been modified to permit a dual real time clock system. The standard 60 Hz clock has been retained and a 5 kHz clock has been added. Selection of the desired clock is accomplished through program control. It should be noted that the original clock instruction, CLON, now selects the 5 kHz clock, not the 60 Hz clock as before.

Figure 3. Applied Dynamics/Four Analog Computer

ANALOG COMPUTER

The Applied Dynamics/Four computer (see Figure 3) is a 100 volt solid-state analog system paralleled with an extensive digital logic system. Components include 220 amplifiers, 48 integrators, 204 servo-set pots, 16 hand-set pots, 16 digital coefficient units and 24 multipliers. Interface data connections are made through 48 analog trunks and 32 logic trunks. A listing of the analog equipment complement is included in Appendix A. Two Brush Mark 200 strip chart recorders provide hard-copy display of computer runs.

DATA INTERFACE

Data interface between the digital and analog computers is provided via a high-speed conversion system manufactured by Adage, Inc. The conversion equipment, shown in Figure 4, includes a multiplexer, analog-to-digital converter, digital-to-analog distributor and converters.

Analog-to-Digital Conversion

Performance specifications for the A/D converter system are listed in Table 1. A block diagram of the A/D subsystem is shown in Figure 5. The A/D converter employs a combination of successive approximation and parallel threshold decoding to perform a 14-bit conversion in 4 microseconds.

TABLE 1. *Multiplexer and Analog-to-Digital Converter
Performance Characteristics*

Number of analog input channels	24, expandable to 64
Full-scale input	± 100 volts
Analog input impedance	1000 ohms/volt
Accuracy	$\pm 0.01\%$ of full scale $\pm \frac{1}{2}$ LSB
Throughput	100 kHz
Digital output	14 bits (including sign) 1's complement binary
Modes	Random Repetitive Sequential Manual
Status output	Overload Busy

Figure 4. Data Interface

FIGURE 5. A/D Converter Functional Block Diagram

An interface was developed to enable output of address, mode, and trigger commands to the A/D subsystem and to provide data input to the digital computer. The A/D subsystem operates in three programmable modes; random, repetitive and sequential. IOT instructions set the appropriate mode selection lines which are sampled when the multiplexer is triggered. Five address control signals are determined by micro-coding in the convert instruction. Status levels are output from the A/D converter to indicate conversion-in-progress (busy) and overload conditions.

Converted data is output to the digital computer in two ways. An IOT instruction can be used to read the A/D output register into the accumulator of the digital computer. Also, data can be input directly into memory by means of a data channel transfer, a method which is extremely useful when operating the multiplexer in repetitive or sequential modes. When using repetitive and sequential modes, another conversion is automatically initiated by hardware when a conversion is completed.

Significant saving of processor time is realized through use of the data channel. In addition to decreasing the elapsed time between a conversion command and read-in of data into the digital computer, use of the data channel permits the elapsed conversion time to be used productively instead of being spent in a flag search.

An IOT instruction must initially be executed to enable the data channel for use with the A/D converter. The use of the data channel also requires that two software counters are initialized to provide memory address and word count information.

An overload detection line is monitored to enable interception of invalid data before it is read into the digital computer. If the A/D overload bit is set, an interrupt occurs on API Channel 0, causing an interrupt service routine to be entered. The overload flag is also tied to the PDP-9 skip facility where it may be sensed by a flag skip instruction. Interface hardware is provided to inhibit the automatic data read-in via the data channel when an overload occurs. A tabulation of the voltage weighting of binary bits for A/D and D/A data is included in Appendix E.

Additionally, manual control may be selected on the front panel of the multiplexer-A/D unit to provide operator control access during maintenance and calibration periods.

Digital-to-Analog Conversion

The operating characteristics of the digital-to-analog (D/A) converter system are shown in Table 2. The system block diagram is shown in Figure 6.

TABLE 2. *Digital-to-Analog Converter Performance Specifications*

Number of analog output channels	24, expandable to 64
Full scale output voltage range	± 100 volts
Full scale output current	± 15 mA
Accuracy	$\pm 0.01\%$ of full scale
Maximum settling time	50 μ sec to reach 0.01 volts of final value for a full scale step
Digital input	14 bits (including sign) 1's complement binary
Buffering	Single buffered
Maximum update rate	500 kHz

The PDP-9 to D/A subsystem interface provides data, address, and convert command information to the D/A distributor. As in the A/D subsystem, addressing is accomplished through micro-coding in the convert instruction. Routing of data and addressing of the various D/A converters is controlled through the distributor in the D/A system.

CONTROL INTERFACE

The hybrid control interface provides the means for routing, gating and level converting all information exchange between the digital and analog computers. Almost all of the functions which are performed at the analog computer console can be executed via control commands from the digital computer. A block diagram of the interface is shown in Figure 7.

FIGURE 6. D/A Converter Functional Block Diagram

FIGURE 7. Hybrid Interface Block Diagram

Interface circuitry is constructed of both discrete component circuit boards manufactured by the Digital Equipment Corporation and PNL developed modules which utilize diode-transistor-logic integrated circuits.

The structure of the analog computer control circuitry allows direct binary inputs for both control and addressing functions. A common IO bus provides all data input to the analog computer. The bus is buffered and gated to provide input to the analog computer address register, mode register, pot coefficient register, digital coefficient register, and control line register.

Analog Addressing

Any component or trunk line at the analog computer can be addressed through the hybrid interface. An address register in the analog computer control logic is loaded with address data contained in the accumulator of the PDP-9 by executing IOT instruction AADR (Analog Address). A table correlating data word and analog address is included in Appendix G. Once an initial address has been established, another instruction, AADI (Analog Address Increment), can be used to increment the analog address.

A status signal is available from the analog computer indicating the validity of a selected address. A level change occurs on this line when the operator requests a nonexisting analog address, but because of relay switching delays in the analog computer, the signal cannot be assumed valid for a period of 300 μ sec after an address change. The valid address flag is interrogated by IOT instruction VASF (Valid Address Skip Flag).

Mode Control

Analog mode and logic mode control of the analog computer are accomplished by loading a control register with a data word from the PDP-9 accumulator via instruction AMOD (Analog Mode). Both the address and mode registers are jam loaded so that prior clearing is not required. Three flags from the analog computer allow sensing of analog modes, IC, HOLD and OPERATE, at the digital computer.

Time scales of X1, X10, X100 and X1000 can be selected by hybrid command. An internal 1 MHz clock or an external clock line may be selected as the timing source for the logic system. Hybrid control of analog and digital logic system modes is provided. Additionally, a LOGIC EXECUTE condition may be selected which gives control of the analog modes to an interval timer in the logic system. This capability is useful in providing cyclic control of the analog computer for iterative operations.

A COEF X in feature can be selected to provide absolute readout of the variable output of a coefficient device in place of the normal readout which is relative to the analog reference supply.

The mode control data bits are defined in Appendix G.

Servo Pot Setting

Setting of the 204 servo potentiometer complement is accomplished rapidly by hybrid command. A coefficient value is first loaded into the AD/4 Servo DAC Register from the PDP-9 accumulator by executing hybrid instruction PCL (Pot Coefficient Load). The bit weights for servo pot and DCU coefficients are shown in Appendices H and I. Instruction SERV causes an addressed potentiometer to servo to the value specified by the data word in the Servo DAC Register. Pot setting requires an average time of about one second. A successful setting is followed by a servo set flag which may be examined by instruction SVSF (Skip on ServoSet Flag). If the pot fails to servo or is not set within 3 seconds, the servo setting circuit is disconnected and a servo reset error flag occurs. This condition may be detected by instruction SRSF (Skip on Servo Reset Flag).

Digital Coefficient Units

The DCU's are operated in much the same manner as servo pots. The instruction DCUL (DCU Load) transfers data from the digital computer accumulator to a digital coefficient register in the analog computer. The next instruction, DCUS (DCU Set), causes the addressed DCU to be set to the voltage value represented by the word in the coefficient register. DCU setting is essentially instantaneous. There are no hardware status flags for the DCU's.

Logic Control and Sense Lines

Sixteen control lines convey control commands to the digital logic panel trunks on the analog computer. These lines may be used arbitrarily to perform programmed steps within a running program by means of the extensive logic system in the analog computer. All 16 control line levels are determined by a single data word which is transmitted to the control line register in the analog computer and subsequently to the digital logic panel. The data bit/control line assignments are listed in Appendix G.

Sixteen sense lines originating at the analog computer digital logic patchboard may be arbitrarily assigned to provide interrupts to the digital computer. All 16 lines are "ored" to cause a program interrupt and 4 lines are wired into the API facility. Upon receipt of an interrupt, the sense line register contents are read into the accumulator of the PDP-9 where software decode determines the interrupting line.

SOFTWARE

Eighty-one instructions have been added to the PDP-9 instruction set to perform hybrid operations. The additional instructions are all IOT executions which require 4 machine cycles. A listing of the hybrid instruction set is included in Appendix C.

ANALOG-TO-DIGITAL CONVERSION

Analog-to-digital conversions may be executed in a step-by-step manner in which data read-in to the digital computer is under program control or in an automatic manner under hardware control in which data is read in through the data channel. Subroutine examples for use of the A/D subsystem are shown in Appendix D.

Random Addressing

Any one of 24 multiplexer channels may be randomly addressed. The instruction MXRN selects multiplexer random mode. Another instruction, MXn, in which n is the channel number (0-23), sets the multiplexer address and starts an A/D conversion. The IOP 2 pulse provides the conversion command while address selection is made by four sub-device selection bits.

Repetitive and Sequential Modes

Repetitive multiplexer mode is selected via instruction MXRP. Sequential mode is set by instruction MXSE. A convert command, ADVT, starts a conversion. In repetitive mode, each execution of the convert instruction causes a conversion on the same channel. In sequential mode, the convert instruction advances the multiplexer address one channel before the conversion is started.

When converting in random mode, or repetitive and sequential modes with the data channel disabled, completion of a conversion is detected by a flag check, ADSF (Skip if A/D conversion is completed). Instruction ADRB (Read A/D buffer) reads the digital representation of the analog voltage into the PDP-9 accumulator.

If the data channel is used for automatic transfer of a block of data conversions into memory, the convert instruction must be preceded by a DCHON instruction which sets a data channel enable flip-flop. In this mode of operation, the user must specify the number of conversions to be made and the initial location in core reserved for input data. These parameters are stored in two memory locations specifically allocated for use with the data channel, a Word Count register (36_g) and a Current Address register (37_g). Following a convert command, the number of conversions specified in two's complement in memory location 36_g will be made and the data will be placed in consecutive memory locations starting at the next address above that which is held in location 37_g. Another conversion is hardware initiated each time the converted data is read into memory until the predetermined number of conversions have been completed, at which time a block transfer done flag will cause a computer interrupt if the program interrupt facility is enabled. Completion of the block of conversions can also be detected by instruction ADSD (Skip if A/D block transfer is completed).

The central processor may perform other tasks while the A/D conversion is in progress. A program break is requested each time a conversion is completed and requires one IOT period to input data into memory and initiate another conversion. Minimum conversion intervals are 16 μ sec, allowing at least 12 μ sec of useful computer time between data breaks. None of the

active registers in use by the program in progress are affected by the data channel break. A timing diagram of the two methods of programming an A/D conversion is shown in Figure 8.

DIGITAL-TO-ANALOG CONVERSION

Digital-to-analog conversions require a data word and one IOT command to address and convert the appropriate D/A channel. A signed one's complement word is placed in the PDP-9 accumulator. Instruction DAn, in which n is the D/A channel number (0-23), addresses the desired D/A channel, gates the digital data through the D/A distributor into the appropriate D/A converter and converts that channel.

ANALOG ADDRESS AND CONTROL

Subroutine examples illustrating the methods used to address, select operating modes, and set coefficient devices on the analog computer are shown in Appendix G. All analog control and coefficient registers are served by a common IO bus. Data are routed selectively by executing appropriate IOT instructions.

INTERRUPTS

Four major levels of interrupts are used in the hybrid configuration and are listed in the order of their priority.

1. Data channel requests
2. Real-time clock counting
3. Automatic priority interrupts (API)
4. Program interrupts (PI)

Data Channel

No service routine is necessary for data channel breaks in a program execution. A data channel request suspends the program in progress and inputs data through the memory buffer without disturbing the accumulator, program counter and other active registers. Thus, there is no requirement to save the contents of these registers as in program interrupts. However, initialization of a word counter (WC) register and a current address (CA) register is

a) Flag Check for Completion

b) Data Channel Input

FIGURE 8. A/D Conversion Timing

required prior to a device request for data transfer. A request for data channel action is granted on completion of the current instruction unless the current instruction is an IOT or XCT instruction. In this case, the instruction sequence cannot be interrupted until the next instruction which is not an IOT or XCT instruction is executed. EAE (Extended Arithmetic Element) instructions are also noninterruptable. The data channel break requires one IOT time interval (4 μ sec).

Real Time Clock

When a clock is enabled, each clock pulse requests a program break which is granted upon completion of the current instruction (subject to the limitations defined in data channel operation). The contents of the clock counter register are incremented once each single cycle break until the register overflows and requests an API break. The clock counter register (7_g) is initialized to the 2's complement of the desired number of clock pulses.

Automatic Priority Interrupt

The API option provides eight levels of interrupt priority. Four levels are assigned to software and the higher four levels are used to service device requests. Each of the four hardware levels can be multiplexed for use by eight devices. Priority within a level is determined by propagation time along the IO bus.

When a device is granted an interrupt, a channel address is transmitted to the central processor and the instruction in the specified address is executed. The instruction must be a JMS to a service subroutine. The service routine must save the contents of the accumulator, clear the interrupting flag, and restore the status of the various registers and mode conditions at the conclusion of the service routine.

An API service subroutine example is shown in Appendix J. Channel assignments are also listed in Appendix K.

Program Interrupt

A program interrupt is granted at completion of the current instruction, subject to the same limitations as other interrupts in regard to IOT and XCT instructions. The status of the link, program counter and extend mode, is

automatically preserved and other active register contents must be saved by the service routine as in the API break. These conditions must also be restored at the conclusion of the service routine. A subroutine illustrating the multiple device PI service program is included in Appendix J.

REFERENCE DOCUMENTS

1. Applied Dynamics/Four Reference Manual. Applied Dynamics, Inc., Ann Arbor, Michigan, 1967.
2. PDP-9 Users Handbook, Digital Equipment Corporation, Maynard, Massachusetts, 1968.
3. PDP-9 Maintenance Manual, Digital Equipment Corporation, Maynard, Massachusetts, 1968.
4. Instruction Manual for VT13AB/VMX55 and YD1358/8Y15-2 Hybrid Linkage System, Adage Publication No. 68-28, Vol. I and II. Adage, Incorporated, Boston, Massachusetts, 1968.
5. Digital Logic Handbook. Digital Equipment Corporation, Maynard, Massachusetts, 1968.

BNWL-1498

APPENDICES

100-1000

100-1000

A-1

APPENDIX A

APPLIED DYNAMICS/FOUR EQUIPMENT COMPLEMENT

<u>Item</u>	<u>Quantity</u>
Total Amplifiers	220
Integrators	48
Summers	60
Inverters (Inv. - Sum)	40
Amp. for Mult./Res.	72
Servo-Set Pots	204
Handset Pots	16
Hard Limiters	12
Dual Res/Relay Ntw.	32
Quarter Sq. Mult	24
Comparators	16
D/A Switches	12
Recorder Tr.	32
A/D Trunks	32
D/A Trunks	24
Analog Trunks	56
Logic Trunks	32
4 Input Gates	16
2 Input Gates	26
G.P. Registers	6
Free Flip Flops	12
Counters, Total	9
2 Decade	3
1 Decade	6
Logic Switches	16
Free Indicators	6
Patching Sets	6
Digital Attenuators	16
Track-Stores	12
Interval Timers	2

B-1

APPENDIX B

INPUT/OUTPUT TRANSFER INSTRUCTION

Input/output transfer (IOT) instructions control peripheral devices via the PDP-9 I/O bus. The modified IOT instruction format is shown below.

FIGURE B. PDP-9 IOT Instruction Format

A six-bit (bits 6-11) device selection code selects one of 64 peripheral devices. Bits 4, 5, 12 and 13 enable sub-device selection for a total of 1024 unique codes. IOP generation is determined by bits 15-17. IOP1 is generally used to check device status by means of the IO skip facility. IOP2 and IOP4 perform device control or strobe data transfers between the device and central processor.

1

2

3

4

5

6

7

8

9

10

APPENDIX C

HYBRID INSTRUCTIONS

Mnemonic	Code	Operation
MXRN	701101	Select mux random mode
MXSE	701102	Select mux sequential mode
MXRP	701104	Select mux repetitive mode
MXØ	701202	Load mux address Ø and convert
MX1	701222	1
MX2	701242	2
MX3	701262	3
MX4	711202	4
MX5	711222	5
MX6	711242	6
MX7	711262	7
MX8	721202	8
MX9	721222	9
MX10	721242	10
MX11	721262	11
MX12	731202	12
MX13	731222	13
MX14	731242	14
MX15	731262	15
MX16	704502	16
MX17	704522	17
MX18	704542	18
MX19	704562	19
MX20	714502	20
MX21	714522	21
MX22	714542	22
MX23	714562	23
@ADOV	701201	Skip if A/D OVL D flag is set
*ADVT	701204	Convert A/D
ADSF	701301	Skip if A/D ready flag is set
ADRB	701312	Read A/D output into AC
*ADCF	704504	Clear A/D flags
+*ADSD	702301	Skip if A/D block transfer done
*DCHON	701344	Enable A/D Data Channel
*DCHOF	701304	Disable A/D Data Channel

C-2

HYBRID INSTRUCTIONS

Mnemonic	Code	Operation
DA0	702002	Select D/A CH0 and convert
DA1	702022	1
DA2	702042	2
DA3	702062	3
DA4	712002	4
DA5	712022	5
DA6	712042	6
DA7	712062	7
DA8	722002	8
DA9	722022	9
DA10	722042	10
DA11	722062	11
DA12	732002	12
DA13	732022	13
DA14	732042	14
DA15	732062	15
DA16	702102	16
DA17	702122	17
DA18	702142	18
DA19	702162	19
DA20	712102	20
DA21	712122	21
DA22	712142	22
DA23	712162	23

HYBRID INSTRUCTIONS

Mnemonic	Code	Operation
*AADR	701401	Load analog address from AC
*AMOD	701402	Load analog mode from AC
*AADI	701404	Increment analog address
SVSF	701501	Skip if servo set flag is set
*PCL	701502	Load pot coef from AC
SERV	701504	Operate pot servo
*SRSF	701601	Skip if servo reset flag not set
*DCUL	701602	Load DCU coef from AC
*DCUS	701604	Set DCU
*HYSF	702001	Skip if hybrid on flag is set
x*VASF	702101	Skip if analog valid address flag is set
*ASCF	702104	Clear analog status flags
+*AOSF	704501	Skip if analog OVLD flag not set
@+*SLSF	702201	Skip if sense line flag not set
*SLRB	702212	Read sense line register into AC
*SLCL	702204	Clear sense line register and flag
*CLRL	702306	Load control line register from AC
*ICSF	702521	Skip if IC mode is set
*HDSF	702541	Skip if HOLD mode is set
*OPSF	712501	Skip if OPERATE mode is set
*CLON	700044	Enable 5 kHz clock
*CLKB	700064	Enable 60 Hz clock

NOTE: * instructions differ from PNL Hybrid 1
 + flag also on priority interrupt
 x flag not valid for 300 μ sec after changing an analog address
 @ also on API

The following flags are also cleared by PWR CLR:

A/D RDY

A/D OVLD

ANALOG OVLD

SENSE LINE

SERVO RESET

1

2

3

4

5

6

7

8

9

10

D-1

APPENDIX D

DATA CONVERSION ROUTINES

The first group of subroutines indicate execution without the use of the data channel.

SUBROUTINE TO RANDOMLY ADDRESS AND CONVERT

MXRN /Select random mode
 MXn /Address and convert mux channel n
 ADSF /Skip if A/D ready flag is set
 JMP .-1
 ADRB /Read A/D buffer into AC

SUBROUTINE TO SEQUENTIALLY ADDRESS AND CONVERT

MXRN /Select random mode
 MXn /Address mux channel n;
 n = Channel number preceding desired starting location.
 (23 precedes 0)
 ADSF /Skip if A/D ready flag is set
 JMP .-1
 MXSE /Select sequential mode

The following commands will convert the next channel in sequence (0 follows 23).

ADVT /Convert
 ADSF /Skip if A/D ready flag is set
 JMP .-1
 ADRB /Read A/D buffer into AC

D-2

SUBROUTINE TO REPETITIVELY ADDRESS AND CONVERT

MXRN /Select random mode
 MXn /Address mux channel n
 ADSF /Skip if A/D flag is set
 JMP .-1
 MXRP /Select repetitive mode

The following commands will convert channel n repetitively each time they are executed.

ADVT /Convert
 ADSF /Skip if A/D flag is set
 JMP .-1
 ADRB /Read A/D buffer into AC

The following subroutines employ the data channel for automatic data read in.

SUBROUTINE TO SEQUENTIALLY ADDRESS AND CONVERT

MXRN /Select random mode
 MXn /Address mux channel n; n = channel number preceding desired starting location.
 ADSF /Skip if A/D ready flag is set
 JMP .-1

The following commands will cause a block of conversions to be made.

LAC WC /2's complement of no. of conversions to be made
 DAC 36 /Word count register for data channel
 LAC CA /Starting (current) memory address -1
 DAC 37 /Current address register for data channel
 MXSE /Select sequential mode
 DCHON /Enable A/D data channel
 ADVT /Convert

E-1

APPENDIX E

A/D AND D/A BINARY TO VOLTAGE CONVERSION

Data word is 13 Bits plus Sign, 1's Complement Binary

<u>DATA BIT</u>	<u>VOLTAGE</u>
0	Sign (1 = Minus)
1	} Not Used
2	
3	
4	
5	50.0 Volts
6	25.0
7	12.5
8	6.25
9	3.125
10	1.5625
11	0.7812
12	0.3906
13	0.1953
14	0.0976
15	0.0488
16	0.0244
17	0.0122

1

2

3

4

5

6

7

8

9

10

APPENDIX F

DATA TRUNK LINE ASSIGNMENTS

<u>TRUNK</u>	<u>FUNCTION</u>
110	ADCØ
111	1
112	2
113	3
114	4
115	5
116	6
117	7
150	ADC8
151	9
152	10
153	11
154	12
155	13
156	14
157	15
310	ADC16
311	17
312	18
313	19
314	20
315	21
316	22
317	23
130	DACØ
131	1
132	2
133	3
134	4
135	5
136	6
137	7
170	DAC8
171	9
172	10
173	11
174	12
175	13
176	14
177	15
330	DAC16
331	17
332	18
333	19
334	20
335	21
336	22
337	23

APPENDIX G

HYBRID CONTROL ROUTINESAnalog Addressing

The hybrid instruction AADR loads an address register in the AD-4 with the contents of bits 6-17 of the Accumulator as follows:

<u>AC Bits</u>	<u>Function</u>
6, 7, 8	Determines class of analog component to be addressed 000 +Amplifier 001 -Amplifier 010 Dig. Coef 011 Pot Coef 100 S.J. 101 DFG S.J. 110 TR A-D
9, 10, 11	Defines field address of addressed component (octal) Field 0, 1, 2, 3
12, 13, 14	Defines area address of addressed component (octal) Area 0-7
15, 16, 17	Defines a component within an area (octal) Number 0-7

EXAMPLE: Address servo pot 201

LAC (3201

AA DR

.
.
.

Mode

Mode control data is set into a register in the AD-4 by hybrid instruction AMOD. The AC bits and corresponding functions are as follows:

<u>AC Bits</u>	<u>Function</u>
7	Coef x in
8, 9	Clock Control
	00 10 ⁶
	01 Digital Input
	10 Ext. Input
10, 11	Time Scale
	00 x1
	01 x10
	10 x100
	11 x1000
12	Logic Exec
13, 14	Logic Mode
	00 Load
	01 Stop
	10 Run
	11 Stop
15	Problem Verify
16, 17	Analog Mode
	00 IC
	01 Hold
	10 Operate
	11 Hold

EXAMPLE: Set OPERATE mode and X100 time scale

LAC (202

AMOD

.
.
.

G-3

Servo Pot Setting

Pot setting is accomplished by first loading the AD-4 Servo DAC Register with data contained in the AC by means of hybrid instruction PCL. Instruction SERV causes the addressed pot to servo to the voltage value specified by the data word in the Servo DAC Register. A successful pot set is followed by a servo set flag which may be interrogated by SVSF (skip if servo set flag is set). If a pot fails to set, a servo reset flag occurs. This condition may be checked by SRSF (skip if servo reset flag not set) or more conveniently, by use of the priority interrupt system. The reset flag will not be valid until 2.5-3 sec. after the servo command.

EXAMPLE: Set servo pot 202

HYSF	/HYBRID MODE ON?
JMP .-1	
CIA	
AMOD	/SELECT IC MODE
LAC (3202	
AADR	/SET POT ADDRESS
JMS DLY	/WAIT 5 MS FOR ADDR SELECTOR
LAC COEF	
PCL	/LOAD POT COEF
SERV	/SET POT
SVSF	/SERVO THROUGH?
JMP .-1	
SRSF	/YES, POT SET CORRECTLY?
JMP RESET	/NO, INDICATE POT NOT SET

.

.

.

G-4

Digital Coefficient Units

DCU's are set in a manner similar to the servo pots. A DCUL command transfers data from the AC to a digital coefficient register in the AD-4. DCUS causes the addressed DCU to be set to the value of the data word in the coefficient register. There are no hardware tests for the status of digital coefficient units.

EXAMPLE: SET DCU 303

INITIALIZE HYBRID MODE, ETC.

.
.
.

LAC (2303

AADR /SET DCU ADDRESS

JMS DLY /WAIT FOR ADDR SELECTOR

LAC COEF

DCUL /LOAD DCU BUFFER

DCUS /SET DCU

.
.
.

H-1

APPENDIX H
SERVO POT COEFFICIENT TABLE

Pot coefficient values are represented in 8421 BCD

<u>AC Bit</u>	<u>Coefficient Values</u>
2	.8000
3	.4000
4	.2000
5	.1000
6	.0800
7	.0400
8	.0200
9	.0100
10	.0080
11	.0040
12	.0020
13	.0010
14	.0008
15	.0004
16	.0002
17	.0001

I-1

APPENDIX I
DCU COEFFICIENT TABLE

DCU Coefficients are represented in binary.

<u>AC Bit</u>	<u>Coefficient Value</u>
4	.8192
5	.4096
6	.2048
7	.1024
8	.0512
9	.0256
10	.0128
11	.0064
12	.0032
13	.0016
14	.0008
15	.0004
16	.0002
17	.0001

J-1

APPENDIX J

INTERRUPT SERVICE ROUTINES*API SERVICE SUBROUTINE*

The following routine illustrates the use of the API to service an A/D overload interrupt.

```

57      JMS SERV
SERV    0          /ENTRY POINT
        DAC AC     ./SAVE AC
        .
        .
        .
        ADCF       /CLEAR A/D FLAG
        LAC AC     /RESTORE AC
        DBR        /DEBREAK AND RESTORE
        JMP* SERV

```

PI MULTIPLE FLAG SERVICE SUBROUTINE

This example illustrates service of a Program Interrupt. Note that in addition to the flag tests shown here, all active device flags tied to the PI facility must be examined

.
.
.

INTERRUPT OCCURS

```

0          /STORE PC, LINK, ETC.
1      EEM          /ENTER EXTEND MODE
2      JMP* 3
3      FLG CK

```

J-2

FLG CK	DAC AC	/SAVE AC
	AOSF	/SKIP IF OVLD FLAG NOT SET
	JMP OVLD	/ENTER OVLD ROUTINE
	SLSF	/SKIP IF SENSE LINE FLAG NOT SET
	JMP SL	/ENTER SENSE LINE ROUTINE
	ADSD	/SKIP IF A/D BLOCK XFER DONE
	JMP OUT	
	JMP AD	/ENTER A/D ROUTINE
OUT	LAC AC	/RESTORE AC
	ION	/ENABLE PI
	DBR	/DEBREAK AND RESTORE
	JMP* O	/RETURN TO MAIN PROGRAM

K-1

APPENDIX K

API CHANNEL ASSIGNMENTS

<u>DEVICE</u>	<u>LEVEL</u>	<u>TRAP ADDRESS</u>
DEC tape	1	44
Paper Tape Reader	2	50
Clock Overflow	3	51
A/D Overload	0	57
Hybrid Sense Lines	3	62
Line Printer	3	56
Display Data	3	65
Light Pen	3	66

APPENDIX L

HYBRID INTERFACE LOGIC DRAWINGS

- 1 Block Diagram
- 2 Module Locator 1
- 3 Module Locator 2
- 4 IO Bus Buffer
- 5 Device Selectors
- 6 IO Data Buffer
- 7 A/D Multiplexer Control
- 8 A/D Data
- 9 D/A Data & Control
- 10 Analog Control Outputs
- 11 Analog Flags
- 12 Analog Flags - Data Channel
- 13 Sense Line Inputs
- 14 Module Locations Analog Control
- 15 Analog Data & Control
- 16 DCU Data Register
- 17 DCU Data Gates
- 18 Sense Line Outputs
- 19 Special Circuits

A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
																	R111	W510	R202	R111	R111	R111	R203	W510	W510	R107					

B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
				R202	R202	R202	R202	R202	R202	R202	R202	R202	R302	R107	R302	W601	W640	W640	W640	R123	R123	R123	CABLE	W510	W510	W510	W510	W510	W510	CABLE	CABLE

C

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
		W104	W104	W104			R602	R107	R107	R107	+5V SUPPLY	R111	W601	W601	W601	W601	W601	W601	W601	W601	R302	CABLE	CABLE	CABLE	CABLE	CABLE	CABLE				

BATTELLE NORTHWEST	
BATTELLE MEMORIAL INSTITUTE PACIFIC NORTHWEST LABORATORY	
P. O. BOX 999, RICHLAND, WASHINGTON 99352 / TELEPHONE 509-942-1111	
ENGINEER	DATE
KM BUSINESS	8/4/70
TITLE	
MODULE LOCATOR (1 OF 2)	
FFTF HYBRID	
2	

D

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
							R141	R123	R111	R107	R202	R203	R111	R111	R123	R123	R302	R111	R107	W640	W640	R111	R107	R107	R107	R107	R107	R203	R107	CABLE	CABLE	CABLE

E

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
IO BUS IN					IO BUS OUT					W500	W500	W500	W640	W103	W103	W103	W103	W103	W103	W103	W103	W103	W103	W103							

F

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
IO BUS IN				IO BUS OUT						R107	R107																				

BATTELLE NORTHWEST	
BATTELLE MEMORIAL INSTITUTE PACIFIC NORTHWEST LABORATORY	
P. O. BOX 999, RICHLAND, WASHINGTON 99352 / TELEPHONE 509-942-1111	
ENGINEER	DATE
KM BUSINESS	8/4/70
TITLE	
MODULE LOCATOR (2 OF 2)	
FFTF HYBRID	
3

BATTELLE-NORTHWEST	
BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY RICHLAND, WASHINGTON 99352	
ENGINEER <i>K M BUSINESS</i>	DATE <i>8/4/70</i>
TITLE <i>IO BUS BUFFER</i>	
<i>FFTF HYBRID</i>	
4

THESE PINS CONNECTED ON ALL MODULES
 EN—EJ
 EN—EP
 EV—EV

BATTELLE-NORTHWEST	
BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY RICHLAND, WASHINGTON 99352	
ENGINEER <i>K BUSNESS</i>	DATE <i>8/4/70</i>
TITLE <i>DEVICE SELECTORS</i>	
<i>FFTF HYBRID</i>

BATTELLE NORTHWEST BATTELLE MEMORIAL INSTITUTE PACIFIC NORTHWEST LABORATORY P. O. BOX 999, RICHLAND, WASHINGTON 99352 / TELEPHONE 509-942-1111	
ENGINEER <i>K. BUSINESS</i>	DATE <i>8/4/70</i>
TITLE <i>IO DATA BUFFER</i>	
<i>FFTF HYBRID</i>

BATTELLE-NORTHWEST

BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY
RICHLAND, WASHINGTON 99352

ENGINEER K BUSNESS

DATE 8/4/70

TITLE D/A DATA & CONTROL

FETE HYBRID

9

BATTELLE-NORTHWEST	
BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY RICHLAND, WASHINGTON 99352	
ENGINEER K. BUSINESS	DATE 8/4/70
TITLE ANALOG FLAGS	
FFTF HYBRID

BATTELLE-NORTHWEST

 BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY
 RICHLAND, WASHINGTON 99352

 ENGINEER *K M BUSINESS*

 DATE *8/4/70*

 TITLE *ANALOG FLAHS*
DATA CHANNEL
FFTF HYBRID

12

BATTELLE-NORTHWEST	
BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY RICHLAND, WASHINGTON 99352	
ENGINEER <i>K BUSINESS</i>	DATE <i>8/4/70</i>
TITLE <i>SENSE LINE INPUTS</i>	
<i>FFTE HYBRID</i>	

					PGA400A PWR GATES	CON001A CABLE CONN	GAT200A 2-INPUT GATES	FFL001A FLIP-FLOPS	FFL001A FLIP-FLOPS	GAT200A 2-INPUT GATES	CON001A CABLE CONN	PGA400A PWR GATES	PGA400A PWR GATES	PGA400A PWR GATES	CON001A CABLE CONN	GAT200A 2-INPUT GATES	CON001A CABLE CONN	CON001A CABLE CONN	GAT200A 2-INPUT GATES	FFL001A FLIP-FLOPS	FFL001A FLIP-FLOPS	PGA400A PWR GATES	PGA400A PWR GATES			
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27

WIRING PLANE VIEW

ELCO VARIPAK CARD ENCLOSURE
WIRING 2VH36/1JND3 72 PIN WIRE-WRAP
CONNECTORS
ANALOG CONTROL RACK POSITION 08

Battelle-Northwest Battelle Memorial Institute / Pacific Northwest Laboratory Richland, Washington 99352	
ENGINEER <i>K. BUSINESS</i>	DATE <i>8/4/70</i>
TITLE <i>MODULE LOCATIONS - ANALOG CONTROL</i>	
<i>FFTF HYBRID</i> 14

BATTELLE-NORTHWEST

BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY
RICHLAND, WASHINGTON 99352

ENGINEER **KM BUSINESS**

DATE **8/4/70**

TITLE **ANALOG DATA & CONTROL**

FFTF HYBRID

15

BATTELLE-NORTHWEST	
BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY RICHLAND, WASHINGTON 99352	
ENGINEER KM BUSINESS	DATE 8/4/70
TITLE DCU DATA REGISTER	
FFTF HYBRID

BATTELLE-NORTHWEST	
BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY RICHLAND, WASHINGTON 99352	
ENGINEER <i>KM BUSINESS</i>	DATE <i>8/4/70</i>
TITLE <i>DCU DATA GATES</i>	
<i>FFTF HYBRID</i>

BATTELLE-NORTHWEST	
BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY RICHLAND, WASHINGTON 99352	
ENGINEER <i>KM BUSINESS</i>	DATE <i>8/4/70</i>
TITLE <i>SENSE LINE OUTPUTS</i>	
<i>FFFE HYBRID</i>

CARD IS LOCATED IN PDP-9 BAY 4 C12

+5V. CLAMP FOR W601 LEVEL CONVERTERS

PIN 21 = +6V.
 PINS A, B, C, D, 1, 2, 3, 4 = +5V.
 PINS 8, 15, 22 = GROUND
 CARD IS LOCATED IN AD-4 CONTROL
 RACK POS. 07-20.

LAMP DRIVERS & +5V. SUPPLY

BATTELLE-NORTHWEST	
BATTELLE MEMORIAL INSTITUTE / PACIFIC NORTHWEST LABORATORY RICHLAND, WASHINGTON 99352	
ENGINEER K BUSNESS	DATE 8/4/70
TITLE SPECIAL CIRCUITS	
FFTF HYBRID	

Distr-1

DISTRIBUTIONOFFSITENo. of
Copies

29	<u>AEC Division of Reactor Development and Technology</u> Director, RDT Asst Dir for Nuclear Safety Analysis & Evaluation Br, RDT:NS Environmental & Sanitary Engrg Br, RDT:NS Research & Development Br, RDT:NS Asst Dir for Plant Engrg, RDT Facilities Br, RDT:PE Components Br, RDT:PE Instrumentation & Control Br, RDT:PE Liquid Metal Systems Br, RDT:PE Asst Dir for Program Analysis, RDT Asst Dir for Project Mgmt, RDT Liquid Metals Projects Br, RDT:PM FFTF Project Manager, RDT:RE Asst Dir for Reactor Engrg, RDT Control Mechanisms Br, RDT:RE Core Design Br, RDT:RE (2) Fuel Engrg Br, RDT:RE Fuel Handling Br, RDT:RE Reactor Vessels Br, RDT:RE Asst Dir for Reactor Tech, RDT Coolant Chemistry Br, RDT:RT Fuel Recycle Br, RDT:RT Fuels & Materials, Br, RDT:RT Reactor Physics Br, RDT:RE Special Technology Br, RDT:RT Asst Dir for Engrg Standards, RDT EBR-II Project Manager, RDT:PM
1	<u>AEC, Chicago Patent Group</u> G. H. Lee
1	<u>AEC, DTIE</u> For UC-32 Distribution

OFFSITE (continued)No. of
Copies

1	<u>United Nuclear Corporation</u> Research and Engrg Center R. F. DeAngelis
1	<u>Bechtel Corporation</u> J. J. Teachnor
1	<u>Westinghouse Electric Corporation</u> Atomic Power Division Advanced Reactor Systems D. C. Spencer
4	<u>AEC Site Representatives</u> Argonne National Laboratory Atomics International General Electric Company Westinghouse Electric Corp
3	<u>Argonne National Laboratory</u> R. A. Jaross LMFBR Program Office N. J. Swanson
1	<u>Atomics International</u> FFTF Program Office
1	<u>Liquid Metal Engineering Center</u> A. E. Miller
2	<u>Babcock & Wilcox Company</u> Atomic Energy Division S. H. Esleeck G. B. Garton
5	<u>General Electric Company</u> Advanced Projects Operation Kark Cohen (3) Nuclear Systems Programs D. H. Ahmann (2)
2	<u>Gulf General Atomic Inc.</u> General Atomic Division D. Coburn

ONSITE - HANFORDNo. of
Copies

1	<u>AEC, Chicago Patent Group</u> R. K. Sharp	
4	<u>AEC, RL</u> D. W. Gossard H. K. Mitchell C. L. Robinson J. M. Shivley	
2	<u>RDT Assistant Director for Pacific Northwest Programs</u>	
2	<u>Battelle Memorial Institute</u>	
35	<u>Battelle-Northwest</u>	31 - <u>WADCO</u>
	R. L. Armstrong	R. J. Ausere
	E. R. Astley	B. E. Dozer
	K. M. Busness (6)	R. A. Harvey (10)
	C. R. Cole	J. A. Hubbard
	M. R. Compton	S. A. Hunt
	V. L. Crow	W. F. Lenzke (2)
	J. L. Deichman	J. D. Lodge
	P. J. Dionne (2)	W. R. Markillie
	G. E. Driver	J. W. Mitchell
	M. D. Erickson (6)	W. H. Payzant
	L. H. Gerhardstein	C. D. Swanson
	R. E. Mahan	G. G. Thieme
	G. W. Main	L. D. Van Hess
	D. L. Rohde	G. L. Waldkoetter
	T. A. Seim	H. L. Walker
	N. B. Smith	G. A. Worth
	G. R. Taylor	FFTF File (703) (5)
	Technical Information (5)	
	Technical Publications (2)	