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DATA DISC CONTROL
GRAPHICS 8*

by

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INTRODUCTION

Because of the effort to maintain the maximum data transfer-rate of the Data Disc, some problems were encountered in the design of this control. After some amount of adjustments and redesign, the control has an acceptable operation level. The hardware described in this file number will be used for the initial prototype of our multi-console graphics configuration. CRT frames will be made on the PDP/8 and stored on the Disc for use as refresh for one or more graphic consoles.

The Data Disc referred to in this file number is manufactured by DATA DISC, Inc. of California. The particular disk is the FPD (Fixedhead Parallel Disk) number 32+32 no. 5042. It has 64 heads and 64 matching tracks.

DISK--GENERAL DISCUSSION

The data disk memory has been organized to transfer information in and out of the PDP/8 core memory as near the core memory speed as possible.

The disk data clock is a 3 MHz clock track used to strobe data onto the disk at a 3 MHz rate. In the disk, PDP/8, configuration the PDP/8 12 bit word is transferred by the data break facility of the PDP/8 into a 12 bit buffer. The buffer is jammed into two six bit shift registers which feed 2 tracks on the disk. There are 64 available tracks on the disk, so this allows 32 groups of two tracks available for selection. The selected group of tracks is fed from the shift registers on a WRITE sequence, and fed to the same shift registers on a READ sequence.

The disk tracks are broken into 12 sectors, with a sector gap between sectors. The gap is approximately 44 usec. and the sectors are approximately 3 msec. The sector track was derived from the disk data track clock, by syncing on the origin pulse of the track and counting 128 pulses for a sector gap, and then 8192 pulses for a sector and repeating this 12 times. This allows about 1260_{10} PDP/8 words to be stored per sector.

The PDP/8 will remain in the data break mode for as long as the device break request line is held up. The break request for the disk is held for a sector time and then released. Thus, a 1260 word transfer is accomplished when the disk is activated.

Since the disk was capable of handling data shifted at a 3 MHz rate, the decision was made to utilize the speed as much as possible. The

method of moving data closest to the PDP/8 memory cycle time was the six bit data shift which yields a six bit shift time of 1.9 usec. (Disk clock pulses occur at 333 nsec. intervals.) The PDP/8 cycle time is 1.5 usec. The PDP/8 memory will yield to a data break at the end of the current instruction. If the machine happens to be in a 3 cycle instruction the delay for a data break would be as long as 4.5 usec. Hence, the decision to stay in a data break mode for the sector time on disk transfer.

The data break mode operates at normal PDP/8 machine cycle timing (1.5 usec.), and the machine clock is a free running clock. The PDP/8 requires two clock pulses to do a full memory cycle. A small piece of logic was put into the PDP/8 to block the PDP/8 clock at the end of the first break cycle on a disk transfer and substitute a clock derived from the disk shift clock for the remainder of the disk transfer. This syncs the PDP/8 memory with the disk during the transfer. The disk clock for the PDP/8 furnishes two pulses, one every .99 usec. for a cycle time of 1.99 usec. for the PDP/8 memory. The 1260 word transfer then takes place in less than 3 milliseconds. (2520 usec. + 44 usec. for the sector gap.)

The disk is a sector and track oriented device and both sector and track information must be transferred to the disk logic to accomplish a transfer. In addition certain bits have been delegated to denote the direction of transfer, and to specify into which memory bank the transfer is to be addressed.

The disk addresses the PDP/8 memory as one large memory, without any regard for the page addressing system. For either reading

or writing the facility exists to gate 15 bits to the disk address register so that 16K of PDP/8 memory may be directly addressed.

The disk instructions are as follows:

IOT 6551 GATE THE 12 BITS OF THE ACCUMULATOR INTO THE DISK ADDRESS REGISTER.

IOT 6562 GATE THE 12 BITS OF THE ACCUMULATOR INTO THE DISK CONTROL LOGIC. THESE 12 BITS CONTAIN SECTOR ADDRESS, TRACK ADDRESS, TRANSFER DIRECTION, AND THE HIGH ORDER 2 BITS OF THE ADDRESS TO SPECIFY THE MEMORY BANK.

IOT 6552 CLEAR THE DISK DONE FLAG AND THE INTERRUPT FLAG.

IOT 6561 SKIP ON DISK DONE

IOT 6554 ENABLE THE DISK INTERRUPT

Sector	Track	T.	Ext. Mem.
Address	Address	Dir.	Field

0	1	2	3	4	5	6	7	8	9	10	11
---	---	---	---	---	---	---	---	---	---	----	----

CONTROL WORD

BLOCK LOGIC DISCUSSION

The following discussion is centered on the disk block logic drawing, (no: 1A). This discussion will concern itself primarily with the lines connecting the various blocks. Each block on the block logic has a name and a number inside the block. These names and numbers associate with the individual logic drawings of the disk.

The block logic is divided into three (3) separate sections. The section labeled "PDP/8" is located in the PDP/8 main cabinet and is composed entirely of DEC logic boards.

The section labeled "interface" is an area dealing with level conversion, driving of lines and miscellaneous I/O type operations. Logic in this area is of the hybrid variety and contains both IC's and DEC logic elements.

The area called "disk logic" deals only with the disk and is entirely composed of IC's. The logic of the disk proper is compatible with IC levels.

INTERFACE AREA

Level Converters and Drivers (8-16)(8-18)(8-20)

The level converters and drivers on this logic are for the purpose of converting signals from the PDP/8 into levels suitable for IC's.

When the levels are converted, they are put through an inverting driver and then through another driver. This gives both polarities of the signal at this area. Both drivers are capable of driving 32 TTL IC loads.

Level Converters (10-a)

These level converters convert from the IC logic level to levels compatible with the DEC logic.

IOT, SKIP, and Interrupt Logic (10-b)

The IOT logic is where the IOT instructions from the PDP/8 are decoded. The inputs are BMB bits 3 through 8 and the three machine timing pulses, IOP 1, 2, 4. Each decoder decodes three instructions according to the IOP pulse available. Both polarities of the instruction pulse are available at the output of the W103 board. These instructions are used for control and gating of the device from the PDP/8.

The interrupt bus to the PDP/8 is entered here. An interrupt may be generated by the disk to the PDP/8 when the disk done flag is set. An interrupt may be sent only when an instruction has been given to enable the interrupt.

The skip bus is also entered here. If the disk done flag is up and an IOT (6561) is done, (SKIP ON DISK DONE), a skip is accomplished.

The signal BK REQ = ($\emptyset$) is used to set the disk done flag. This indicates that all information in the sector has been transferred.

PDP/8 AREA

The PDP/8 area is composed of two logic areas. The DMO 1 multiplexer is a standard DEC option for the PDP/8 and allows 7 channel multiplexing of control, address, and data signals.

The Disk Clock Control Logic is the area in which the clock switch takes place. When the disk break request is up, at "mem. done" time, a flip-flop is switched. The flip-flop gates out the PDP/8 clock and gates the clock pulses from the disk in for use as the PDP/8 main clock. When the signal BK REQ goes down, the clock is switched back to the PDP/8 clock. The clock select mechanism is biased with power clear to always start out in the normal clock state.

DISK LOGIC

Address Register (2-11)

The address register is a 12 bit register to accept 12 bits from the PDP/8 accumulator. The accumulator bits are gated in by an IOT instruction 6551. The contents of this register is used to specify the location in core memory of the PDP/8 to which, or from which, information is to be sent, or received, on a data break.

There are two additional bits attached to the top of the address register. These bits are used to specify the extended memory bank to be used, if any. The inputs are accumulator bits 10 and 11 and the gate is the IOT (6562).

The register is primarily an up count register and is bumped by one each time a break cycle occurs. The signal address accepted from the PDP/8 bumps the register.

The up count facility extends also to the two extended memory bits. This has the effect of allowing the disk to directly address all 16K of the PDP/8 core memory with no wrap around on bank boundaries.

Disk Control (2-10)

This control contains primarily the coincidence logic, the track selection logic, and the Data Break Control logic.

Coincidence Logic

The coincidence logic is a method of finding the sector one wishes to transfer from or to. Bits 0, 1, 2, 3 are transferred from the

PDP/8 accumulator to a register. (IOT (6562)). A four bit counter is continually running and counting the sector gap pulses from the disk clock track. The counter is reset each time by the disk track origin pulse. The counter counts from 0-11 and is matched with the 4 bit sector address sent over from the PDP/8. When they agree, the coincidence line is raised indicating the sector address has been found.

Track Selection Logic

The track selection logic is a five bit register. The inputs are AC bits 4, 5, 6, 7, 8. The bits are gated in by the IOT (6562). The outputs are called GD 0 through 4. These outputs are sent to the track selection logic to select track groups 0-31.

Data Break Control Logic

The BREAK request control is composed primarily of two flip-flops. One is called break enable, and the other break request. The break enable flop is set by the IOT (6562) at the same time the sector and track selection information is set in. The break enable signifies a transfer is to be made and conditions the break request flop so it can be set when coincidence is attained. Coincidence is set on the leading edge of the sector gap signal so plenty of time can be allowed for track selection and miscellaneous functions. A one shot is used to guarantee break request is not set if coincidence is sensed too far into the sector gap to allow proper set up time.

When break request to the PDP/8 is raised, the break enable flop is cleared and no more breaks can be generated by coincidence until the IOT (6562) is given again.

Transfer Direction

The transfer direction flop is set by the IOT (6562) and AC bit 9. This determines if the transfer is to or from the PDP/8 memory.

Disk Control (2-9)

This control area contains the bulk of the timing and control logic for the disk.

Sector Track Clock

The sector track clock is brought into this logic and shaped and distributed here. The sector gaps are detected here and the bit clock data screened out. The nice clean sector gap signals are used for counting and timing operations.

The bit clock track read and write delays are used for lining up the clock tracks starting pulses with the read and write data.

PDP/8 Timing Clock

The PDP/8 timing clock is generated here and transferred to the PDP/8. The signal out is called CNT6 V CNT3. The clock is generated by counting a 3 bit counter with the digit timing pulses from the disk clock track. Three, three input nand gates are used to detect 3 times called, CNT3, CNT5, and CNT6. The time CNT6 is used to clear the counter for a new count. CNT3 and CNT6 are used to form the signal CNT3 V CNT6. CNT5 is used to transfer the data from the PDP/8 memory buffer to the disk buffer register. This data must be settled for gating to the shift register at the CNT6 time.

One Shot and Shaper (2-6)

The one shot logic is a hybrid board containing four variable length one shot and a shaper circuit. The shaper is used for sector gap detection. The one shot triggers on a positive going level change and the output is not inverted. The output pulse width is variable with the trimpot and ranging is accomplished with the capacitor size.

Delay (2-7)

The delay element is a fixed length delay line which is driven and restored. The delay length can be changed by changing the size of the delay line.

R/W Buffer (2-8)

The read/write buffer is composed of a 12 bit buffer and two (2) six bit shift registers. There are jam transfer gates to the shift registers from the buffer for the write case, and jam transfer gates from the shift register to the buffer for the read case. The buffer is also jam set during the write case with the information from the PDP/8 memory buffer (MBB BITS).

Write Case

During the write, the MBB bits from the PDP/8 memory are jammed into the buffer by the signal, gate buffers. A short time later the signals Buffer 1 and Buffer 2, jam the buffer contents into the shift register. The signal called R/W clock shifts the data out of the shift registers to the disk write selection logic. The data is

called $\overline{DW1}$ and $\overline{DW2}$. (DATA WRITE). When six shifts occur the process is repeated until the sector ends.

Read Case

During the read case the read data from the DR-A and DR-B (DATA READ) is shifted into the shift register by the R/W clock. After six shifts the signal, Read Transfer Enable, jams the information from the shift registers into the buffer register. The buffer register outputs, (DB BITS) are presented to the multiplexor inputs for the entry to the PDP/8 memory.

Group Selection (1-10) and (1-11)

The group selection logic utilizes the GD SIGNALS from the DISK CONTROL LOGIC. The GD bits 1, 2, 3, 4 are decoded to form 16 outputs. GD bits 0, 1 are used in conjunction with the 16 outputs as a second level decode. This enables a selection of 32 lines. Each line enables two track drivers (a track group). The ultimate selection then is 32 groups of 2 tracks per group.

Write Enable (1-6)(1-7)(1-14)(1-15)

The write enable logic is for the express purpose of raising the individual write enable lines of each track. The group enable lines from the group selection logic each drive two (2) write enable drivers. The write enable logic enables the selected pair of lines when the Select Write Enable line is raised.

Write Data (1-8)(1-9)(1-12)(1-13)

The write data logic is for the driving of data to selected track pairs. The DW1 and DW2 (DATA WRITE) lines from the shift register is one entry on each write gate. The GE (group enable) lines again select a pair of tracks. When the data write information is present on the DW lines it is gated to the pair of tracks selected.

Read Data (2-4)(2-5)(2-16)(2-17)

The read data logic is used to gate the DR (DATA READ) signals into the shift register inputs.

Each individual track is brought into a gate and combined with the desired group enable signal. Each group of 16 read lines is gated down to one output signal, DR. In all, four DR signals are generated--two for the lower 16 pairs of tracks and two for the upper 16 pairs. The final output of all read lines is combined to generate the signals called DR-A and DR-B.

DEC TO IC'S.

LEVEL CONVERTERS & DRIVER LOGIC

W-512

(MULTI)

10-A

DISC-IOT, SKIP + INTERRUPT LOGIC

DISC-CLOCK CONTROL LOGIC

PF

DISC-READ

2-4

2-5

2-7

+5V

DB0
(10B-3-H)

MBB0(1)
(8-20-B)

DB1
(10B-3-K)

MBB1(1)
(8-20-D)

DB2
(10B-3-M)

MBB2(1)
(8-20-F)

DB3
(10B-3-P)

MBB3(1)
(8-20-J)

DB4
(10B-3-S)

MBB4(1)
(8-20-L)

DB5
(10B-3-U)

(8-20-N) MBB5(1)
BUFFER 1
(2-9-11)

DB6
(10B-4-E)

MBB6(1)
(8-20-R)

DB7
(10B-4-H)

MBB7(1)
(8-20-T)

DB8
(10B-4-K)

MBB8(1)
(8-20-V)

DB9
(10B-4-M)

MBB9(1)
(8-20-X)

DB10
(10B-4-P)

MBB10(1)
(8-20-17)

DB11
(10B-4-S)

MBB11(1)
(8-20-19)

(2-9-9) GATE BUFFERS
(2-9-12) BUFFER 2
READ TRANSFER ENABLE
(2-10-F)

GRD

DW1
(1-12-N)
(1-9-N)

R/W CLOCK
(2-9-B)

(R/W CLOCK)
(T.DIR(1))-a
(2-10-C)
DR-A
(2-16-L)

DW2
(1-12-M)
(1-9-M)

R/W CLOCK
(2-9-B)

(R/W CLOCK)
(T.DIR(1))-b
(2-10-D)
DR-B
(2-17-L)

2-8

DISC-R/W BUFFER

1	2	3	4	5	6
7474	7474	7474	7474	7474	7474
7400	7400	7400	7400	7400	7400
7400	7400	7400	7400	7400	7400
7474	7474	7474	7474	7474	7474
7474	7474	7474	7474	7474	7474
7474	7474	7474	7474	7474	7474
7474	7474	7474	7474	7474	7474

CNT6 V CNT3
(10B-23-E)

T DIR(0)
(2-10-7)
BKEN(0)
(2-10-B)

(2-6-D)

CNT6 V CNT3 CLEAR
(2-6-E)

SECTOR GAPS
(2-6-J) (2-10-J)
(2-6-K)

SECTOR TRACK
(2-12-4)

R/W CLOCK
(2-10-E)
(2-8-16)
(2-9-8)

(2-6-F)

(2-6-H)

DISC - CONTROL II

2-9

- ① CIRCUIT LOCATED ON CARD 2-7
- ② CIRCUIT LOCATED ON CARD 2-6

DISC-CONTROL I

DISC-ADDRESS REGISTER

DISC - READ

2-16

2-17

NOTES:
1. DP=DISK PLUG
2. RT=READ TRACK
3. WT=WRITE TRACK

PALLET BOARDS TO DISC PLUGS

	1	2	3	4	5	6	
							A
							B
							C
							D
7400	7400	7400	7400	7400	7400	7400	
7400	7400	7400	7400	7400	7400	7400	

DISC-WRITE ENABLE

1-6

	1	2	3	4	5	6	
							A
							B
							C
7400	7400	7400	7400	7400	7400	7400	D

DISC-WRITE ENABLE

1-7

1	2	3	4	5	6	
						A
						B
						C
						D
7400	7400	7400	7400			

DISC-WRITE

1-8

1	2	3	4	5	6	
						A
						B
						C
7400	7400	7400	7400	7400		D

DISC-WRITE

1-10

1	2	3	4	5	6	
						A
						B
						C
7400	7400	7400	7400	7400		D

DISC-WRITE

	1	2	3	4	5	6
A						
B						
C					7400	7400
D	7400	7400	7400	7400	7400	7400

DISC-WRITE ENABLE

11-14

1	2	3	4	5	6	
						A
						B
						C
						D
7400	7400	7400	7400	7400	7400	

DISC-WRITE ENABLE

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