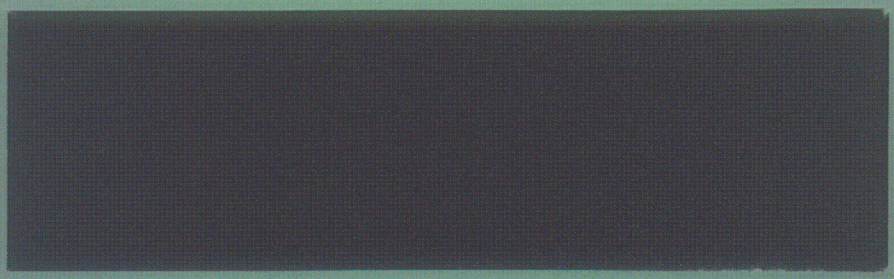
# Technical Memorandum



SCTM 190-60(14)

## A TRANSISTORIZED REACTIVITY MEASUREMENT SYSTEM



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# A TRANSISTORIZED REACTIVITY MEASUREMENT SYSTEM

Leonard Ehrman, 1414-2

## ABSTRACT

An all-transistor system has been developed to be used in measuring the reactivity of the reactor in the Sandia Engineering Reactor Facility. In operation, the system triggers a Pulsed Neutron Source (PNS) in the Reactor and counts the resulting neutron flux, thus giving a measure of the time constant of the Reactor. The counting is done in eleven time-sequenced counting channels. The Reactor time constant is a measure of the Reactor reactivity.

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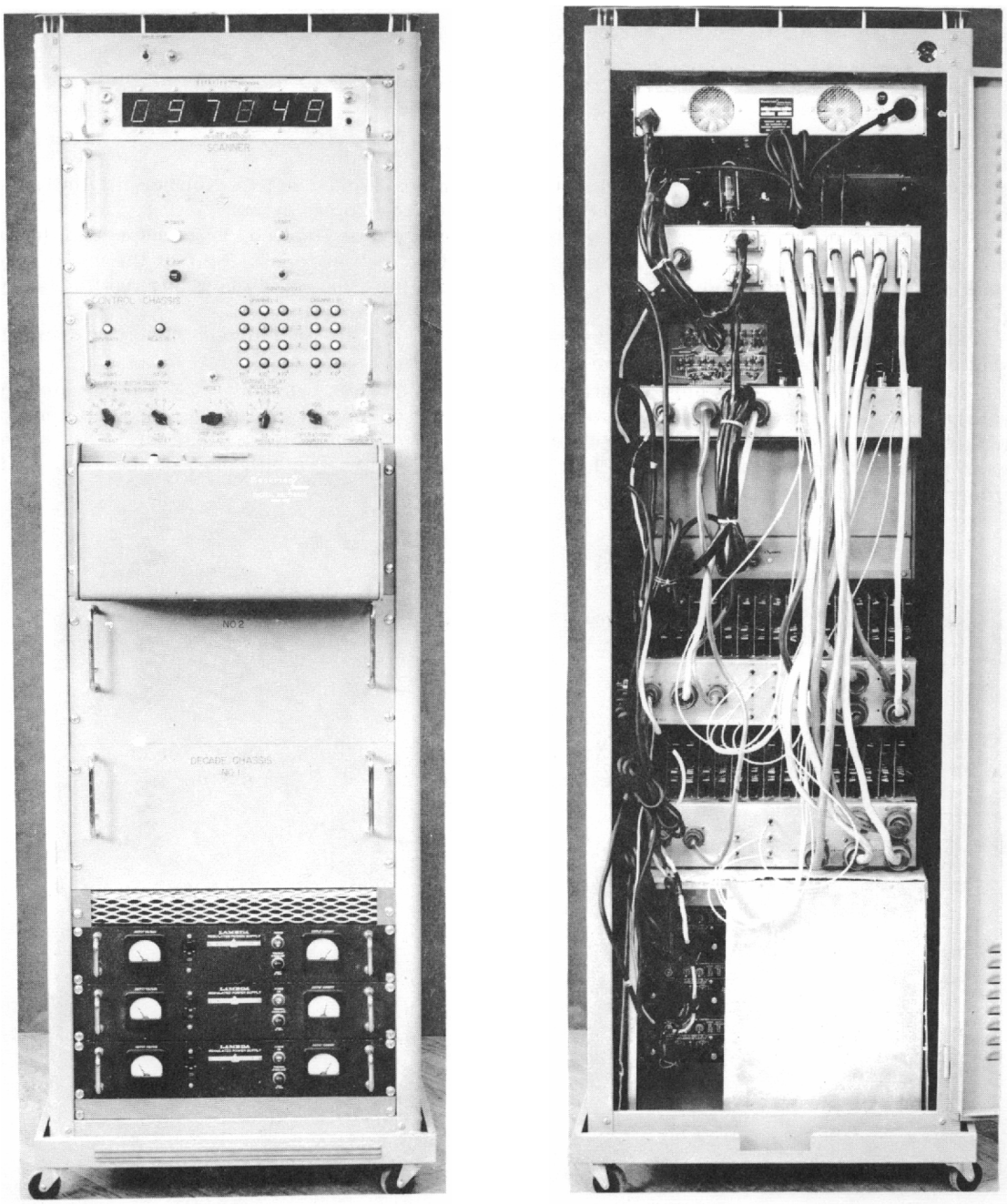

Frontispiece. Reactivity Measurement System

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ACKNOWLEDGMENT


The basic technique for reactivity measurement employed in this system is described in a memorandum entitled "A Pulsed Neutron Technique for Reactivity Determination," by B. E. Simmons and J. S. King, of Knolls Atomic Power Laboratory. This memorandum presents a complete mathematical description of the pulsed neutron measurement technique.

Several people at Sandia Corporation have contributed to the success of this project. H. B. Durham and J. Marceau worked on the initial system design, and J. J. Newman checked out the entire system after its initial construction.

# A TRANSISTORIZED REACTIVITY MEASUREMENT SYSTEM

## Section 1 -- Design Criteria of the Pulsed Neutron Technique for Reactivity Measurements[1]

If a nuclear reactor, operating in the range from \$ = -15 to delayed critical, (\$ = 0), is pulsed with a short burst of neutrons at time t = 0, and a neutron detector is placed in the reactor assembly to monitor the neutron flux decay rate, one can, by neutron counting, determine the reactivity of the reactor. The monitoring period should begin after the early transients from the burst of neutrons have died out, and continue until the delayed neutron fraction has become a sizeable fraction of the neutron flux. The desired monitoring time interval for observation is indicated in Figure 1. During this time interval, the flux $\phi$ can be shown to decay exponentially, i. e.,

$$\phi_T = \phi_o e^{-\alpha t}$$

where any steady-state background is considered subtracted out.

The decay constant, $\alpha$, is to be measured and related to reactivity.

$$\alpha = \frac{B}{L_g}\left(1 - \frac{\Delta K}{B}\right) ,$$

where B = delayed neutron fraction

$L_g$ = prompt neutron generation lifetime

$\Delta K = K_{eff} - 1$, where $K_{eff}$ is the neutron multiplication factor .

The term, $\frac{\Delta K}{B}$ , defines a unit of reactivity called "the dollar" or \$ .

Therefore $\alpha = \frac{B}{L_g}(1 - \$)$

then $\alpha$ delayed critical = $\alpha_c = \frac{B}{L_g}$ .

The constant $\alpha_c$ can be determined by a measurement of $\alpha$ with the reactor at delayed critical (\$ = 0) .
For any other $\alpha$

$$\alpha = \alpha_c (1 - \$) ,$$

or $\$ = 1 - \frac{\alpha}{\alpha_c}$

Therefore, with $\alpha$ determined at delayed critical, reactivity can be calculated if $\alpha$ is measured between the limits \$ = 0 to \$ = -15 .

---

[1] Simmons, B. E., and King, J. S., A Pulsed Neutron Technique for Reactivity Determination, Knolls Atomic Power Laboratory, Schenectady, New York.

One method of measuring $\alpha$ is to detect the changes in neutron flux levels, after a short burst of neutrons is injected into the reactor, by counting during discrete intervals ($\Delta t$) over the time interval of interest as shown in Figure 1. The count for each discrete interval is a point on a curve. The slope of this curve is $\alpha$.

The method described in this report to measure $\alpha$ is an 11-channel, time-sequenced counting system. One channel of the system is used for background counting; the other 10 channels count the decaying neutron flux over discrete, and equal, time intervals. The design of the electronics for this counting system is based on the following considerations.

Let $N_o$ be the initial count rate expected, where $N_o \sim \phi_o$ (neutron flux), and $N_t \sim \phi_t$ ,

then $N_t = N_o e^{-\alpha t} + \underline{N_{\text{background}}}$ .

Define $\tau = \frac{1}{\alpha}$ as the reactor time constant, then $N_T = N_o e^{-\frac{t}{\tau}}$ (background assumed subtracted) .

At delayed critical: $\tau_c : \frac{L_g}{B}$ .

For the Sandia reactor, assume: $L_g = 54 \times 10^{-6}$ seconds

$B = 8.5 \times 10^{-3}$

then

$$\tau_c = \frac{54 \times 10^{-6} \text{ sec}}{8.5 \times 10^{-3} \text{ sec}} = 6.35 \times 10^{-3} \text{ sec} .$$

At a reactivity of \$ = -15

$$\tau_{-15} = \frac{6.35 \times 10^{-3} \text{ sec}}{1 - (-15)} = \frac{6.35 \times 10^{-3} \text{ sec}}{16} = 0.4 \times 10^{-3} \text{ sec} .$$

In three time constants the neutron flux counts should decay from $N_o$ to $0.005 N_o$. Since the reactivity measurement range of interest is contained between \$ = 0 and \$ = -15, the reactor time constants indicate the monitoring time intervals.

For \$ = 0

$3\tau_c = 3 \times 6.35 \times 10^{-3}$ sec $= 19.05 \times 10^{-3}$ sec

For \$ = -15

$3\tau_{-15} = 3 \times 0.4 \times 10^{-3}$ sec $= 1.2 \times 10^{-3}$ sec .

The counting channel "width" depends on the reactor time constant and the number of counting channels used. For 10 adjacent counting channels, the channel width will be one-tenth of 3 reactor time constants. Thus, the maximum and minimum time intervals for monitoring are $20 \times 10^{-3}$ seconds and $1 \times 10^{-3}$ seconds respectively, giving counting channel width of from $2 \times 10^{-3}$ seconds to $0.1 \times 10^{-3}$ seconds.

The estimated maximum number of counts per channel, which should occur at delayed critical, neglecting the background count, is calculated in the following manner:

$$N_T = \int_0^t N_o e^{-\frac{t}{\tau}}$$

$$N_T = N_o \tau \left[1 - e^{-\frac{t}{\tau}}\right]$$

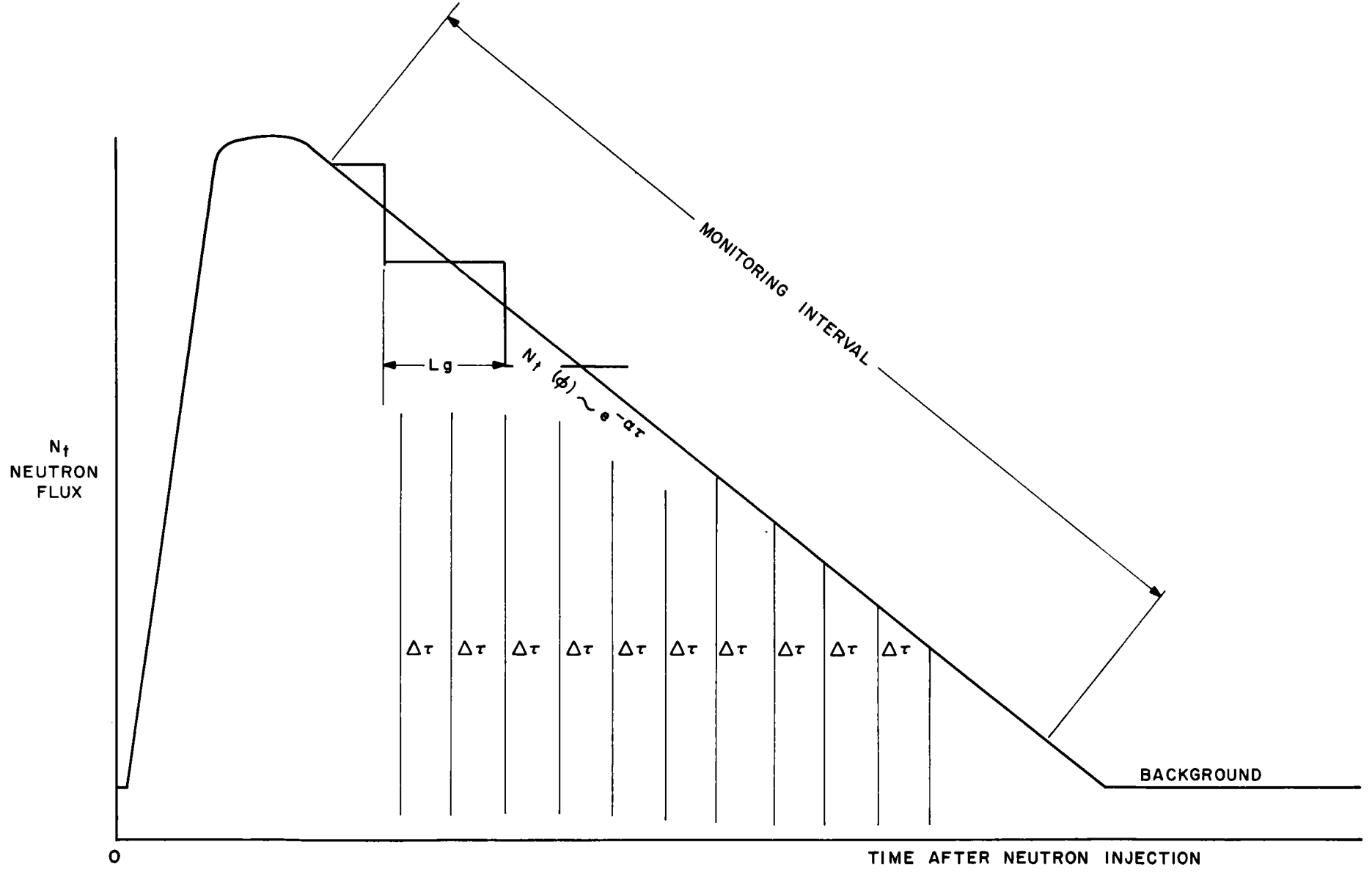



Figure 1. Neutron Flux Decay

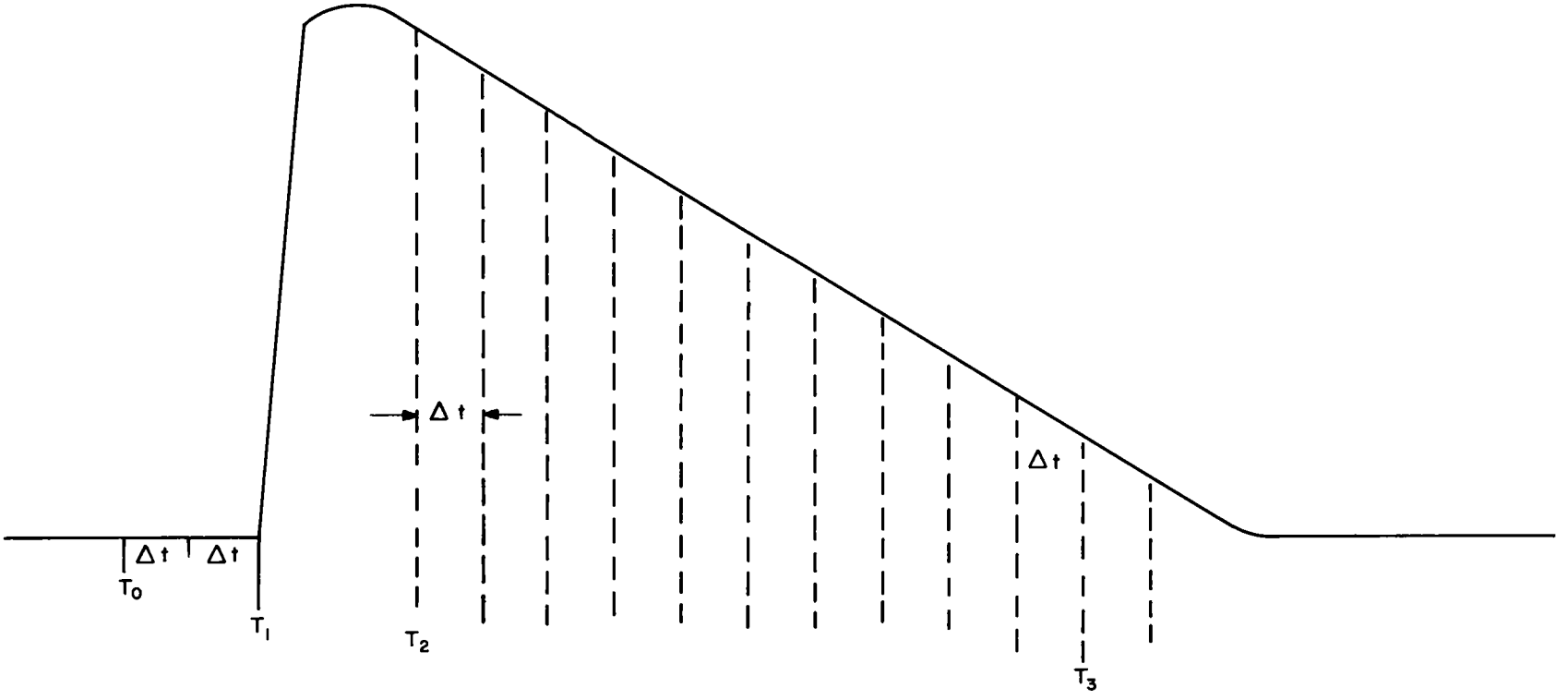



Figure 2. System Timing Requirements

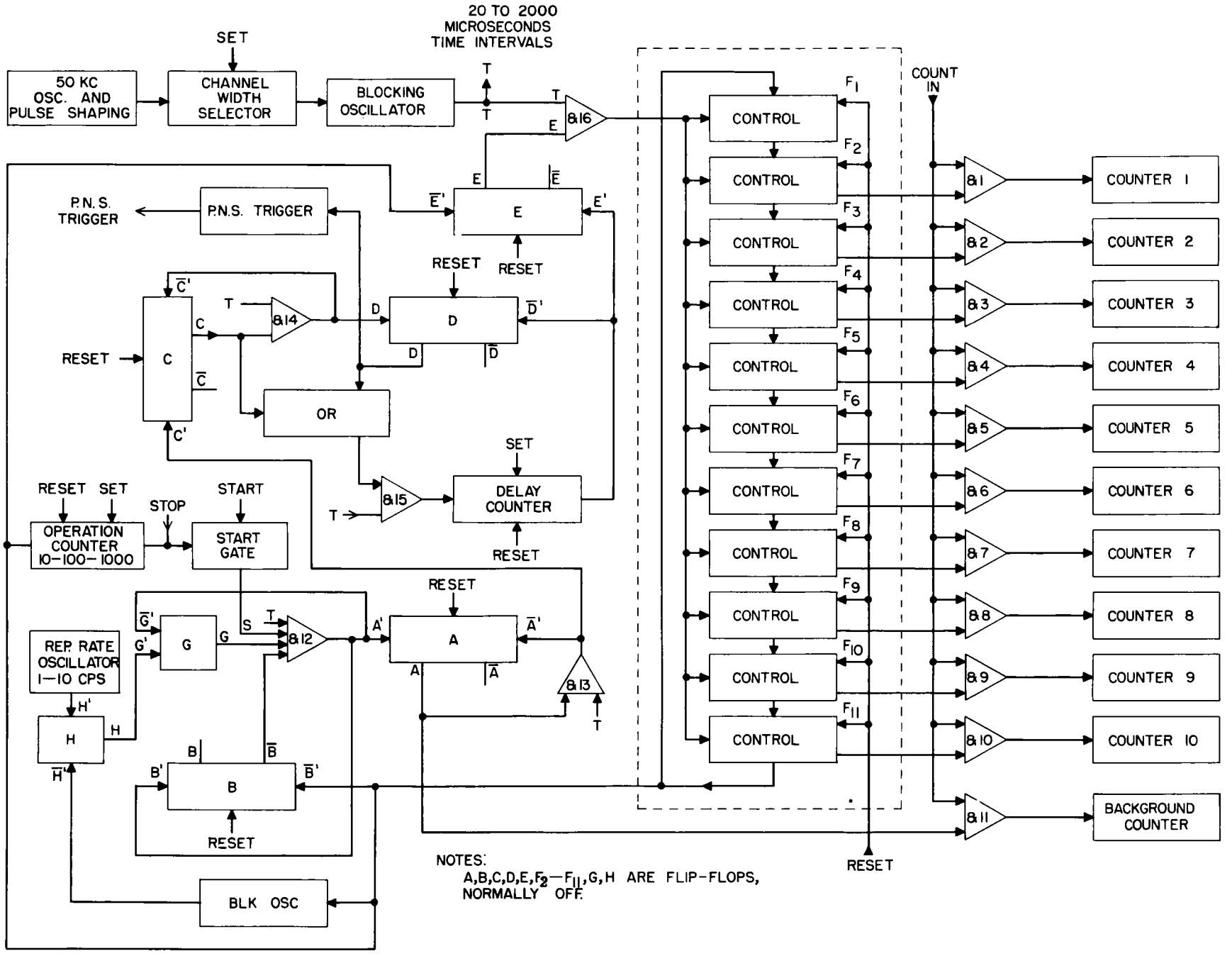



Figure 3. Block Diagram, Reactivity Measuring System

Assign T values, 0.3, 0.6 - - - - - - 3.0, and solve the equation for $N_T$ in terms of $t/\tau$ and $N_o$. A value of $N_o$ can be assumed on the basis of the maximum counting rate of the fission-chamber detector. Assume $N_o = 10^5$ counts per second, then the maximum counts per channel are:

| Channel Number | Counts |
|---|---|
| 1 | 164 |
| 2 | 122 |
| 3 | 90 |
| 4 | 67 |
| 5 | 49 |
| 6 | 37 |
| 7 | 27 |
| 8 | 20 |
| 9 | 15 |
| 10 | 11 |

The number of counts per channel are subject to statistical variation. Therefore, to smooth the statistical variations, the counting cycle is repeated 1000 times before a counter readout is made.

The background count was assumed to be subtracted for the previous calculations to be correct. To correct the counts in the 10 channels, a background count is made just prior to triggering the pulsed neutron source. The background counter has the same channel width as the 10-channel counters. The channel widths can be varied by 20 microsecond time intervals; that is, the channel widths vary from 100 microsecond to 2000 microseconds in 20 microsecond steps.

The cyclic repetition rate is variable from 1 cycle per second to 10 cycles per second. The trigger for the pulsed neutron source, a 3-volt positive pulse into a 50-ohm load, is supplied from the counting system.

The timing requirements for the system are illustrated in Figure 2. A background count is started at time $T_o$, and is ended at time $T_o + \Delta t$. The time interval for the background count is $\Delta t$, the counting channel width. At $T_1$ time, the pulsed neutron source is triggered. At $T_2$ time, the monitoring time interval is initiated and continued until $T_3$ time. During this interval, each counting channel is gated on for an interval $\Delta t$. At $T_3$ time, all resets are made, and a count is added to an operation counter which is variable in decade steps, 10-100-1000.

The next cycle starts at $T_o$ time. After the set number of operations, the cycle is stopped and a visual readout of the counters is made. Figure 3 shows the block diagram of the system. The building blocks are transistor logic circuits. The operation of the system is described in the following paragraphs.

The timing pulses, T, for the system, are generated from a crystal-controlled 50-kilocycle oscillator. The channel width selector can be set to trigger the blocking oscillator at intervals in multiples of 20 microseconds from 20 microseconds to 2000 microseconds. Initially, the flip-flops, A, B, C, D, E, $F_2$ - $F_{11}$, G, H are set OFF, $A = \overline{A}$, $B = \overline{B}$, etc. $F_1$ is set ON. The operation counter is preset to zero and the delay counter if preset to the desired delay in terms of the number of timing pulses required.

Reference to the timing diagram of the system Figure 4, will indicate the operation of the flip-flops. A start signal arms the Start Gate so that the S term into AND Gate No. 12 is true. A pulse from the repetition rate oscillator turns flip-flop H ON. The leading edge of H is used to set flip-flop G ON. The next timing pulse, T, sets flip-flop A ON. The logic for setting A ON is:

$$A' = GST\overline{B} \ ,$$

where the sumbol A' means set flip-flop A to the ON condition. The terms on the right-hand side of the logic are the necessary conditions for A to be true.

Flip-flop B is set ON with the same logic,

$$B' = A' = GST\overline{B} \ ,$$

inhibiting the next T pulse at AND Gate 12.

A is ON for the interval between two clock pulses, T

$$\overline{A}' = AT \ ,$$

also,

$$C' = \overline{A}' = AT \ .$$

C is turned ON when A is turned OFF. AND Gate No. 14 and the OR Gate are set so that the next clock pulse, T, sets one count into the delay counter, turns C OFF, and turns D ON. The leading edge of flip-flop D operates the PNS trigger.

$$\text{PNS Trigger} = D$$
$$C' = CT = D'$$
$$\text{Delay Counter} = T\,(C+D)$$

The Delay Counter sets D OFF and E ON after N-1 clock pulses, where, N is the delay time, in terms of clock pulses, between triggering the PNS and counting the output pulses of the neutron detector. AND Gate No. 17 is armed by E, so that, the next and subsequent clock pulses, T, are applied to the Shift Register shift line. $F_1$ is set OFF and $F_2$ is set ON according to the logic expressions:

$$\overline{F}'_1 = \overline{F}_2\ \overline{F}_3\ \overline{F}_4\ \overline{F}_5\ \overline{F}_6\ \overline{F}_7\ \overline{F}_8\ \overline{F}_9\ \overline{F}_{10}\ \overline{F}_{11}\ T \ ,$$
$$F'_2 = \overline{F}_1\ \overline{F}_3\ \overline{F}_4\ \overline{F}_5\ \overline{F}_6\ \overline{F}_7\ \overline{F}_8\ \overline{F}_9\ \overline{F}_{10}\ \overline{F}_{11}\ T \ .$$

At the next clock pulse $F_2$ is set OFF and $F_3$ is set ON. The counters, No. 1 through No. 10 are each sequentially turned ON for the interval between two clock pulses.

When the flip-flop $F_{11}$ is set OFF' and $F_1$ set ON, flip-flop B is set OFF, flip-flop E is set OFF, flip-flop H is set OFF through a blocking oscillator, and a count is added to the operation counter.

The next pulse from the repetition rate generator starts the cycle again. The operation counter turns the START Gate OFF when the preset count is completed.

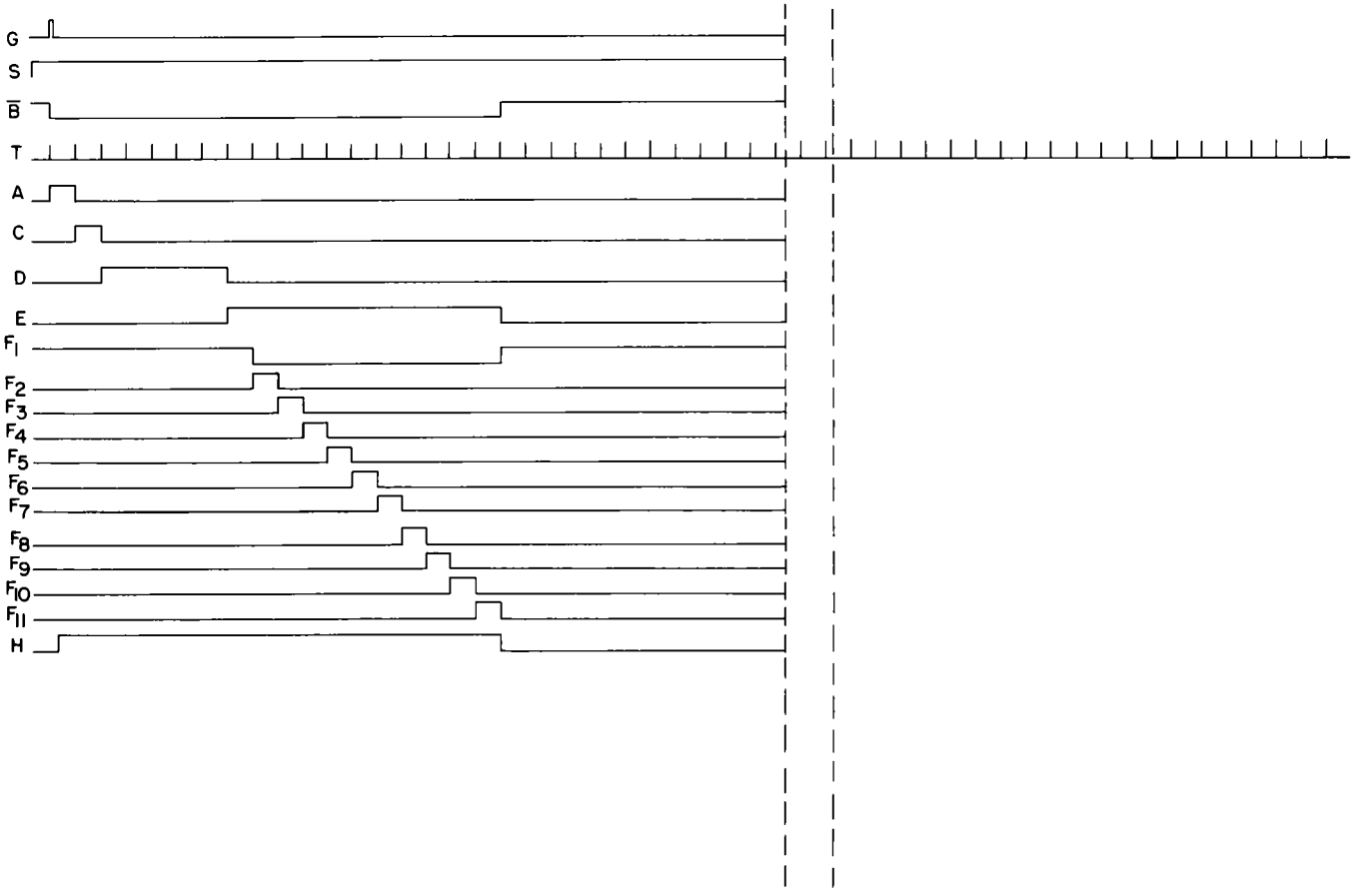



Figure 4. Timing Diagram, Reactivity Measuring System

## Section 2 -- Electronics

### System Design

The entire purpose of the system under discussion is to implement the block diagram of Figure 3. A small number of basic transistor building blocks, constructed on printed circuit cards, have been developed, which, when properly interconnected with each other and with some chassis mounted components, perform this function. The cards which have been developed are: 1 megacycle decade counter, 200 kilocycle shift resistor, and a two-input diode transistor AND Gate. In addition, one special purpose AND/OR Gate card has been made. If the forward signal and the feedback loop connections of the decade counter are omitted from the card, we then have a card with 4 flip-flops mounted on it, each with an X' and $\overline{X}$' input, as well as an X and an $\overline{X}$ output. A standard decade counter can be modified to be used as a preset counter by the addition of two transistors in parallel with transistors Q3 and Q5 of the decade. Thus we have the capability of individually setting or resetting any of the stages of the decade. If a decade is set to what would normally be a count of N, it will then count 10-N times before its register is full. If we then use the transition of the last stage to reset all the stages, through a suitable delay, to N, we have converted the counter from a decade counter, or count by 10, to a count by N counter, where N is between 1 and 10. Two counters can be cascaded and used to count from 1 to 100. The reset logic is controlled by a separate 10-position rotary switch for each stage of a preset counter, while the delay is obtained with a blocking oscillator.

The outputs of the 11 channels of decade counters are presented in two ways. A permanent record is printed by a Berkeley Model 1452 Digital Recorder, while a visual display is shown on a Berkeley Model 5916 In-Line Readout. By means of a stepping switch scanner the channels are scanned sequentially, starting with the background channel. The scanning can be done automatically, if it is desired to read all eleven channels at 1-second intervals, or manually, if it is desired to monitor one channel for a long interval of time. In addition, decades 4, 5 and 6 of channel 1, and decades 3 and 4 of channel 10 are displayed continually in binary coded decimal form by means of indicator lights.

The frontispiece is a photograph of the complete system. The remainder of this section will be devoted to a discussion of the individual components.

### Power Supplies

The regulated power supplies used in the system are Lambda Model 2095M's. Two are used for -5 volts, and a third for +5 volts. Supply regulation against both line and load disturbance is 0.15 percent. The two negative supplies are designated -5 (A) and -5(B). The drain on -5 (A) is 1.75 amperes, -5(B) is 1.25 amperes, and +5 is 1.7 amperes. The supplies are rated at 2 amperes each. Due to power dissipation within the supplies, they are isolated from the interior of the rack by a sheet metal enclosure which is cooled by a Rotron muffin fan.

### Decade Counter Chassis 1 and 2

The Decade Counter Chassis contains the 11 channels of decades necessary to count and store the neutron flux rate. Chassis 1 consists of 5 channels of decades, with 6 decades per channel. These channels are used to count the second through sixth channels of information. Chassis 2 contains 6 channels of decades. It is broken down into 1 channel of 6 decades, and 5 channels of 5 decades. The 6 decade channel measures the first channel of information, while the remaining channels measure the background count and the seventh through tenth channels.

The wiring of the individual chassis is shown in the Appendix, Figures A-1 and A-2. A typical decade counter is shown in Figure A-3.

Figure A-3 is a 1-megacycle decade, with a 1-2-2-4 code. The signal level is either 0 or -4 volts, and is emitter-follower coupled. The decade output is brought out from pins E, K, U and Y, isolated by 18,000-ohm resistors, and transmitted through the appropriate cabling to the Scanner Chassis.

Control Chassis

All the timing functions necessary to gate the signal pulses to the counters are generated internally in the Control Chassis. The inputs to this chassis are the START signal and the neutron detector output, "Count In." The outputs are the PNS trigger and the gated counts to the decade counter chassis. The control chassis wiring diagram is shown in Figure A-4. Individual components will be discussed in this section - there will be no attempt to give an integrated operational description, as this would parallel the description given in Section 1.

The timing pulse source is shown in Figure A-4. Transistors Q7 and Q8 form a crystal controlled 50-kc sine wave oscillator. Transistors Q9 through Q11 shape the sine wave into a 0.15 microsecond pulse train with a 50-kc repetition rate. This pulse then goes to the channel-width selector, a two-stage preset counter, which can be set to give one output pulse for from 1 to 100 input pulses. This pulse, in turn, is shaped by a blocking oscillator whose output is a -3v, 0.15 microsecond pulse. Thus, starting with a 50-kc oscillator, we have a crystal-controlled pulse source whose frequency is variable from 50 kc to 500 cps, giving a channel width of from 20 to 2000 microseconds.

The low-frequency oscillator, Q14 of Figure A-4, is used to determine the repetition rate of the system. It is a double-base diode oscillator, the frequency of which is controlled by a 250 K-ohm potentiometer. The oscillator output is a negative pulse, with a repetition rate varying from 1 to 10 cps.

The neutron count pulse is converted into a standard negative pulse by means of transistors Q5 and Q6 of Figure A-4. A positive pulse with an amplitude greater than 10 volts into Q5 will produce a -3 volt, 0.15 microsecond pulse at pin 6 of $T_2$.

The gate control binaries are emitter-follower coupled flip-flops, with transistor ON and OFF inputs. The output levels are nominally 0 and -4 volts. These have been fabricated on printed circuit cards, with four flip-flops per card. The circuitry is the same as that of the 1-mc decade counters, with the complementary triggering and cross-coupling circuits removed.

The fourth component, shown in Figure A-5, is the shift register. It is composed of eleven identical stages, ten of which are used to gate the 2-Input AND Gates ON, while the eleventh is used as a neutral position. The shift registers have been fabricated on printed circuit cards, with five stages per card. To operate as an eleven-stage register, three cards have been placed in series. The integral feedback loop from Q27 to Q5 has been broken, and the feedforward and feedback signal paths have been provided by proper wiring of the plug-in sockets.

The circuit used to gate the neutron count pulses to the various decades is a diode-transistor AND Gate, shown in Figure A-6. The load on the output is a 91-ohm coaxial cable. One input to the AND Gate is a shift-register pulse, while the other input is the neutron count pulse as reshaped by Q5 and Q6 of Figure A-4. These Gates have been fabricated with five Gates per printed circuit card.

AND Gates 12 through 16, and the OR Gate are contained on the board shown in Figure A-7. Only one such card is used in the system.

The delay selector is a single-stage preset counter, similar in design to the channel width selector.

Scanner

The purpose of the scanner chassis is to permit the operator to select any channel of decade counters and to read out non-destructively the stored count. The schematic of the scanner is shown in Figure A-8. The operation of the scanner is as follows:

The decade counter outputs are cabled into the stepping switch. The stepping switch output goes to three low-frequency amplifier cards, which change the signal level to either 0 or -22 volts. The outputs of the amplifiers are then monitored by the In-Line Readout and the Digital Recorder.

There are two possible modes of operation of the scanner. In the continuous mode, the scanner will upon operation of the START switch, automatically scan all 11 channels and return to a home position. In the manual mode, the scanner will scan only as long as the START switch is depressed. When the START switch is released, the scanner remains in its last position.

The stepping rate of the scanner, 1 cps, is determined by the double-base diode oscillator, Q1. A negative pulse from the oscillator sets the flip-flop, composed of Q2 and Q3, ON. This, in turn, energizes a murcury relay through transistor Q4. When the mercury relay closes, the coils of the stepping switches are grounded, causing the interrupter contacts of the stepping switches to open. When all three interrupters are open, the flip-flop is reset, causing the stepping switch to step.

A microswitch is mechanically connected to one of the stepping switches, and is used as an off-normal contact. When this stepping switch is in its last position, the microswitch opens, thus opening the SET line to the flip-flop, and preventing any further rotation of the stepping switch. To start the scanning cycle again, the start button, S1, is depressed, bridging the open microswitch. If manual operation is desired, toggleswitch S2, in series with the microswitch, is opened. The stepping switches will then operate only as long as S1 is depressed.

Cabling

The cabling diagrams of the system are given in Figures A-9, A-10, A-11.

## Section 3 -- Operation

The measurement system has been designed to be as simple to operate as possible. There is one switch on the front of the relay rack which controls all AC power in the system. Turning this switch ON powers the entire system.

Four quantities must be decided upon before measurements are made. They are the trigger repetition rate, channel width, count delay and total number of cycles desired. The repetition rate can be varied between 1 and 10 cycles per second by means of a front panel control.

The channel width is chosen by means of two rotary selector switches. The basic timing frequency of the system is 50 kc. This can be divided by any integer from 1 to 100, giving a frequency range of 500 cps to 50 kc. The channel width is thus variable between 20 and 2000 microseconds.

The delay counter selector switch can be set to give a delay of from 1 to 10 channel widths before the neutron pulse counting begins.

The total number of cycles desired is controlled by a rotary switch. By this means, the measuring cycle can be ended after 10, 100 or 1000 pulse cycles.

Once these four parameters have been set, the operation is straight forward. The Trigger Output is connected to the PNS, the neutron detector output is connected to the Count Input, and the system is reset. Then the START button is pushed. As long as the operating cycle is still on, the Operate light is lit. When the cycle is over, the light goes out. The stored count can then be printed out by operating the scanner switch. The scanner should not be operated during the operating cycle of the control chassis.

The operating cycle can be stopped at any point by operating the STOP button. This will stop the system at the end of the current operation cycle. The operation can be continued by use of the START button.

The entire system can be cleared by means of the RESET switch.

# APPENDIX

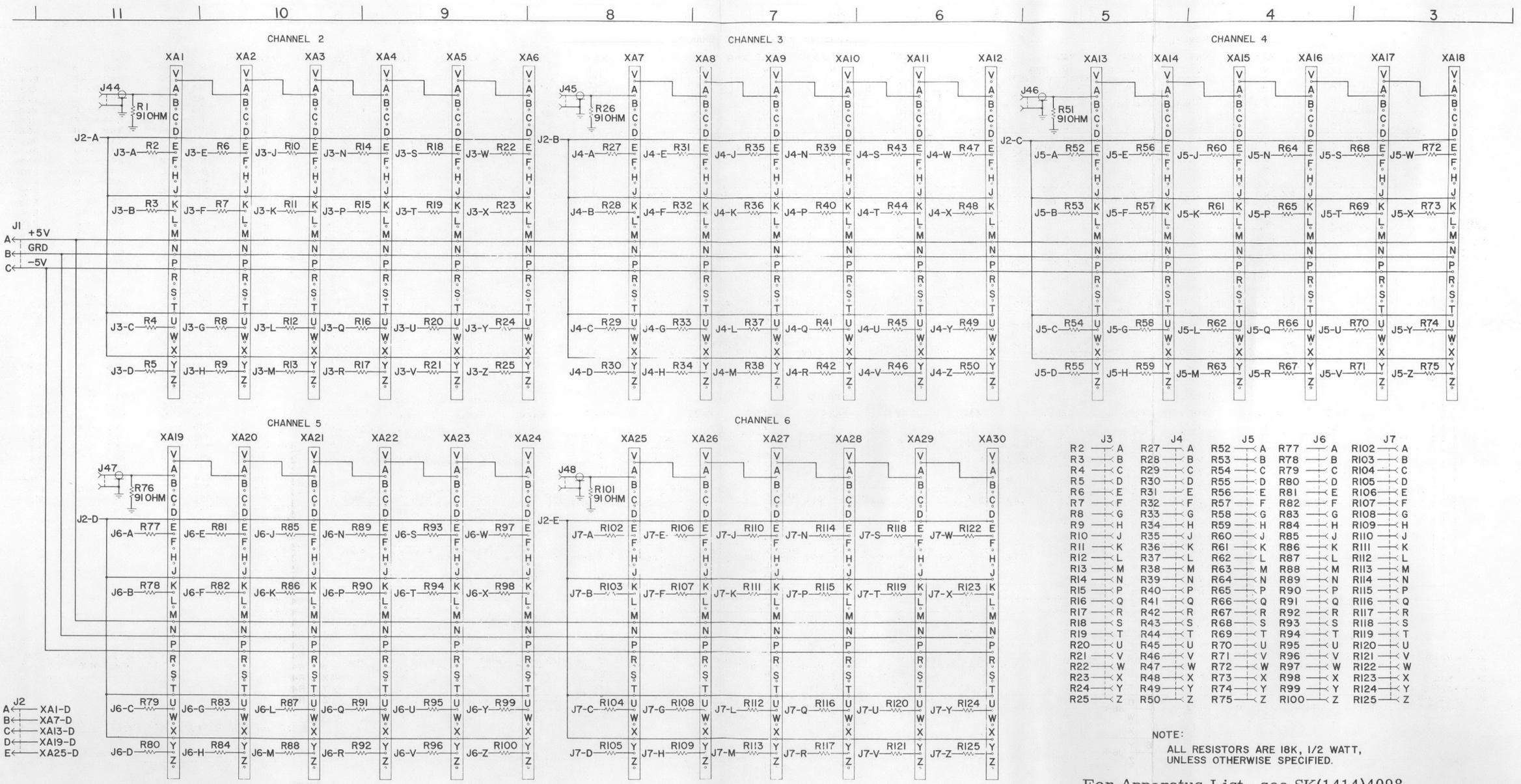



Figure A-1. Schematic, Decade Chassis No. 1

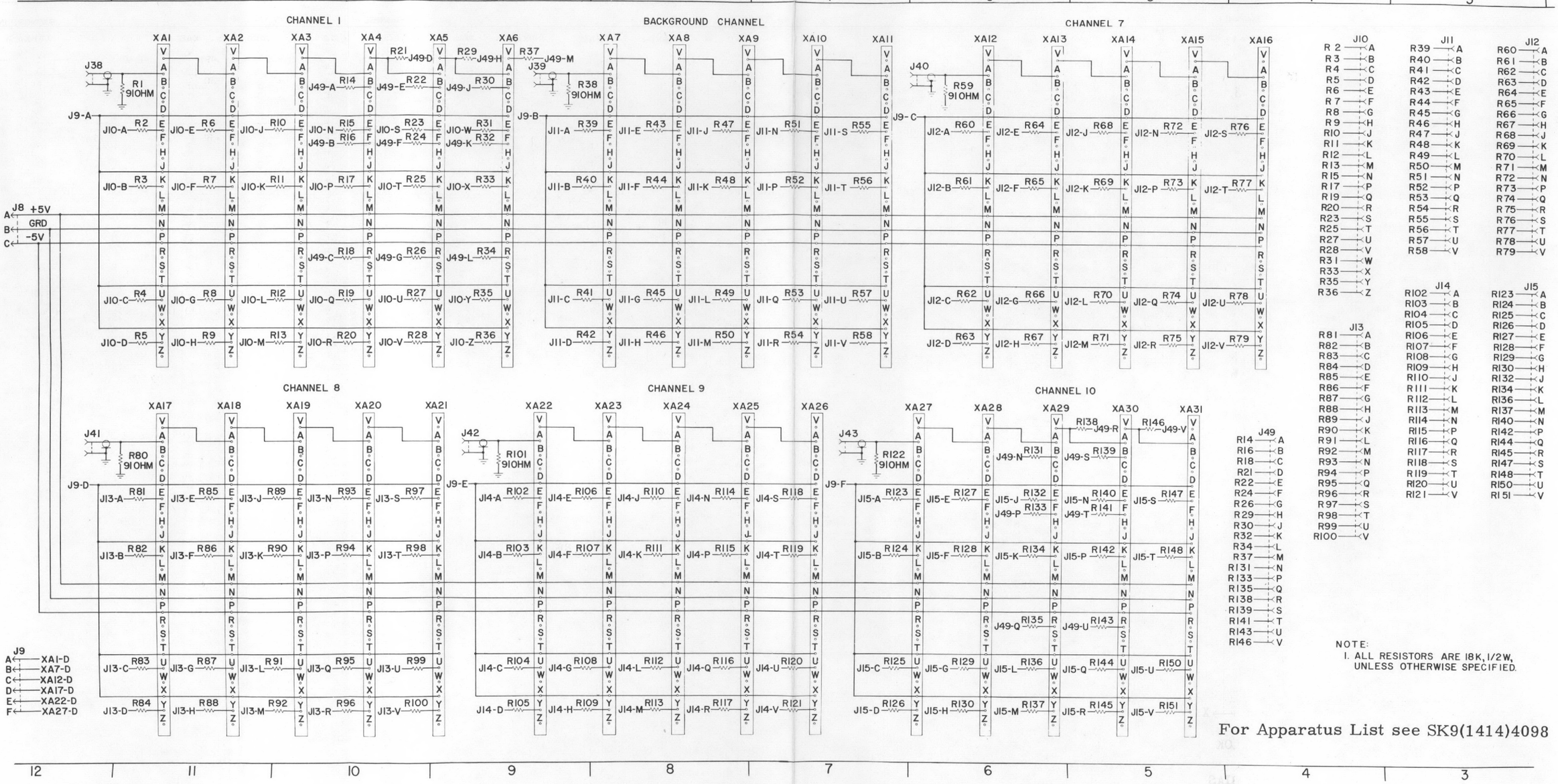
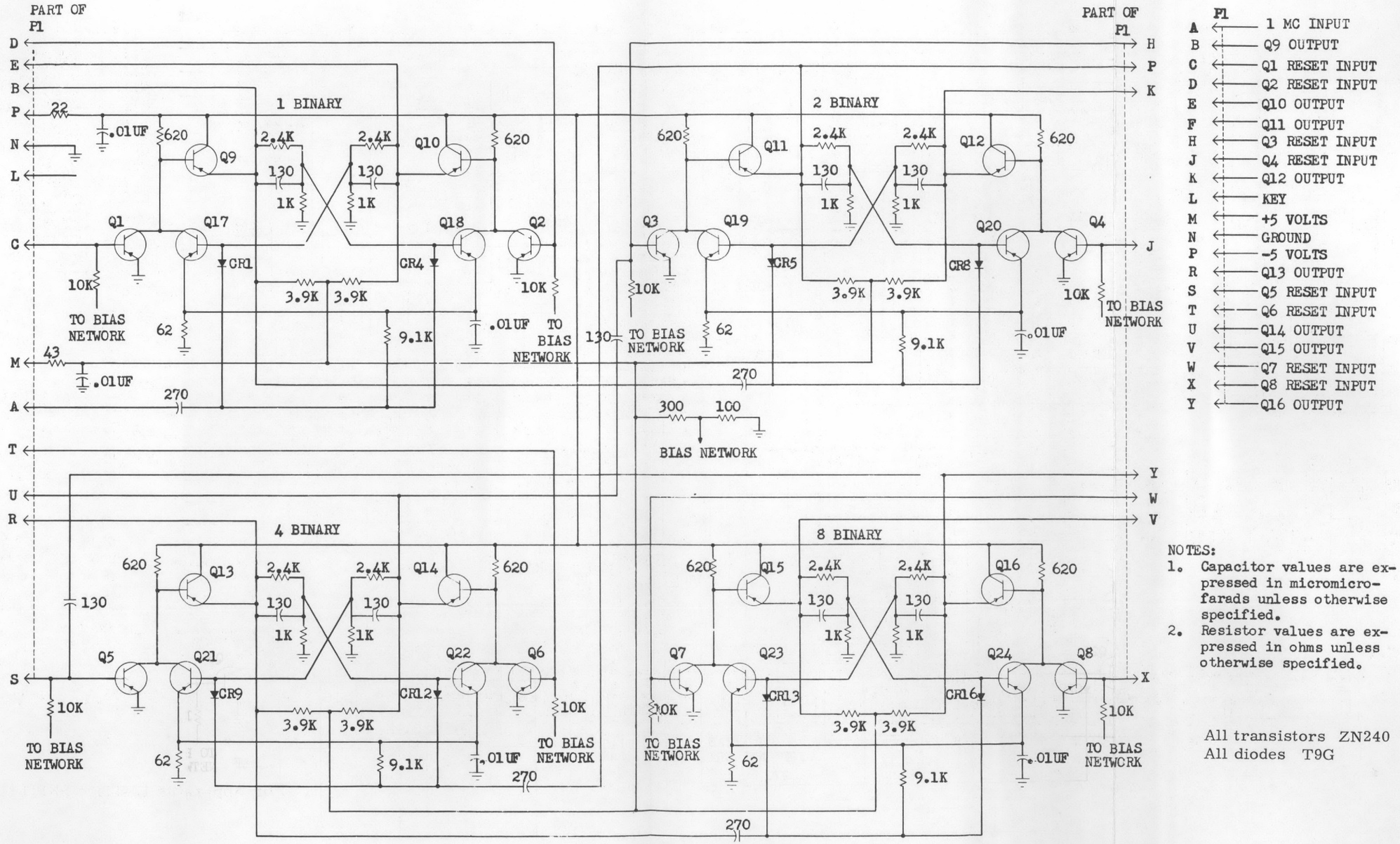



Figure A-2. Schematic, Decade Chassis No. 2




F1

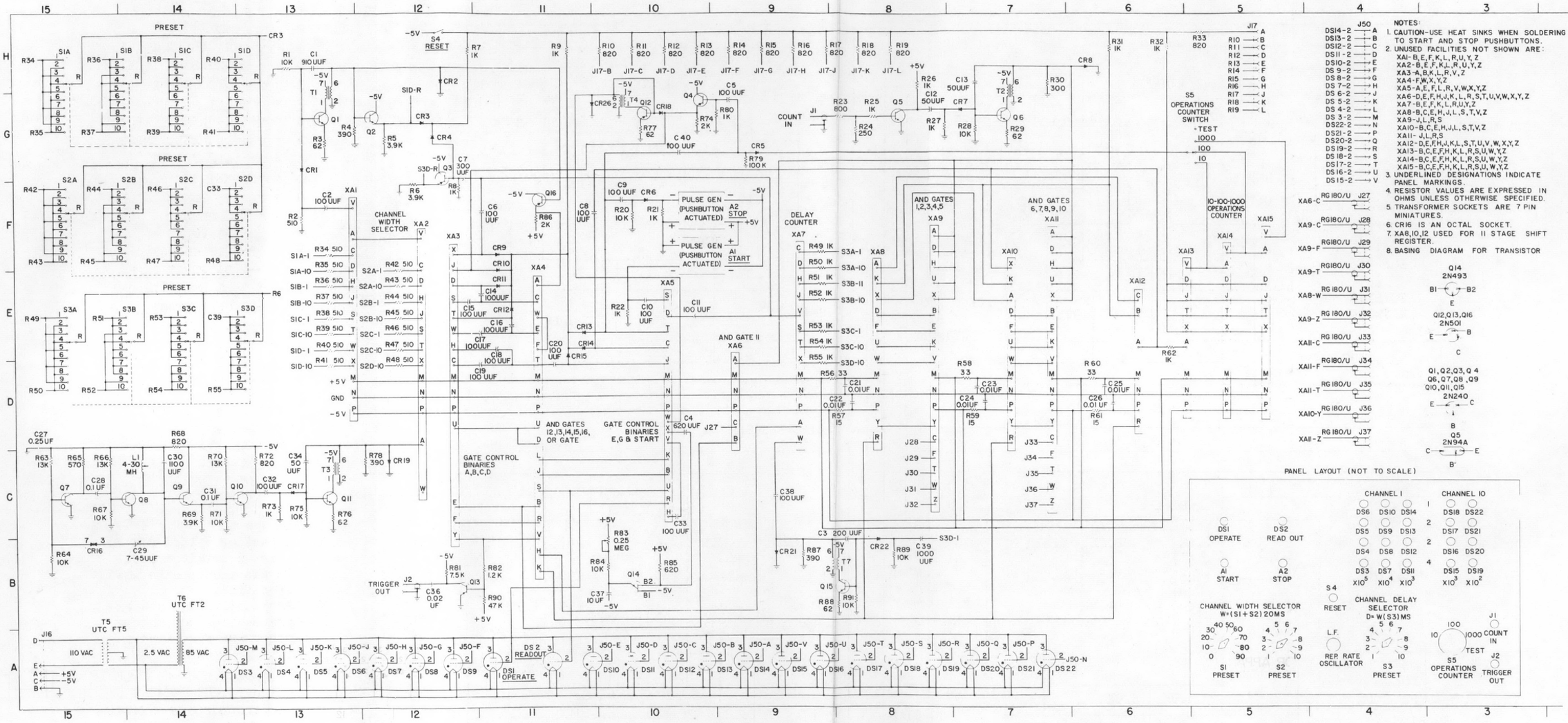
| | |
|---|---|
| A | 1 MC INPUT |
| B | Q9 OUTPUT |
| C | Q1 RESET INPUT |
| D | Q2 RESET INPUT |
| E | Q10 OUTPUT |
| F | Q11 OUTPUT |
| H | Q3 RESET INPUT |
| J | Q4 RESET INPUT |
| K | Q12 OUTPUT |
| L | KEY |
| M | +5 VOLTS |
| N | GROUND |
| P | -5 VOLTS |
| R | Q13 OUTPUT |
| S | Q5 RESET INPUT |
| T | Q6 RESET INPUT |
| U | Q14 OUTPUT |
| V | Q15 OUTPUT |
| W | Q7 RESET INPUT |
| X | Q8 RESET INPUT |
| Y | Q16 OUTPUT |

NOTES:

1. Capacitor values are expressed in micromicrofarads unless otherwise specified.
2. Resistor values are expressed in ohms unless otherwise specified.

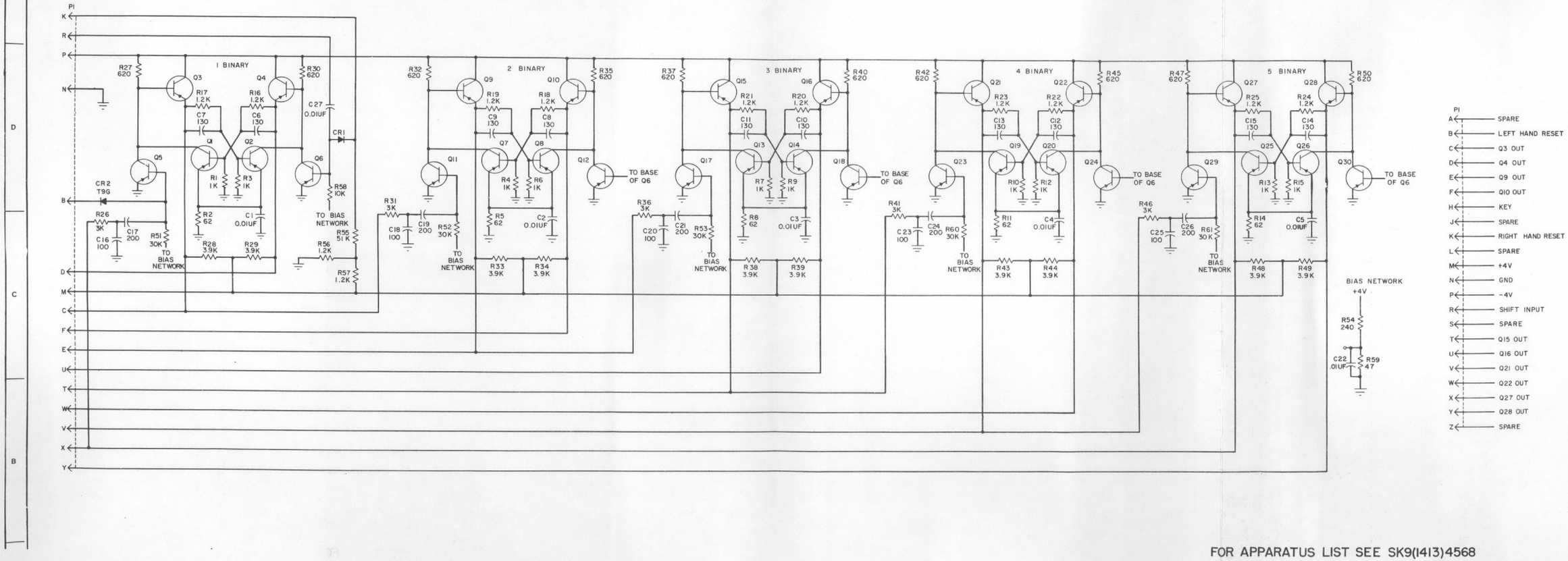
All transistors ZN240
All diodes T9G

Figure A-3. A Typical Decade Counter




For Apparatus List see SK9(1414)14095

Figure A-4. Schematic, Control Chassis




FOR APPARATUS LIST SEE SK9(1413)4568

Figure A-5. Schematic, 5-Stage Shift Register

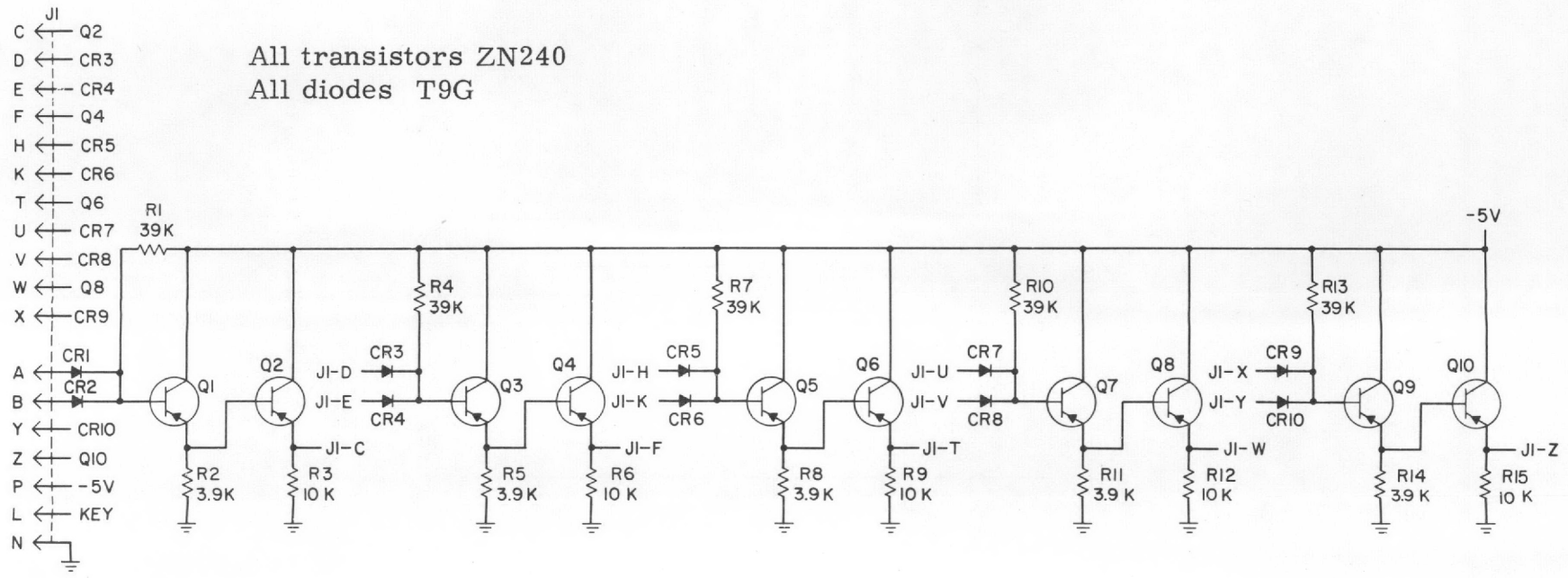
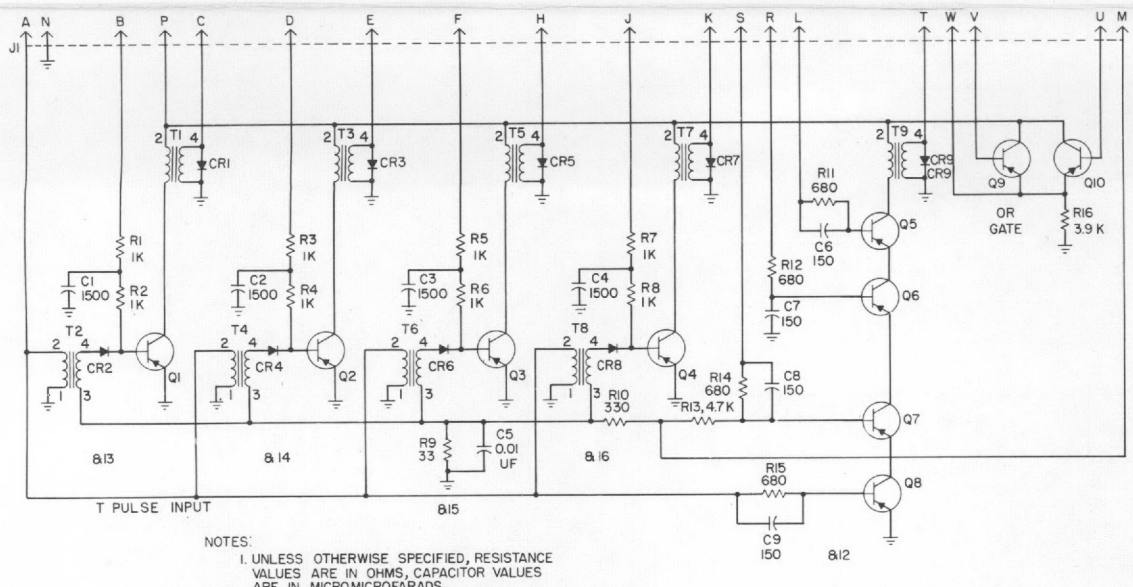



Figure A-6. Schematic, 2 Input and Gate




NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROMICROFARADS.
2. FUNCTION OF JI IS AS FOLLOWS:

| | |
|---|---|
| A- T PULSE INPUT | M- +5V |
| B- 8I3 INPUT | N - GND |
| C- 8I3 OUTPUT | P - -5V |
| D- 8I4 INPUT | R - 8I2 INPUT |
| E- 8I4 OUTPUT | S - 8I2 INPUT |
| F- 8I5 INPUT | T - 8I2 OUTPUT |
| H- 8I5 OUTPUT | U - OR INPUT |
| J- 8I6 INPUT | V - OR INPUT |
| K- 8I6 OUTPUT | W - OR OUTPUT |
| L- 8I2 INPUT | X - KEY |

| | | | | | | |
|---|---|---|---|---|---|---|
| C1 | 1500UUF | | | | | |
| C2 | 1500UUF | | | | | |
| C3 | 1500UUF | | | | | |
| C4 | 1500UUF | | | | | |
| C5 | 0.01 UF | | | | | |
| C6 | 150UUF | | | | | |
| C7 | 150UUF | | | | | |
| C8 | 150UUF | | | | | |
| C9 | 150UUF | | | | | |
| | | | | | | |
| CR1 | | | | T9G | | |
| CR2 | | | | T9G | | |
| CR3 | | | | T9G | | |
| CR4 | | | | T9G | | |
| CR5 | | | | T9G | | |
| CR6 | | | | T9G | | |
| CR7 | | | | T9G | | |
| CR8 | | | | T9G | | |
| CR9 | | | | T9G | | |
| | | | | | | |
| JI | | | | 143-022-01 | | AMPHENOL |
| | | | | | | |
| Q1 | | | | 2N240 | | |
| Q2 | | | | | | |
| Q3 | | | | | | |
| Q4 | | | | | | |
| Q5 | | | | | | |
| Q6 | | | | | | |
| Q7 | | | | 2N240 | | |
| Q8 | | | | 2N240 | | |
| Q9 | | | | 2N501 | | |
| QIO | | | | 2N501 | | |
| | | | | | | |
| R1 | 1 K | | | | | |
| R2 | 1 K | | | | | |
| R3 | 1 K | | | | | |
| R4 | 1 K | | | | | |
| R5 | 1 K | | | | | |
| R6 | 1 K | | | | | |
| R7 | 1 K | | | | | |
| R8 | 1 K | | | | | |
| R9 | 33 | | | | | |
| R10 | 330 | | | | | |
| R11 | 680 | | | | | |
| R12 | 680 | | | | | |
| R13 | 4.7K | | | | | |
| R14 | 680 | | | | | |
| R15 | 680 | | | | | |
| | | | | | | |
| T1 | | | | OIL 3 321 | | VALOR |
| T2 | | | | OIL 3 321 | | VALOR |
| T3 | | | | OIL 3 321 | | VALOR |
| T4 | | | | OIL 3 321 | | VALOR |
| T5 | | | | OIL 3 321 | | VALOR |
| T6 | | | | OIL 3 321 | | VALOR |
| T7 | | | | OIL 3 321 | | VALOR |
| T8 | | | | OIL 3 321 | | VALOR |
| T9 | | | | OIL 3 321 | | VALOR |

Figure A-7. Schematic, AND Gates 12-16 and OR Gate

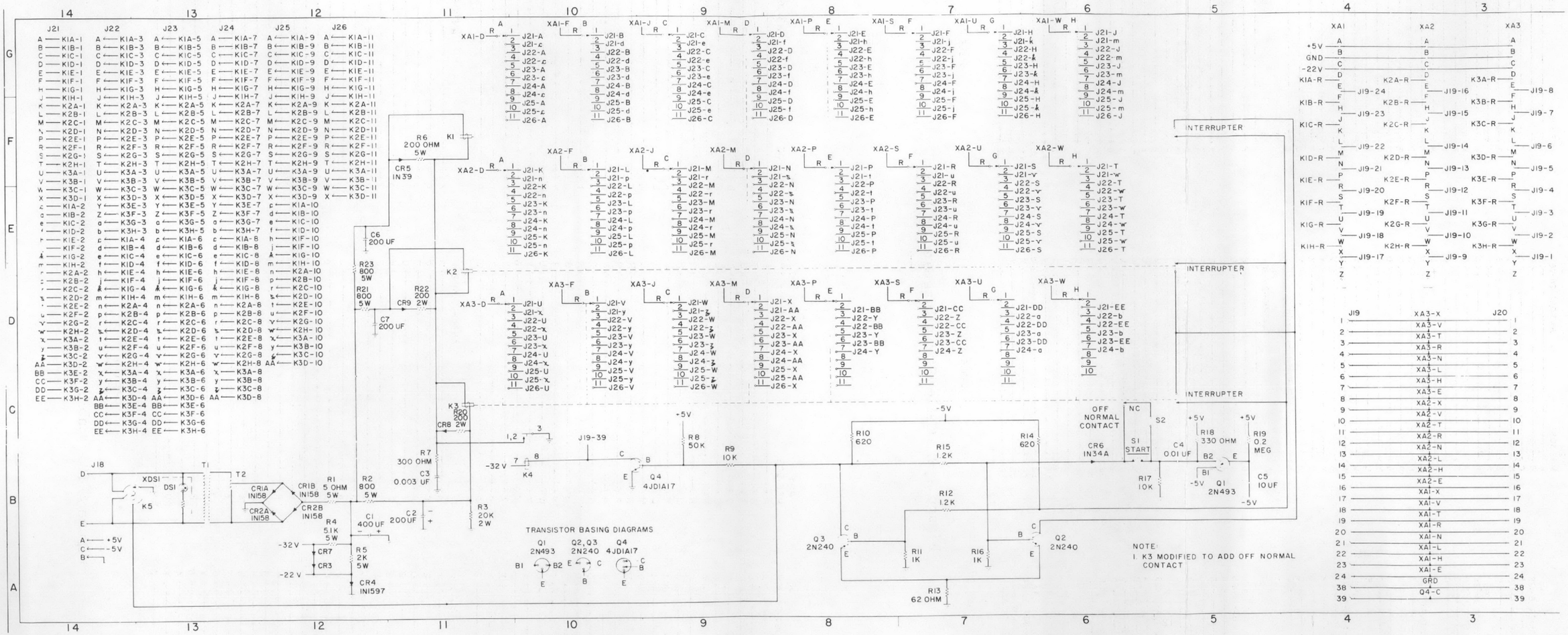
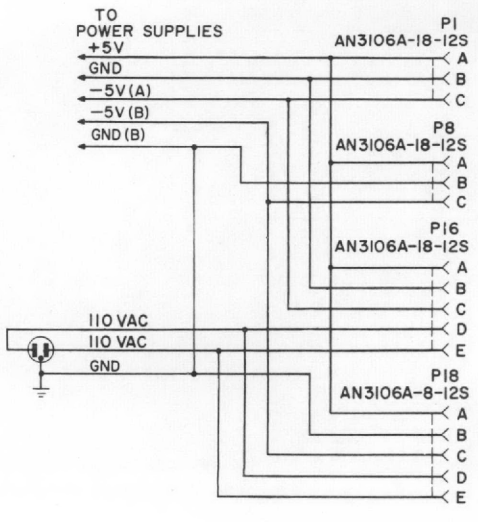
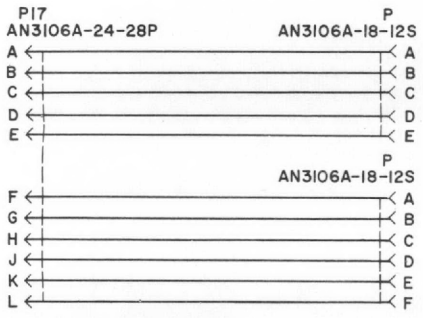


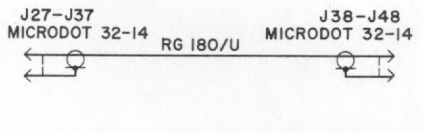

Figure A-8. Schematic, Scanner Chassis



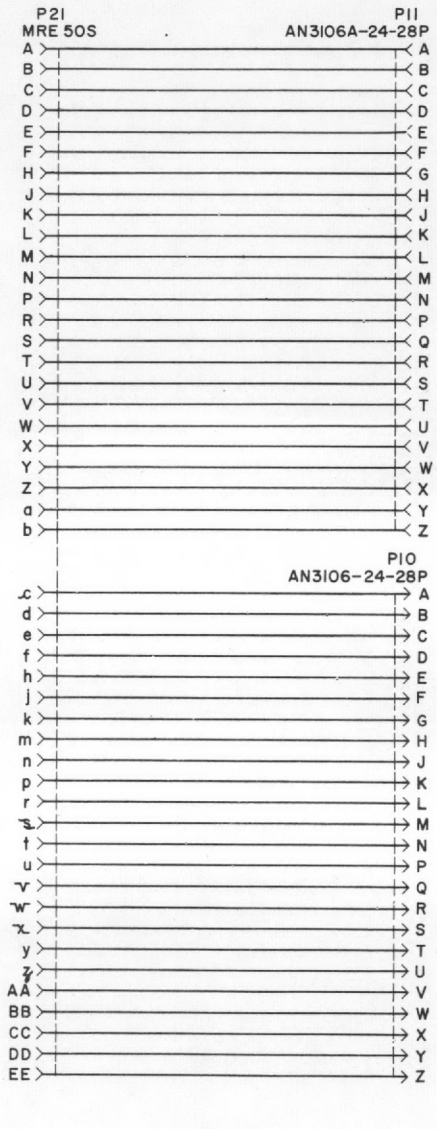

CABLE 1




CABLE 2




CABLE 3




CABLE 4

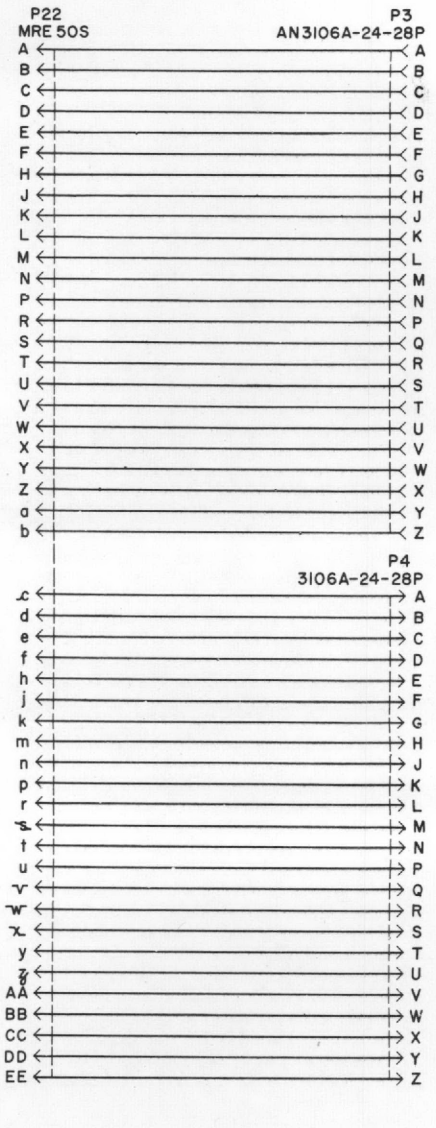
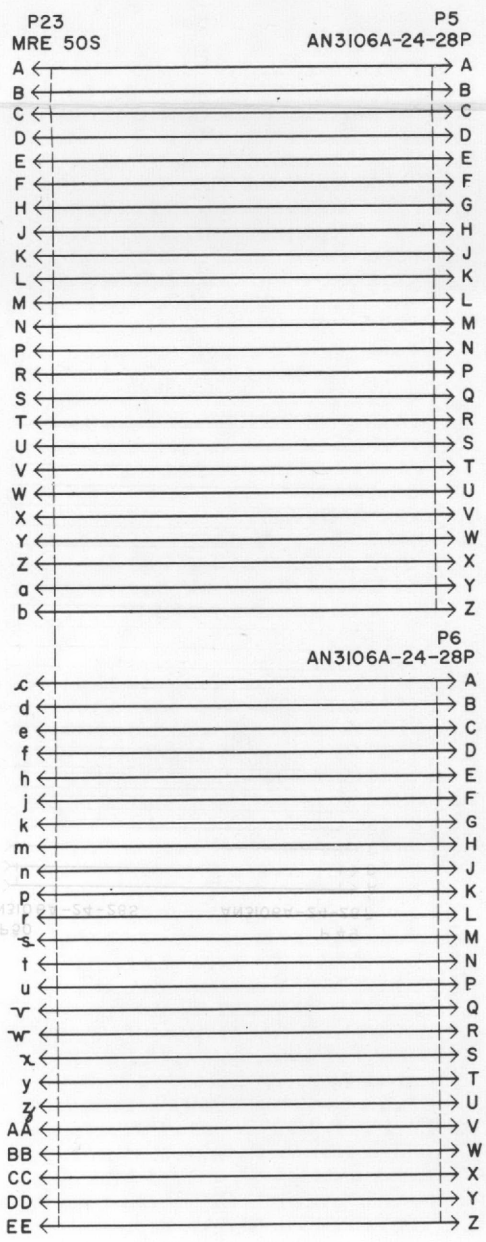
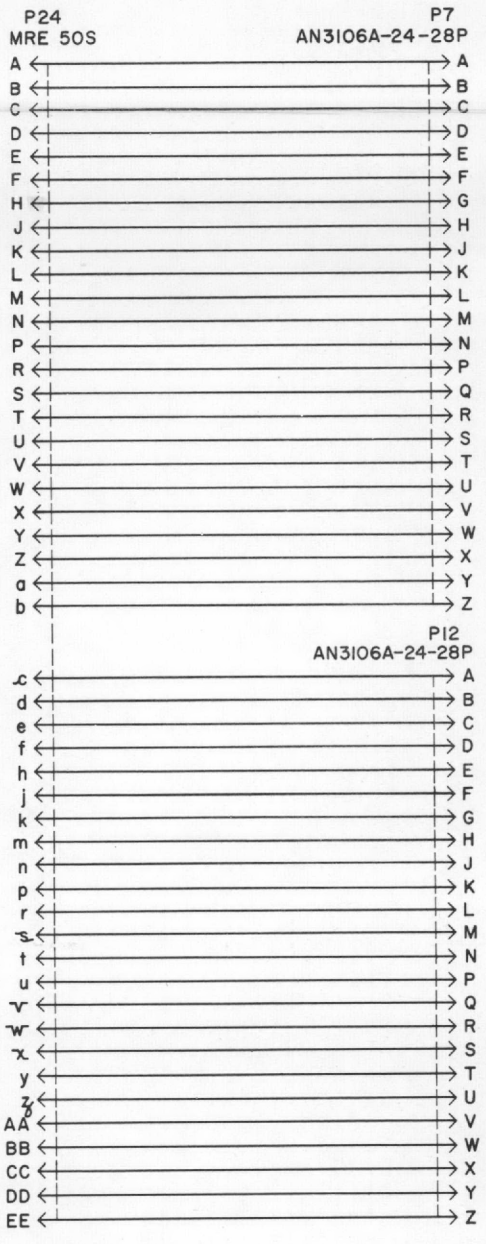


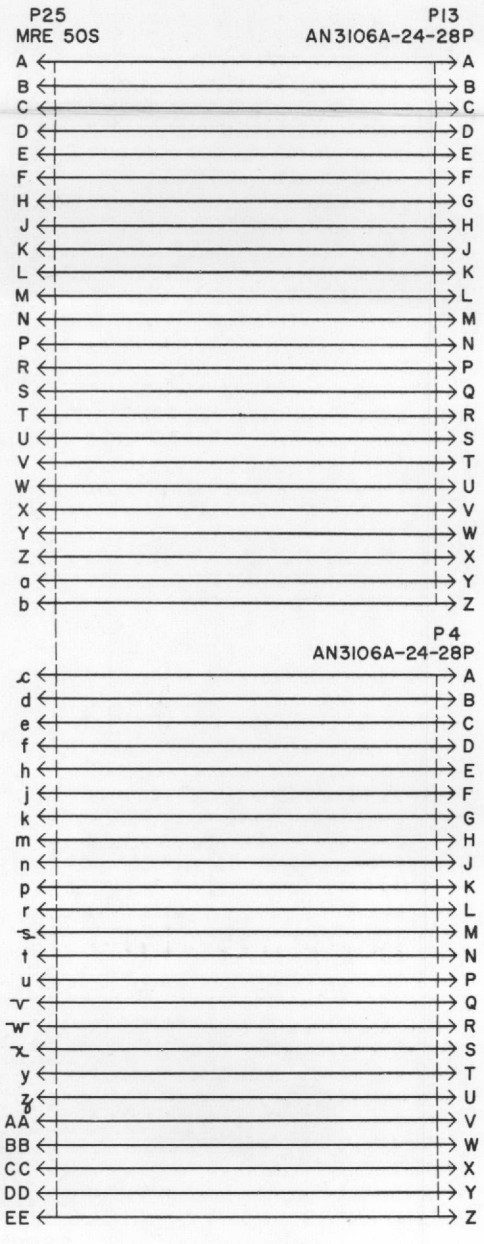

Figure A-9. Cable Wiring Diagram, R. M. S.




CABLE 5




CABLE 6




CABLE 7

Figure A-10. Cable Wiring Diagram, R. M. S.

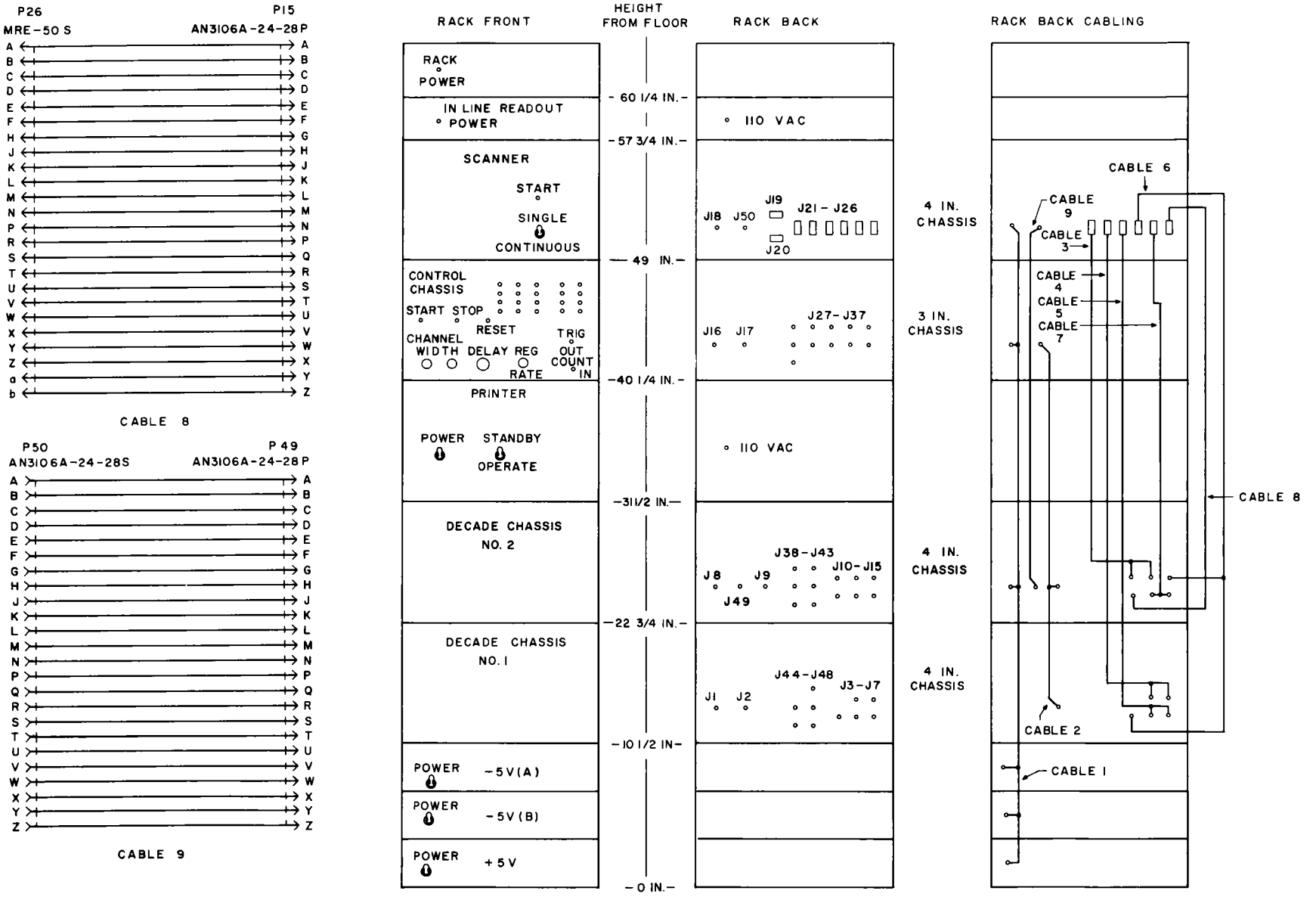



Figure A-11. Cable Wiring Diagram, RMS

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