ANALYSIS AND OPTIMIZATION OF GRAPHENE FET BASED NANOELECTRONIC INTEGRATED CIRCUITS

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In summary, the dissertation is to expected to aid the state of the art in following ways: 1) A non-EDA based tool has been used to characterize the device and measure the circuit performance. The results well matches to that obtained from the EDA tools. This tool becomes very handy for new device concepts when the simulation needs to be fast and accuracy can be tradeoff with. 2)Since an analog domain lacks well-design design paradigm, as compared to digital domain, this dissertation considers case study circuits to design the circuits and apply optimization. 3) Performance comparison of GNRFET based SRAM to the conventional silicon based SRAM shows that with maturation of the fabrication technology, graphene can be very useful for digital circuits as well.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION AND MOTIVATION

Silicon technology has undergone an unprecedented advancement in terms of device density, performance, productivity and cost. From the past three decades, the complementary metal-oxide-semiconductor (CMOS) has been scaled down by following the "constant field scaling" theory. The constant field scaling theory says that for the electric fields in the new scaled device to remain the same, the scaling has to be done by a factor of α (where $\alpha = \sqrt{2}$ for geometric scaling) to the device dimensions (W, L, t_{ox}) and to the device voltages (V_{dd} and V_{th}). Following this simple scaling theory, designers are able to increase the number of transistors per unit area from past few decades. However CMOS technology scaling in nanometer regime is accompanied by many serious problems [**77**, **79**, **80**]. Particularly beyond 10 nm, small-geometry effects like increase in the leakage currents, large threshold variations, gate losing control over channel, increase contact resistance are some of the many serious problems. With supply voltage V_{DD} approaching 1 V, it is difficult to lower the threshold voltage (V_{th}). As threshold voltage is proportional to the thermal voltage ($V_t = KT/q$), it is not possible to scale down the thermal voltage (K and q being constants) without having adverse effect in the device performance. It is from this point onwards, the scaling of threshold voltage becomes a problem. Also with the reduction in the threshold voltage, the sub-threshold leakage current increases exponentially. This leakage dominates the total leakage current in the future electronics. It is thus necessary to keep enough margin for V_{th} variation from reaching its minimum possible value so as to control this sub-threshold leakage. Also, for high performance logic technology, it is necessary to maintain the value of ($V_{DD} - V_{th}$) to a certain level [**64**]. Clearly, there is a trade off between performance (speed)and efficiency (leakage power) in the future electronics.

In order to reduce the short channel effect, various solutions have been proposed like use of high-κ materials to increase the electrostatic control over the channel, employing multi-gate structures to increase drive current for constant drive voltage, adopting high mobility channel materials to improve carrier mobility [**18**,**79**,**83**]. However all of these proposed options possess some

other serious challenges like mobility degradation, increment in band-to-band tunneling and gate induced drain leakage and threshold voltage fluctuation due to random dopants. All these factors severely affects reliability, performance, efficiency, yield and cost in CMOS at nanometer regime.

TABLE 1.1. Performance Metric for "End-of-the-roadmap" CMOS 2020 [**2**].

Device Parameters	Specific Values
Energy	10 aJ/operation
Power	10^7 W/cm^2
Speed	0.1 ps/op (10 THz, f_T = 100 GHz circuit)
Size	L_g = 5 nm, Cell = 100 nm
I_{DN}	3 mA/μm
Density	10^{10} cm^{-2}
Cost	10^{-12} dollar/gate
Bit Information Throughput (BIT)	100 Gbit/ns/cm^2

Table 1.1 shows the projected performance metrics for transistor at 10 nm node. Even though some requirements like transistor density and binary information though-put (BIT) can be achieved with multi-gate transistors and high mobility channels, other requirements like clock frequency of 100 GHz, energy requirement of 10 aJ/switching operation and power dissipation of 10^7 W/cm^2 are well beyond the capacity of current CMOS technology. Thus researchers are exploring the possibility of new device material (i.e. beyond silicon) and new device concepts (i.e. beyond CMOS). As an alternative to silicon, various materials like graphene, carbon nanotubes(CNT), memristor, compound semiconductors and free magnetic layers have been the key research in last few years [**18**, **44**, **45**, **77**, **78**, **83**]. Similarly, instead of designing devices based on conventional CMOS, researchers are trying to develop both charge based devices like ambipolar MOS devices, tunnel FETs [**116**], graphene PN junction, CNTFET [**11**, **121**] and non-charge based devices like nano-magnetic logic [**94**], spin wave [**91**], spin torque devices [**100**].

Since the first mechanical exfoliation of graphene, it has been considered as the most promising material beyond CMOS material. Apart from having some unique and excellent properties necessary for future electronics, there are some other advantages of graphene based electronics

like: abundant raw materials and thus can produce electronic devices at low cost, no need to go for entirely new fabrication process as they share more or less the same conventional method used in silicon technology. So this dissertation considers graphene as a future replacement for silicon.

1.1. Issues for Nanoscale MOSFETs

The issues for sub nanometer CMOS based electronics are categorized according to their region of problem [**64**, **77**].

(1) Channel:

There are a number of issues in channel for future nanoelectronics like:

(a) Sub-threshold leakage current and threshold voltage variation (V_{th}):

The sub-threshold leakage current is the diffusion current flowing between source and drain when $\mid V_{GS} \mid < \mid V_{th} \mid$ and is given by the relation [**64**]:

$$I_{sub-thres} = \mu C_{dep} \left(\frac{W}{L}\right) V_T^2 \left(\exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)\right) \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{1}$$

where μ is the carrier mobility, C_{dep} is the depletion region capacitance under gate, W and L are the effective transistor width and length respectively, V_{GS} is the gate voltage w.r.t source, V_{DS} is the drain voltage and n is the sub-threshold parameter, V_T (=$\frac{KT}{q}$) is the thermal voltage. K is Boltzmann constant, T is the operating temperature and q is the electron charge.

In order to keep the dynamic power consumption within a limit, it is necessary to scale down the supply voltage. Similarly, to maintain the drive current capability the threshold voltage also has to be scaled [**40**]. However with reduction in threshold voltage, the subthreshold leakage current increases exponentially as seen from equ. (1).

The sub-threshold swing (SS), as given by (2) [**64**], measures how fast the transistor can be turned off with decreasing gate voltage and it is preferred to have this value as small as possible.

(2) $$SS = \frac{\partial(log_{10} I_{sub-thres})}{\partial V_{GS}}$$

In short channel devices, due to increase in the drain voltage the depletion region advances significantly into the channel. This reduces the threshold voltage and the leakage current become significantly larger. This effect is commonly known as short channel effect (SCE). In order to prevent the depletion region from extending towards source, if higher doping level is used in the substrate then it increases the SS, band-to-band-tunneling and gate-induced drain leakage (GIDL).

Furthermore, at nanoscale MOSFETs, there exist a variation in the channel length among transistors even in the same die. This causes a variation in the V_{th} among transistors, which in turn affects the device speed and sub-threshold leakage. The transistor with lowest V_{th} has exponentially high sub-threshold leakage as compared with the transistor having higher V_{th}. It is therefore very important to maintain sufficient margin for V_{th} variation so that V_{th} of any transistor does not become the lowest possible V_{th}. Similarly, for a high performance logic technology, it is necessary to keep the $V_{DD} - V_{th}$ within a certain limit in order to maintain the drive current and the performance of the chip. This makes scaling of supply voltage (V_{DD}) extremely difficult for future electronics.

(b) Carrier mobility degradation:

The supply voltage has not been able to scale at the rate of device size scaling. This increases the electric field inside the MOSFET. For a low electric field, the drift velocity of the carrier is proportional to the longitudinal electric field across the channel. However at higher electric field, the drift velocity does not increases proportionally. This is known as velocity saturation and is the result of various scattering mechanisms like optical phonon scattering, phonon dispersion, phonon absorption and so on. It increases the transient time for carriers in the channel and also decreases the drain current as predicted by the mobility model.

(c) Hot carrier effects (HCEs):

Due to high electric fields, there are other problems like threshold voltage shifts and transconductance degradation which affect the device reliability. Once the carrier velocity starts saturating, the carrier can attain high kinetic energy. These hot carriers can migrate to unwanted areas like gate dielectric, gate or substrate of a transistor. They can also generate new electron-hole pairs by colliding with the silicon atoms resulting in impact ionization. The impact ionization can significantly increase the substrate current into the gate dielectric. These charges can also get trapped in the gate oxide which causes threshold voltage shift and may turn device unstable or even fail.

(d) Direct source to drain tunneling:

With channel length (or the barrier width) becoming so small in future electronic devices, the electrons can tunnel through the barrier even with a slight increase in the gate voltage. This limits MOSFET to operate as a switch.

(2) Gate:

As the transistor size is decreasing, high-k dielectrics are preferred over conventional SiO_2 in order to increase the gate capacitance and increase the drive current to improve the device performance. The high-k materials allow for equivalent oxide thickness (EOT) scaling. For future electronics, using conventional SiO_2 increases the leakage current due to tunneling effect and thereby increasing power consumption and reducing the reliability. Higher capacitance at the gate enables better control of electrons which speeds up the device as less voltage is needed to charge up the gate. However finding the suitable material is a challenging task. There are certain properties these materials need to possess like:

(a) Should be crystalline and remain thermodynamically stable even at very high temperature.

(b) Should have high bandgap and large conduction and valence band offset.

(c) Should be able to withstand large electric field.

(d) Should have large dielectric constant.

However the proposed high-k materials like Al_2O_3, HfO_2, ZrO_2, Y_2O_3, TiO_2 and Ta_2O_5 all have dielectric constant higher than silicon but lower bandgap as well as smaller conduction and valence band offset. This increases the leakage current problem for future electronics. Though the use of polycrystalline silicon as a gate electrode reduces the parasitic capacitance by having a tighter overlap between gate and drain/source region, however it increases the RC time delays and also decreases the driving capability of the transistor.

(3) Drain/source:

The main problem in the drain/source region is due to the parasitic capacitance and resistance. The effect of parasitic resistance during on-current increases as the device gets smaller. In order to suppress short channel effect, shallow source/drain junctions are desired but that in turns increases the sheet resistance as well as band-to-band-tunneling leakage current. Furthermore, with device scaling, the parasitic capacitance increases which limits the performance improvement for future electronics.

(4) Substrate (bulk):

Leakage current like reverse-biased junction leakage current (I_{res}) and gate-induced drain leakage current are the main concern for future electronics as the device scales down to nanometer range. Due to reverse biased pn junction, there is a leakage current flowing between the source and substrate, and between drain and substrate. For heavily doped source, drain and substrates, the band-to-band tunneling (BTBT) dominates due to high electric field at nano-scale electronics. This BTBT in turn increases due to shallow source and drain junction in future electronics. Furthermore with high electric field at narrower depletion layer under gate and drain region, a significant amount of surface BTBT current flows from drain to substrate.

1.2. Challenges for Graphene Based Electronics

Though graphene is considered as the most promising candidate to replace silicon in future electronics, it is still in its initial experimental stage. There are few challenges that has to sorted

out before it can be accepted in wide scale for future electronics. Some of these challenges in graphene fabrications are

(1) Substrate selection:

Since carriers are confined in a single layer, the graphene film is highly influenced by the surrounding environment and hence degrades the performance. Though the charge carrier mobility of 100,000 $cm^2/(Vs)$ is observed for suspended graphene where the substrate is etched way, for graphene with substrate the maximum mobility of 20,000 $cm^2/(Vs)$ has been demonstrated. Since substrate are necessary for proper heat dissipation, suitable choice of substrate should be wisely selected.

(2) Contact resistance:

Metallization in graphene should be done carefully in order to reduce the contact resistance. All the possible metal combinations like Cr/Au, Ti/Pt and Ti/Pd/Au give contact resistance in the order of 10^{-4} ohm/cm^2 [**90**]. Also since the graphene gets doped by the environment very easily, the metal on graphene can easily dope the underlying graphene. This limits the speed of graphene device by increasing RC time constant.

(3) Gate dielectric deposition:

Finding a suitable gate dielectric material is also very important for graphene processing. This can also possess problem in the speed of the graphene based devices.

(4) Bandgap engineering:

Unlike silicon which has a bandgap of 1.1eV, graphene is a zero bandgap semi-metal material. This restricts the ON/OFF current to around 10^{-15} and hence limits the application of graphene in digital logic. For graphene to be used in digital logic application, the ratio of ON current to OFF current should be in the range of 10^4 to 10^7. Various methods have been proposed to increase this ratio in graphene by creating suitable bandgap in graphene like:

(a) By using bilayer graphene, few hundred milli-electron volts of bandgap has already been created under the influence of perpendicular electric field [**89**].

(b) By quantum confinement (i.e. using graphene nanoribbon (GNR)), it has been pos-

sible to create a bandgap in graphene [**43**]. However the roughness in the edges and width variations significantly affect the electrical properties of GNR [**120**]. Furthermore the fabrication of GNR is also a challenging task at the moment.

(c) By applying different types of strains to a bilayer graphene so as to alter its electronic structure. Some of the strains induced bandgap engineering are by applying perpendicular strain to introduce electron-hole asymmentricity near K-points, applying lateral strain in the case of bilayer graphene to create an indirect bandgap [**114**].

1.3. Graphene as Material

Since its first discover in 2004, graphene has drawn a lot of attention due to its remarkable properties like super-strong (stronger than diamond) and stiffness, highly transparent, extremely light-weighted, excellent conductor of heat and electricity and some electronic properties that makes them suited for future electronics.

Due to its one atomic thickness, the graphene transistors offer very high packing density and extremely light weight. Also due to its single atom layer, photons can easily penetrate the layer in graphene as compared to other thick materials. This makes graphene highly transparent and is able to transmit about 89-98% of light compared to window glass, which can only transmit around 80-90% light incident on it.

The flat planes of carbon atoms in grahene can very easily bend and stretch (by around 20% of its initial length), without breaking apart the atoms. This gives graphene super-strength and elastic like property. Also the flat hexagonal lattice structure of graphene offers it very little resistance for electron to flow. This in turns allows for quick and easy electron movement across the graphene sheet. Since electrons are responsible for conducting both heat and electricity, low resistance in graphene makes it a better conductor of heat and electricity than copper, silver and diamond.

Electrons travel across graphene sheet with very less noise. This implies that when the electrons travel from one side of the sheet to another (like from source to drain across channel), they travel in a straight line. The carriers in graphene have large value of mean free path even at room temperature, which allows large number of electrons to travel across the sheet. Furthermore,

electrons in graphene travel more like a wave-like particle of light (i.e. phonons) at a speed close to the speed of the light. All these inherent properties in graphene suggest that graphene based devices can operate at small voltage with low heat dissipation.

The carbon atoms in graphene sheet is very closely tied up which can stop other materials like gases, water to get through. This increases the impermeability property in graphene.

1.4. Graphene Based Devices

From the past few years, graphene has been extensively studied both to replace MOS transistor and as a hybrid with conventional MOS transistors. With an aim to enhance future electronics, some of the most popular alternative graphene based technology to conventional CMOS are graphene field effect transistor (GFET), graphene nanoribbon FET (GNRFET), graphene nanoribbon tunnel FET (GNRTFET), graphene based spin FET and bilayer pseudospin FET (BiSFET).

When graphene sheets are rolled at specific and discrete angles (chiral) then a new structure, called carbon nanotube (CNT) is formed. CNTs are also getting lot of attention from both academics and industries due to their extraordinary mechanical, electrical, thermal, optical and chemical properties. However there are more challenges to implement CNT than graphene based FETs.

1.5. Graphene Based Circuits

Some of the unique properties of graphene such as high carrier mobility and saturation velocity, high stability and low noise make graphene a good candidate for high frequency electronic applications. Since the I_{on}/I_{off} ratio of graphene is very low, its application in digital circuits has been questionable but the results have suggested that using sophisticated technology, these GFETs can also be used for digital circuits. For example, dual-gate and bi-layer GFETs in [**122**] were measured to have an I_{on}/I_{off} ratio of 100. These GFETs have been used in all analog, digital as well as RF circuits such as inverters [**54**, **99**, **111**], frequency multipliers [**97**, **117**, **119**], an RF mixer [**118**], amplifiers [**53**, **125**], a photo detector [**82**], and low-noise amplifiers (LNAs) [**28**, **29**]. The concept of wafer scalable analog circuits was verified with an RF mixer example in [**72**]. Apart from these analogue, digital and RF applications, graphene is also considered crucial in

bioelectronics [**30**, **86**]. Due to its large surface-to-volume ratio, excellent electrical and optical properties, high thermal conductivity, carrier mobility and density, they are extremely useful in biosensors and diagnostics. Recent researches on DNA sensors, gas sensors, PH sensors, strain and pressure sensors, environmental contamination sensors have focused on implementing graphene based nanoelectronic devices.

1.6. Application of Graphene

The success of any new material and device concept depends on how widely it is accepted in different fields. Since silicon has been accepted as a universal fabricating material, its new replacement should also be universal, versatile and should have the ability to change different aspect of life. Graphene, due to its unique properties, has this ability to replace silicon for future electronics and can be used in many different applications from power management including energy storage to hybrid electronics including flexible electronics. Some of the applications of graphene are discussed below:

(1) Medicine:

Graphene has been found to be very useful in medical field like tissue engineering, bioimaging and polymerase chain reaction (PCR). Due to its mechanical properties like flexibility and compression ability, it is highly preferred in bone tissue engineering. Due to its non-toxicity at low concentration, they have been used as a drug delivery agent for treating cancerous cells [**106**]. Due to its high thermal conductivity, it has been used to increase the yield of DNA product in PCR [**95**].

Similarly, its unique chemical properties (i.e. modifiable chemistry), large optical range (from ultraviolet to near-infrared), electrical properties (i.e. gatable structure and atomic thickness) and electrochemical properties (i.e. ability to transfer electrons between enzyme and electrode surface) makes graphene very much preferable in biosensors. For examples, its high detection sensitivities and its effective fluorescence-quenching ability are preferred in making graphene based DNA detection devices. In [**76**], graphene was successfully fabricated in electronic devices such as microbial detection and diagnosis devices for detection of bacteria, protein, glucose, glutamate, cholesterol, hemoglobin,

DNA and many more. Its ultra-high surface area, excellent carrier mobility and high sensitivities can be explored for electrochemical sensing of glucose, DNA and proteins [**73**]. Also the graphene has been used as a drug delivery agent [**106**] and in the detection of diseases by observing the changes in graphene in the presence of certain diseases.

(2) Electronics:

Due to high carrier mobility and low noise, graphene can be used as a suitable channel in field effect transistor. On the application of perpendicular electrical field, graphene can be used as a field effect transistor and can be especially very useful for radiofrequency applications. Further exploiting its high mobility, graphene can be used as detector allowing ultrahigh band frequency selectivity from tera hertz to infra-red range. Graphene can be installed on any materials like plastic or any other substrate and this allows to build flexible and wearable electronic gazeds. Unlike CMOS based electronics which requires both n-type and p-type semiconductors, a single graphene transistors can perform both type of functions. This helps to reduce the device size, power consumption and cost, at the same time improving the device speed. Graphene's high electrical conductivity, mechanical strength and flexibility, and high optical transparency can be used in touch screens, liquid crystal displays (LCDs), organic photo-voltaic cells and organic light emitting diodes (LEDs). Due to its strong interactions with photons, graphene is a promising elements for optoelectronics and nano-photonic devices. By tuning the Fermi level, the optical absorption range of graphene can be changed which in turns gives broad bandwidth for optical modulation. Similarly, it can be used as an infrared detection device due to its response to infrared spectrum producing very little heat, thus minimizing the need of sophisticated cooling mechanisms.

(3) Energy and Storage:

Graphene can also be used in energy related areas like photovoltaic devices as in solar cells, supercapacitors and lithium-ion batteries. The use of graphene in such areas can make these devices very cheap, flexible, lightweight and highly efficient as these are the major issues with present technology in these aspects.

High carrier mobility, optical transparency and excellent electron transport properties of graphene are very advantageous in solar cell. Graphene's high transparency, extremely good conductivity property and an ideal 2D material makes them very suitable to assemble into film electrode in solar cells. Similarly, graphene in conjugated polymers can be used to improve the charge transport properties of the material for photo-voltaic devices. Furthermore, the ability of graphene to generate multiple current driving electrons for each absorbed photon increases the conversion efficiency by compared to the silicon based solar cells. Similarly, its high surface area and ballistic transport properties makes them very suitable to be used catalyst for fuel cells.

Graphene also has the potential to improve the energy storage, charging/discharging life and charging rate in rechargeable lithium ion batteries. This in turn can prolong battery life in electronic devices like cell phone, laptops, cameras and so on and reduces the charging time as well. Similarly, graphene films can be used as a protective layers against corrosion in battery cases.

Due to stable chemical properties, high surface-to-area ratio and high electrical conductivity, graphene is an ideal material for super-capacitor applications. Such super-capacitors can store more energy per unit volume/mass and are particularly useful in applications which requires rapid charge/discharge cycles [**21**].

(4) Sensors:

Some of the properties like large surface-to-volume ratio, large optical range, high electrical and thermal conductivity, high carrier mobility and density makes graphene as a natural selection for sensor applications. These properties not only makes graphene based sensors to be very fast, smaller, lighter, flexible and transparent but also allows sensors to have high response and recovery time. For example, Bosch's magnetic sensors, based on Hall effect, were found to be 100 times more sensitive than the equivalent silicon based sensors [**8**]. Furthermore, the small bandgap in graphene makes it very easy to conduct electrons between biomolecules and the electron surface. Similarly, in [**19**] graphene based wearable sensors were demonstrated in order to monitor human bodily

motion. Sensors for such application needs to be cheap, light weighted, mechanically compatible and should have sensitivity for all types of strains and graphene demonstrates all such properties. Due to its extreme sensitivity, graphene shows change in its electrical conductivity when even a single gas molecule is absorbed on its surface and this property is very useful in gas sensors [**55**]. As the carrier density in graphene can be very easily modified by applying electric field, this property is very beneficial for electric field sensors [**55**]. Similarly ambipolar property in graphene can be explored in pH detector. The Dirac point in the GFET moves towards positive direction with the increase in pH value. This can be used to detect pH value exploring the electrical characteristic of GFET [**88**]. Other type of sensors where graphene are equally applicable are environmental contamination sensors, strain and pressure sensors, humidity sensors, photo-detectors, electric and magnetic field sensors, mechanical sensors and so on .

(5) Environmental Protection and Detection:

High surface area, good absorption capacity, excellent conductivity and optical properties of graphene are very useful for detection, removal and degradation of pollutants in environment. For example, heavy metals like lead, cadmium, chromium, mercury, copper and arsenics are considered to be very harmful for human and environment. Graphene can be employed to remove such heavy metals from soil and water [**73**]. Graphene and its modified forms can absorb such heavy metal ions and form complexes with metal ions, which can then be recycled. Similarly, graphene can be used to remove radioactive nuclides from water and the graphene based filters have been found to be very effective in desalination by significant margin. Graphene also act as a very good coating in windows to block radio-waves while being transparent to visible light.

(6) Waterproof Coating and coolant:

Graphene can also be used to make either water super-absorbent or super-repellent. This water super-repellent property can be used to make devices waterproof. Similarly, its high thermal conductivity can be used to make graphene as a suitable coolant. For example, copper-graphene or indium-graphene can be better suited to cool down the devices

than the pure copper due to their high thermal conductivity. This reduces the cooling devices cost in future electronics as well as increases the reliability of the devices.

1.7. Motivation for this Research

It is expected that by 2026, silicon will reach its fundamental limits and it will not be possible to scale the technology further down. So as an alternative to silicon, in both digital logic circuits and in radio frequency applications, many device concepts like carbon nanotube, graphene, nanowires and so on are continuously been explored by both academics and industries. Recently, carbon nanotubes (CNTs) and graphene has drawn lots of attention due to its extraordinary properties like high carrier mobility, extremely high thermal conductivity, high Fermi velocity, ambipolar property and so on. Though CNTs and graphene shares many similar properties, they have some differences as well. Apart from the fact that CNT is 1D and graphene is 2D structure, it is shown that there is a presence of bandgap in semi-conducting CNT. However the main problem associated with CNT is due to their different chiralities, it is very difficult to have a well defined starting material for CNT based technology. However in graphene, due to their planar geometry, already well established techniques of silicon can be used for graphene technology.

The biggest problem with graphene though is the difficulty to make it. Peeling off a tiny sheet at a time with sticky tape is not really scalable. Though a very thin layer of graphene sheet can be developed by hitting up a sheet of hydrocarbons like methane until the hydrogen get separated and leaving behind the carbon, the quality of graphene will be very low. So, it is difficult to create one atom thick layer and that too with complete purity. For future electronics, both of these requirements need to be met simultaneously. However it does not mean that graphene has no future. The silicon industry faced the same purity problem fifty years back but the problem has been managed eventually with time. So, it is very likely that today's problem for graphene can be easily solved in future with more research and study. Furthermore, when there is a search of a new device concept and technology for future electronics, it is a very right time to focus on the possible implementation of graphene in some of the electronic devices. So this dissertation takes one step towards exploring graphene for future electronics.

1.8. Organization of this Dissertation

The rest of the dissertation is organized as follows.

Chapter 2 reviews some of the peculiar properties of graphene as a material which gives new heights to future electronics. Some of the graphene derivatives device concepts are explored in the same chapter, followed by some of the graphene based circuits that have been studied till far in the literature. Novel contribution of this dissertation is covered at the end of that chapter.

Chapter 3 covers the Verilog-A based modeling and analysis of graphene. The chapter begins with the importance of Verilog-A model for future electronic designs, followed by the device structure of graphene field effect transistor (GFET). Device level modeling of GFET is discussed then. As a case study, cross-coupled version of LC-VCO is considered. Experimental results are given at the end of the chapter.

Chapter 4 covers the non-EDA, i.e. Simscape®, based modeling and analysis of graphene circuits. First the importance of Simscape® as a simulation tool for new device concept like graphene is discussed, followed by comparison with conventional EDA tools. Simscape® based modeling and simulation flow is then discussed. The experimental results obtained from Simscape based GFET model is compared with that obtained from the conventional EDA tools. This is followed by two case study circuits: low noise amplifier (LNA) and cross coupled version of LC oscillator, both modeled in Simscape, are discussed along with the experimental results.

Chapter 5 covers the optimization for Graphene based circuits. The first section highlights the importance of optimization which is then followed by the design flow proposed for the cross coupled version of LC-VCO. As an optimization algorithm, multi swarm optimization (which is an improved version of particle swarm optimization) is discussed. The results of the optimized circuit is then given at the end of the chapter.

Chapter 6 compares the performance of graphene based digital circuit to the silicon transistor based circuit taking static random access memory (SRAM) as a case study. Graphene being a semimetal, it as zero bandgap. This leads to a small ON-OFF current ratio, leading to a very poor performance in terms of power consumption. Thus to meet this key requirement in digital circuits, graphene nanoribbon fied effect transistor (GNRFET) is considered in the chapter. GNRFET have

a bandgap and is more suitable to the digital circuit design.

Chapter 7 provides the conclusion and the direction for future research.

CHAPTER 2

GRAPHENE NANO-ELECTRONICS: AN OVERVIEW

In this 21^{st} century, the electronic devices in the form of electronic products such as smart mobile phones, laptops, tablets, and media players have profound effect on the society. Today's world has witnessed an unprecedented and unforeseen changes in the electronic technology. The easiest way of tracking this technological revolution is by measuring the speed, size and cost of the electronic devices. From this perspective, today's electronics devices are "nano" in terms of size and cost; yet very powerful and computationally intensive. Faster, cheaper and smaller electronics are more than a slogan for both electronic driven society and industries. With transistor count already reaching billions in a chip, it is becoming extremely challenging to shrink the transistor further down, particularly at 10 nm and below. Relentless demand for smaller, faster, cheaper and lower power consumption electronic products have forced designers to explore in depth two possible options:

(1) Combine analogue, digital, mixed-signal, memory, radio frequency (RF) and software components into a single chip, leading to analog mixed signal systems on chip (AMS-SoC) [**41**, **77**].

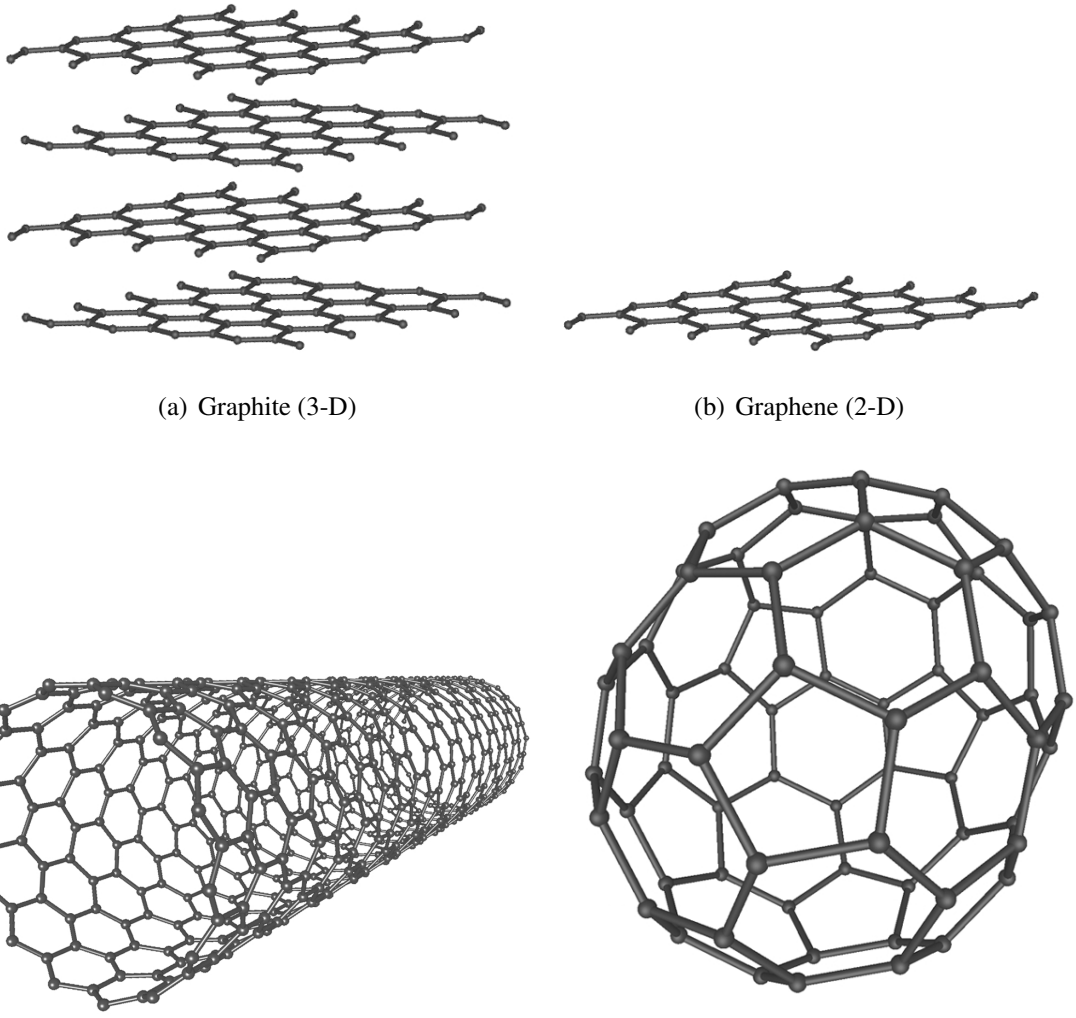
(2) Search for alternative technologies which can replace silicon to meet future demand.

The former option necessitates a fusion of two design domains, namely analog and digital so that the energy and performance trade-offs can be done [**41**, **77**] while the latter demands alternative material to silicon so as to achieve more flexibility in the design in terms of speed, size.

2.1. Graphene as a Material

Carbon is a non-metallic elements and the sixth most abundant element in the universe. Some of the most common allotropes of carbon are diamond and graphite (3-D), graphene (2-D), carbon nanotube (1-D) and fullerene (0-D), as shown in Fig. 2.1 [**23**].

Graphite is a crystalline form of carbon in which each atom is only bonded to three other carbon atoms. These atoms form a two-dimensional sheet of hexagons in which each atom has one unpaired electron left over. These electrons fly across the matrix of atoms when an electric current



(a) Graphite (3-D)

(b) Graphene (2-D)

(c) Carbon nanotube (1-D)

(d) Fullerene (0-D)

FIGURE 2.1. Various allotropes of carbon. [Source: Wikipedia through Wikimedia Commons licence for free to use].

is applied, allowing it to readily conduct electricity. Graphite natural form consists of layers of sheets and if a voltage is applied to it, those free electrons have lot of different directions to go in.

A single layer of graphite is called graphene. Graphene is a repeating hexagonal arrangement of carbon atom. The layer is so thin, just one atom thick, that it is considered as 2-D structure. By taking a single layer of graphite, an electron super highway can be created i.e. a flat matrix of carbon atoms where current can fly across. These sheets of carbon are pretty easy to separate because they are not molecularly bonded to each other. Instead they are held together by Van Der

Waals bonds (a kind of weak, electrostatic bond) which makes graphite so soft. A graphene layer of one atomic layer thick can be extracted from a slab of graphite by sticky tape. Because of its extremely good conductive properties, it has a very high probability of replacing silicon in microchips. Not only electrons move faster across graphene but they are also subjected to less noise which implies that the electrons can move from one side of the sheet to the other in a straight line without detouring around the whole lot of atomic potholes.

The Fig. (2.2) shows the full band graphene structure [**103**]. The two bands (i.e. valence band and conduction band) in graphene touch each other at 2 points (k and k′). These points are called Dirac points or neutrality points where the effective carrier density is zero and are independent of each other. Since the bands touch at Dirac points, graphene has zero bandgap. As the band structures are symmetric around these Dirac points, the electrons and holes have same properties in pure graphene. The nature of the doping (i.e. either p-type or n-type) and transport carrier (i.e. either electrons are the major carrier or holes are the major carrier) are determined by the position of Fermi level in graphene as shown in Fig. (2.3) [**12**].

At low energies, the bands in graphene have a linear energy dispersion instead of quadratic energy dispersion in semiconductors. This implies that the speed of the electrons is constant and independent of the momentum and the electrons in graphene behave as zero effective mass. Unlike other 2D systems with parabolic dispersion, the density of state (DOS) in graphene increase linearly with the energy and it vanishes at Fermi energy. Therefore, graphene is also termed as zero-gap semiconductor with vanishing DOS at the Fermi energy [**92**].

The carrier mobility in graphene shows an inverse relation with the carrier density i.e. as the carrier density increases, the mobility decreases. The mobility of carrier also depends on the supporting material and the defects in the graphene itself. In suspended graphene where there is no interaction with the substrate the mobilities as high as around 200,000 $cm^2V^{-1}s^{-1}$ has been observed [**90**]. Graphene on insulators like SiO_2 shows much decrease in the mobility and is found to be around 1,000 - 10,000 $cm^2V^{-1}s^{-1}$ depending on the nature and purity of the underlying insulator substrate. Epitaxial and chemical vapor deposition (CVD) grown graphene shows the carrier mobility in the order of 1,000 $cm^2V^{-1}s^{-1}$ [**12**].

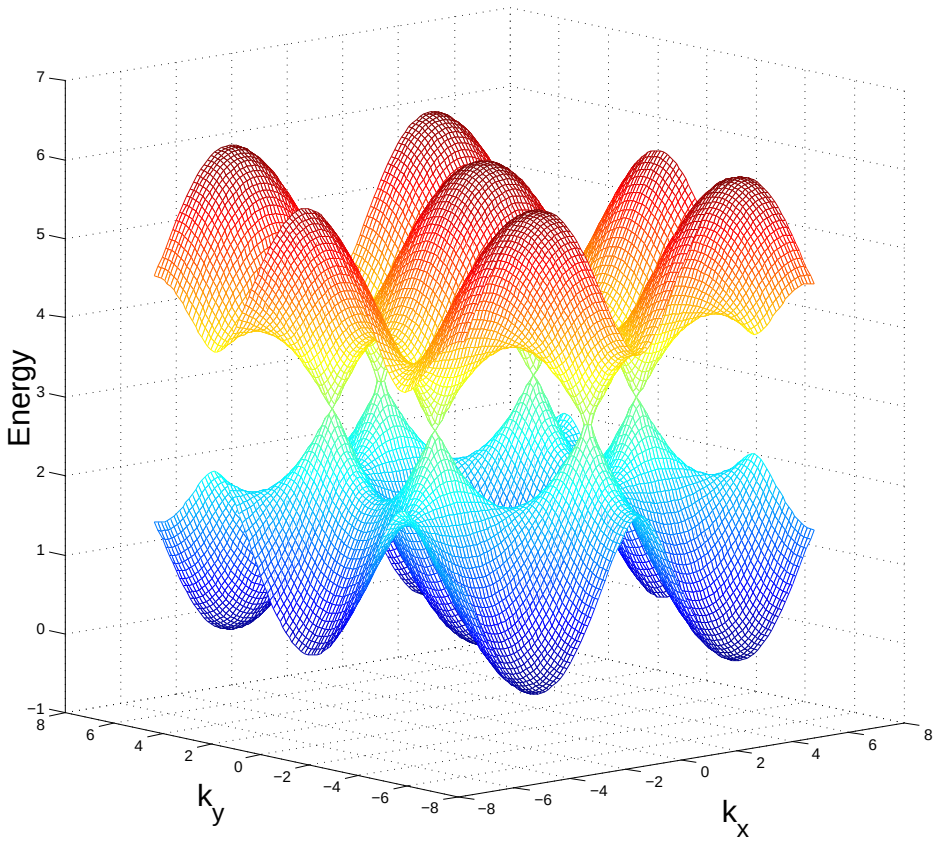


FIGURE 2.2. Electronic Dispersion in Graphene. After [**103**].

The transport of carrier in the graphene channel is controlled by the gate. When the negative gate voltage is applied, the Fermi level raises up and for positively biased gate voltage, the Fermi level falls down. When the gate voltage V_g is less than V_{Dirac} then the transport in graphene is due to holes while for V_g greater than V_{Dirac}, the transport in graphene is due to electrons. Thus the gate voltage changes with Fermi energy, DOS and the carrier density. However even when the DOS =0 at Dirac energy (E_{Dirac}), the graphene is not turned off completely.

The sheet resistivity of graphene is maximum at the Dirac point and thereafter decays on both sides with change in the gate voltage as shown in the fig. (2.4) [**65**]. The location of the Dirac point depends on the work function difference between the gate electrode and the graphene, doping and the underlying substrate where the graphene is formed. For the pure graphene, this Dirac point is located near zero gate voltage. Similarly the symmetricity of the curve also depends on the charge impurities and the graphene-electrode contacts. The asymmetric curve leads to different in

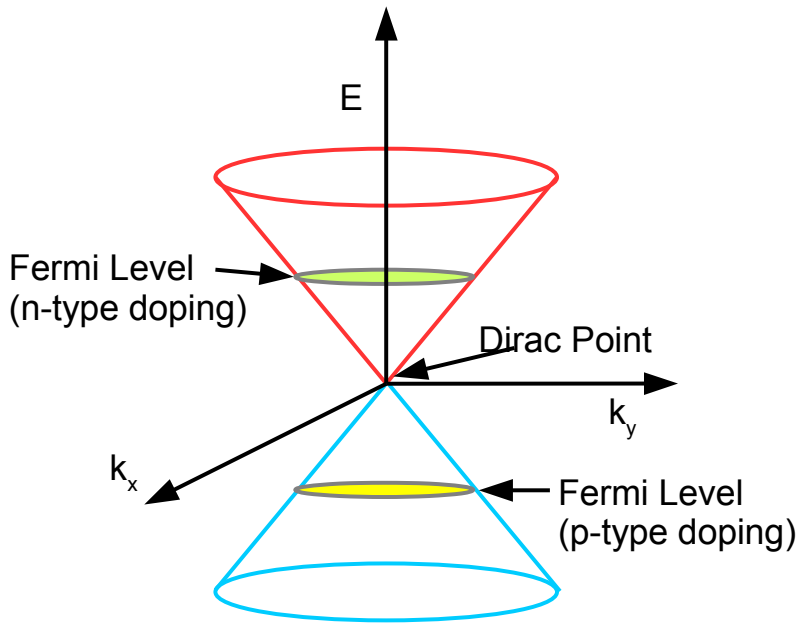


FIGURE 2.3. At low energy, bandstructure as two cones touches at the Dirac point, where Fermi level determines the nature of the doping and the transport carrier. After [**12**].

electrons and holes mobility [**103**].

Similarly as a channel material, graphene displays self-doping property. This implies that it does not require any impurity to conduct electricity. Self-doping implies the electric field effect and it allows the charge carrier type and concentration to be controlled by external electric field or by the gate voltage. This eliminates the need for doping in graphene and hence eliminates the problem of variation that is introduced during doping.

The ambipolar property in graphene allows graphene transistor to operate with either p-type carrier (i.e. holes) or n-type carrier (i.e. electrons) or both simultaneously. Thus simply by changing the Fermi level, the conduction can shift from electrons to holes.

Some of the properties of graphene that makes them suitable material for future electronics are as follows:

(1) Mechanical Property:

Due to the strong bonds between carbon atoms, it is extremely difficult to break through the sheet of graphene and even the patches of graphene stitched together remains

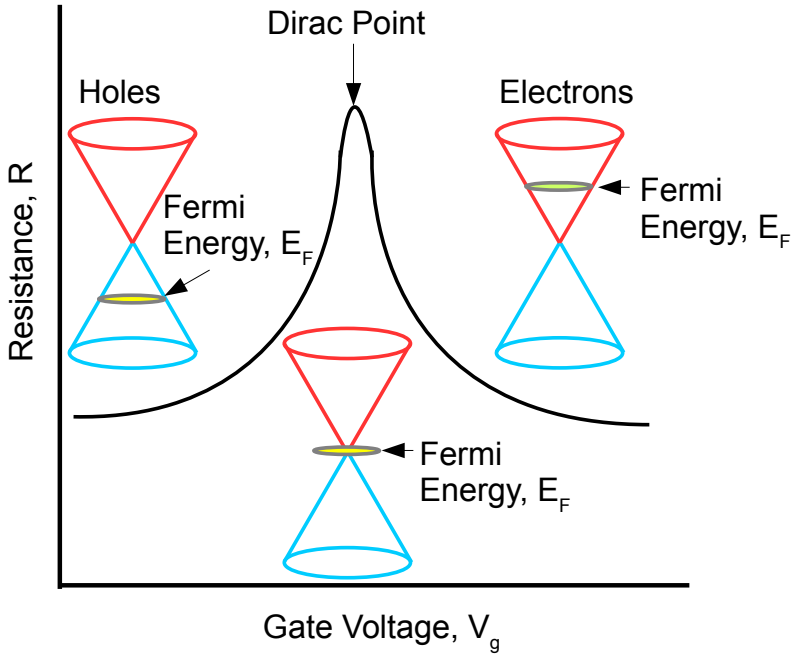


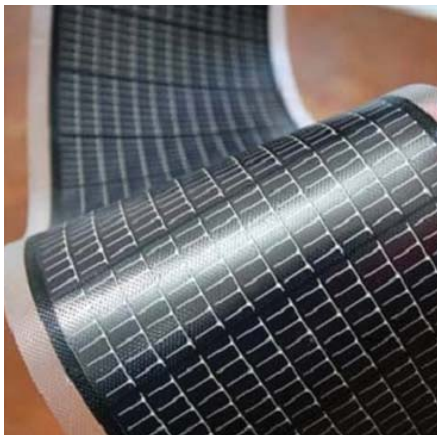
FIGURE 2.4. Transfer Curve showing graphene resistance as a function of gate voltage. After [**65**].

very strong. Furthermore, the bonds are very flexible which enables them to be twisted, pulled and curved to a large extend without breaking. These property enable graphene to be used as wearable devices. Graphene shows extraordinary stiffness. For a few layer of graphene with thickness less than 8 nm, a spring constant of 1-5 N/m and a Youngs modulus of 0.5 TPa was observed in [**93**]. For a monolayer graphene, the second and third order elastic stiffness was found to be 340 and 690 N/m respectively, with a breaking strength of 42 N/m. This corresponds to the Youngs modulus of 1.0 TPa and the intrinsic strength of 130 GPa. These figures suggest that the suspended graphene can support significant extra load like copper nano-particles and can protect the device from accidental shock and mishandling.

(2) Electronic Property:

All few layers of graphene (like mono layer, bilayer and tri-layer) are good conductors [**115**]. Beyond three layers of graphene, the properties resembles the graphite. However upon applied by perpendicular electric field, these few layers of graphene show different nature of electronic band structure [**102**]. For example, in monolayer graphene the gate

(a) Strength



(b) Lightweight

(c) Flexibility

(d) Transparent

(e) Wearable

FIGURE 2.5. Future Electronic due to graphene

voltage modulates the current but it cannot be switched off due to the absence of bandgap. In the case of bilayer graphene, the bandgap can be created by an application of external perpendicular electric field and it is the only gate tunable graphene semiconductor. In the case of trilayer graphene, with the application of external gate , the conduction band and

the valence band overlap each other thereby acting as a semi-metal [**102**].

Furthermore, by using the dual gate configuration , it is possible to independently tune the electronic bandgap and carrier doping concentration in graphene. A monolayer graphene is a zero bandgap semiconductor which shows the linear band structure around the Fermi energy. The bilayer graphene is a semi-metal like material which shows parabolic band structure around the Fermi energy and a band overlap of 0.16 meV, while the graphite also shows semi-metal like behavior but with a band overlap of 41 meV [**115**].

(3) Optical Property:

In [**85**], it has been shown that the opacity of suspended graphene depends only on the fine structure constant, α = e^2/(hc) = 1/137, which describes the coupling between the light and relativistic electrons. It has been shown that the light opacity values for monolayer and bilayer graphene is around 2.3% and 4.6% respectively in the visible light range of 450 nm -750 nm [**115**]. With increase in the number of layers, up to five layers, the opacity value increase linearly. This very low opacity value for graphene is due to the relativistic massless Dirac Fermion behavior of electrons and holes in graphene.

(4) Thermal Property:

In [**13**], the thermal conductivity of suspended monolayer graphene near room temperature was recorded to be 5300 W/(mk) with a mean free path of 750 nm for phonon. With the increase in the number of layers, the value decreases down. This observed value is higher than the CNT ($\sim$ 3000 W/(mk) for multi-walled CNTs and $\sim$ 3500 W/(mk) for single walled CNTs) and diamond ($\sim$ 1000 - 2200 W/(mk)) [**115**]. This high value of thermal conductivity of graphene can make it extremely good material in thermal management and also allows graphene to integrate with Silicon CMOS technology. For future electronics devices where size will play very crucial role, it allows the necessity of sophisticated cooling mechanism and enhance the device life span.

(5) Other exciting properties of graphene are as follows:

(a) Excellent carrier mobility,

(b) High carrier saturation velocity,

(c) High Fermi velocity,

(d) High current density,

(e) Extremely thin due to one atomic thick,

(f) Highly stable and less noisy,

(g) High carrier mean free path (about 400 nm @ room temperature)

2.2. Graphene Based Devices

There are many possible alternative transistors that can be designed using graphene for future electronics. All of these novel concepts have drawn attention due to their individual advantages and at this time it is very difficult to predict which one will win the race.

(1) Graphene Spin FET:

Spintronics is the study of intrinsic spin of the electrons. The magnetic moment of the electrons can be used to represent, compute and transmit information in more efficient way than the electron charge [**84**]. The electronic circuits build on spintronic concepts are advantageous due to their higher storage capacity, higher processing power and lower heat dissipation as compared to those circuits build on classical electronics concepts. For example, by adding more states for logic bits, it is possible to increase the storage capacities and processing power in computers and other data processing applications. Similarly, the new compounds (like graphene) used in such devices enable electrons to flow without energy loss which in turn reduces heat dissipation.

The structure of spinFET as proposed by [**31**] is similar to metal oxide semiconductor field effect transistor (MOSFET) with a major difference of source and drain being ferromagnetic metals. The magnetization in these metals are aligned parallel to each other. The spin-polarized carriers are injected from the source and are collected at the drain side. When traveling from source to the drain side, these carriers precess due to Rashba Effect and reach the drain side with different polarization state. The polarization angle (ϕ) of the carriers with respect to drain depends on the number of factors like length of the channel, rate of the precession and transverse electric field in the channel, which can be controlled by the gate voltage. Due to this difference in polarization angle of the carriers with respect

to the drain, there is a difference in the net current, which can be modulated by the gate voltage.

As shown in the Fig. (2.6-a), when V_g is greater than zero, then the precession of the electrons is controlled by the electric field which makes it possible to reach the drain side with the same polarization hence the net current is increased. When V_g is made zero, as shown in the Fig. (2.6-b), then the electrons injected into the channel start precessing and then they reach the drain side its orientation is different to that at the drain side thereby decreasing the net current. Thus gate acts as a switch to control the flow of current in the channel just like in conventional MOSFET. In spintronics, the spins are manipulated by both magnetic and electrical fields.

However, the spin-based devices need to satisfy some parameters like the follow [**84**]:

(a) A need for proper spin carrier injection and detection mechanism in order to have low read and write current,

(b) A need of proper spin modulation mechanism, and

(c) A need for very high spin transit time (or de-coherence time) so that the spin polarized electron can travel a long distance without any loss in encoded information.

Graphene is an attractive material for spin based electronics due to the following reasons:

(a) Large spin coherence length,

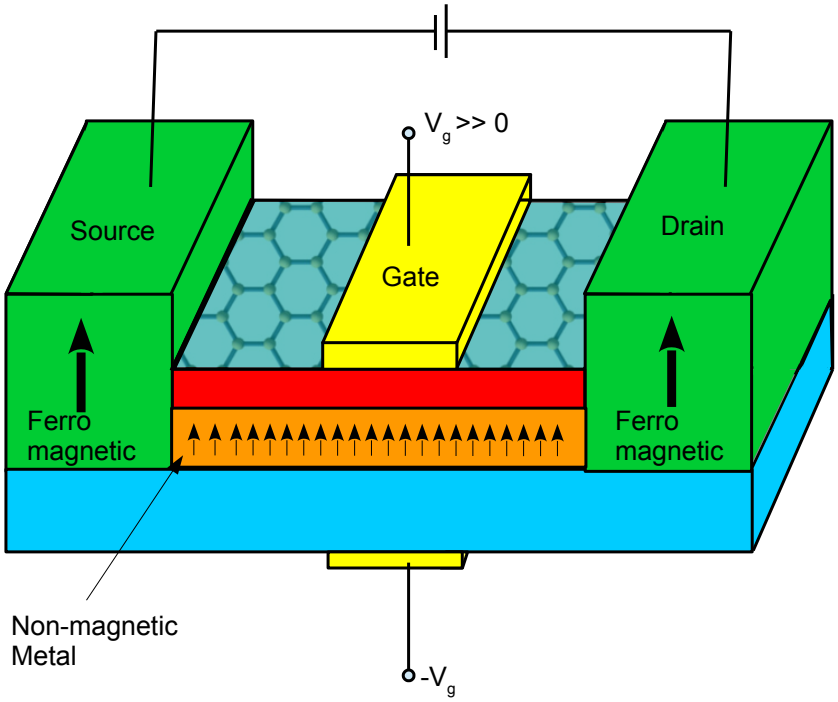
(b) Zero nuclear spin,

(c) Reduced spin scattering, and

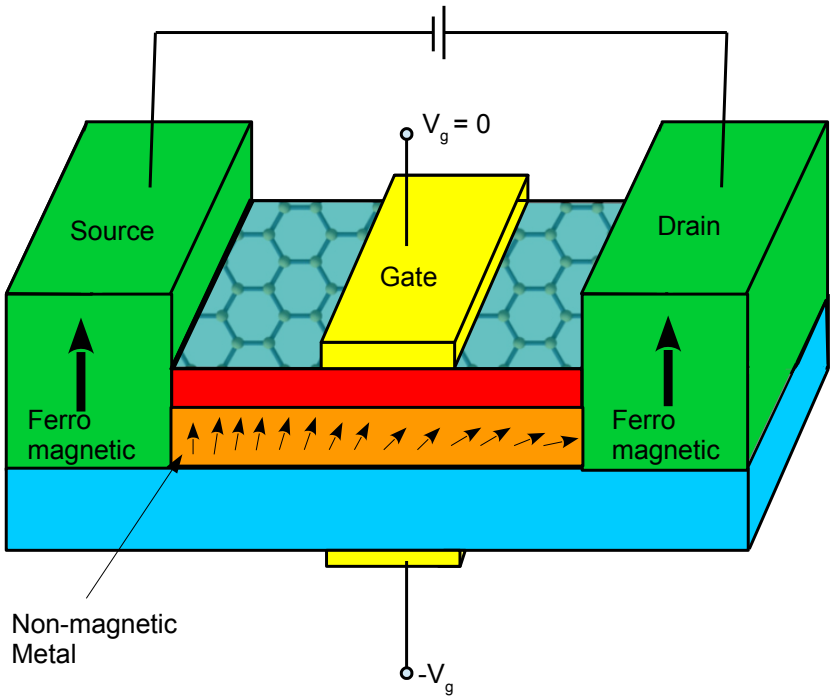
(d) Better spin tunnel junction contacts thus providing a path for high spin polarization injection

Since it is difficult to modulate spin information in graphene due to weak spin orbit interaction, it is still possible to enable spin modulation through spin-splitting of bands and gate modulation [**84**]. In graphene based spin FET, graphene (either single layer or multi-layer) is used as a channel between two ferromagnetic contact.

(2) Bilayer pseudo spin field effect transistor (BiSFET):



(a) Spin Control when $V_g \gg 0$



(b) Spin Precessing when $V_g = 0$

FIGURE 2.6. Graphene based SpinFET. After [**3**].

Bilayer pseudo spin field effect transsitor (BiSFET) has the potential to be ultra-low power replacement of metal oxide semiconductor field effect transistor (MOSFET) [**14**]. The switching energy per device with BiSFET can be on the scale of 10 zJ (i.e. 10^{-21} J), which is two order of magnitude below CMOS transistors [**98**].

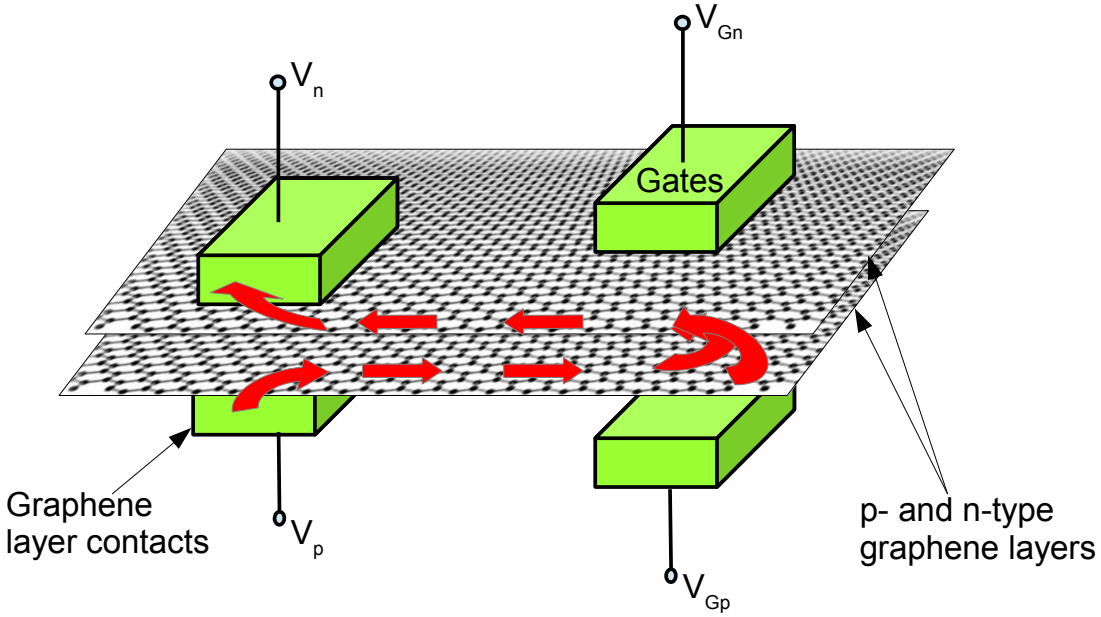


FIGURE 2.7. Bilayer pseudo spin field effect transsitor (BiSFET) Structure. After [**98**].

As shown in the fig. (2.7), BiSFET consists of two layers of graphene, one n-type and another p-type, which are separated by a thin insulating dielectric. The device concept is based on the possibility of super-fluid condensation of excitons (i.e. bounded electron-hole) in two graphene layers above room temperature and thus enhancing the interlayer tunneling [**98**]. Under certain condition, electrons from one layer can form a pair with holes from opposite layer and this will create a bounded electron-hole pair, known as excitons. When these excitons condensate, they effectively shorts the two layers, which in turns reduces the tunnel resistance [**15**]. There is a debate whether or not such super-fluid condensation can exist at the room temperature. However if it exists then it can take future electronics to a new height.

Such interlayer superfluid condensation has been seen in high magnetic field at low

temperature for group III-V elements systems but it is suggested that in graphene such condition can exist even at the room temperature, due to its properties like [**98**]:

(a) Due to one atomic layer thickness, graphene can be placed very close to maximize interlayer Coulomb interaction.

(b) Symmetric electron-hole band structure over energy range of interest,

(c) Zero bandgap such that all interlayer electrostatic potential difference can induce electron hole pair,

(d) Low density of states which gives high Fermi energy at Dirac points for relatively low carrier density.

The gate voltages V_{Gn} and V_{Gp} are used to create super-fluid between gates and allow imbalance of charge distribution to weaken the superfluidity. The interlayer voltages V_n and V_p are used to control the tunneling conductance, which becomes large at small interlayer bias ($V_n - V_p$) and vice versa [**15**].

(3) Graphene Nanoribbon Field Effect Transistor (GNRFET):

Graphene based circuits can achieve lower energy-delay product (EDP) as compared to silicon based CMOS which results them to be used as low power future electronics as these transistors work with V_{DD} = 0.5 V as compared to 0.7 V or 0.9 V in Si CMOS. Since 2-D graphene is a zero-band gap material, it makes them excellent conductor rather than semiconductor. To open bandgap and make them behave as a semiconductor, so as to use in digital logic application, 2-D graphene structure can be converted into 1-D narrow strips of graphene ribbons known as graphene nanoribbons (GNRs) [**25**]. Since the bandgap in GNR is inversely proportional to the nanoribbon width, for nanoribbon width less than 2 nm, GNR shows excellent semiconductor properties and GNRFET shows high I_{on}/I_{off} ratio and low subthreshold swing [**38**]. However, the performance of these novel devices is greatly affected by the variation of the ribbon width, edge roughness of the ribbon and missing atoms in the edges. The width of the ribbon is generally defined as the number of dimer lines as shown in the Fig. (2.8).

Due to ballistic transport in GNRFET as compared to drift-diffusion transport in Si,

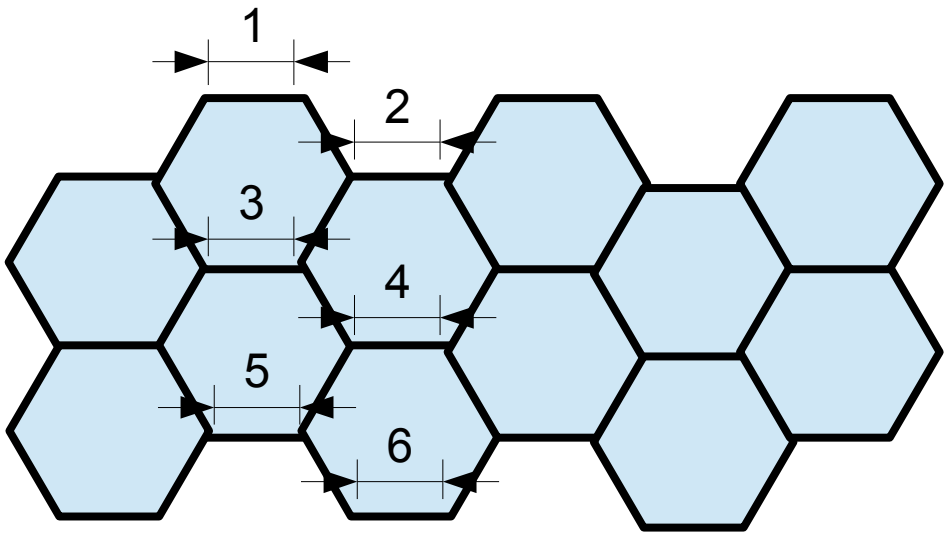
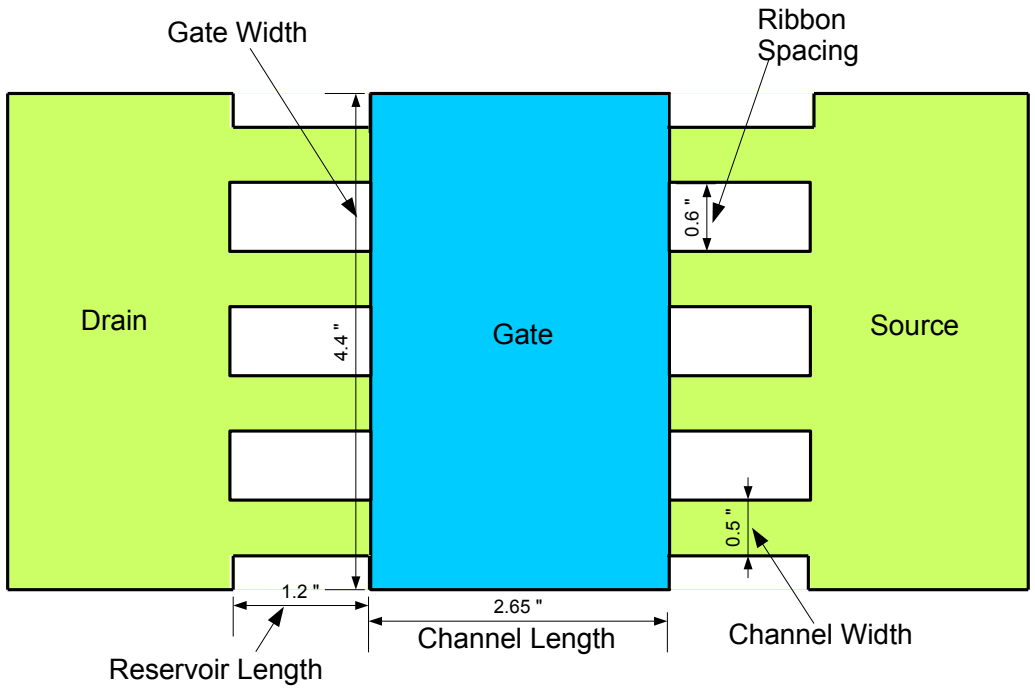


FIGURE 2.8. Graphene width defined in terms of dimer

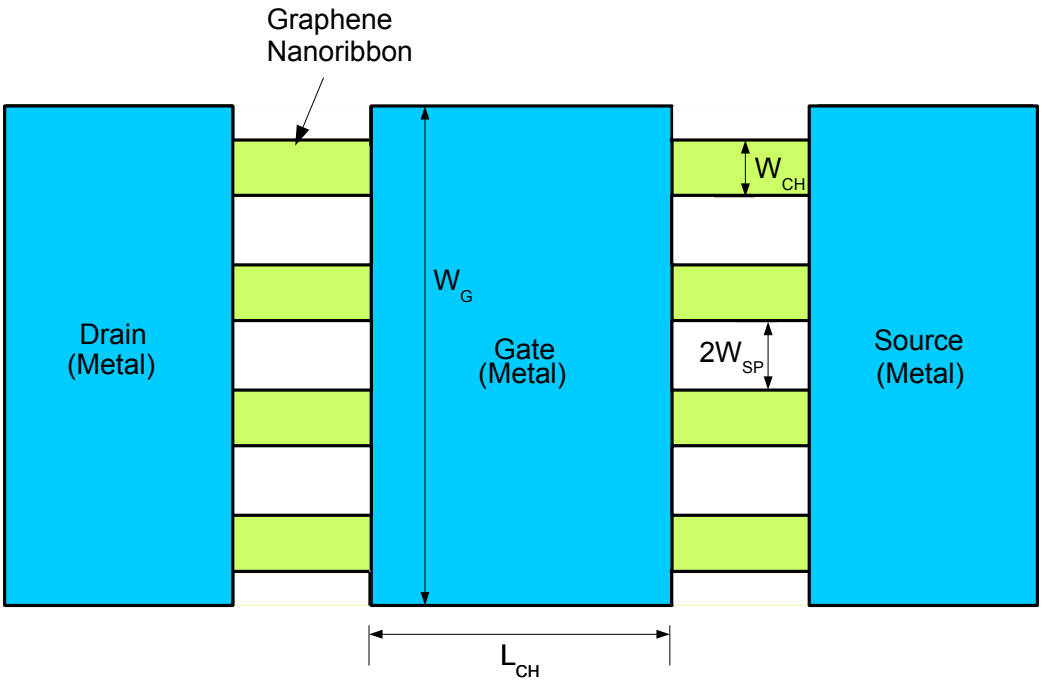
the mean free path is much larger in GNRFET than in Si. In GNRFET, the current flow through a narrow ribbon as compared to large surface area. This, on one hand, reduces the load capacitance in GNRFET which thereby reduces the dynamic power and in the other hand due to ballistic transport more current are injected through GNRFET. Based on the edge geometry, GNRs are classified into mainly two types: armchair-GNR and zigzag-GNR. Armchair GNRs are predominantly semiconducting whereas zigzag GNR demonstrate metallic properties [**24**]. However bandgap can be created in zigzag with either rough edge or by passivating the edges with hydrogen atoms. There are mainly two types of GNRFETs: Metal-Oxide Semiconductor-(MOS-)type GNRFETs (MOS-GNRFETs) and Schottky-Barrier-type GNRFETs (SB-GNRFETs).

(a) Metal-Oxide Semiconductor-(MOS-)type GNRFETs (MOS-GNRFETs) [**24**]

As shown in the fig. (2.9-a), MOS-type GNRFET is constructed with metal gate, GNR based drain, source and channel. In MOS-type GNRFET, reservoirs (source and drain) are the portions of GNR not covered by the gate and are heavily doped GNRs. By choosing the type of dopants in these reservoirs, the MOS-type GNRFETs are either made n-type or p-type. Since either n-i-n or p-i-p doping profile can be



(a) MOS-type GNRFET. After [**24**].



(b) BS-type GNRFET. After [**47**].

FIGURE 2.9. GNRFET and its types

formed, the current conduction is mostly based on thermionic conduction. In order to connect source and drain to the outside world, metal layers are needed which and they are connected with these graphene layers (drain and source) by vias. This introduces graphene-metal junction and significantly increases contact resistance. This severely limits the circuit performance. Due to monotonic I-V curve, it gives higher I_{on}/I_{off} ratio than SB-GNRFET. Thus they are more preferred in digital logic applications and low power applications. However the contact resistance limits their performance. Further, its performance is limited by the process variation that occurs inside the reservoir while doping. However these reserviors in MOS-GNRFET observes the minority carriers during the off conduction state and hence results in very small I_{off} current.

(b) Schottky-Barrier-type GNRFETs (SB-GNRFETs) [**25**, **47**]

As shown in the fig. (2.9-b), in SB-type GNRFET, gate, drain and source are metal and the channel is constructed with graphene nanoribbon passing between drain and source under gate. Since SB-GNRFETs exhibit ambipolar I-V curve, they are neither n-type nor p-type. It is possible to design logic circuits using such ambipolar characteristics. In order to implement CMOS based logic circuits using SB-GNRFET, the corresponding I-V curve need to be shifted accordingly as as to make them either p-type or n-type [**25**]. The current conduction in SB-GNRFET is based on Schottky barrier tunneling due to metal-graphene junction. Since drain and source are made of metal, hence this structure does not introduce any contact resistance.

The ambipolar characteristic of SB-GNRFET makes it difficult to completely turn off even at zero gate voltage. Thus the leakage current increase and thereby increases the power consumption. However due to its low EDP and low delay, it is mostly suitable for high performance and, high energy efficient application where power consumption is not an issue. It has higher I_{off} due to the absence of doped reservoir to observe minority carrier as in MOS-GNRFET.

(4) Graphene Nanoribbon Tunnel Field Effect Transistor (GNRTFET):

The subthreshold swing (SS), which is the voltage required to change the current, in Si CMOS is limited by thermionic emission to 60 mv/dec. This results in the increase of static power dissipation when Si CMOS is scaled down. Thus in order to obtain SS less than 60 mv/dec, graphene has been preferred due to its symmetric band structure, light effective mass and direct band gap which assist tunneling phenomenon. Graphene nanoribbon tunneling field effect transistor (GNRTFET) is another graphene based transistor which has drawn attention from past few years due to its low subthreshold swing, high I_{on}/I_{off} ratio and these contribute high speed, low dynamic power, low off-state power dissipation, superior gate control and a reduction of traversal energy component in 1-D tunneling transport [**127**]. To enhance the IN-state tunneling it is preferred to use a narrow bandgap materials with smaller effective masses.

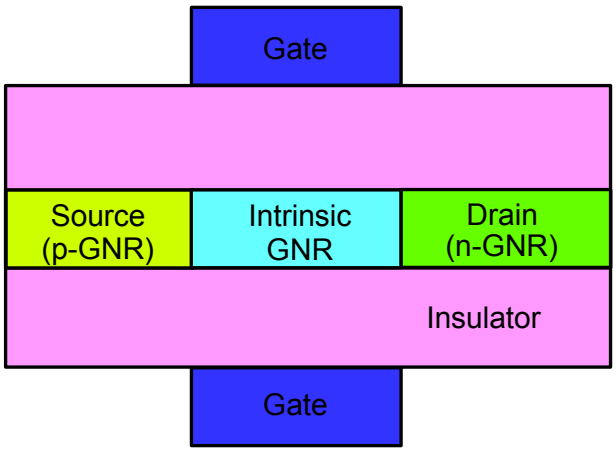


FIGURE 2.10. Double gate GNRTFET. After [**124**].

As shown in the fig. (2.10), the graphene nanoribbon based TFET consists of p-type GNR source, n-type GNR drain with intrinsic GNR as a channel. HfO_2 is used as a gate insulator whose dielectric constant is 16. Since the source is p-type and drain is n-type, the thermionic current is negligible in GNRTFET. The current flow is due to band to band tunneling phenomenon which is more sensitive to terminal bias than thermionic current and thus leads to a very low SS like 0.19 mV/dec [**127**]. When the gate voltage is zero and the drain voltage is applied, the conduction band in the channel becomes

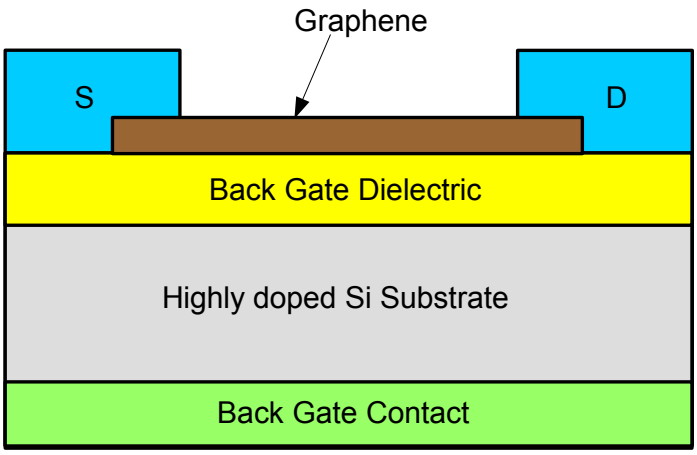
higher than the valence band at the source side. Similarly, the valence band in the channel becomes lower than the conduction band in the drain side. This makes both electrons and holes conduction difficult to tunnel through the channel. However when the gate voltage is increased to a level where the conduction band in the channel becomes lower than the valence band in the source side then the electrons from the source (i.e. valence band) can tunnel into the channel (i.e. conduction band). This increases the electron current. Similarly, when the gate voltage is reduced to a level where the valence band in the channel becomes higher than the conduction band in the drain side then the holes from the channel (i.e. conduction band) can tunnel into the drain (i.e. conduction band). This increases the hole current. Thus the current can be due to holes or electrons and can be controlled by simply changing the gate voltage. If this ambipolar characteristic is not needed for any application then it can be reduced using the techniques like gate underlapping, asymmetric doping [**124**].

2.3. Graphene Based Integrated Circuits

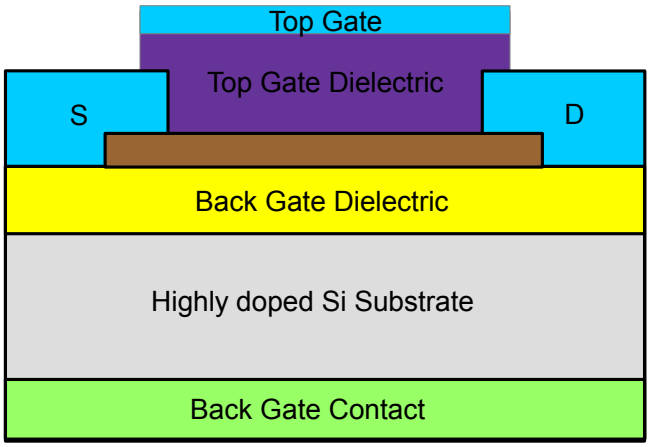
In the recent years, several graphene transistor structures have been studied like: back-gated graphene transistor, dual-gate graphene transistor and epitaxial growth of graphene on SiC as shown in Fig. 2.11 [**60**, **65**, **77**].

In back gate GFET structure, as shown in Fig. 2.11(a), the graphene flake is deposited on the top of the substrate making a channel between source and the drain. The underlying substrate is heavily doped so it acts as a back gate. As this structure is relatively simpler to fabricate, it is suited for research and conceptual purpose only. There is no other layer above graphane except passivation layer which makes Dirac point mobility and the hysteresis profile of the transistor vary with the environment [**67**]. Furthermore this structure suffers from large parasitic capacitance and due to the absence of top layers, integration with other components becomes a serious limitation. [**104**].

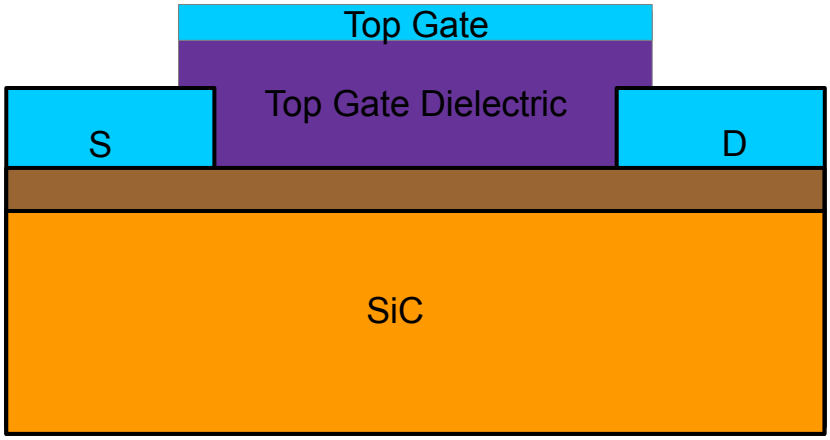
In Fig. 2.11(b), graphene (either monolayer or bilayer) is sandwich between the top gate dielectric and the substrate. The substrate act as a global back gate while the top gate act as a main gate electrode for normal FET operation. While the top gate modulates the carrier, the back gate is



(a) Back gate graphene transistor



(b) Dual gate graphene transistor



(c) Epitaxial graphene from SiC and transistor structure

FIGURE 2.11. Different GFET Configuration. After [**60**, **65**, **77**].

responsible for doping the channel. Thus with the dual gate configuration, it allows precise control of the access resistance thereby allowing an increase in the device transconductance. Similarly by applying a perpendicular electric field across the graphene channel, it is possible to create small bandgap in graphene. So both bandgap and carrier doping concentration can be independently tuned using dual gate configuration.

In Fig. 2.11(c), a epitaxial graphene is synthesized on silicon carbide wafers (SiC) in order to gain high structural integrity. SiC is an excellent low loss substrate and is suitable for high temperature, high electric fields and high speed devices [**39**]. Graphene can be grown on either silicon face or carbon face. In terms of mobility, it is preferred to grow graphene on carbon face (i.e. 5,000 $cm^2/(Vs)$ in graphene on C-face versus 1,000 $cm^2/(Vs)$ in graphene on Si-face), whereas it is relatively easier to grow both monolayer of bilayer graphene in Si-face as compared to C-face. The biggest advantage of this technique is a precise control of the thickness of graphene at the wafer scale [**87**] and such graphene displays the carrier mobilities equivalent to those of the suspended graphene and other properties similar to ideal graphene. Epitaxial graphene on SiC is expected to be better than silicon in terms of speed, feature size and power consumption [**101**].

Using these three graphene structures, various graphene based electronic circuits have been designed and analysed. Semiconductor electronics can be categorized into either digital logic devices or radiofrequency devices, each of these category has different set of requirements and design complexity. The design of digital logic circuits and RF circuits differs in the following three main aspects [**104**]:

(1) Making the transistor smaller has been the main objective in digital logic whereas size is not the major concern for radio-frequency circuits. Thus digital logic circuits are much more complex than the RF circuits .

(2) Power consumption is the key requirement in the digital logic circuits. Since most of the transistors in the digital logic circuits needs to be turned off during steady state, this demands for the device to have very low leakage current (i.e. off current) and hence the ratio of ON current and OFF current should be very high. However in the case of RF circuits, switching the transistor off is not required. Thus ON state circuit performance is

more important than low leakage current.

(3) RF circuits have been more open to new device concepts than digital logic circuits. For example, different types of bipolar transistors, compound semiconductors and high-electron mobility transistors (HEMTs) have been continuously used in RF circuits, whereas in digital logic there have not been much change in the device material and transistor type.

As is Moore's law for counting the number of transistors in electronics, there is another famous law known as Edholm's law [**26**] in wireless communication to predict the demand for bandwidth in wireless communication. According to Edholm's law, the demand for higher bandwidth doubles every 18 months in wireless communication. The current wireless local area network, which is already having a data rate of around 200 Mbps, operates at a carrier frequency of 5 GHz. In order to meet the future target of 5 Gbps data rate, the carrier frequency needs to exceed 100 GHz. This is very much achievable with graphene due to its high thermal conductivity (about 5000 W/(mk), which is better than most crystals), high Young modulus (about 1.5 TPa, ten times more than steel), high mobility (around 200,00 cm_2/(Vs) in suspended graphene), zero electron and hole effective mass at room temperature (due to symmetric honeycomb lattice structure), high Fermi velocity (about 10^6 m/s) at room temperature, carrier confinement within a single layer of one atom thickness and so on. These properties of graphene can address some of the limitations that existing radio frequency(RF) applications are facing in terms of maximum frequency, linearity and power dissipation.

Some of the graphene based circuits that have been studied in last few years are as follows:

2.3.1. Low Noise Amplifier (LNA)

Graphene is suited for high frequency LNA due to its:

(1) extremely low source-to-drain resistance

(2) extremely high current density

(3) high efficiency operation

(4) carrier confinement in one single layer of one atomic thickness minimizes short channel effect and thus operates at very high frequency

In [**69**], SiO_2 was used as a gate dielectric in the top-gated graphene transistor. The top gated transistor offered higher gate capacitance and modulation capability but the use of SiO_2 as a gate dielectric causes significant reduction in carrier mobility. In [**81**], GFET was fabricated in SiC substrate in a self-aligned devices with a gate length of 1 μm. The cutoff frequency of 4.2 GHz and maximum frequency of 14 GHz was recorded. In [**71**], a cutoff frequency of 100 GHz was demonstrated for non-self aligned device on graphene flake. However still there are several issues that need to be addressed for graphene to be used as LNA like [**90**]:

(1) mobility for top gated GFET is much less than that of the suspended graphene.

(2) lack of bandgap reduces ON-OFF ratio thus decreasing devise efficiency

(3) high output conductance due to ambipolar transport and lack of bandgap limits power gain performance.

2.3.2. Ambipolar Electronics

Exploiting the ambipolar property of graphene has received a lot of attentions for radiofrequency applications like frequency doublers, digital modulators, RF mixers, full wave rectifiers and so on instead of compromising mobility for bandgap. The advantage of ambipolar devices over conventional semiconductor are the reduction in the number of transistors required to implement the circuit [**90**]. This results in simpler circuits, less power consumption and smaller size. Furthermore, exploiting the ambipolar nature of graphene, it is possible to achieve circuits that can operate at higher frequencies due to higher mobility in graphene. For such applications, the symmetricity of I_{DS} vs V_{GS} around Dirac point is very important such that the drain current can be expressed as [**130**]:

$$I_{DS} = a_0 + a_2.(V_{GS} - V_{Dirac})^2 + a_4.(V_{GS} - V_{Dirac})^4 + ..., \tag{3}$$

where V_{GS} and V_{Dirac} refer to the gate voltage and voltage at Dirac point respectively. a_0, a_2 and a_4 are the constants. For exploiting the ambipolar property in GFET, the gate electrode is always an input with respect to source and output is taken across drain electrode which is biased to V_{DD} via a load resistor R_L [**130**] . Then the output voltage is given as follows:

$$V_{DS} = V_{DD} - I_{DS}R_L. \tag{4}$$

2.3.2.1. Frequency Doubler

Given an input voltage with amplitude A and frequency ω radian biased at Dirac point as given below:

$$V_{GS} = V_{Dirac} + A \sin \omega t. \tag{5}$$

The I_{DS} vs V_{GS} showing perfect parabolic curve around Dirac point as shown in Fig. (2.12), then the output drain voltage gives a signal with double the input frequency as follows:

$$V_{DS} = V_{DD} - a_0 R_L - \frac{a_2 R_L A^2}{2} + \frac{a_2 R_L A^2 \cos 2wt}{2}. \tag{6}$$

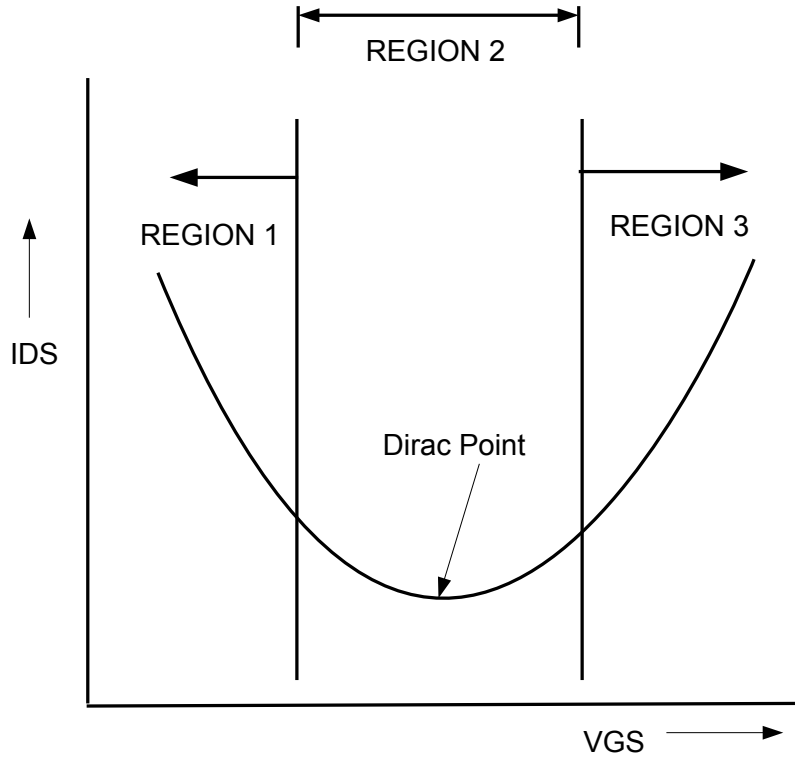


FIGURE 2.12. Transfer curve of GFET. After [**130**].

The cutoff frequency can be increased with shrinking the gate length and graphene with higher mobility. For example, for gate length of 60 nm, the frequency can exceed 100 GHz[**90**]. However for any assymmetricity in I_{DS} vs V_{GS} curve, more number of odd harmonics are introduced in the output.

2.3.2.2. RF Mixers

For any two sinusoidal signals of amplitudes A_1 and A_2 and frequencies w_1 and w_2 respectively at the input gate electrode, the output shows the original frequencies along with their sum and difference frequencies but with no odd order harmonics, which is a great advantage in terms of dynamic range of circuit operation. However any deviation from symmetric I_{DS} vs V_{GS} curve will introduce some odd-order intermodulation harmonics. In [**72**], it is shown that a wafer-scale graphene circuit on SiC operating at a frequency as high as 10 GHz with very high thermal stability.

2.3.2.3. Digital Modulators

The Fig. 2.12 shows the symmetric $I_{DS} - V_{GS}$ curve around Dirac point. The region I is the p-region which shows positive gain due to negative transcondutance. The region III is the n-region and shows negative gain due to positive tranconductance. The region II shows transition between n-region and p-region. By changing the bias voltage at the input electrode in such a way that the region of operation alters between region I and region III then binary phase shift Keying (BPSK) can be realized. In region II, the GFET acts as a frequency doubler making a transition between p-region and n-region. By marking the fundamental frequency as '0' and doubled frequency as '1' respectively, a binary frequency shift keying (BFSK) can be realized.

2.3.2.4. Full Wave Rectifier

The I-V charactersistic of graphene is V-shaped which resembles to an ideal full-wave rectifier. Thus a single graphene transistor can be used to produce full-wave rectification with zero voltage threshold voltage. The same circuit can be otherwise produced by four diodes or an operation amplifier if traditional Si based semiconductor is used. Thus the use of graphene can make future electronics much small sized.

2.3.2.5. Graphene Resonator

Graphene is a very god candidate for nanoelectromechanical (NEMS) applications due to its high stiffness and low density. In [**90**], monolayer graphene was used as a nano-mechanical resonator at an operating frequency of 50-80 MHz.

2.3.2.6. Graphene Switch

In [**90**], two polycrystalline graphene films were used to demonstrate graphene as an electromechanical switch.

2.3.3. Further Options for Graphene Devices

It is also possible to create all graphene based devices where the active device as well as interconnects are made of graphene. Graphene, as an interconnect material, also out-stands the conventional copper based interconnect in terms of current density and thermal conductivity.

2.4. Novel Contribution of this Dissertation

The **novel contribution of this dissertation** to advance the state-of-art are as follows:

(1) Verilog-A modeling of graphene FET has been presented in chapter 3 followed by the design flow of GFET based cross coupled version of LC voltage controlled oscillator has been presented in chapter 5. This is the first attempt to propose a design flow for GFET based cross coupled version of an LC oscillator.

(2) A new optimization algorithm called multi-swarm optimization (MSO) is used in the design flow in chapter 5, which is also a new attempt. The output of this optimization flow gives the proper sizing of the GFET device so as to achieve the maximum frequency within given constraints.

(3) In chapter 4, a Simscape® based ultra-fast design exploration is presented. This is a non-EDA flow and a paradigm shift from conventional EDA flow.

(4) In the same chapter, modeling of a GFET is presented in Simscape®, which is the first attempt for graphene device. The case study circuits: LNA and LC oscillator are also modeled in the Simscape® graphical environment. The experimental validation of the Simscape® device level models is done with the existing EDA models (i.e VHDL-AMS or Verilog-A models).Also the case study circuits have been compared with Verilog-A based designs.

(5) In the chapter 6, graphene nanoribbon FET is used for the design of SRAM and is compared with 45-nm silicon transistor based SRAM based on stability and power consump-

tion. This is the first ever comparison done for the graphene based SRAM in such a detail.

CHAPTER 3

VERILOG-A BASED MODELING AND ANALYSIS OF GRAPHENE CIRCUIT

Semiconductor device modeling refers to the creation of a model which can capture the electrical behavior of the components. It is the link between physical world and the design world where physical world represents technology, manufacturing, etc and design world represents device simulation, timing simulation etc. Modern Integrated Circuits (IC) is a set of very complex electronic components interconnected within a small die. The first step in the design of any actual system starts with the prototype design of that system so that its performance can be measured under wide range of operating condition, process variation and interaction between different set of system components. General circuit/system prototype design is shown in Fig. 3.1 [**77**]. The simulation engine requires three set of inputs: input and setup, circuit/system description, and models. The simulation engine is setup and proper input to the simulation engine are given in the input and setup set. The simulation engines uses models and circuit/system description and performs the simulation for the given input and setup. Since an IC consists of different components, the description of each of those components are given in the circuit/system description set. The model input refers to the description of how each of these circuits/systems are supposed to work.

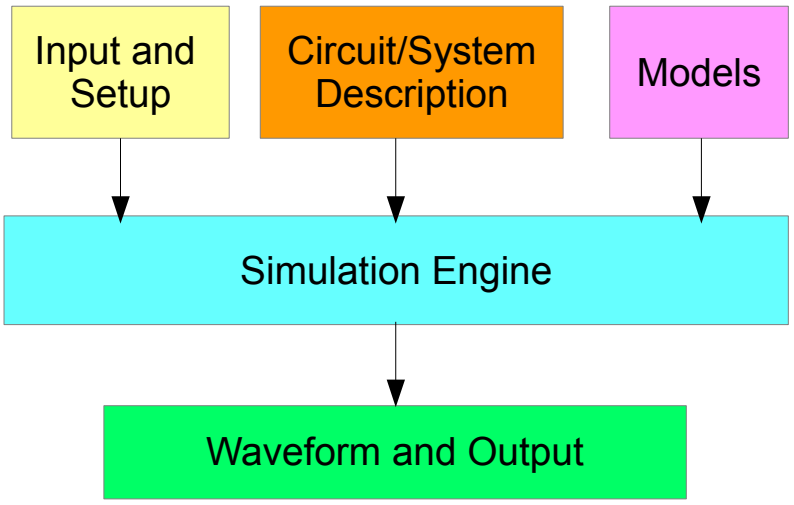


FIGURE 3.1. Typical IC Prototpye Design Flow. After [**77**].

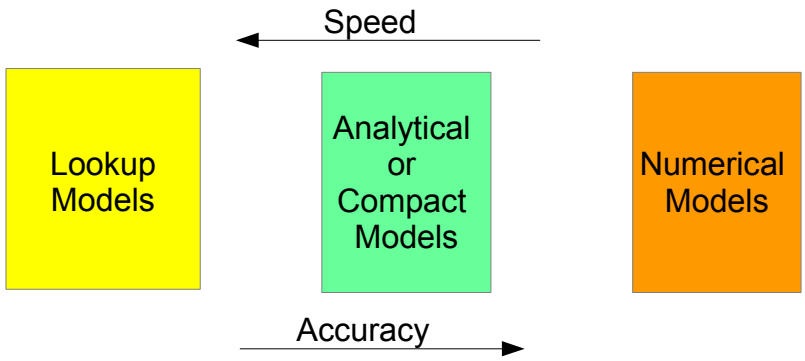


FIGURE 3.2. Accuracy Vs Speed Comparison of different types of model [**77**].

Generally device models are categorized into three types: numerical models, lookup models and analytical model (also called compact model). The numerical models (e.g. technology computer-aided design, TCAD models) are based on the fundamental of physics which includes fabrication processes like diffusion and ion implantation and electrical properties of the components. They produce accurate results but computationally they are extremely slow and intensive and are not so common for modern complex and large system design. Models based on lookup tables represents current and capacitor as a function of bias voltage and the information stored in the lookup table are used to simulate circuit. These models comprises speed with accuracy. The most commonly used model for circuit simulation is the analytical models (also called compact models), which are characterized by the set of mathematical equations. These equations are derived from the device physics but to make the equations simple, computationally efficient and remove the convergence issues, approximation plays a crucial role in these models. Fig. 3.2 shows the speed and accuracy comparison of these models, which is the major challenge for model developer in modern semiconductor design.

These models can be written in various language which depends on the following:

(1) Based on signal type: Analog, Digital or mixed signal

(2) Based on design abstraction level: System, architecture, logic, switch, circuit, layout or technology level

Physics based models will be discussed in Chapter 4. In this Chapter, Verilog-A based compact model is explored for graphene based circuits.

3.1. Why Verilog-A Model is Necessary

Simulation Program with Integrated Circuit Emphasis (SPICE) has been the cornerstone in analog simulation from past few decades. However SPICE is not a high-level language and it becomes extremely complex and tedious to describe modern circuits and systems using SPICE language [**6**]. Thus Compact Model Coalition (CMC) (formerly, Compact Model Council) [**1**] is now encouraging on Verilog-A based compact model for its next generation semiconductor devices. Verilog-A based model offers lots of advantages over SPICE based compact model in the following aspects [**7**]:

(1) It allows behavioral model of analog component so that the higher level design abstraction can use them without the need to know the underlying lower level modules. This allows easy hierarchical modeling which is extremely helpful for complex and large modern circuits [**77**].

(2) Verilog-A language removes the burden of handling simulator interface like allocating memory, reading the model parameters, initializing values, checking the topology. This provides easier and faster design of the model [**27**].

(3) The Verilog-A base modules can be parameterized easily within the specified range and is easily compatible with Verilog-AMS. This is very helpful for modeling mixed-signal circuits.

(4) Since Verilog-A is a high-level C-like language, the model developers can be easily switched to Verilog-A with an additional benefits:

   (a) For easier modeling of complex circuitry, the branches can be named in Verilog-A and use that name later in modeling.

   (b) Verilog-A can take the advantages of operators like derivative, integration, trigonometric functions, Laplace transform, z-transform, circular integration, slew [**50**].

   (c) Verilog-A allows multi-disciplines modeling like electrical, mechanical and thermodynamics.

(5) SPICE simulation needs to solve large number of equations especially when the circuit consists of active elements. However using Verilog-A based modeling, a single calcula-

tion can give current for the circuit. This considerably reduces the complexity, improves simulation time and system resources [**75**].

3.2. Discussion of Device Structure

The cross sectional view of the dual gated graphene FET is shown in the fig. 3.3, where S represents the source and D represents the drain contact, respectively [**65**]. The GFET, like silicon FET, is a symmetric structure and source is usually electrical reference (i.e. grounded).

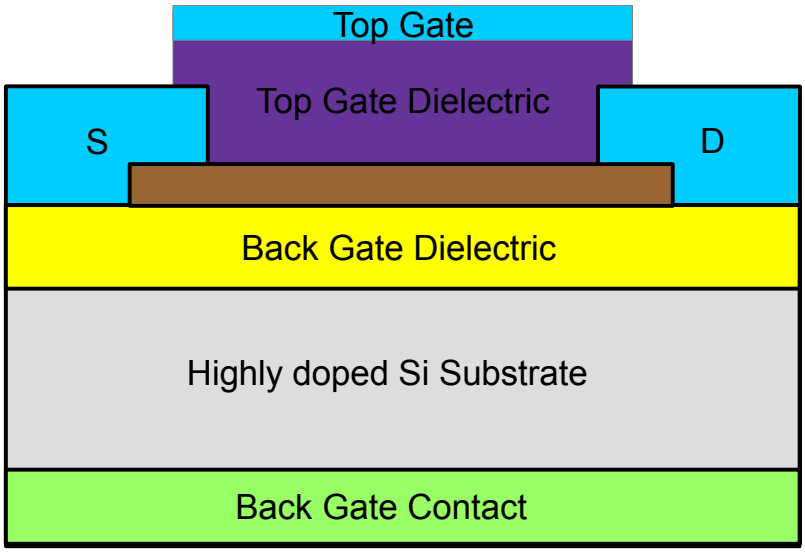


FIGURE 3.3. Dual gate graphene transistor. After [**65**].

The dual gate configuration has been selected for analysis of graphene based circuits due to its advantages like the following:

(1) It makes possible to independently tune the electronic bandgap and carrier concentration in graphene, which are the two key semiconductor parameters.

(2) It gives more control on doping by controlling gate voltage, which allows precise control of device resistance. This allows the circuit to have large transconductance by minimizing the channel resistance.

(3) The application of perpendicular electric field into the graphene layers can create bandgap i.e. electric field tunable bandgap.

The top gate length, L_g, of 3 μm forms the active region of the channel of width 2.1 μm. The top gate dielectric (i.e. Hafnium oxide with dielectric constant = 16) of thickness 15 nm, is sandwiched between the top gate electrode and the graphene channel. Reports indicates that the use of Hafnium oxide reduces phonon and Coulomb scattering thereby preserving the carrier mobility [**112**]. Silicon oxide (whose dielectric constant is 3.9) is used as a back gate dielectric material, which is also the substrate for the GFET. The thickness for the substrate is considered to be 285 nm. A single layer of graphene is used as a channel whose thickness is considered to be 2.1 μm. By applying an electric field perpendicular to the graphene channel, a tunable bandgap can be opened which can then be modulated by the gate voltage.

The potential difference between the channel and the gates (top gate and back gate) determines the carrier density and the carrier type (i.e. either electrons or holes). The top gate modulate the carrier in the channel while the back gate is responsible for doping the channel. For a large positive gate voltage, the channel become n-type and hence promotes an electron as a majority charge carriers while for large negative gate voltage, the channel becomes p-type, promoting holes as a major charge carriers. Due to this, a symmetric type of current-voltage relationship is developed across a Dirac point, whose position depends on difference of work functions of gate and the graphene, type and density of the charge carriers in the channel and doping concentration of the graphene.

Before going in the transistor model, it is important to understand the carrier transport model based on the device and the application node. There are basically three type of transport models [**96**]:

(1) Drift-diffusion model, which is used when the channel length is large enough as compared to the mean free path of the carriers. In such situations, the carriers (either holes or electrons) as it passes from the source to the drain side, they get scattered due to one or many phonons, electrons, holes, ionized impurity, photon and neutral impurities. Thus the path of the carrier is not a straight path from source to the drain but is a zigzag path.

(2) Ballistic model, in which the channel length is small as compared to the mean free length of the carrier. So, the carriers can travel from source to the drain in a straight path without

any scattering mechanism.

(3) Quasiballistic model, in which the channel length is comparable to the mean free path. So, both drift-diffusion and ballistic transport mechanism can be used to explain the carrier transport.

So depending on the channel length, the carrier transport mechanism varies and hence the transistor model.

3.3. Device Level Modeling and Simulation Results

In the following discussion, L denotes the graphene channel length, W represents the width of the graphene layer, t_{ox} denotes the thickness of oxide layer between the top-gate and the substrate and H_{sub} denotes the substrate thickness. Hafnium oxide (HfO_2) is used as the top-gate dielectric with dielectric constant, $k = 16$ and SiO_2 is used as the substrate with $k = 3.9$.

The two electrodes namely top gate and back gate, act as a parallel plate with dielectric layer in between them. This creates an equivalent series parasitic capacitance namely C_{top} and C_{back}, consisting of top and back components respectively [**104**, **110**, **112**] for the GFET. The top component is given by the following:

$$C_{top} = \frac{C_e C_q}{C_e + C_q}, \tag{7}$$

where $C_e = \epsilon_{ox}/t_{ox}$ is the oxide capacitance and C_q is the quantum capacitance. Quantum capacitance is an extra capacitance which originates from the low density states of graphene around the Dirac point. It can act as a barrier in scaling of graphene devices. Due to its linear band structure, the quantum capacitance increase with the square root of the charge density given by [**74**, **112**]:

$$C_q = \frac{q^2\sqrt{\frac{n}{\pi}}}{v_F \hbar}, \tag{8}$$

where q is the electron charge, n is the electron concentration, $v_F \sim 10^8$ cm s^{-1}, and $\hbar$ is Planck's constant. The drain-source current (I_{ds}) of a GFET is given by [**105**, **112**]:

$$I_{ds} = W q n v_{\text{drift}}, \tag{9}$$

where v_{drift} is the electron drift velocity expressed as [**74**, **110**, **112**]:

$$v_{\text{drift}} = \left(\frac{\mu E}{1 + \frac{\mu E}{v_{\text{sat}}}} \right), \tag{10}$$

where E is the electric field, μ is carrier mobility and v_{sat} is the saturation velocity. $V_{g0} = V_{gs} - V_0$ shows the relation between gate voltage and the threshold voltage, V_0, which is given by [**74**, **112**]:

$$V_0 = V_{gs}^0 + \frac{C_{back}}{C_{top}}(V_{bs}^0 - V_{bs}), \tag{11}$$

where V_{gs}^0 is the top-gate voltage and V_{bs}^0 is the back-gate voltage at the Dirac point, which is defined as the point in the electronic band structure of graphene where charge neutrality is obtained [**128**]. Taking into consideration the source resistance (R_s) and combining (9)–(11), when $V_{ds} > V_{sat}$ for high negative back gate voltage while forming a p-channel, the drain-source current can be expressed as [**74**, **110**, **112**]:

$$I_{ds} = \frac{1}{4R_s}\Big(V_{ds} - V_c + I_0 R_s + \sqrt{(V_{ds} - V_c + I_0 R_s)^2 - 4 I_0 R_s V_{ds}}\Big), \tag{12}$$

where

$$I_0 = 2\left(\frac{W}{L}\right)\mu V_c C_{top}\left(V_{gs} - V_0 - \frac{V_{ds}}{2}\right), \tag{13}$$

where $V_c = E_c L$ and E_c is the critical electric field.

For the condition, $V_{ds} \leqslant V_{sat}$,

$$I_{ds} = I_{ds-sat} + I_{\text{disp}}, \tag{14}$$

where I_{disp} is the displacement current [**112**] and the critical voltage V_{ds-sat} is given by the following eqn [**105**, **112**]:

$$V_{ds-sat} = \frac{2\gamma V_{g0}}{1+\gamma} + \frac{1-\gamma}{(1+\gamma)^2}\left(V_c - \sqrt{V_c^2 - 2(1+\gamma)V_c V_{g0}}\right) \tag{15}$$

where γ is a coefficient given by:

$$\gamma = R_s\left(\frac{W}{L}\right)\mu C_{top} V_c. \tag{16}$$

The saturation current I_{ds-sat} is given by [**105**, **112**]:

$$I_{ds-sat} = \frac{\gamma}{R_s(1+\gamma)^2}\left(-V_c + (1+\gamma)V_{g0} + \sqrt{V_c^2 - 2(1+\gamma)V_cV_{g0}}\right), \tag{17}$$

where the displacement current I_{disp} is expressed as follows [**112**]:

$$I_{\text{disp}} = \left(\frac{W}{L}\right)\mu C_{back}\left(\mid V_{bs} - V_{bs}^0 \mid\right)\frac{V_{ds}}{10}\left(\frac{V_{ds}}{V_{ds-sat}} - 1\right)^2. \tag{18}$$

3.4. Verilog-A Simulation of GFET Based Case Study Circuit

As a case study, cross couple version of LC oscillator is considered in this section. Oscillators are the heart of any communication systems which are not only used to up- and down- convert the signals, but are also used to provide carrier and pilot signals for communication systems including navigation. They are also used to provide clock signals in data processing applications, provide reference signals in the circuit. So for proper functioning of these devices, it is very important to have oscillator with high accuracy and stability.

For any oscillation to occur, it is very important to have the following properties:

(1) Amplification: To amplify the signal without any external power supply,

(2) Frequency determining device: To determine the frequency of the signal that is to be produced, and

(3) Positive feedback path: To build up the signal strength for oscillation.

In voltage controlled oscillator, by name, input voltage controls the oscillation frequency. Since VCO is a non-linear circuit, the prediction of oscillation frequency, output voltage and power consumption is very difficult. Similarly, the phase noise in the oscillator plays a critical role in the design. The cross couple version of LC-VCO has been used due to its very low phase noise, easy start-up and low power consumption.

As shown in the fig. 3.4, the LC-VCO consists of LC tank circuit which is controlled by 2 symmetric varactors (i.e. voltage controlled capacitors) C_1 and C_2. These varactors are used to adjust the capacitance of the tank circuit in response to the input voltage(V_{tune}) and thus provides the tuning mechanism for the oscillator. The capacitor and inductor forms the tank circuit.

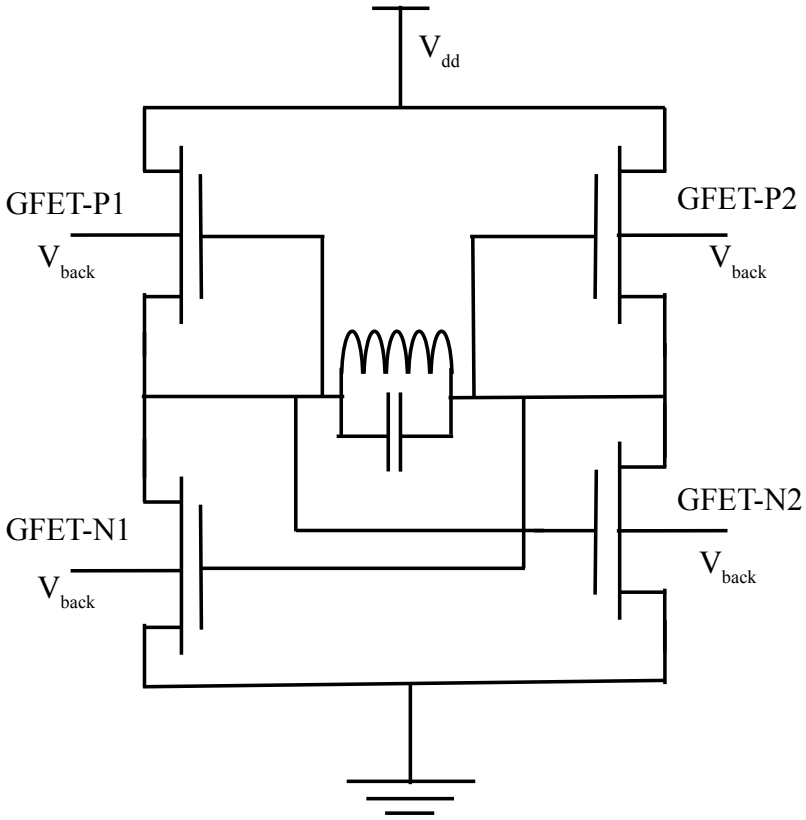


FIGURE 3.4. GFET based cross coupled version of LC-VCO. After [**62**, **77**].

The use of crossed coupled transistors forms the active devices in the configuration and provide enough negative parallel resistance on the tank circuit to keep the tank oscillation[**34**]. They also provide the needed negative feedback. These GFETs compensate for the losses in the LC tank circuit. The advantages of using both n-channel and p-channel FET are as follows:

(1) Easy start-up,

(2) Increases the transconductance without increasing the quiescent current,

(3) Compensate the loss from LC tank circuit,

(4) Less current consumption, and

(5) Wide tuning range and controls the phase noise around the carrier

The frequency of oscillation (f_0), decided by LC tank circuit, is given by [**62**]:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{19}$$

where L is the inductance and C is the capacitance given by [**62**]:

$$C = C_{gs} + C_{gd} + C_{varactor} \tag{20}$$

where C_{gs} and C_{ds} are the parasitic capacitance in the GFET structure. In order to self-sustain oscillation, it is necessary to satisfy the following condition [**62**]:

$$g_{active} > \frac{RC}{L} \tag{21}$$

where g_{active} is the transconductance of the active device and R accounts for the parasitic resistance of GFET as well as the resistance of the inductor. The condition:

$$I_{bias} \leq I_{max} \tag{22}$$

ensures that the power dissipation is within the required range. Here, I_{bias} is the bias current and I_{max} is the maximum allowable current.

In order to have an oscillation, the GFETs are required to satisfy both equations (21) and (22). This is the required operating point for the GFETs. However it should be noted that the inductance value is affected by factors like inductor width, spacing and number of turns. So these must be fixed before determining the tank load conductance. Once the bias current (I_{bias}) and tank load conductance (g_{tank}) are known, the voltage swing of the oscillator is given by [**62**]:

$$v_{tank} = \frac{I_{bias}}{g_{tank}} \tag{23}$$

3.5. Verilog-A/SPICE Based Modeling and Simulation Flow

Using equation (7) - (18), the model for graphene FET is implemented in Verilog-A. The complete algorithm is given in Algorithm 1.

3.6. Experimental Setup of Results

Table 3.1 summarizes the GFET parameters used for the design. The carrier mobility for suspended graphene is around 100,000 $cm^2/(Vs)$ which decreases to 20,000 $cm^2/(Vs)$ when subjected to substrate. On insulators like SiO_2, it is around 1,000 - 10,000 $cm^2/(Vs)$, depending upon the nature and purity of underlying substrate. So, it is considered 3,000 $cm^2/(Vs)$ in the design. For simplicity of the model, both holes and electrons are characterized by same mobility

Algorithm 1 Proposed Verilog-A model for a GFET [**77**].

```
'include "disciplines.vams"  //contains electrical definition of disciplines like current, voltage
'include "constants.vams"  //contains mathematical and physical constants like PI, charge

//declare module name to be graphene with 4 ports: drain, gate, back-gate and source
module graphene(drain, gate, back_gate, source);

//Parameter definitions : ways to pass information into the module at the time of instantiation
parameter real Rs = 600.0;           //series resistance
parameter real mu = 300.0e-4;        //carrier mobility
parameter real Ec = 15e5;            //critical electrical field
parameter real Cq = 0.02;            //quantum capacitance
parameter real Cgio = 0.8072;        //top-gate capacitor factor
parameter real Hsub = 285.0e-9;      //substrate thickness
parameter real tox = 15.0e-9;        //top-gate dielectric thickness
parameter real L = 3.0e-6;           //gate length
parameter real W = 2.1e-6;           //gate width
parameter real ntop = 2.1209e16;     //carrier concerntration
parameter real Vgs0 = 1.45;          //gate-to-source voltage at Dirac point
parameter real Vbs0 = 2.7;           //bulk-to-source voltage at Dirac point
parameter real k = 16.0;             //top-gate dielectric
parameter real k_sub = 3.9;          //back-gate substrate dielectric

inout drain, gate, back_gate, source;   //defining ports to connect to other modules or devices

electrical drain, gate, back_gate, source;  //attirbutes electrical disciplines to the ports
electrical drainint, sourceint;

//branches to refer paths between two nets
branch(drainint,  sourceint) Ids;
branch(drain, source) Vds;
branch(gate, source) Vgs;
branch(gate, drain) Vgd;
branch(back_gate, source) Vbs;
branch(back_gate, sourceint) Vbsint;
branch(gate, sourceint) Vgsint;
branch(gate, drain) Vgdint;
branch(back_gate, drainint) Vbdint;
branch(drain, drainint) Resistor1;
branch(source, sourceint) Resistor2;

parameter real c1 = ('P_EPSO * k * Cgio * W * L/tox) from [0:inf);
parameter real c2 = ('P_EPSO * k_sub * W * L* 0.5/Hsub) from [0:inf);
parameter real r = 600.0;

real ids;  //real type variable declared

analog function real Fgfet;   //user defined analog function

//input parameters
input Vds, Vgs, Vbs, Rs, mu, Ec, Cgio, Hsub, tox, L, W, ntop, Vgs0, Vbs0, k, k_sub;

//variables to be used in the statement blocks
real Vds, Vgs, Vbs, Rs, mu, Ec, Cgio, Hsub, tox, L, W, ntop, Vgs0, Vbs0, k, k_sub;
real Ce, Ctop, Cback, Vc, Ids, Rc, Gamma, V0, Vg0, Vdsat, I0, Cq;

begin
Cq = pow((ntop/'M_PI),0.5)*pow('P_Q,2)/1.0E6/('P_H/(2*'M_PI));  //Equation(8)
Ce = Cgio*'P_EPSO*k/tox;                                        //oxide capacitance
Ctop = Cq*Ce/(Cq+Ce);                        //capacitance between channel and top-gate: Equation(7)
Cback = 'P_EPSO*k_sub/Hsub;                    //capacitance between channel and back-gate
V0 = Vgs0 + (Cback/Ctop)*(Vbs0 - Vbs);       //device threshold voltage: Equation(11)
Vg0 = Vgs - V0;                              //relation between gate voltage and threshold voltage
Vc = Ec * L;                                  //critical voltage
Rc = 1.0/((W/L) * mu * Ctop * Vc);          //total resistance of contact: Equation(16)
Gamma = Rs/Rc;
Vdsat = 2.0 * Gamma * Vg0/(1.0 + Gamma) + ((1.0 - Gamma)/pow((1.0 + Gamma),2.0))
         * (Vc - sqrt(pow(Vc,2.0) -  2.0 * (1.0 + Gamma) * Vc *Vg0));     //Equation(15)
I0 = 2.0 * (W/L) * mu * Vc * Ctop * (Vgs - V0 -Vds/2.0);               //Equation(13)

//employing charge control model
if (Vds < Vdsat)
Ids = -1.0/4.0/Rs*(Vds - Vc + I0 * Rs + sqrt(pow((Vds - Vc + I0 * Rs),2.0) - 4.0* I0 * Rs * Vds));
//drain current during non-saturation region i.e. in 1st linear region
```

```
     else if (Vds >= Vdsat)
          Ids = -(Gamma/Rs/pow((1.0 + Gamma),2.0) * (-Vc + (1.0 + Gamma) * Vg0
                   + sqrt(pow(Vc,2.0) - 2.0 * (1.0 + Gamma) * Vc * Vg0)) - mu * Cback
                   * abs(Vbs - Vbs0) * Vds * W/L/10.0 * pow((Vds/Vdsat  1.0),2.0));
          //drain current in 2nd linear region when Vds > Vds,sat. Inflection point at Vds=Vds,sat
     else
          Ids = 0.0;

      Fgfet = Ids;      //value returned by the function
end
endfunction

//Analog block describes the behavior
//Procedural statements in this block describes the analog behavior of the components
analog begin

//function call
ids = Fgfet( V(Vds) , V(Vgs) , V(Vbs) , Rs , mu , Ec , Cgio , Hsub , tox ,
                 L , W , ntop ,  Vgs0 , Vbs0 , k , k_sub);

//Branch contribution statements where branch extends from 1st net of the function to the 2nd net
I(Ids) <+ ids;
I(gate, source) <+ c1 * ddt(V(Vgs));    //time derivation
I(gate, drain) <+ c1 * ddt(V(Vgd));
I(back_gate, sourceint) <+ c2 * ddt(V(Vbsint));
I(back_gate, drainint) <+ c2*ddt(V(Vbdint));

if(r > 1e12*Resistor1.flow.abstol)
begin
I(Resistor1) <+ V(Resistor1)/Rs;
end

else
begin
V(Resistor1) <+ Rs * I(Resistor1);
end

if (r > 1e12*Resistor2.flow.abstol)
begin
I(Resistor2) <+ V(Resistor2)/Rs;
end

else
begin
V(Resistor2) <+ Rs * I(Resistor2);
end

end
endmodule
```

and saturation voltage. The channel length and width are heuristically selected to be 6.0 μm and 1.6 μm respectively. In order to consider the electron-hole asymmetricity, the contact resistance is considered different in n-channel and p-channel. As stated in [**58**], the resistance for electron is higher than that for holes and following that the series resistance in p-channel and n-channel are considered to be 600 Ω and 4,000 Ω respectively.

Similarly, Table 3.2 shows the characteristics of the designed GFET based LC-VCO.

Fig 3.5 shows the source-drain current-voltage relationship for NFET and PNFET around the operating region. As can be seen from the fig. 3.5(b), there is an evident of small saturation region at the operating region in the case of P-FET. For a V_{ds} less than $V_{ds,sat}$, the device operates

TABLE 3.1. GFET Device Parameters [**60**, **62**].

Device Parameter	Specific Values
mobility (μ)	0.3 m^2/(Vs)
length	6.0 μm
width	1.6 μm
Rs (p-channel)	600 Ω
Rs (n-channel)	4000 Ω
V_{supply}	9 V
I_{bias}	0.7 mA

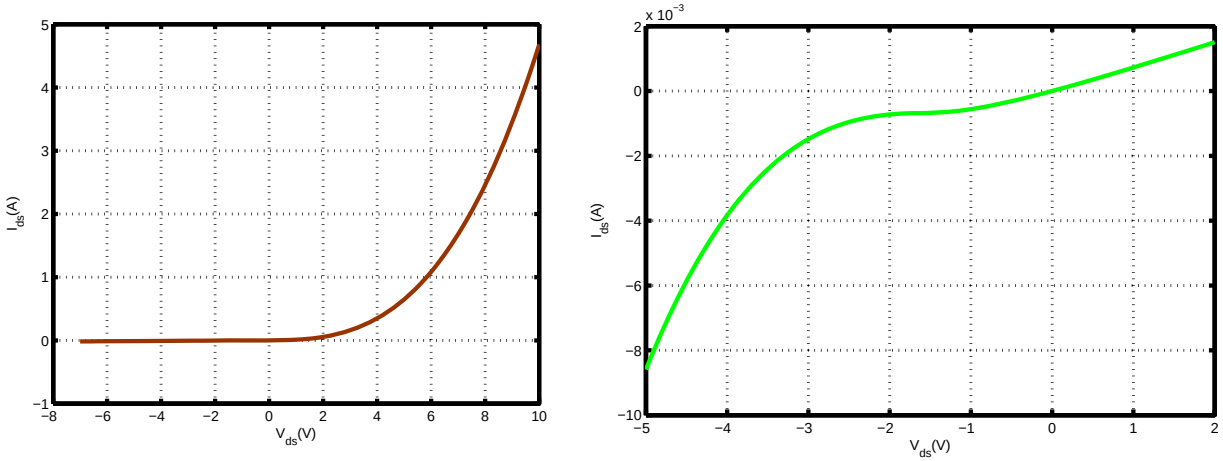
TABLE 3.2. Characteristization of GFET Based LC-VCO [**60**, **62**].

LC-VCO Characterization	Specific Values
f_{center}	2.56 GHz
$V_{tank,p-p}$	0.8 V
I_{bias}	0.77 mA
Tuning Range	4.88%
Phase Noise (1 MHz offset)	-88.25 dBc/Hz

in the first linear region after which the drain current saturates for the small range of V_{ds}. With increase in the V_{ds}, the drain current enters into the second linear region with a pronounced "kink" in the characteristic curve. The presence of "kink" signifies the presence of an ambipolar channel [**74**]. However in the case of N-FET, in fig. 3.5(a), the device operates in the second linear region, which lies above the kink region.

Fig 3.6 shows the tuning characteristics and the phase noise performance of the LC-VCO.

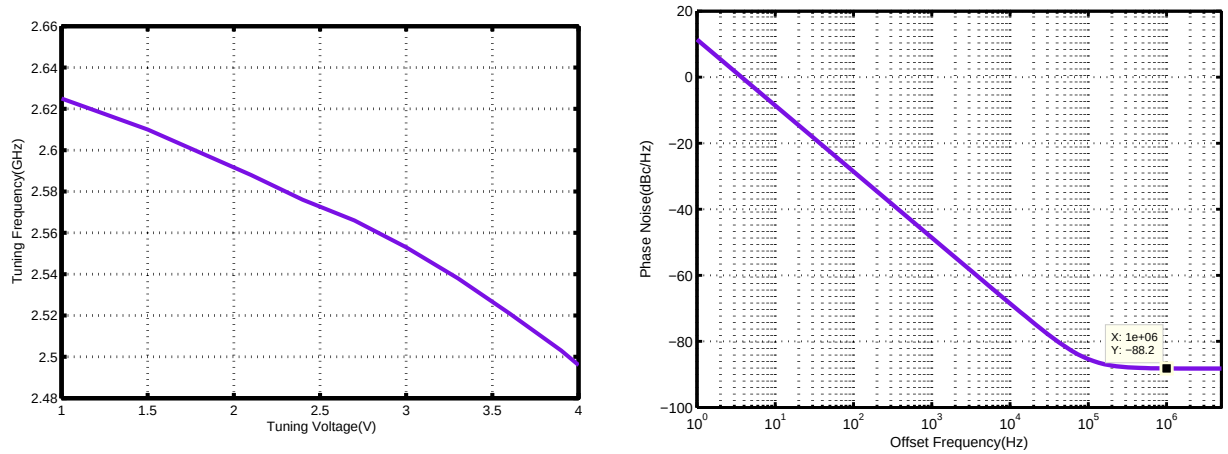
Fig. 3.7 shows the parametric analysis of the FET based LC-VCO. In fig. 3.7(a) and fig. 3.7(b), a sudden sharp fall in the frequency is observed in the frequency curve which corresponds to the resonating condition and is created in the tank circuit due to the GFET capacitances. In the optimal design of the VC-LCO, the GFET length and width should be chosen such that this resonance condition has to be avoided. Similarly, in fig. 3.7(c) and fig. 3.7 (d), the dependence of power dissipation on the channel length and width are shown respectively. According to Leeson's



(a) I_{ds} Vs V_{ds}

(b) I_{ds} Vs V_{ds}

FIGURE 3.5. (a) $I - V$ curve of NFET around operating region. (b) $I - V$ curve of PFET around operating region.

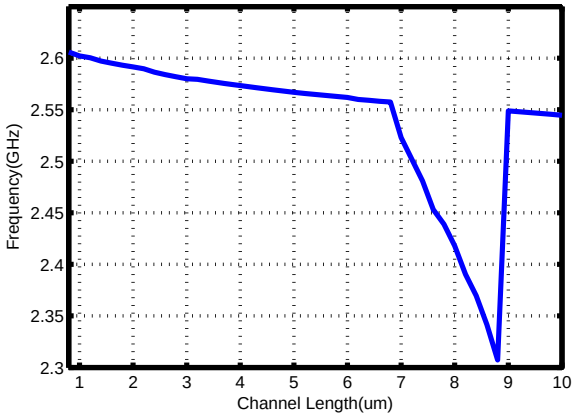


(a) Fequency Vs Tuning Voltage

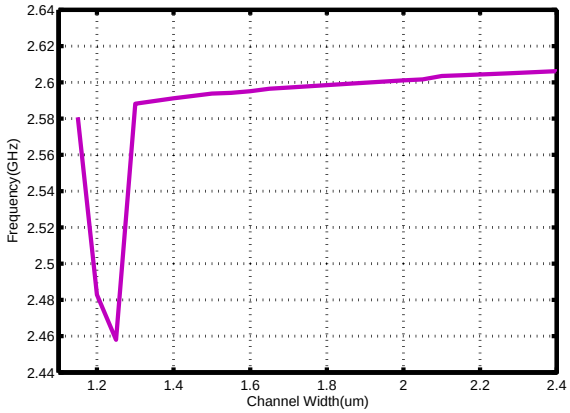
(b) Phase Noise Vs Offset frequency

FIGURE 3.6. (a) Tuning range (b) Phase noise Characteristics of the baseline GFET based LC-VCO.

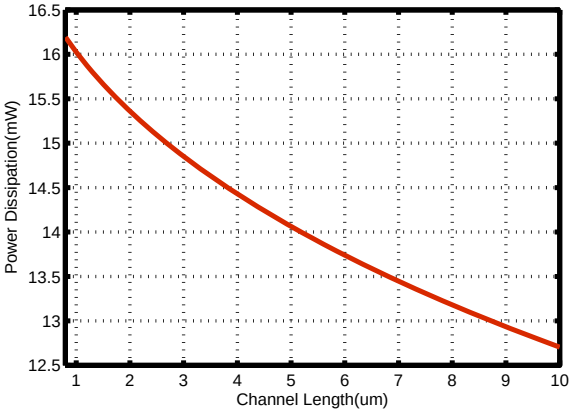
equation [**57**], the phase noise is proportional to the inverse of signal power and inversely proportional to the square of quality factor [**68**]. Thus the proper choice of channel length and width directly affects the operating frequency, power dissipation and phase noise in the LC-VCO design.



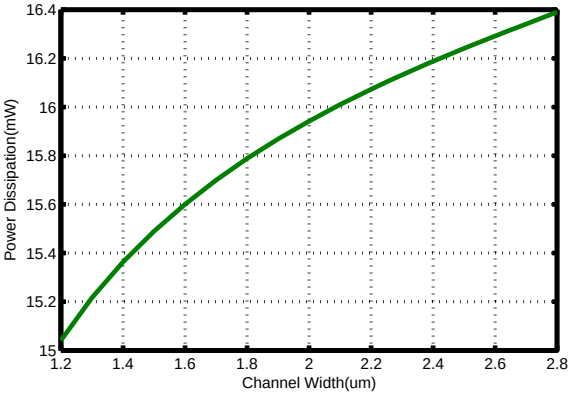
(a) Fequency Vs Length



(b) Frequency Vs Width



(c) Power Dissipation Vs Length



(d) Power Dissipation Vs Width

FIGURE 3.7. Characteristics of the GFET based LC-VCO.

CHAPTER 4

SIMSCAPE BASED MODELING AND ANALYSIS OF GRAPHENE CIRCUIT

Today electronic technologies have undergone an unprecedented and unforeseen advancement in its size, speed, computational efficiency, energy efficiency and cost. With already transistor count reaching billion in a die and the rate constantly increasing, it is becoming extremely challenging to shrink the transistor further down. Particularly below 10 nm, silicon (Si) looses its crystalline structure and becomes amorphous. Silicon in amorphous form have atoms in a continuous random order and due to this randomness, some atoms have dangling bond. These dangling bond show anomalous electrical properties which limit Si to shrink further down. Due to this inherent limitation of Si at lower technology node, designers are continuously opting for a possible replacement of Si for future nano-electronics. Also, the demand for nano-devices from consumer side has forced designers to bring more and more analog counterparts within a single chip, leading to analog mixed signal system-on-chip (AMS-SoC).

Since 1970s, SPICE has been an obvious choice for designers due to its accuracy. As already seen in chapter 3 that there are two device-level options available for SPICE/analog simulator to simulate a circuit netlist: verilog-A model and compact model. However conventional electronic design automation (EDA) based design flow posses few problems for future technologies in terms of accuracy, cost and complexity.

Thus as a paradigm shift of the conventional design simulation flow, this chapter presents a complete non-EDA based design simulation for ultra-fast design exploration of graphene based nano-electronic systems. In this chapter, a complete Simscape® based behavioral model of a GFET is presented [**4**, **10**, **48**]. The model accuracy is verified with the datas available from MATLAB [**74**], SPICE [**32**] and VHDL- AMS [**112**] based models presented in the literature. The same simulation framework is used to perform design exploration of two case study RF circuits: a low-input low-noise amplifier (LNA) and an LC-tank oscillator, which makes possible to compare the EDA and non-EDA based models. This is the first attempt ever to present GFET models written in the MATLAB® Simscape® physical modeling language. The novel contributions to the state-of-art

in nano-electronics based system simulation are the following:

(1) A Simscape® based ultra-fast design exploration which is a non-EDA flow and a paradigm shift from conventional EDA flow.
(2) Modeling of graphene FET devices using Simscape®.
(3) Modeling of a GFET based LNA using the Simscape® graphical environment.
(4) Modeling of a GFET based VCO using the Simscape® graphical environment.
(5) Experimental validation of the Simscape® device level models with existing VHDL-AMS or Verilog-A models.
(6) Characterization of GFET based case study circuits and comparison with Verilog-A based designs.

4.1. Verilog-A/SPICE Versus Simscape

With the growing demand for integration and shrinking process technology, more and more analog circuits are added into a single chip. It is estimated that at 45 nm and below technology, more than 60% of the SoC designs get re- spin due to the mixed signal error. Each of these re-spin is expensive in terms of cost (extra 5-10 millions) and time-to-market (8-10 weeks delay). Thus from the industries' perspective, it becomes very necessary to shorten these delays and minimize the cost as much as possible. It would not be an overstatement to say that all AMS-SoC design undergoes through a series of SPICE simulation. SPICE has been the obvious choice for industries since 1970s due to its capability to accurately simulate the integrated circuits (ICs) at schematic level (without parasitics) and at layout level (with parasitics) [**52**]. The major drawbacks with SPICE simulations are:

(1) Prolong design time due to heavy computational requirement. This increases the non-recurrent design cost of the chip.
(2) Need of fab data or TCAD simulation, which may not always be available especially for new and emerging technologies.
(3) Design optimization support is very limited.

In order to overcome these difficulties associated with the SPICE based design flow, this chapter proposes a non-EDA design flow. This non-EDA design flow, which is based on Simscape® , offers two distinct advantages over conventional SPICE simulation:

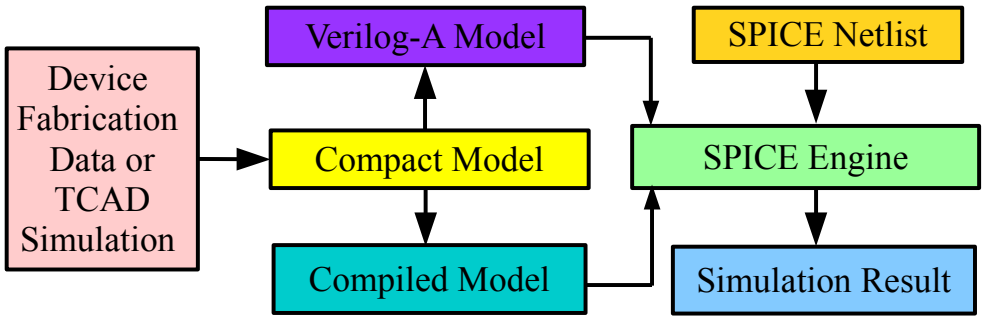
(1) The device level modeling is done using the basic physics and semiconductor principles. Thus, it does not need any fab data for modeling the components, which is very advantageous for emerging technologies, where fab datas are not yet available.

(2) It provides fast and easy optimization at system level. These advantages result in significant reduction in the design cycle time and hence the cost of ICs.

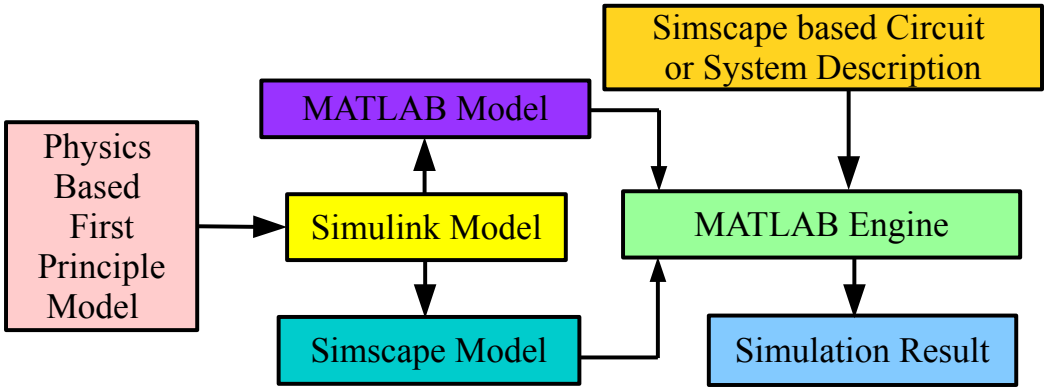
4.2. Why Simscape® is Necessary

Fig. 4.1 shows the comparison between the proposed non-EDA based design flow to the well-accepted conventional EDA based design flow [**59**]. In the conventional EDA based design as shown in Fig. 4.1(a), fab data or TCAD simulation for the specific technology is needed in order to derive the compact model. This first step itself introduces significant delays in the implementation of emerging technologies like graphene. The compact models are then converted to compiled models for incorporation in SPICE or analog simulation engine. These are quite effort intensive tasks and may increase the design cost as well as slows the simulation process. Due to heavy computational requirement, the conventional SPICE based EDA design flow used for large circuits is extremely slow. Furthermore, SPICE tools do not have comprehensive design optimization options available which in effect makes it difficult to manage trade-off among requirements like stability, robustness and performance.

In contrast, the proposed Simscape® based non-EDA design flow depends on the first principle models published in the physics/semiconductor literatures. This implies that any emerging technology can be implemented immediately without the need to wait for fab data. This becomes conducive to evaluate the new technologies and their performance. Hence, making it very adaptable to a new emerging technology. The target circuit or system can then be designed using the Simscape® graphical based tool interface. As shown in Fig.4.1(b), the device level models presented in the MATLAB®, Simulink®, or Simscape® language is then simulated in the MATLAB® engine. Furthermore, using MATLAB® optimization function or Simulink® optimization toolbox,



(a) SPICE based Design Simulation Flow



(b) Simscape based Design Simulation Flow

FIGURE 4.1. SPICE versus Simscape® based Design Simulation Flow.

it is ultra-fast and easy to finely tune the design parameters with minimal computational overhead. An added feature of Simscape® is that the results are automatically saved in the MATLAB® workspace thereafter making it extremely easy for analyzing and post-processing. However, this design flow shows some loss of accuracy which can be considered as a design trade-off between cost and\or computational time vs accuracy.

4.3. Simscape Based Modeling and Simulation Flow

Simscape® is part of MATLAB®/Simulink® which is capable of multi-domain, multidiscipline modeling and simulation of physical systems. The Simscape® framework includes a variety of physical component libraries. Essentially, there are two ways to build custom Simscape® models for emerging devices like the GFET: (i) a graphical method using fundamental Simulink® /Simscape® blocks, or (ii) textually with the Simscape® physical modeling language. Since the later

approach offers better portability and is easier to maintain, the modeling is done with this approach. In addition, this approach makes hierarchical modeling and simulation of complex system easier as well.

This section briefly explains the GFET modeling in Simscape® environment. A physical component is designed in Simscape® using three sections: declaration section, setup section and an equation section, as shown in the Fig. 4.2 [**4**].

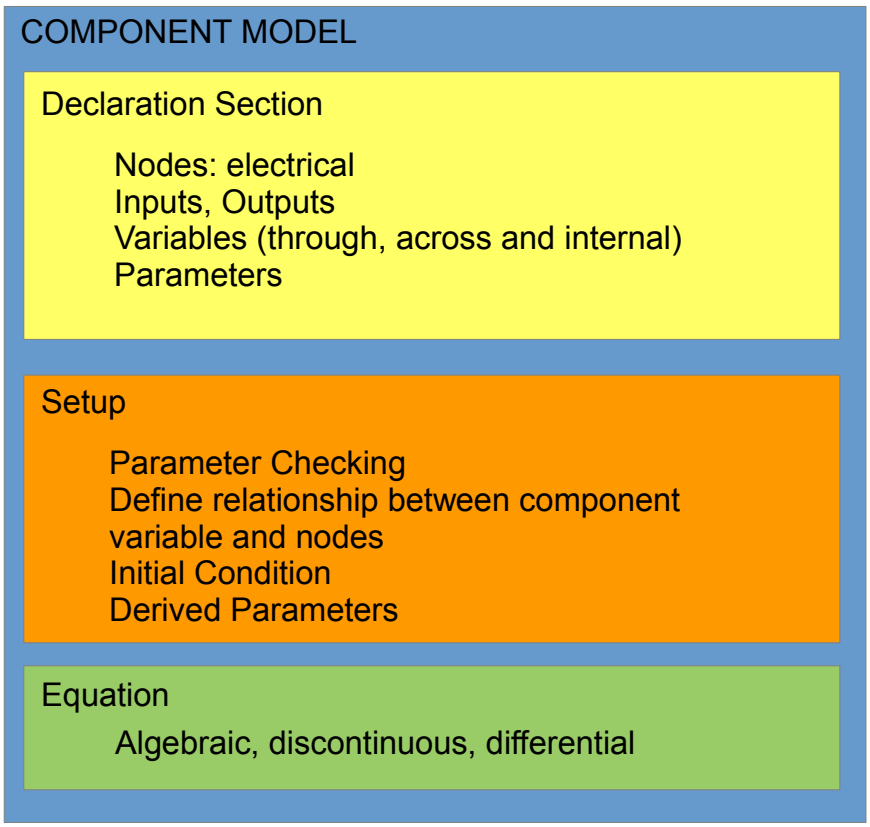


FIGURE 4.2. Simscape simulation setup for GFET device simulation. After [**4**].

The declaration section starts with the keyword "component" which specifies that a component is going to be designed in the Simscape® built-in domain. In this section, component members (like nodes, inputs, outputs, variables, parameters) are declared. The nodes define the physical ports and reuse the Simscape® physical domain to create domain compatible components. GFET have four nodes defined as S, G, D, BG for source, gate, drain and back gate respectively. The variables defined in this section are used later in the equation sections. The last part in the decla-

ration section is the parameters, which are the values that users want to change. Both the variables and parameters are needed to be defined along with their units.

The next section is the setup section, which is used to validate parameters, compute derived parameter, set initial conditions and define relationship between node and variables. The across and through variables are also defined here. This section is executed once per component instance during model compilation, using regular MATLAB® commands.

The final section is the equation section, which establishes mathematical relationships among component variables, inputs, outputs, time and time derivatives. In the equation part, conditional statements can be defined using the if statements exactly the way it is used in MATLAB®. The "==" operator is used to specify the symmetrical mathematical relationship and is nothing to do with assignment or logical operation.

Once the model is written in Simscape®, it needs to be built for later use in the Simulink® , where the circuit/system is built using that component, as shown in fig. 4.3. In order to built the component in Simscape®, two conditions need to be satisfied: (1) the parent directory must begin with the "+" sign, and (ii) the parent of the top level directory must be in the MATLAB® path. After satisfying these two requirements, the model can be built using "ssc_build" command in MATLAB® command window, which then generates the .mdl model in the parent of the top level directory. The complete proposed Simscape® model for GFET is presented in Algorithm 1.

4.4. Experimental Setup of Results

In order to compare the proposed Simscape® model with well accepted EDA model, the GFET model is based on the VHDL-AMS model from [**112**] and the Verilog-A model from [**62**]. The Simscape® simulation results show good agreement with the prior results presented in [**61**, **74**, **104**, **105**, **112**]. The set of equations from (7) to (14) are used in order to model the GFET in Simscape®. The component built using Simscape® is then used in Simulink® as shown in fig. 4.3.

The $I-V$ characteristic of the GFET drain-to-source voltage and current is shown in fig. 4.4. The device parameters selected are based on published results [**122**]. For a negative V_{bs}, the GFET source/drain region is p-type [**74**, **105**, **112**] and the mobility $\mu = 700$ cm^2/V/s, $R_s = 800\,\Omega$, and $E_c = 4.5$ kV/cm. The top-gate voltages of 0 V, -1.5 V, -1.9 V and -3 V were used and V_{ds}

Algorithm 2 Proposed model for a GFET.

```
component GT
nodes
p1 = foundation.electrical.electrical; % S:top
p2 = foundation.electrical.electrical; % G:top
p3 = foundation.electrical.electrical; % D:top
p4 = foundation.electrical.electrical; % BG:bottom
end
parameters
Rs = {800, 'Ohm'};
mu = {700,'cm^2/s/V' };
Ec = { 4.5e5,'V/m' };
Cgio = { 0.8072,'1' };
Hsub = { 285.0e-9,'m' };
tox = { 15e-9, 'm' };
L = { 1e-6, 'm' };
W = { 2.1e-6, 'm' };
ntop = { 2.1209e16,'cm^-3' };
Vgs0 = { 1.45, 'V' };
Vbs0 = { 2.7, 'V' };
k = { 16, '1' };
k_sub = { 3.9, '1' };
pi = { 3.1415926, '1' };
q = { 1.60e-19, 'c' };
eps0= { 8.854187817e-12, 'F/m' };
h= { 6.62606876e-34, 'J*s' };
vf={1e6,'m/s'};
end
variables
Vds= {1,'V'};
Ids={1,'A'};
Vgs= {1,'V'};
Vbs= {1,'V'};
Ctop ={1,'F/cm^2'};
Cback ={1,'F/cm^2'};
Vo ={1,'V'};
Vg0 ={1,'V'};
Vc ={1,'V'};
Rc ={1,'Ohm'};
Gamma ={1,'1'};
Vdsat ={1,'V'};
Io={1,'A'};
end
function setup
across(Vds, p3.v, p1.v);
through(Ids, p3.i, p1.i);
across(Vgs, p2.v, p1.v);
across(Vbs, p4.v, p1.v);
end
equations
let
Cq = q^2*(ntop/pi)^0.5/(vf*(h/(2*pi)))
Ce = Cgio*eps0*k/tox;
in
Ctop == Cq*Ce/(Cq+Ce);
end
Cback == eps0*k_sub/Hsub;
Vo == Vgs0 + (Cback/Ctop)*(Vbs0 - Vbs);
Vg0 == Vgs - Vo;
Vc == Ec*L;
Rc == 1.0/((W/L)*mu*Ctop*Vc);
Gamma == Rs/Rc;
Vdsat == (2*Gamma*Vg0/(1+Gamma)+ (1-Gamma)/(1+Gamma)^2*(Vc-(Vc^2-2*(1+Gamma)*Vc*Vg0)^0.5));
Io == 2.0*(W/L)*mu*Vc*Ctop*(Vgs-Vo-Vds/2.0);
if (Vds > Vdsat)
Ids == 1/4/Rs*(Vds-Vc+Io*Rs + ((Vds-Vc+Io*Rs)^2 - 4*Io*Rs*Vds)^0.5);
else
if (Vds <= Vdsat)
Ids == (Gamma/Rs/(1+Gamma)^2*(-Vc+(1+Gamma)*Vg0+(Vc^2-2*(1+Gamma)*Vc*Vg0)^0.5) +
mu*Cback*abs(Vbs-Vbs0)*Vds*W/L/10*(Vds/Vdsat -1)^2);
else
Ids == 0.0;
end
end
end
end
```

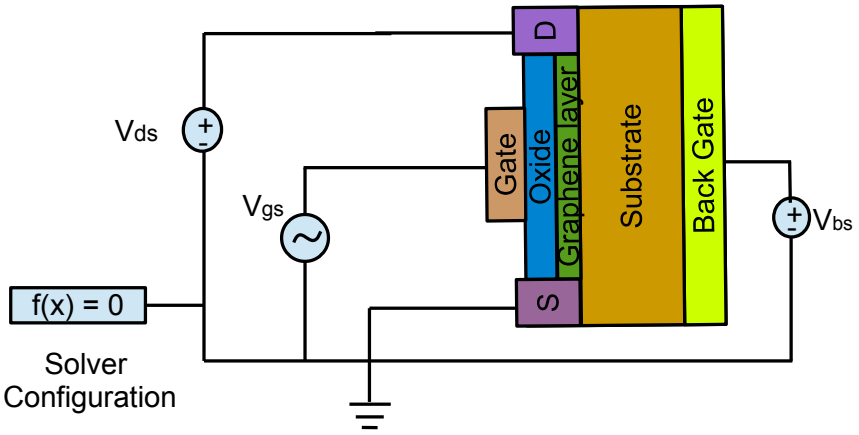


FIGURE 4.3. Simscape simulation setup for GFET device simulation.

is varied from 0 to -3 V. When $V_{bs} = 4.0$ V, the source/drain region is n-type. with $\mu = 1200$ cm^2/V/s, $R_s = 1500\ \Omega$, and $E_c = 15$ kV/cm. In Fig. 4.4, top-gate voltages of -0.8 V, -1.3 V, -1.8 V, -2.3 V, and -2.8 V were used and V_{ds} is varied from 0 to -3 V. The top gate capacitance (C_{top}) of the transistor was 759.5 nF/cm^2 and $C_q = 1.995\ \mu$F/cm^2 while the back gate capacitance was 12.12 nF/cm^2. The resultant $I - V$ characteristic curves are similar to the results obtained in VHDL-AMS [**74**, **112**] and in Verilog-A models discussed in [**62**].

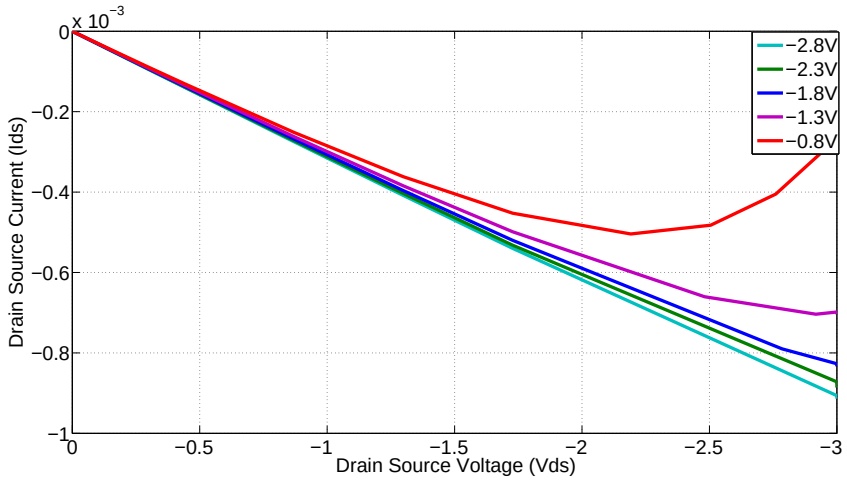
In order to demonstrate the applicability and accuracy of the Simscape® based design simulation flow, the following two sections demonstrate two test circuits used as case study.

4.5. Case Study 1: GFET Based Amplifier Circuit

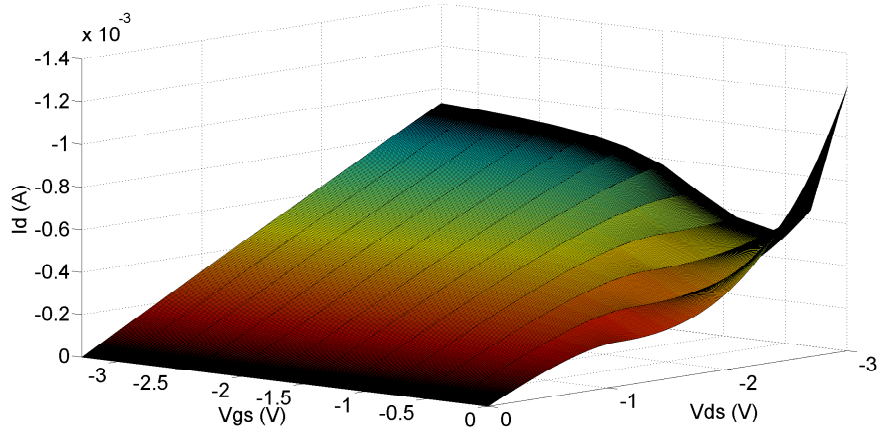
This section considers an amplifier circuit as the first case study for this paper.

4.5.1. Theoretical Perspective

The Low-Noise Amplifier (LNA) is one of the most important components of an RF receiver and is used to amplify very weak signal in RF circuits. It is located close to the antenna and is highly susceptible to electromagnetic, thermal and transmission noise. Since it can detect even a small change at the receiver, the LNA must have intrinsically low noise. The four important design parameters in LNA design are the following: (1) gain, (2) noise figure (NF), (3) non-linearity, and (4) impedance matching. Low NF results in better signal reception and in order to process signals effectively, high gain is necessary. If the LNA does not have high gain then the signal will be



(a) I-V Characteristics



(b) Surface Plot

FIGURE 4.4. $I - V$ characteristics for discrete and continuous values of V_{gs} for N-type GFET.

affected by the noise in the LNA circuit itself. The typical trade-off is to minimize the noise of the circuit by accepting fairly low gain which is alleviated in subsequent stages of the receiver. In its simplest form, an LNA consists of a common source amplifier and a load. Fig. 4.5 shows the schematic diagram of such a simple, all-graphene LNA [**28**]. In this circuit, G_1 acts as a load and G_2 acts as a common source amplifier transistor. The graphene nanoribbon widths W_1 and W_2 for devices G_1 and G_2 are chosen as the design variables. The gain (G), bandwidth (F_T) and

power consumption (P_{LNA}) are considered as the figures-of-merits (FoMs) of the LNA. Due to its simplicity, this circuit is amenable to exhaustive design exploration and is one of the reasons for its adoption as a test case to validate the Simscape® model.

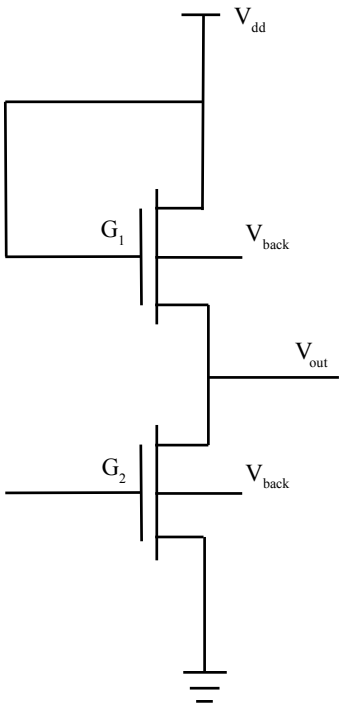


FIGURE 4.5. Schematic of a GFET based LNA circuit. G_1 is the load transistor and G_2 is the amplifier.

For the following discussion, g_m, and g_d denote the small-signal transconductance and output conductance of the transistor G_2, respectively, and R_L is the the load resistance of the transistor G_1. Simple small-signal analysis of the equivalent circuit gives the gain of the LNA as follows:

$$G = \frac{R_L g_m}{R_L g_d + 1}. \tag{24}$$

The bandwidth f_T is given by the following expression:

$$f_T = \frac{g_m}{2\pi C_{in}}, \tag{25}$$

where C_{in} is the input capacitance of the circuit. In this analysis, the effects of interconnect and overlap capacitances (gate to drain/source) are neglected. However, given a particular process and

the device geometry, these can be readily added to the model. Similarly, the power consumption can be approximated as the sum of the active power dissipated by G_2 and the passive power dissipated by G_1, which is presented as follows:

$$P_{LNA} = P_{G_1} + P_{G_2}, \tag{26}$$

The above expression can be rewritten as follows in terms of current and voltage:

$$P_{LNA} = I_{ds}^2 R_L + V_{ds} I_{ds}. \tag{27}$$

Given fixed lengths L_1 and L_2 for devices G_1 and G_2, respectively, the set of equations (24), (25) and (27) defines a multi-objective optimization problem with W_1 and W_2 as the design variables, f_T as a constraint and the concurrent optimization of G (max.) and P_{LNA} (min.) as the objective functions. A typical objective function that satisfies these requirements could have the form:

$$\text{minimize} \quad \alpha P_{LNA} + \tfrac{\beta}{G}, \tag{28}$$

$$\text{s.t.} \qquad \tfrac{|\Delta f_T|}{f_T} \leq \epsilon, \tag{29}$$

where α and β are the weights based on the relative importance of the power and gain, respectively, $\Delta f_T / f_T$ is the relative perturbation of the bandwidth during the optimization process and ϵ is an acceptable margin in this perturbation.

A quantitative justification for the selection of W_1 and W_2 as the design variables can be obtained by examining the dependence of the parameters in (24), (25) and (27) on these variables. Bare graphene is semimetal with zero bandgap (E_g). E_g can be created with graphene nanoribbon (GNR) due to size quantization. It has been shown that E_g is inversely proportional to the width of the nanoribbon [**28**]:

$$E_g = \frac{k}{W}, \tag{30}$$

where k is a proportionality constant, W is given in nm and E_g is given in eV.

It has been experimentally verified that g_m is proportional to the width of a GFET transistor. Thus, from (30) we see the following relation [**28**]:

$$g_m \propto W \propto \frac{1}{E_g} \tag{31}$$

The drain-source voltage is related to the channel voltage (V_{ch}) by [**28**]:

$$V_{ds} = V_{ch} + \frac{E_g}{2}, \tag{32}$$

while the relationship between channel voltage and gate-source voltage at that operating point is straightforward:

$$V_{gs} = V_{ch}. \tag{33}$$

I_{ds} vs. V_{gs} and I_{ds} vs. V_{ds} characteristics of device G_2 in the LNA are shown in fig. 4.6(a) and fig. 4.6(b), respectively. The results obtained from the simulation for the amplifier transistor closely matched published data [**29**,**74**]. In particular, the kink in I_{ds} is accurately modeled by the inclusion of a displacement current, as shown in equation (14).

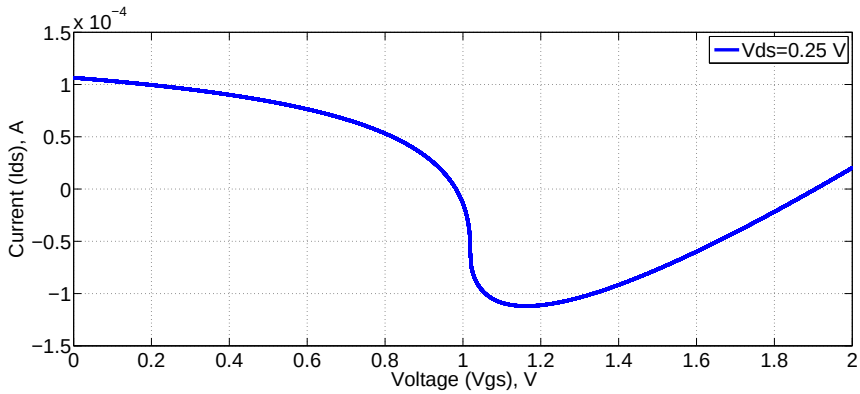
4.5.2. Simscape® Modeling of the LNA

For simulation of LNA, the transistor configuration is modified. The Simscape based simulation setup of the LNA is presented in Fig. 4.7. In the LNA simulation, GFETs with $T_{ox} = 1$ nm, $H_{sub} = 2.85$ nm, and $L = 50$ nm were used. W for both transistors has been varied for all simulations. Fig. 4.8 shows the relation of $R_L,\ E_g$, and g_m with the width of the transistor. From the result, it can be observed that $R_L,\ E_g$, and g_m are inversely proportional to W as is given in (31). The results match those presented in [**28**].

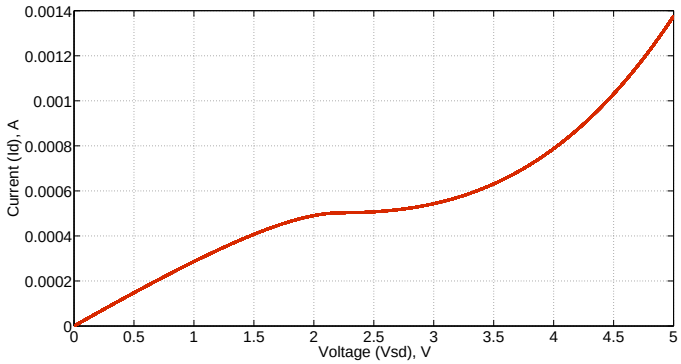
The result showed the inverse relationship between the band-gap and gain as demonstrated in [**28**] and the GFET based LNA is shown to have a small-signal bandwidth of 3.119 GHz. Table 4.1 summarizes the basic characteristics of the LNA for two different transistor sizes.

4.6. Case Study 2: Graphene Based Oscillator Design

The second case study circuit considered in this Simscape® based design simulation is an oscillator circuit.



(a) I_{ds} vs. V_{gs}.



(b) I_{ds} vs. V_{ds}.

FIGURE 4.6. GFET charasteristics (amplifier device G_2 in the LNA).

TABLE 4.1. GFET based Amplifier Figures-of-Merit

Parameters	Values	Values
W_1	20 nm	30 nm
W_2	10 nm	15 nm
Gain (G)	14.54 dB	15.41 dB
Bandwidth (f_T)	3.12 GHz	3.12 GHz
Power (P_{LNA})	23.8 mW	27.2 mW

4.6.1. Theoretical Perspective

Oscillators are widely used in data communication systems and are the most important components of Phase-Locked Loops (PLLs). Due to their high carrier mobility even at room tem-

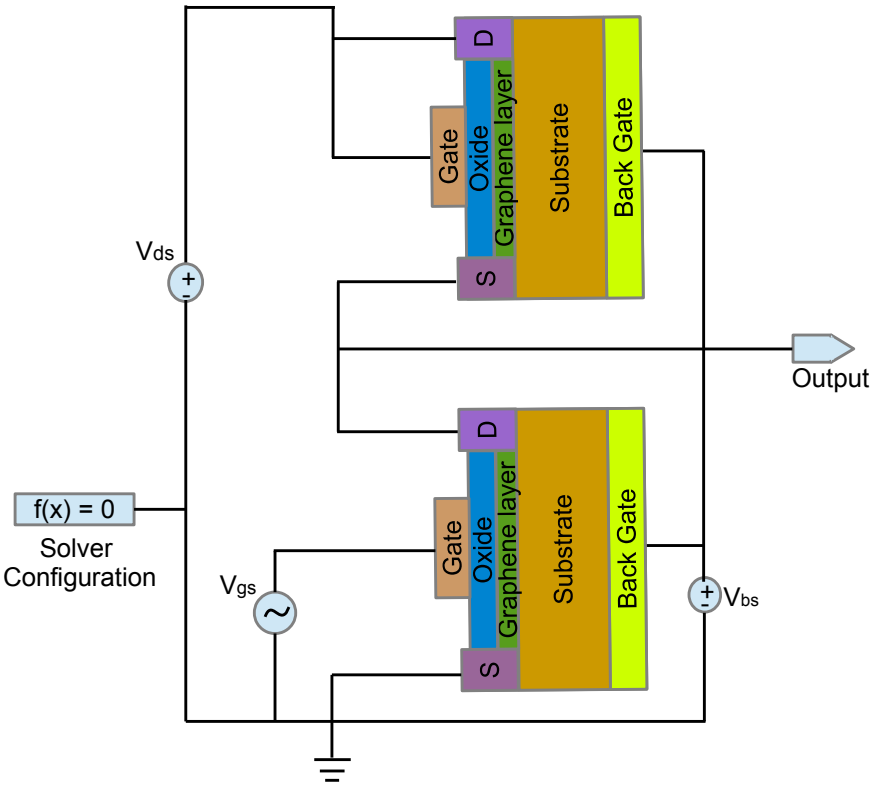
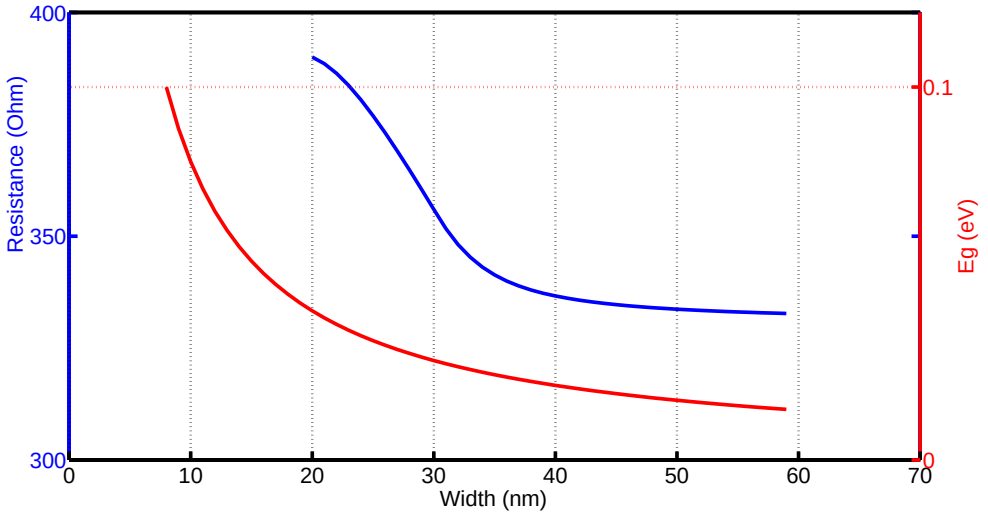


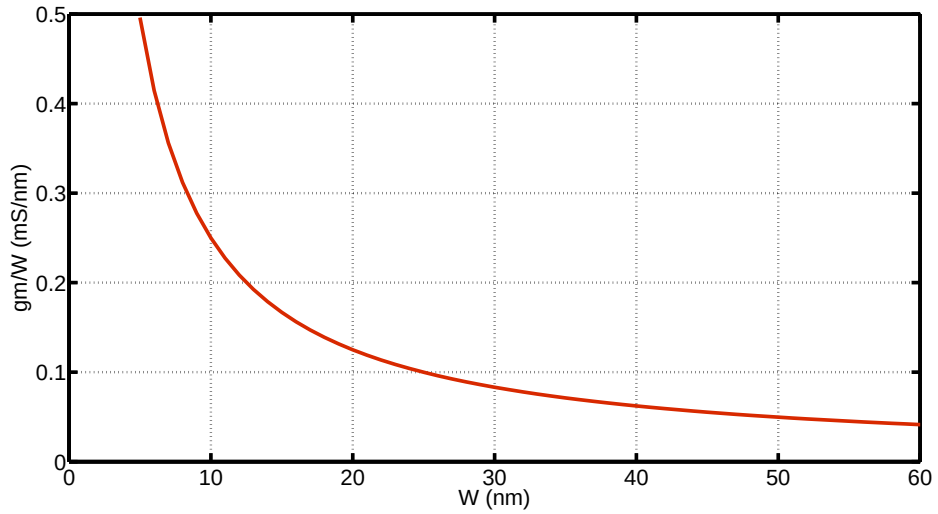
FIGURE 4.7. Simscape® Experimental Setup for LNA Simulation.

perature, GFETs can be used for high speed and high frequency communication systems. In order for GFETs to be useful as a building blocks for analog and digital electronics, it must exhibit intrinsic gain (i.e. ratio of transconductance to output conductance) greater than 1. Recent reports have showed that over-unity voltage gain has been achieved at room temperature, which enabled the use of GFETs in analogue electronics [**99**]. [**71**] showed that the GFETs with a cut-off frequency of 100-300 GHz has been fabricated.

Fig. 4.9 shows the schematic of cross-coupled oscillator. NFETs are used to set an appropriate bias point. The back gate and top gate voltages are applied to control the threshold voltage following equation (11) [**112**]. In order to create an n-type channel, the top gate voltage is biased positively as compared to the threshold voltage and to create a p-type channel, the top gate voltage is biased negatively compared to the threshold voltage [**105**]. The frequency of oscillation is given



(a) R_L and E_g vs. W



(b) g_m/W vs. W

FIGURE 4.8. GFET based LNA charasteristics.

as:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{34}$$

Fig. 10(a) and fig. 10(b) show the I–V characteristics for NFET for different top gate voltages.

In order to start the oscillation, the transconductance of the active device should follow the

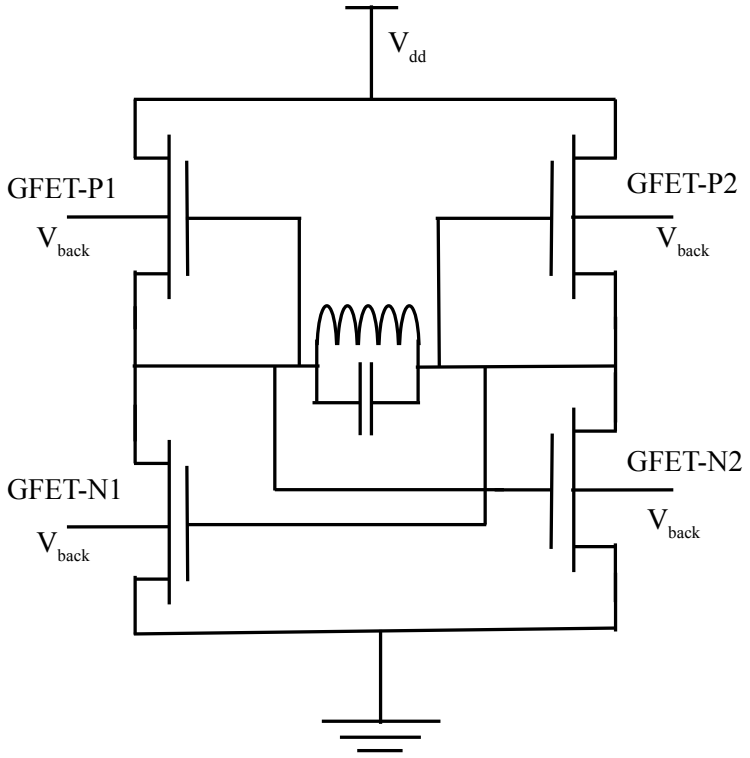


FIGURE 4.9. Schematic of LC oscillator using GFET (Same Circuit presented in the previous Chapter.).

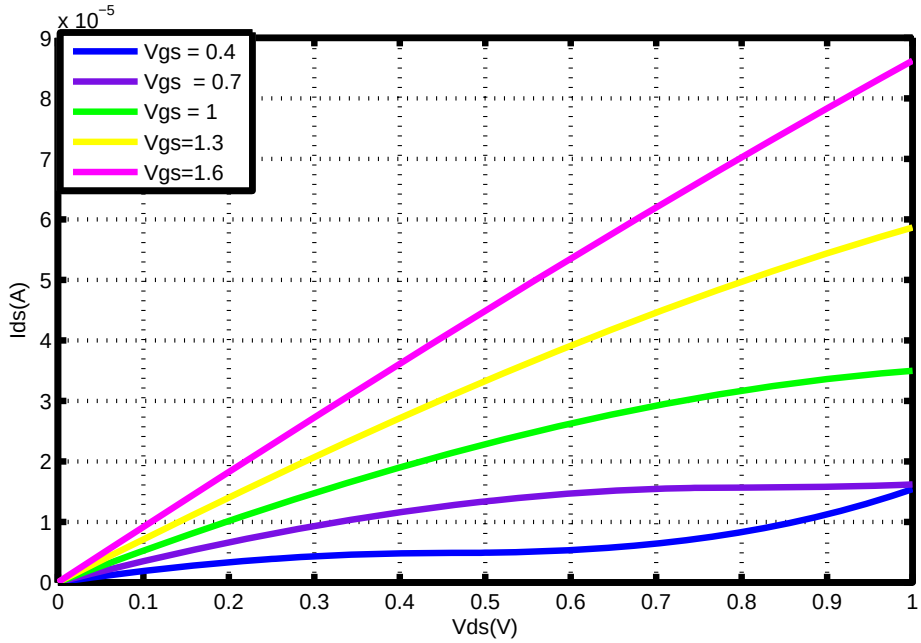
following equation:

$$g_{active} \geq \frac{RC}{L}, \tag{35}$$

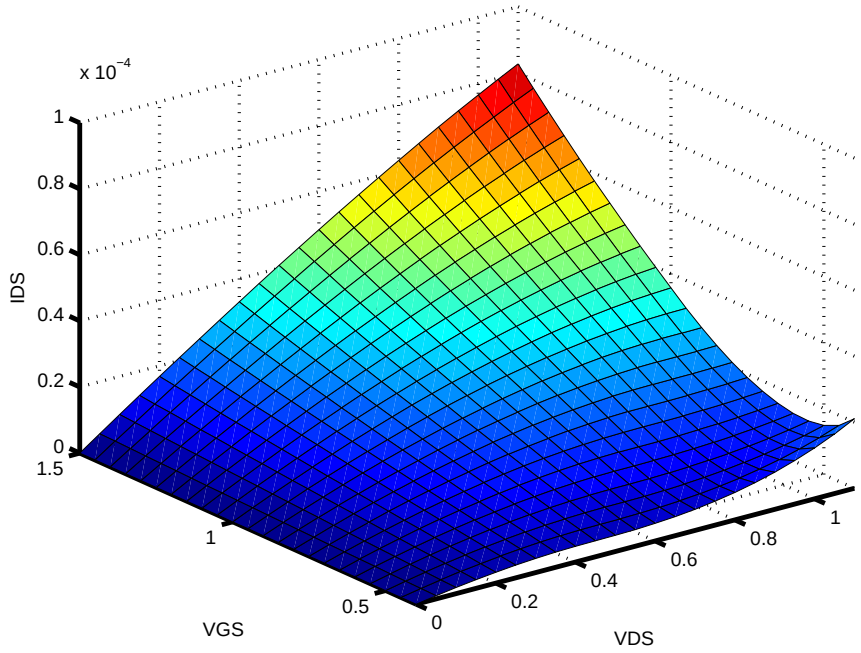
where R is the resistive loss of the tank due to the parasitic resistance of inductor. The transconductance of the active device is controlled by modifying the parameter W while keeping the channel length of both PFET and NFET fixed. In the current limited region, the output voltage swing is defined by:

$$V_{tank} = \frac{I_{bias}}{g_{tank}}, \tag{36}$$

where I_{bias} denotes the bias current and g_{tank} is the total tank conductance. When the oscillator enters the voltage limited region, output voltage amplitude is limited by supply voltage and the operating region of active device.



(a) I_{ds} Vs V_{ds}



(b) I_{ds} Vs V_{ds}

FIGURE 4.10. (a) $I-V$ characteristic of NFET for different top gate voltages. (b) Surface plot showing $I-V$ curve for continuous change of the top gate voltage.

4.6.2. Simscape® Modeling of the Oscillator

To configure the n-channel transistor, the critical electric field (Ec) is set to 15 KV/m [**122**]. The back gate voltage and width of the channel are characterized to obtain the desired bias point. Fig. 4.11 shows the Simscape® based simulation setup. In order to perform accurate simulation, the solver used in this paper is ODE14X (Extrapolation), which has the minimum possible step size. The PFETs are arranged in a cross coupled topology and are characterized to operate close to the saturation region, as shown in Fig. 12(a). In order to achieve over unity intrinsic gain, the source to drain conductance are reduced. The back gate voltage is set to obtain appropriate charge neutral point and so forth desired bias point.

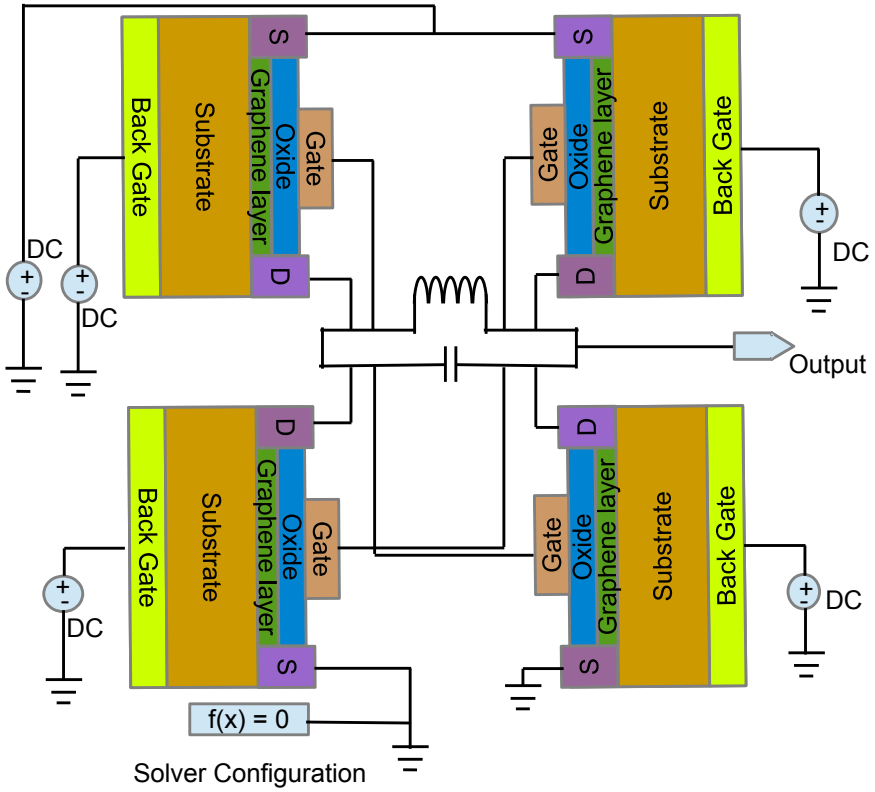


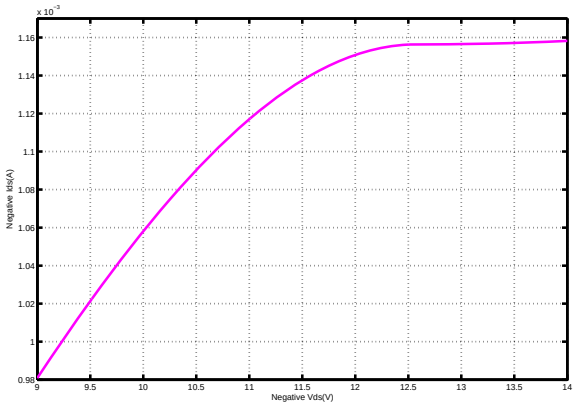
FIGURE 4.11. Simscape® Model of Graphene based Oscillator.

Figs. 4.12(b) and 4.12(c) illustrate the desired curves to obtain the required transconductance and drain conductance parameters. Fig. 4.12(d) shows the obtained drain current and drain voltage curve. Table II summarizes the basic features of the oscillator. The oscillator is designed to operate at an 1.8 GHz frequency having tank voltage swing 1.286 $V(p-p)$. Eqn.(36) suggests

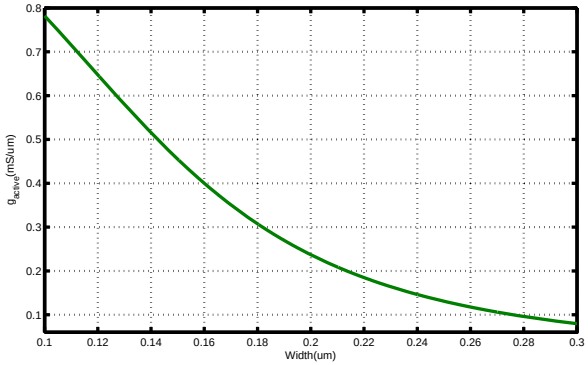
that the tank amplitude should be higher but the operation region of the active device limits this amplitude. Since in GFET saturation doesn't persist for large operating region, so to keep output voltage swing in the inductive limited region, either bias current has to be increased or the tank conductance has to be reduced. But if either steps is taken, oscillation doesn't build up. So an optimization is needed and it is kept as a further research. The Simscape® based LC-VCO results are consistent with the Verilog-A based discussed in [**62**]. Thus, the proposed Simscape® based design flow generates consistent results as the well-proven EDA based design flow.

TABLE 4.2. GFET based Oscillator characterization.

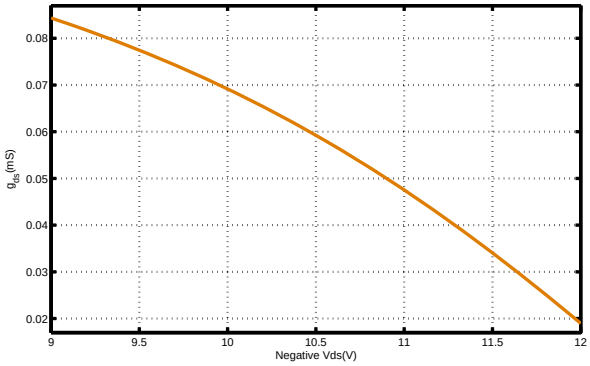
GFET Oscillator Characteristics	Estimated Values
f	1.8 GHz
$V_{tank}(p-p)$	1.286 V
I_{bias}	4.6 mA
g_{tank}	0.1336 mS
g_{active}	4.6787 mS
g_{ds}	1.7238 mS



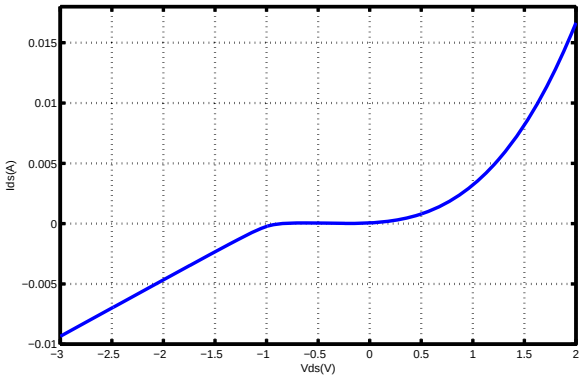
(a) I_{ds} Vs V_{ds}



(b) g_{active} Vs W



(c) g_{ds} Vs V_{ds}



(d) I_{ds} Vs V_{ds}

FIGURE 4.12. (a) $I - V$ Characteristic of PFET around operating point. (b) Transconductance of PFET for variation in width. (c) Drain to source conductance of PFET encompassing operating point. (d) $I - V$ characteristic of NFET around operating point.

CHAPTER 5

OPTIMIZATION FOR GRAPHENE BASED CIRCUITS

A design flow for graphene FET based analog circuit is presented in this chapter. The design of digital circuits in digital domain is comparatively simple due to the fact that the designer can segment the problem into various abstraction levels and solve those segments using tools comprehended at that particular level. There are industrial standards in this domain and any new tool can be proposed and allocated properly in the design flow. However in the analog domain, there is still no well-defined flow due to several reasons like:

(1) complex interrelation between several stages of the design,

(2) interconnected design flow through feedbacks where low-level design needs to be considered even at high level stage,

(3) greater number of freedom in the design variables and a lack of clear interconnection among them,

(4) infinite range of values and measurements needed for considering second order and higher order effects,

(5) trade-offs are not straight forward like speed vs power in digital domain,

(6) integration of analog, RF and digital design onto the same die brings issues like substrate noise and so on.

So there is a clear gap in the automation level between analog and digital domain. So to reduce the time-to-market for analog design and also for mixed-signal design, it is required to have a proper analog design flow. Still most of the steps in analog design are handcrafted which runs through a manual place and route. Furthermore simulation, data analysis and the effects of process variation make the overall design time longer. In addition to it, optimization of such circuit requires longer design cycles in order to search for the optimum design space to obtain the design goal.

So, this chapter considers a cross coupled version of LC oscillator (same circuit from chapter 3) as a case study to propose fast design optimization for a mixed-signal integrated circuit design flow. Various optimization techniques have been used in the literature in optimizing ana-

log circuits. Swarm optimization, simulated annealing, and evolutionary algorithms are common [**36**, **42**, **49**]. Bee colony optimization and particle swarm optimization are examples of swarm optimization techniques. However in this chapter, a multi-swarm optimization algorithm is used to explore the design space of the GFET based LC-VCO, where the objective is to maximize the frequency with phase noise and power dissipation considered as constraints. The design variables for the optimization are the length (L) and width (W) of the graphene channel. The multiple swarms of particles are generated to search the design space. The oscillator is implemented in Verilog-A based on [**112**].

This is the first attempt to propose a design flow for GFET based cross-coupled version of an LC oscillator. A new optimization algorithm called multi-swarm optimization (MSO) is used in the design flow, which is also a new attempt. The output of this optimization flow gives the proper sizing of the GFET device so as to achieve the maximum frequency. Thus, this chapter is a forward step in the design and optimization of GFET based RF circuits where an LC oscillator is used as a case study.

5.1. Why Optimization is Necessary

The objective of an optimization problem is to achieve the best possible design for a given set of constraints. It has a wide range of applications in management science, industry and engineering. With the scaling of semiconductor devices, the level of integration and the number of circuit components have increased tremendously in an integrated circuit (IC). The functionalities of the ICs are also increased. Thus the design of electronics components are becoming very challenging. For example, choosing proper component size like lengths and widths can be very crucial in terms of performance, reliability, size, efficiency, time-to-market and cost while meeting the design constraints like performance, efficiency, noise, reliability, time-to-market.

With the additional challenges like process variations, interconnect, reliability, manufacturability, power dissipation, power consumption, clock distribution, noise and cross-talk at the nanometer level, the design of modern circuit design is increasingly becoming more and more complex. Furthermore, there is a very complex inter-relationship among device variables like length, width, dielectric thickness and so on. So choosing proper values to the design variables

and satisfying the design constraints is one of the crucial challenge for modern semiconductor designers. Manual design of the modern electronic device is a very complex, tedious and laborious and requires skilled professionals. Thus in this scenario, it becomes very efficient approach to formulate the design objective function, choose the appropriate design variables, specify the design constraints and then solve the optimization problem. The final solution then obtained gives the best fit of the objective function meeting all the constraints.

Furthermore, the design of modern analog and digital systems undergo through a series of complex and time consuming steps. The search space grows exponentially with the problem size. So it becomes very critical to design the circuit in less number of iteration so as to reduce time-to-market. Thus choosing proper values for design variable along with choosing proper optimization techniques are an important part of the modern circuit design.

5.2. Introduction to Optimization

Optimization is a mathematical technique which is used to find the maximum or minimum of a given problem (or function) in a feasible region. All optimization problem has a fitness function, which either needs to be maximized or minimized. If a fitness function f(x) is to be maximized then it is equivalent to minimizing the function -f(x). The final solution gives the best value of the fitness function in a given search space for the given problem satisfying all set of constraints. Depending upon the way the problem is characterized, an optimization problem can be a constrained optimization (where the variable(s) need(s) to satisfy certain criteria), unconstrained optimization (where the variable(s) has/have no restriction) or a dynamic optimization (where the fitness function changes with time). Similarly, an optimization problem can be a linear optimization problem or non-linear optimization problem. Most of the real life problems are non-linear in nature. Linear optimization techniques are generally simple and fast. So, the traditional optimization approach is to convert non-linear problem into a linear one and then use a linear optimization techniques to solve it. Solving non-linear problem by linear techniques may not always give accurate solution. Furthermore, it is extremely difficult to convert non-linear problems into linear form due to the complex nature of the objective function as well as the constraints. Non-linear optimization problems are generally difficult to solve and for this reason many techniques have been evolved in the

past decade to solve these class of problems.

Modern optimization techniques like swarm intelligence, neural network, genetic algorithm, fuzzy optimization are quite effective in solving complex engineering problems [**109**]. In this chapter swarm intelligence technique is going to be explored.

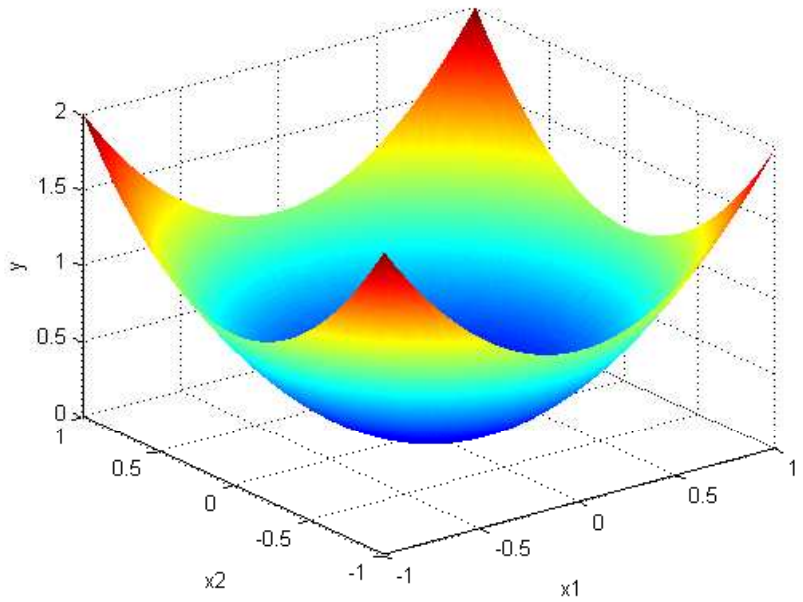
5.2.1. Swarm Intelligence

Swarm intelligence explores the collective behavior of self-organized systems like ant colony, bee swarming, bird flocking, fish schooling and so on to solve the given problem. Among many swarm intelligence techniques, Particle Swarm Optimization (PSO) and Ant Colony Optimization (ASO) are the most commonly used. These optimization algorithms learn from the individual's as well as group's knowledge about the scenario (or search space) in order to solve the optimization problem (i.e. to obtain the required optimum value). Like when the birds go for migration or ants search for the food, none of the members in the group knows exactly where to go. They collectively work in a group and explores different direction in the search space. During their entire search, they keep track of their own history as well as other members'. They share their information to each other and based on these informations they proceed further exploration. When one member reaches the most favorable search space, other members follow the same path i.e. converge to the best search space. This is the basic idea explored in this class of optimization.

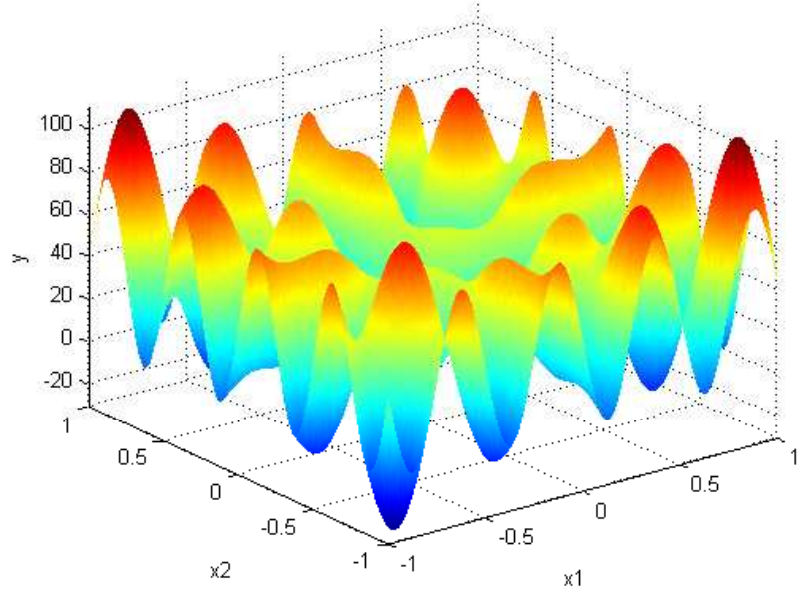
5.2.1.1. Particle Swarm Optimzation

PSO is an efficient and powerful heuristic technique to solve the global optimization. It has drawn a lot of attention in recent years due to its ease of implementation, rapid convergence, robustness and efficiency. It has limited number of parameters to adjust and unlike other optimization algorithms it is a derivative free algorithm. Unlike genetic algorithm, it does not involve complex operators like genetic crossover and mutation.

In PSO, particles form a population, called swarm. Actually, particles are the position in the search space, which form members of the swarm. For a given fitness function f(x), an objective can be either to maximize or minimize the given fitness function over a given search space. The complexity of an optimization problem depends on the type of fitness function. For a unimodel



(a) Unimodal Function



(b) Multimodal Function

FIGURE 5.1. Types of fitness function possible to use in this research.

function as shown in fig. 5.1(a), it is comparatively easy to find the optimum value as it has a single optimum point. However for a multi-model function as shown in Fig. 5.1(b), it is computationally extensive task to find the global optimum as it has a number of local optima. So for these types of functions, the particles have to start from different location and then explore the regions around them. During the process of particle exploration, each particle communicates with other particles

in a population and shares its information about its best vale obtained so far. From these local informations, a global information is extracted. In other words, there are two types of best values: local best value (P_{best}) and global best value (G_{best}). During each move, each particle has some position in the search space. At that position in the search space, the fitness function is evaluated for each particle separately. If an optimization problem is minimization then the best value means the smallest possible value the fitness function can have in a feasible search space. So if a particle has moved 'N' steps then each particle will find its best value (computed from fitness function) in all of its 'N' moves. The best value that each particle obtains from these 'N' moves is its personal best value (P_{best}). Thus, personal best position for particle 'i', given by $P_{best,i}$, refers to the best fitness value the particle 'i' has obtained so far in all its moves. The global best value (G_{best}) refers to the best value among all the particles in the population i.e. it is the best fitness value discovered by any particle in the entire swarm in all the moves. Based on this individual experience and social knowledge (i.e the knowledge obtained by sharing information with other particles), the particles explore the search space to reach the global optima as shown in Fig. 5.2.

If $\mathbf{x}_i^t$ denotes the position vector of a particle 'i' at time 't' and $\mathbf{v}_i^t$ represents the velocity vector of that particle at time 't' then based on the particle's individual knowledge and the shared knowledge of other particles' location, the velocity vector of each particle is updated first. Once the velocity of the particle is updated, its new position at time 't+1' is updated as follows:

$$\mathbf{x}_i^{t+1} = \mathbf{x}_i^t + \mathbf{v}_i^{t+1} \tag{37}$$

Initially, the particle's position vector $\mathbf{x}_i^0$ is randomly selected from the [x_{min}, x_{max}], where x_{min} and x_{max} are the minimum and maximum values of the search space.

For the minimization problem, the personal best position $P_{best,i}$ at the next time step 't+1' is given by the following:

$$P_{best,i}^{t+1} = \begin{cases} P_{best,i}^t & \text{if } f(x_i^t) > P_{best,i}^t \\ x_i^{t+1}, & \text{otherwise} \end{cases} \tag{38}$$

where $f(.)$ is the fitness function.

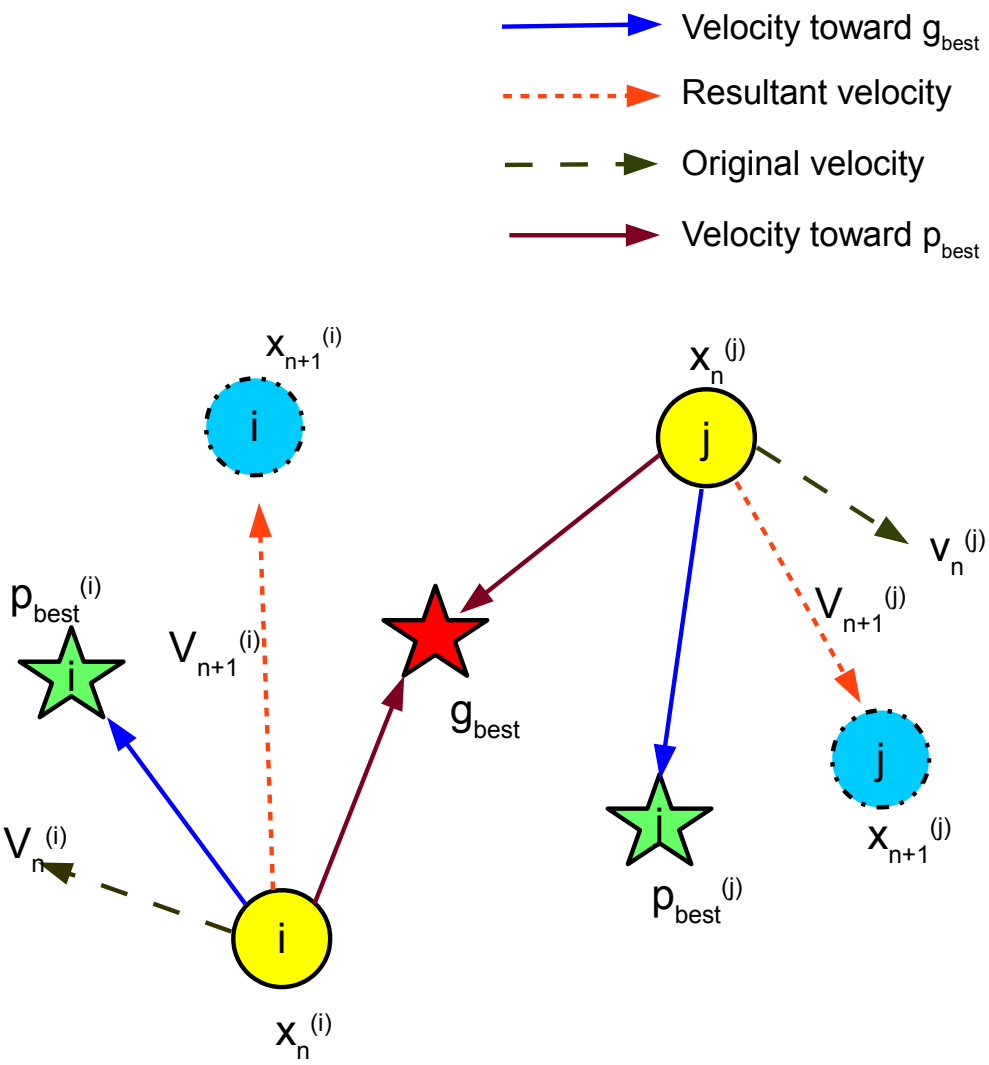


FIGURE 5.2. Particle velocity updating where particles i and j are accelerated to wards their best location, g_{best} and p_{best} [**66**].

Since the global optima is obtained from the particle's personal information, this social information at time 't' is obtained as:

$$G^t_{best} = min\{P^t_{best,i}\} \quad where \quad i \in [1, 2, ..., n] \quad and \quad n > 1 \tag{39}$$

where 'n' is the number of particles in the swarm.

So based on these personal best positions and global best position, the velocity of the particle 'i' for next move at time 't+1' is updated as:

$$\mathbf{v}^{t+1}_i = \mathbf{v}^t_i + c_1 r^t_1 [P^t_{best,i} - \mathbf{x}^t_i] + c_2 r^t_2 [G^t_{best,i} - \mathbf{x}^t_i] \tag{40}$$

where $\mathbf{v}_i^t$ is the velocity vector of particle 'i' at time 't'

$\mathbf{x}_i^t$ is the position vector of particle 'i' at time 't'

$P_{best,i}^t$ is the personal best position of particle 'i' found from all previous moves till time 't'

G_{best} is the global best position of particle 'i' found from all previous moves till time 't'

c_1 and c_2 are the positive acceleration constants used to control the balance between the cognitive and social components respectively

r_1^t and r_2^t are the random numbers $\in$ (0,1) at time 't'.

The second component in the equ. (40) is called the cognitive component. It measures the particle's own performance with respect to its past. Thus this component tries to return the particle to the previous position where it was most satisfied in the past. The third component in the equ. (40) is called the social component. It compares the particle's own performance with respect to the group's performance. This component tries to move the particle close to the best position found by the particle's neighbors.

The influence of cognitive and social component is controlled by the acceleration constants together with the random values. The components c_1 expresses the confidence of particle to itself while c_2 express the confidence towards its neighbors. So for different values of acceleration constant, the particles behaviors are different.

Case 1: For $c_1 = c_2 = 0$

The particles continue moving to its current location until they hit the search space boundary. Once the particle moves out of the search space then the particle is either:

- **:** relocated at the wall of the solution space and set velocity to zero in the dimension where it crosses the search space, or
- **:** relocated at the wall of the solution space and reverse the velocity direction for the dimension in which the particle crosses the search space.

Case 2: For $c_1 = 0$ and $c_2 > 0$

The particle gets attracted to the global best position.

Case 3: For $c_1 > 0$ and $c_2 = 0$

The particles are independent and follow their individual knowledge.

Case 4: For $c_1 \gg c_2$

Each particle trusts its individual knowledge more than the global or social knowledge. This can cause excessive wandering in search of the best position [**35**].

Case 5: For $c_1 \ll c_2$

The particle trusts more on the group knowledge than its individual knowledge. This may result in prematurely converge to a local optima.

Particle's velocity is a very critical parameter in PSO. An improper choice of particle velocity can cause excessive exploration or exploitation [**109**]. If the velocity is set too large then the particle tries to explore large search space which can cause particle to cross the search space. Too small value for the velocity can cause particle to wander around a small search space in a hope to find the better solution. Thus there need to maintain a balance between exploration and exploitation. Over time, the basic PSO velocity formula (i.e equ. (40) has been modified in order to the following:

- **•:** improve the speed of convergence,
- **•:** control the exploration and exploitation trade-offs,
- **•:** avoid pre-mature convergence to a local optima.

To restrict a large velocity to a particle, in [**20**], the concept of a maximum velocity, V_{max} has been introduced. This maximum velocity maintains the balance between global exploration and local exploitation. Each each particle's velocity is checked to see if the particle's velocity exceed this maximum value or not, and the new velocity is set as:

$$v_{ij}^{t+1} = min(v_{ij}^{t+1}, V_{max}), \tag{41}$$

where the suffices 'i' and 'j' are used to specify two dimension. This maximum velocity can be obtained as:

$$V_{max} = \varepsilon(x_{max} - x_{min}), \tag{42}$$

where x_{max} and x_{min} are the maximum and minimum values of x and $\varepsilon \in (0,1]$.

Since there is a likelihood of all the particles getting this maximum velocity of V_{max} and this may again cause particle to wander round and round. So, an inertia weight has been introduced in [**107**] to adjust the influence of previous velocities in the process. With the inertia weight, the equ 40 is been modified to:

$$\mathbf{v}_{ij}^{t+1} = \omega \mathbf{v}_{ij}^{t} + c_1 r_{1j}^{t}[P_{best,i}^{t} - \mathbf{x}_{ij}^{t}] + c_2 r_{2j}^{t}[G_{best,i}^{t} - \mathbf{x}_{ij}^{t}] \tag{43}$$

where, ω is the inertia weight. This new particle velocity (i.e. equ (43)) converges more accurately to the global optima as compared to the previous equ (40). The inertia weight can have a static [**108**] or dynamic value [**123**]. However the dynamic value have been preferred so that the particle can explore more space during the initial iteration and then at the later iteration the particles exploit the space for better optimum. So, the initial inertia value is set high which allows particles to move quickly in different directions in the search space. Over time, the inertia value is reduce, so that the particle can exploit its local search space better for better optimum. This shifting of particles' search mode from exploratory mode to the exploitation mode has produced better optimum results.

In [**109**], the inertia weight has been varied as follows:

$$w^{t+1} = w_{max} - \frac{w_{max} - w_{min}}{t_{max}} \tag{44}$$

In [**107**], inertia weight is varied in a similar linear form. A non-linear inertia weight has been proposed in [**129**] in order to improve the performance of global search irrespective of random particle initialization. In [**37**] an adaptive inertia weight has been proposed to improve the solution quality and the convergence speed.

Apart for the particles' velocity, there are other parameters which are critical in PSO for better performance. They are as follows:

(1) Swarm size

Swarm size refers to the number of particles used to search the global optimum i.e. it is the population size in the swarm. When larger number of particles are used in the search, the performance of the search is improved due to the fact that more particles means they can explore more space in search of better solution. However, the computational complexity and delay increases in each iteration due to the large swarm size.

(2) Search termination

Loop termination refers the condition that determines when the search needs to be stopped. This ending condition has to be set before starting the search. There are a number of ways to define this ending condition:

(a) By setting an iteration to loop for a set number of times. A large value to this iteration number may add up unnecessary computational complexity and delays while the small value may lead to premature result [**35**].

(b) By setting a minimum value that the loops result should satisfy [**35**]. If there is no improvement over number of iteration then it implies that the particle has reached the global optimum. In that case, it is unnecessary to continue searching. Again the care has to be taken to set this value. Too large or too small value can lead to unnecessary computation versus premature convergence.

However there are some disadvantages in PSO that limits the performance of the search and hence the quality of the final solution. Some of these drawback are the following:

(1) Like any other evolutionary computational techniques, it also suffers from premature convergence[**108**].

(2) As PSO achieve its global best value by interaction of particles, limiting this interaction can trap the particle to the local optimum thereby restricting the search capacity [**70**].

(3) During the PSO initialization, all the particle are assigned a random position. The final search result is affected by improper choice of initial position[**108**].

5.2.1.2. Multi-Swarm Optimization

In the basic PSO algorithm, at each step only one g_{best} is obtained. For a multi-peak objective function, the basic PSO may often get trapped in a local optimum rather than the global optimum. Even if the population size is increased endlessly, the probability of getting global best value does not increase accordingly [**113**].

In the multi-swarm optimization (MSO), the basic idea is to obtain multiple g_{best}s using the same number of particles as in basic PSO. The particle is randomly initialized in the same

way as in basic PSO. The population then gets divided into 'M' groups randomly. Each of these individual group now forms a new population (i.e. swarm). So with 'M' groups, there are total of 'M' population or 'M' swarms. Each particles in a group behaves as a separate population and they synchronously update their velocities and position with other population. This parallel calculation of each 'M' population (or 'M' swarms) gives a total of 'M' number of g_{best} values. When the stopping condition is met, the iterative process stops. These 'M' groups then get combined into a single population and the algorithm again starts taking g_{best} as their new initial values. This new population updates their position and velocity in the same way until the stop condition is met again.

The idea of dividing a single population into 'M' groups and later combining into a single group is to reduce the probability of getting stuck into a local optima and thereby increasing the chance of getting a real global optima. With this MSO approach, the effect of random particle initialization greatly decreases which thereby increasing the searching efficiency and probability of finding the real global best value. Since the number of particles in MSO is same as that in the basic PSO, the calculation volume does not increase in MSO with respect to basic PSO [**70**].

5.3. Proposed Optimization Design Flow

Fig. 5.3 shows the proposed design flow for the LC-VCO circuit. The design process starts with determining the approximate design points from the behavioral analysis. The baseline design of the circuit is performed from which a netlist is generated. Various figures of merits (FoMs) such as frequency, phase noise and power dissipation are chosen to characterize the oscillator. After choosing the FoMs for the circuit, design variables (length (L) and width (W)) of the GFET are selected. The netlist obtained from the baseline design is then parameterized with respect to these design variables. In order to obtain the distribution of the variation of the characteristics due to the variation of design parameters, parametric analysis is performed on the FoMs. This gives the variable range and the constraints are then chosen based on the design requirement. In the final step of the design, optimization is performed to obtain the maximum frequency for the given constraints. After the successful completion of optimization, a netlist is obtained from this final sized circuit.

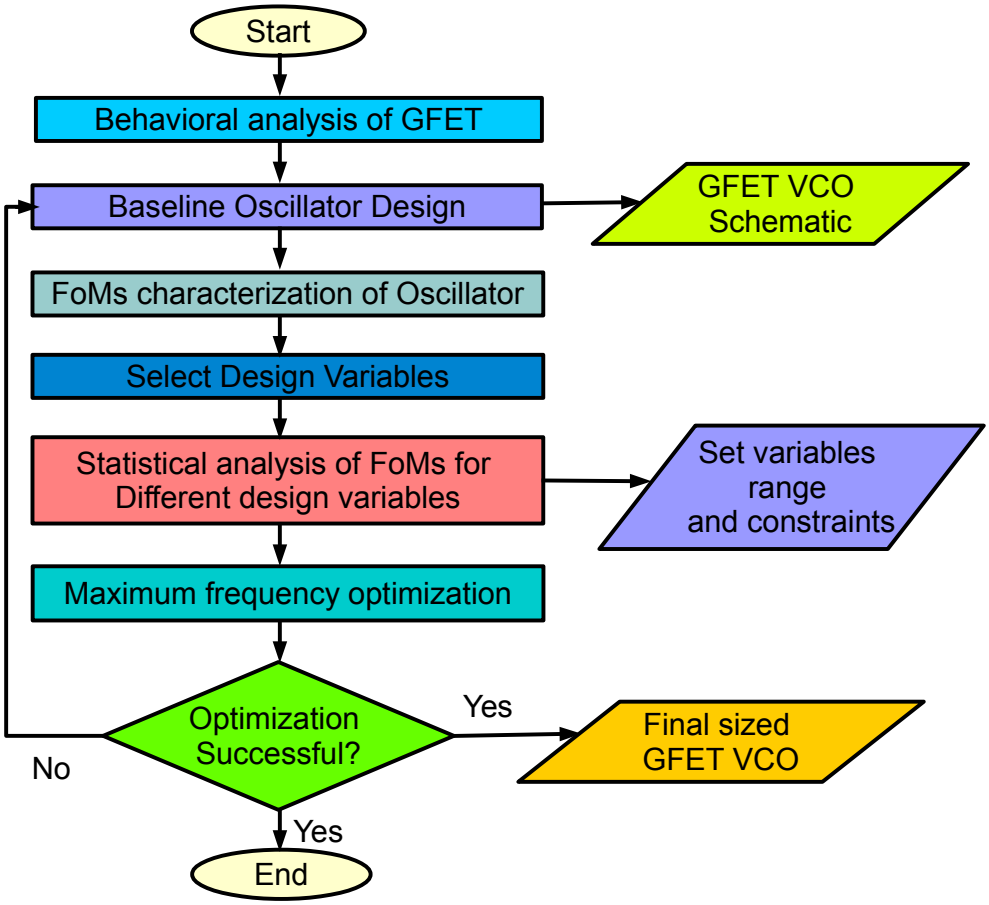


FIGURE 5.3. Design Flow of GFET based LC-VCO Circuit Optimization [**66**].

5.4. Specific Algorithm

In the basic PSO algorithm, at each step only one g_{best} is obtained. For a multi-peak objective function, the basic PSO may often get trapped in a local optimum rather than the global optimum. Even if the population size is increased endlessly, the probability of getting global best value does not increase accordingly [**113**].

Multi-swarm optimization(MSO) is an improved version of particle swarm optimization(PSO). In MSO, the idea of PSO is extended in the sense that instead of single swarm in PSO, MSO uses several swarms and each swarm interact with each other. The large number of swarms and partciles increases the probability of finding the optimum value but at the cost of slow performance. The key difference in MSO Algorithm is how a particles new velocity is calculated in each iteration, which is given by:

$$v(t+1) = w * v(t) + (c_1 * r_1) * (p(t) - x(t)) + (c_2 * r_2) * (s(t) - x(t)) + (c_3 * r_3) * (g(t) - x(t)) \quad (45)$$

where v(t+1) is the new velocity at time (t+1),

v(t) is the velocity at time t,

x(t) is the position at time t,

p(t) is the particles best known position at time t,

s(t) is any particle's best position in a particular swarm at time t,

g(t) is the global best position of any particle in any swarm at time t,

w is the inertia factor as in PSO,

c_1 (also known as cognitive weight), c_2 (also known as social weight) and c_3 (also known as global weight) are the parameters to bound the change of each component in a new velocity and determined the influence of each term in the new velocity and hence in their position,

r_1, r_2 and r_3 are the random values between 0 and 1 included to provide more randomness in the velocity update there by decreasing the chance of getting stuck in local optimum.

When a new velocity is calculated, it needs to be ensured that its value is not too large so as to avoid the algorithm from moving too far in one iteration. Also the lower bound velocity can be incorporated to ensure there is some movement. Once the new velocity is obtained, it is used to calculate particles new position based on:

$$x(t+1) = x(t) + v(t+1) \quad (46)$$

where, x(t+1) is the particles new position at time (t+1). Similarly the particle's new position can be constrained within a range like in the case of PSO.

The error associated with the particle's new position is then determined and check whether it is the new best error for the current particle. Following the error check, the new position is also checked to see if it is a new swarm best value or a new global best value. For a new global-best position, it obviously also has to be a swarm's best position.

As compared to PSO, MSO is a bit complicated algorithm in the sense that the addition of more swarms takes into consideration the particles death and immigration phenomenon. When a particle dies, a new particle is created at a random position and when a particle immigrate, a particle is randomly selected form a random swarm and is swap with the immigrate particle. These death and immigration mechanism further adds randomness in the MSO and increases the chance of optimal solution. The way of incorporating death and immigration mechanism can be either based on a fixed probability or as a function of maximum number of iteration loop. With this MSO approach, the effect of random particle initialization greatly decreases which thereby increasing the searching efficiency and probability of finding real global best value. Since the number of particles in MSO is same as that in the basic PSO, the calculation volume does not increase in MSO with respect to basic PSO [**70**].

5.5. Results

An optimization problem is formulated with an objective to maximize the frequency for the given constraints- phase noise and power dissipation and design variables: channel length and width. A parametric analysis of frequency, phase noise and power dissipation is performed over the design variables. Constraints are selected for phase noise and power dissipation once the parametric analysis is complete. The results obtained from the parametric analysis are shown in Fig. 3.7. Datas are extracted from this analysis and are then fed to the optimization algorithm to optimize the circuit. The values for phase noise and power dissipation are chosen to be less than -80 dBc/Hz and 16 mW respectively so as to optimize the circuit for maximum possible frequency.

TABLE 5.1. GFET-based LC-VCO Design Variables and Constraints.

LC-VCO Parameter	**Parameter Type**	**Minimum Value**	**Maximum Value**
L	Design Variable	$3\mu m$	$7\mu m$
W	Design Variable	$1.4\mu m$	$2.2\mu m$
Power Dissipation	Design Constraint	Minimize	$16mW$
Phase Noise	Design Constraint	Minimize	$-80dBc/Hz$

Algorithm 3 Proposed Multi-Swarm Technique for GFET based LC-VCO Optimization.

$ITER \leftarrow$ Maximum number of iterations.
$S \leftarrow$ All swarms to be used.
$P \leftarrow$ Particles in each swarm.
for $t = 1$ to $ITER$ **do**
  for all $s \in S$ **do**
    for all $p \in P$ **do**
      if $t = 1$ **then**
        Generate initial position/coordinate of each particle: length (L) and width (W) of GFETs.
        Evaluate cost function, e.g. calculate oscillating frequency of GFET LC-VCO.
        Assign initial particle as best particle.
      end if
      if $t > 1$ **then**
        Evaluate cost function, e.g. calculate oscillating frequency of GFET LC-VCO.
        if Cost function is better e.g. frequency increases. **then**
          Assign current particle as the best particle.
        else
          Retain previous particle as best particle.
        end if
      end if
      Compute particle velocity.
      Update particle position/coordinate.
      if Particle tends to go out of boundary or design specification range. **then**
        Negate the velocity.
        Revert particle back from boundary.
      end if
    end for
    Find best particle in each swarm or maximum frequency from each swarm.
  end for
  Find best global particle or maximum frequency among all swarms.
end for
Plot best global particle or frequency for all iterations.
Output should settle around final optimized value.

Table 5.1 shows the design variable range used in this chapter. As mentioned before, particles in each step shift their position based on velocity which accounts for the particle's own behavior, the swarm's behavior as well as the global behavior. Since the maximum velocity can play crucial role in the final result, it can also be selected as proposed in [**9**]:

$$v_{max} = \left(\frac{x_{max} - x_{min}}{N} \right) \tag{47}$$

In Eqn. 47, x_{max} and x_{min} are maximum and minimum values in any particular dimension in the position coordinate of the design hyperspace. As stated in [**16**, **56**], the initial difference between maximum and minimum velocity is set equal to the search space. N is some optimum value which is set based on problem region so it set to be equal to the total particles of all swarms.

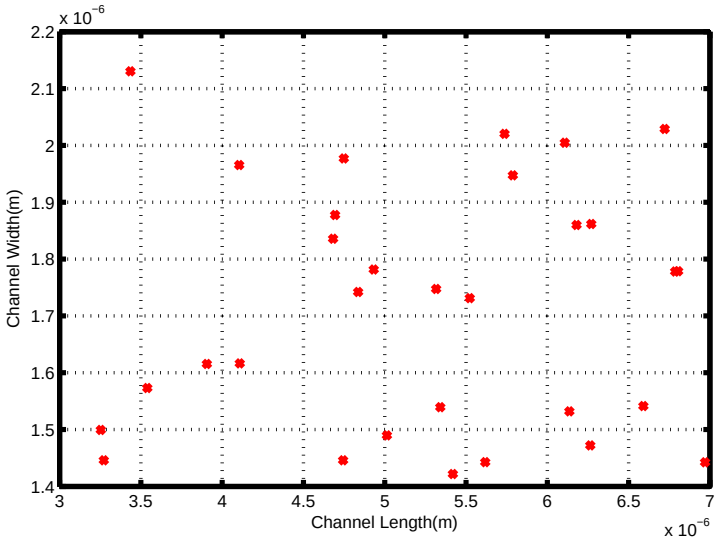
To facilitate optimization further, the inertia constant is considered as a decreasing function of time so that at the initial stage of iteration, the particles are allowed to explore more search space and as the iteration number increases the particles are restricted from further exploring and are subjected to exploit the search space. So, the value of inertia constant is gradually decreased from an initial value of 0.7 to a final value of 0.33. These values have been chosen after exhaustive trial and error and till the satisfactory results were obtained. Based on particle movement, the maximum iterations is set. Table 5.2 summarizes the parameters in defining particle velocity.

TABLE 5.2. Multi-Swarm Optimization Algorithm Parameters.

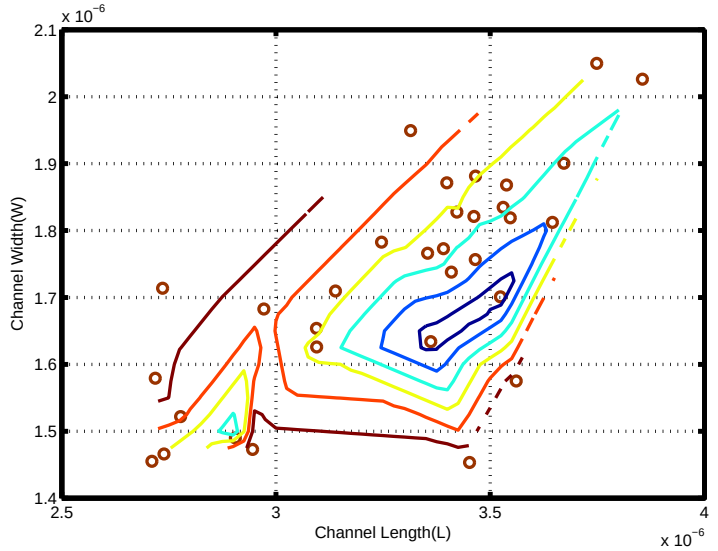
Algorithm Parameters	**Values**
w	0.7 - 0.33
$c1$	0.2
$c2$	0.2
$c3$	0.2

Similarly, critical parameters are the acceleration constants. Small values for these constants make particle to roam far away from the target global region and high values results in abrupt particle movement, thereby causing pass the target region and causing an undesired oscillation in the optimization. The acceleration constants are chosen small as compared to the values

selected in [**33**] for single swarm PSO. The Table 5.2 shows the values chosen for acceleration constant after several trial and error.



(a) Channel Width (W) Vs Channel Length(L)

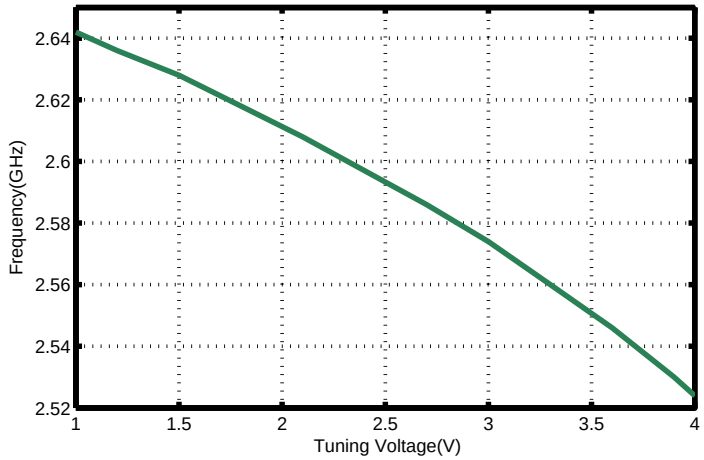


(b) Channel Width (W) Vs Channel Length(L)

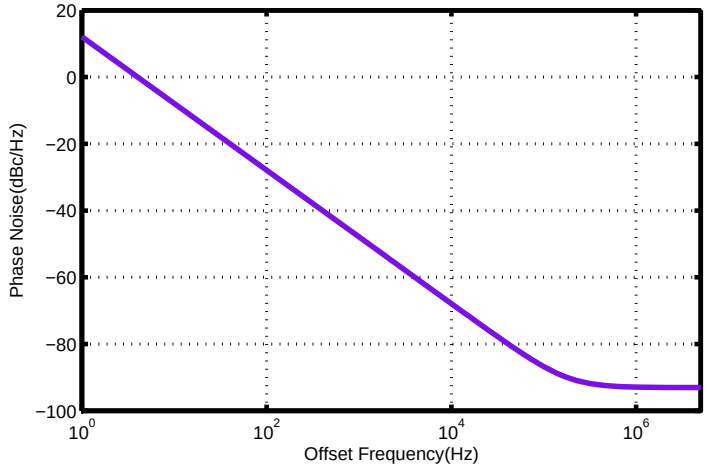
FIGURE 5.4. GFET based LC-VCO Optimization: (a) Initial particles (x), (b) particles after 20^{th} iteration (o).

The optimization steps and results are shown in Fig. 5.4. The initial and final particles position after 20 iterations are shown in fig. 5.4(a) and fig. 5.4(b) respectively. As can be seen in these figures, the initial particles are spread all over the design space and after 20 iterations, the

particles of all swarms are converged around the global optimum particle position. The interpolated contour in fig. 5.4(b) helps to visualize the convergence step where each line illustrates connected isometric values. The global best particle position is obtained by averaging across all steps and Table 5.3 illustrates the optimal oscillator values obtained after optimization. Fig. 5.5(a) and fig. 5.5(b) show the tuning range and phase noise of the optimized LC-VCO.



(a) Fequency Vs Tuning Voltage



(b) Phase Noise Vs Offset Frequency

FIGURE 5.5. (a) Tuning range of optimized LC- VCO (b) Phase noise of Optimized GFET based LC-VCO.

The required LC-VCO oscillator is successfully designed following the design flow and the optimization algorithm. The design constraints of phase noise and power dissipation are well met. The baseline LC-VCO with center frequency of 2.56 GHz is initially design and the final LC-VCO

TABLE 5.3. Characteristics of the Optimal LC-VCO.

LC-VCO Parameters	**Estimated Values**
Channel Length	3.35 μm
Channel Width	1.82 μm
Frequency	2.58 GHz
Power Dissipation	11.74 mW
Phase Noise (at 1MHz offset)	-92.92 dBc/Hz
Tuning range	4.26%
$V_{tank(p-p)}$	0.75 V
I_{bias}	0.83 mA

with center frequency of 2.58 GHz is obtained, where the power dissipation and phase noise are 26.625% and 16.15% below the maximum value.

CHAPTER 6

GRAPHENE BASED DIGITAL CIRCUITS DESIGN

Digital electronic circuits make distinction from analog or radio frequency (RF) integrated circuits from the fact that the formers are driven by low power/energy requirement, followed by area and cost aspect while the latter is driven by performance and power/energy is not as critical as in digital circuits. Today no digital systems get complete without having memories in it and these memories are the major power consuming components in any digital system. With the need to make devices faster and superior in performance in each generation, the size of the memories are ever increasing. However the size of the device is shrinking and the supply voltage is decreasing. This makes a memory design a challenging task for future nanoelectronics. So this chapter focuses on the design of static random access memory (SRAM) based on graphene transistors.

There are mainly two major families of memory circuits used today: dynamic memory and static memory. Dynamic random access memory (DRAM) is built from a transistor and a capacitor, where the capacitor is used to hold one bit of information and the transistor acts as a control circuitry enabling the capacitor to change its state. Since only two circuit elements are used to store one bit of information, the obvious advantage of DRAM are its ability to store millions of them in a small area, leading to high chip density and low cost. However on the negative side, since the capacitor is used to store information, there is an inherent leakage which makes them lose their stored content with time. So within a few millisecond or microsecond the content in DRAM lost and to retain the content, it has to be periodically refreshed before they get discharged. Thus DRAM always come with periodic refreshing circuits and due to these refreshing cycles, this type of memory is typically slow. On the other hand, SRAM uses a concept of flip-flop to hold each bit of information. Since flip-flop takes 4 or 6 transistors to store one bit of information, it occupies lot more chip space than DRAM and hence more costly. However the advantage of SRAM is that the information is restored as long as the power is on and there is no need of refresh cycles to retain the stored information. This make SRAM much faster than DRAM. Due to this basic differences, SRAMs are typically used in speed-sensitive caches whereas DRAMs are used

to form larger memory where speed is not a major concern.

The aim of this chapter is to design 8x8 array of 6T SRAM using graphene transistors. The complete circuit is designed to simulate the read and write cycle. Since the memory cell occupies most of the memory area, hence the SRAM cells are built using graphene transistors while all other peripheral circuits are built using traditional silicon based transistors. The novel contribution of this chapter is to compare the advantages of GNRFET SRAM with silicon based SRAM at 45 nm technology node providing detailed cell level characterization as well as array based characterization. This is the first ever attempt to provide such a detailed level of comparison in terms of stability and power consumption.

6.1. Advantages of Graphene Based SRAM

According to [**5**], it is expected that by 2016, embedded memories is going to account upto 95% of modern SoC area . In order to meet the high performance and computational requirement, the density of the on-chip cache has been growing steadily and hence the size of the SRAM bt cells have been aggressively scaled down. However this scaling trend has been reduced by 30% to 50% due to several challenges at nanoscale regime such as leakage, variabilities and so on [**63**]. Thus it is very important to incorporate new materials and device concepts to meet the growing performance requirements and graphene can very well meet these requirements. The advantages of graphene based SRAM for future electronics as compared to silicon based SRAM are as follows:

(1) Due to higher carrier mobility in graphene, the graphene based SRAM facilitates high speed low power switching applications.

(2) Graphene based SRAM are batter as compared to silicon based SRAM in terms of speed, density and performance metrics.

(3) The noise margin of graphene based SRAM is superior than the CMOS counterparts.

(4) Unlike in silicon, graphene does not need to be doped with impurities for conduction. Hence it reduces one important step (of doping) which is the major cause of device variation at nanoscale regime.

(5) Graphene can also be used in the existing CMOS memories at the interconnect as it conducts larger current than copper or aluminum wires.

6.2. Introduction and Working Principle of SRAM

In modern days, the application areas for memory is very broad and each of these areas have different sets of constraints and hence different sets of requirement. Thus it is important to design the SRAM with the application in mind so that the trade-offs for that particular application can be managed carefully.

The main factors that dominates the design of SRAM are power, performance and size and they have a very complex relationship among themselves. For e.g., minimizing the size of the SRAM leads to the increase in the power consumption and reduces the performance. Also it is not necessary that all these factors are equally important in all the area of applications. So depending upon the intended application, some factors needs to be strictly satisfied while leveraging the other. Thus design trade-off plays a very critical role in SRAM design. Other than power, performance and size, cost always plays a decisive role in the success of any electronic devices.

Two such highly constrained applications are briefly discussed to highlight the application requirement:

(1) Biomedical: In biomedical applications like pacemakers, cochlear implants, neural sensors and stimulators; lifetime of a battery is very important. So while designing the SRAM for these applications, power consumption of SRAM must be given utmost priority. In wearable applications like hearing aids, body-area sensors, size of the SRAM is more critical than the power consumption.

(2) Mobile Multimedia: In multimedia applications, the devices have to deliver high definition video and high quality audio to the users and these devices operate at a very high frequency so performance plays a very important role. However in the case of mobile and other hand held devices, power consumption also becomes critically important so that the devices do not need to be plugged to the supply frequently.

6.2.1. Design of graphene Based SRAM

SRAM consists of homogeneous structure of memory cell arranged in a matrix form, as shown in Fig. 6.1 [**77**]. Each of these memory cells are connect to the row line, known as Word

Lines (WL), and a pair of column lines known as Bit Lines (BL) and Bit Line Bar (BLB), where BL and BLB are complementary to each other. The WL is used to control the access to the cell thereby deciding when to change the state of the memory cell. The two bitlines, BL and BLBs, are used to conduct the data flow to and from the cells, during read and write operation. Whenever the circuit needs to change its states from one state to another, there is a need of some sort of memory. So, all memories must at least have two inputs: one is the data that needs to be stored or memorized and another is the control signal which direct what is to be stored. Once the data is stored in the memory circuit, it needs to remain there indefinitely until the data is changed intentionally or is no longer needed.

The location of memory cell is selected by the row decoder and column decoder, giving each of these memory cell a distinct address. For R number of rows and C number of columns, the memory address is composed of $R + C$ bits. At any time only one memory cell is selected. So when any particular cell is to be accessed to read or write, the row decoder enables the corresponding WL to high and rest to low. This allows the cell for read or write operation. The column decoder then selects the particular column where the cell resides and depending on whether the read operation or write operation to be done, information flows into/from the cell for write/read operation respectively. Let us now consider each of these blocks in detail:

(1) Memory Cell:

The data to be stored in the form of two inverters (T_1,T_2,T_3 and T_4) connected back-to-back as shown in the Fig. 6.2. These transistors are responsible for storing the data as long as these inverters are supplied with the supply voltage, V_{cell}. As long as the cell is driven by the power supply, it can retain the data stored in it for indefinite amount of time. Remaining two transistors(T_5 and T_6) form a gateway, controlled by the wordline (WL), for bidirectional access between the bitlines (BL and BLB) and the cell. Transistors T_1 and T_2 are called pull-up transistors (or load transistor or driven transistor), T_3 and T_4 are called pull-down transistors (or driver transistor) and transistors T_5 and T_6 are called access transistors (or pass gate transistors). The size of these transistors are very critical for normal operation of the memory, as will be seen later. When the wordline(WL) is set

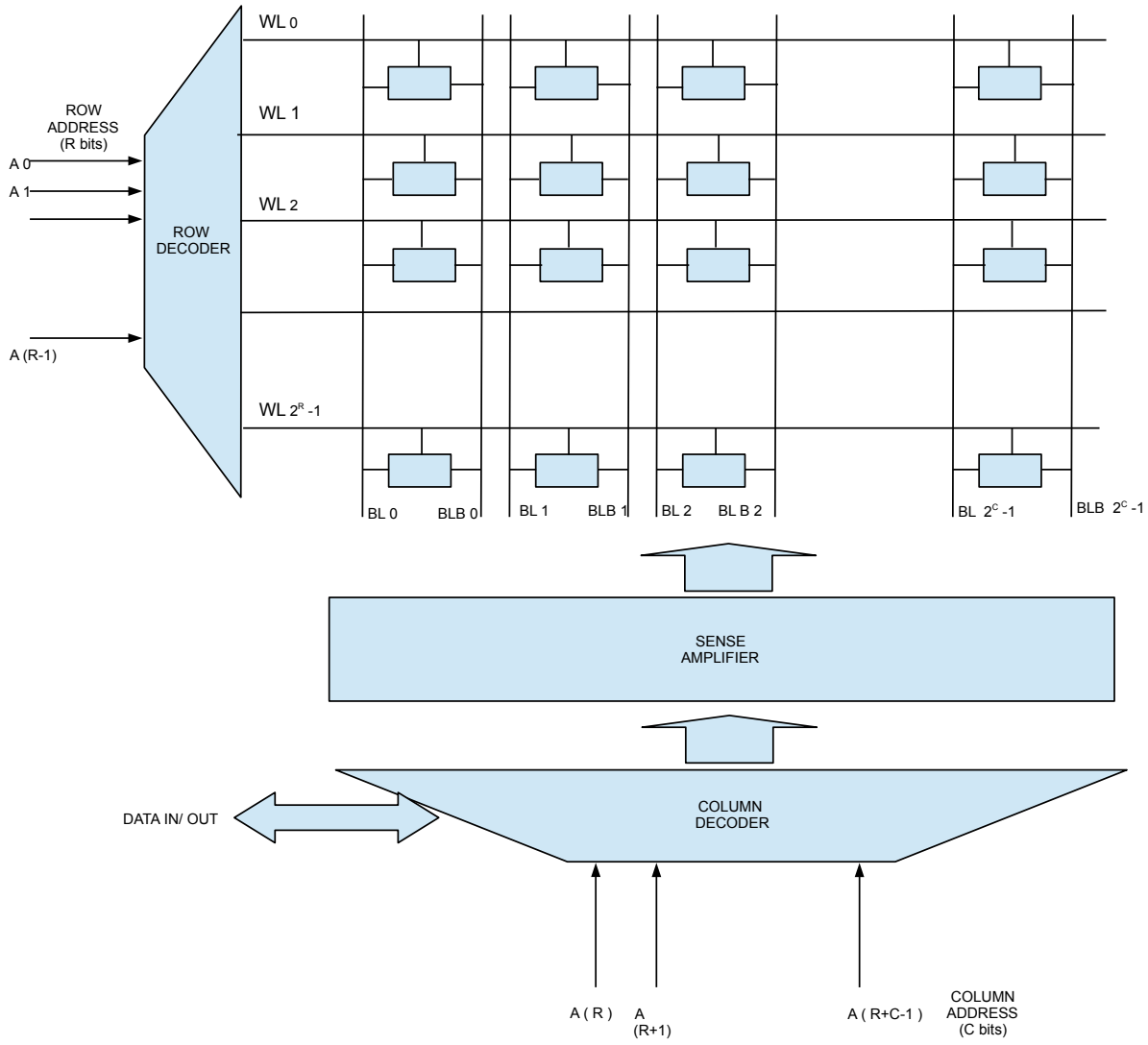


FIGURE 6.1. Complete Block Diagram of a SRAM array.

high, the cell is selected for read or write operation using the two bitlines (BL and BLB). When the WL is set low, the two transistors (T_5 and T_6) are disabled and hence the cell is isolated from the bitlines. The cell is then said to be in the standby mode (also known as data retention state), where the stored information is retained. The data to be stored in the cell is stored in BL while its complementary value is stored in the BLB. Thus the internal storage node Q, which is connected to BL stored the same value while the other storage node $\bar{Q}$ stores the complementary value.

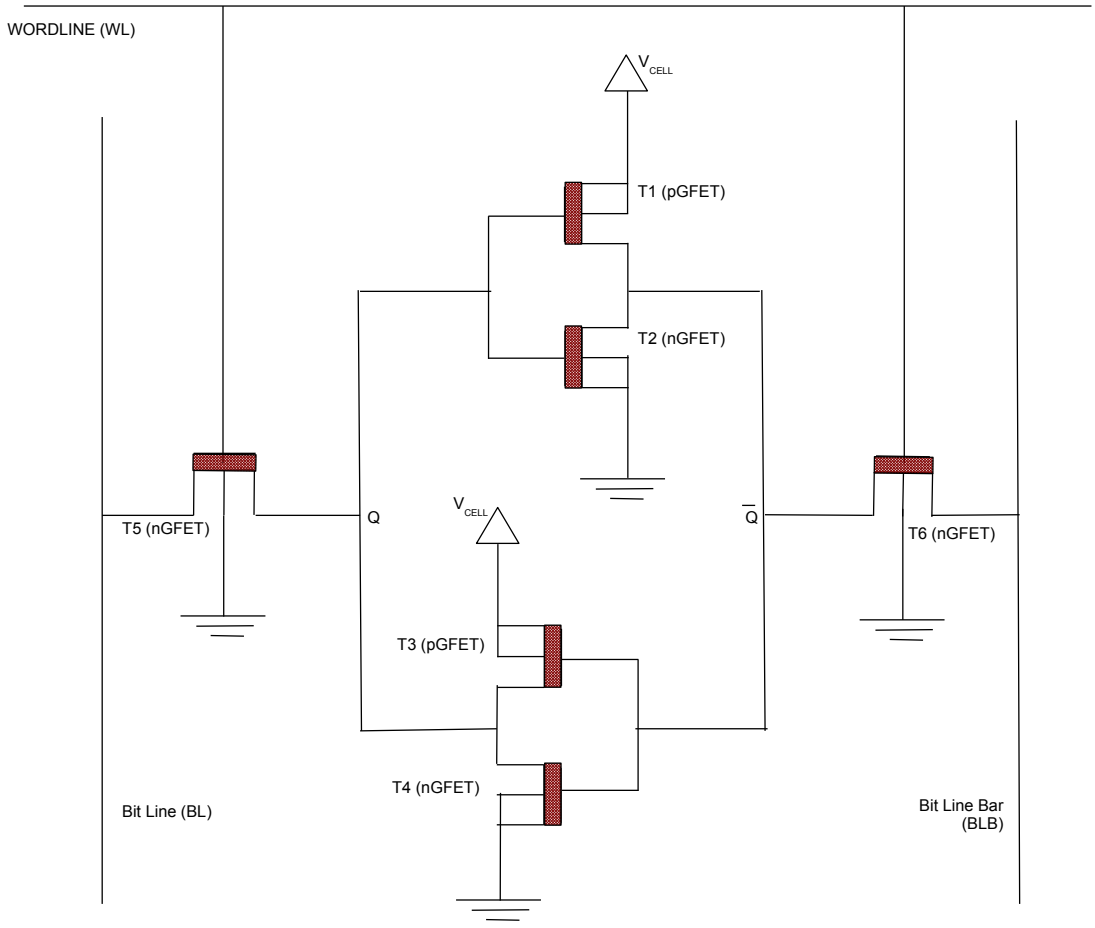


FIGURE 6.2. A GNRFET based 6T based SRAM Cell.

(2) Read and Write Peripherals:

The row decoder enables just one wordline at a time, thereby only cells in that particular row can be accessed for read and write operation. The cell where the read or write operation is to be performed is then selected by the column decoder. Thus each column requires one read and write peripheral for successful read and write operation respectively.

(a) Write circuitry

The write circuitry enables the data to be written in the intended cell through the use of two bitlines (BL and BLB). In order words, to write a data into the cell, one bitline has to be held at VDD level while the other bitline at ground level. To write a 1 into the cell, 0 is written in the storage node $\bar{Q}$ which thereby stores "1" at the other storage node Q. Thus the bitline which is held to the ground is used to write in the

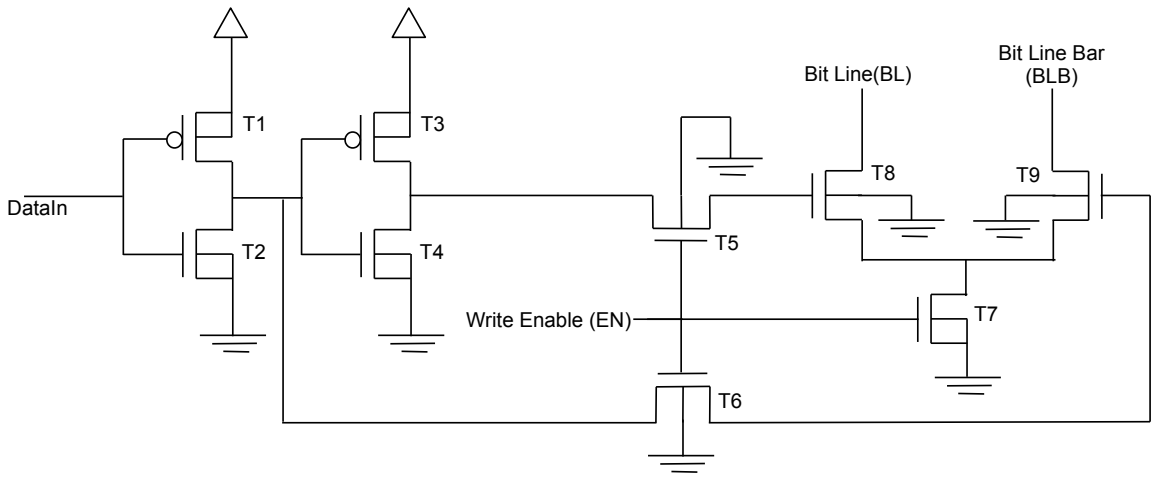


FIGURE 6.3. Write Driver for SRAM

cell. As can be seen from the Fig. 6.3, write enable (WE) is connected to the gate of the three nMOS (T_5,T_6 and T_7). So when the WE is asserted high, the two transistors (T_5,T_6), turns either one of the two transistors (T_8 or T_9) ON and the current flows from one of them to the ground through transistor (T_7). This makes one bitline high and another bitline low.

(b) Precharge and Equalization Circuitry

The bitline must be precharged and equalized before each read and write operation so that the sense amplifier can detect the small voltage difference between the two bitlines. It is necessary to precharge and equalize the bitlines before each read so as to ensure that the difference in bitlines are caused due to the difference in the values stored in the storage nodes Q and $\bar{Q}$. If the bitlines are not precharged before the read cycle then the sense amplifier can misread the value stored in the cell. Similarly if the bitlines are precharged and equalized before each write operation then the write operation would be much faster due to shorter time required to pass the inverter trip point.

(c) Sense Amplifier

The purpose of sense amplifier are to detect the slightest change in the bitlines, amplify the difference and decide whether the cell is storing 1 or 0. The Fig. 6.4 contains

both precharge and equalizer circuit together with the sense amplifier. The operation of sense amplifier is as follows:

Initially sense enable (SE) is set low, turning the sense amplifier off. The bitlines in the memory cell and the inverters in the sense amplifier are precharged by turning PC low. The bitlines are also equalized by turning EQ low at the same time. After the wordline in the memory cell is asserted high, the EQ and PC are lifted discontinuing the precharge stage. The column selector (CS) is then lowered connecting the inverters to the bitlines.When the sense enable(SE) is raised up, the source of the bottom nMOS connects the two nMOS in the inverter to the ground. The storage node with the highest initial voltage will make the opposite nMOS (whose gate is connected to that storage node) draw current faster. This in turns make the voltage at other storage node fall faster drawing less current from the higher storage node. An increase voltage difference between these two storage node will finally make the node flip into a stable state.

It is important to note that the storage node holding 1 is left unchanged by the cell and 0 is detected for the cell. The output is determined based on which side 0 is on. 0 in the storage node Q results in 0 as the output while 0 in the storage node $\bar{Q}$ results in 1 in the output.

(3) Address Decoders:

For the SRAM array of size $R * C$, there are R number of rows and C number of columns. Thus to select any cell, it is needed to have an address of at least $(R + C)$ bits at any time. The first R number of bits from the address bits are given to the row decoder and the remaining $(R + 1)$ to $(R + C)$ bits are given to the column decoder.

(a) Row decoder

The R bits from the address are given to the R number of input lines of the row decoder. From these R number of input bits, one wordline is selected by the row decoder.

(b) Column decoder

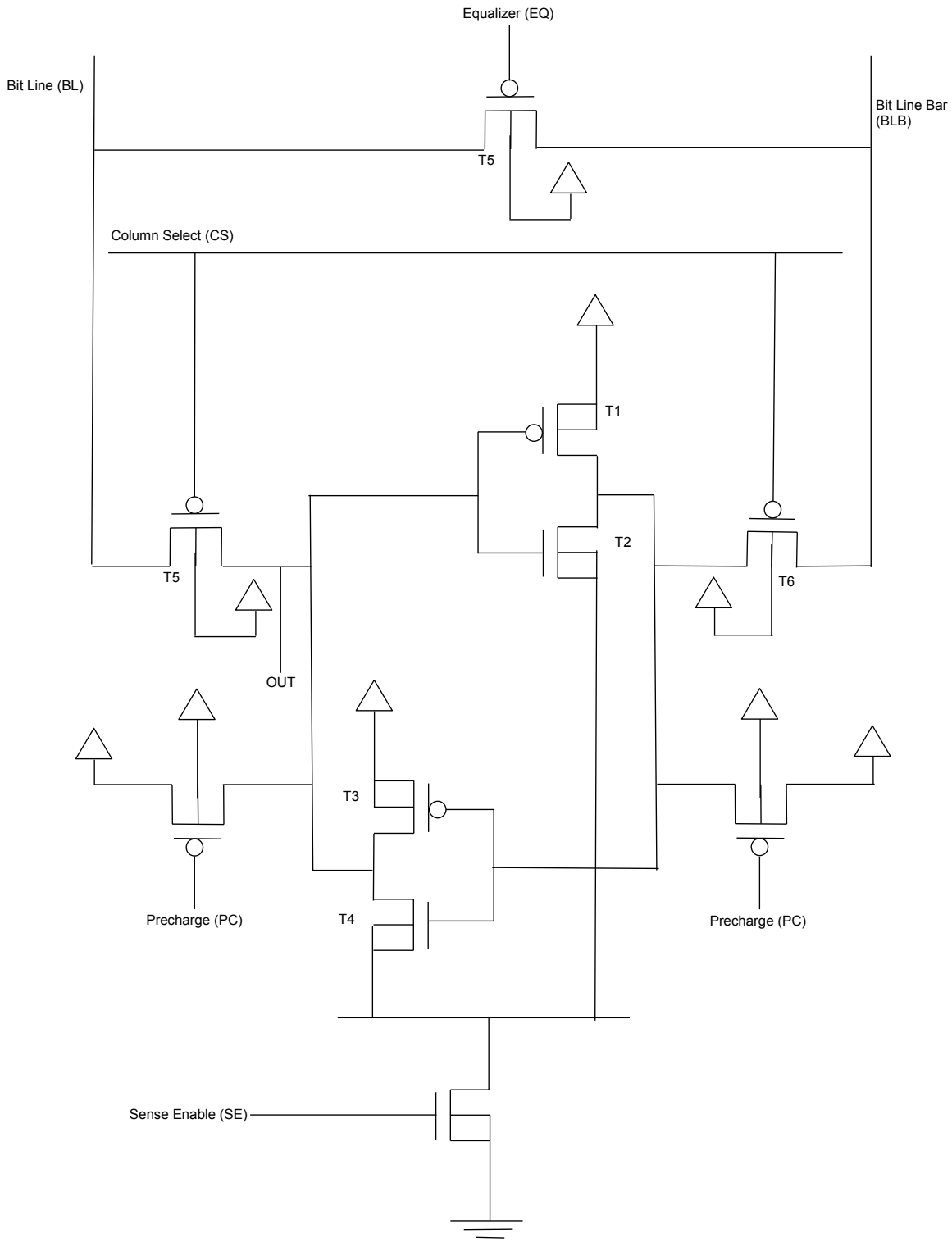


FIGURE 6.4. Sense Amplifier for SRAM

The remaining $(R+1)$ to $(R+C)$, a total of C, bits from the address are given to the C number of input lines of the column decoder. From these C number of input bits, one bitline pair (BL and BLB) is selected by the columm decoder.

6.2.2. Working Principle of SRAM

In order to understand the working of a memory array, it is important to understand the working of 1 bit memory cell. Then the same concept can be extended for any array.

(1) Read Operation:

When the cell is holding 0, the storage node Q is holding 0 and other node $\bar{Q}$ is at level 1. When the wordline is asserted high, the bitlines are also asserted high at the same time. Through the access transistors, the bitlines are connected to the storage nodes. During this condition, the storage node $\bar{Q}$ ad BLB both are both at logic 1 level, so no charge transfer can take place through this side. However at the other side, storage node is at logic 0 (i.e. in ground level) and BL is high, so charge transfer can take place from BL to the storage node and can flip the state of the cell. For this the transistor T_4 is made stronger than the access transistor T_5, and since the gate of the transistor T_4 is at high level, the storage node at Q cannot be raised higher to flip the cell content.

(2) Write Operation:

To write 0 in the cell, the BL is set low while to write 1 in the cell BLB is set low. So writing in SRAM cell s done by lowering one of the bitline to the ground while asserting the wordline high. Considering the cell is storing 0 initially which implies that the storage node Q is at $0V$ while other storage node $\bar{Q}$ is at V_{DD} (i.e.1 is there).In order to prevent accidental writing during the read operation, transistor T_4 was made stronger than the transistor T_5. Thus this condition avoids intentional write operation from BL side, even when the transistor T_5 is turned ON. In this case, when T_5 is turned ON, the current flows from BL (if BL is set high) to storage node Q and from transistor T_4 to the ground. So, the node Q is never allowed to reach close to the switching point. Thus to write 1 to the storage node Q, we need to store 0 in the other storage node $\bar{Q}$, which then force node Q to hold 1. When the WL is set high and BLB is set low, the current flow

from the V_{cell} through transistor T_1, storage node $\bar{Q}$ and access transistor T_6 to the BLB. Thus for writeability, the access transistor (which is a n-type) is made stronger than the pullup transistor (which is a p-type). When the voltage at node $\bar{Q}$ is drawn lower then the transistor T_4 can no longer be left open and will flip the state, changing the cell state from 0 to 1 [**22**].

It is important to note that, in traditional silicon based transistor, the mobility of electrons is roughly around 1400 $cm^2V^{-1}s^{-1}$ and that of hole is around 450 $cm^2V^{-1}s^{-1}$. The majority carriers in p-type transistor are holes and electrons for n-type transistors, and they are responsible for current. So to make p-type transistor conduct as much as current as that in the n-type, it is usually made double the width of n-type transistor. However in the case of graphene, the mobility for holes and electrons are the same. So it is not necessary to make p-type transistor of double the width as that of the n-type which considerably saves lot of chip size.

To summarize, the steps for read and write operation are as follows:

Algorithm 4 Steps for writing in the cell

1: Sense amplifier is turned OFF by setting phiS to 0. Followed by this, the precharge(phiP) is set high, which immediately turns ON the equalizer circuit.
2: Precharge(phiP) is set low
3: Write enable (WE) high to write into the cell.
4: Sense amplifier is then activated by turn phiS high and the wordline(WL) is asserted high.

Algorithm 5 Steps for reading the cell content

1: Sense amplifier is turned OFF by setting phiS to 0. Followed this the precharge(phiP) is set high, which immediately turns ON the equalizer circuit.
2: Precharge(phiP) is set low.
3: Wordline(WL) is asserted high
4: Sense amplifier is then activated by turning phiS high
5: Read enable(RE) is set high to get the data stored in the cell.

6.3. Graphene Nanoribbon Field Effect Transistor (GNRFET)

In this chapter, a graphene nanoribbon(GNR) FET is used for the design of SRAM. The model for GNR Univeristor of Illinois and the circuit is implemented in Cadence.

There are two varieties of GNRFETs: schottky-barrier (SB)-type and MOS-type. Though in [**126**], it highlights the advantages of MOS-type GNRFET over SB-type GRFET such as larger maximum on-off ratio due to absence of ambipolar transport, much larger on current, larger transconductance, better saturation behavior due to smaller output conductance, larger cutoff frequency, faster switching speed giving very small delay, large transconductance, but the most important advantage of SB-type GNRFET over MOS-type GNRFET is that there is no doping required in the channel or in the terminal. This reduces the technical difficulties during fabrication as well as the major source of variation which is inevitable in nanometer regime [**46**].

Double gate SB-type GNRFET structre is considered as it provides better gate control over the channel giving higher on-to-off current ratio. As shown in the fig. 6.5, the SB-GNRFET consists of a GNR-based channel while gate, drain, and source are metal electrodes. Thus the interface between drain-channel and source-channel forms a Schottky barrier at the graphene-metal junction. Hence SB-type GNRFET exhibit ambipolar properties where minimum current is at $V_{GS} = (1/2)V_{DS}$ L_{CH} is channel length, W_{CH} is the ribbon width, W_G is the gate width, and $2W_{sp}$ is the spacing between the ribbons. Increasing the number of the nanoribbon, n_{Rib}, increases the drive current strength. Bandgap in GNRFET is inversely proportional to the GNR width, so if the width is increased beyond $10nm$, the properties of GNR retains back to graphene sheet.

W_{CH} is commonly defined in terms of number of dimer lines N as [**46**]:

$$W_{CH} = \sqrt{3}d_{cc}\frac{(N+1)}{2}. \tag{48}$$

where d_{cc} (=$0.142nm$) is the carbon-carbon bond distance in graphene and N is the number of dimer lines in the GNR lattice. The gate width W_G is then computed as:

$$W_G = (2W_{SP} + W_{CH})n_{Rib} \tag{49}$$

As the objective is to determine, the upper range of performance of GNRFET in SRAM, edge roughness has not been included. As the fabrication technology get mature, the problem with

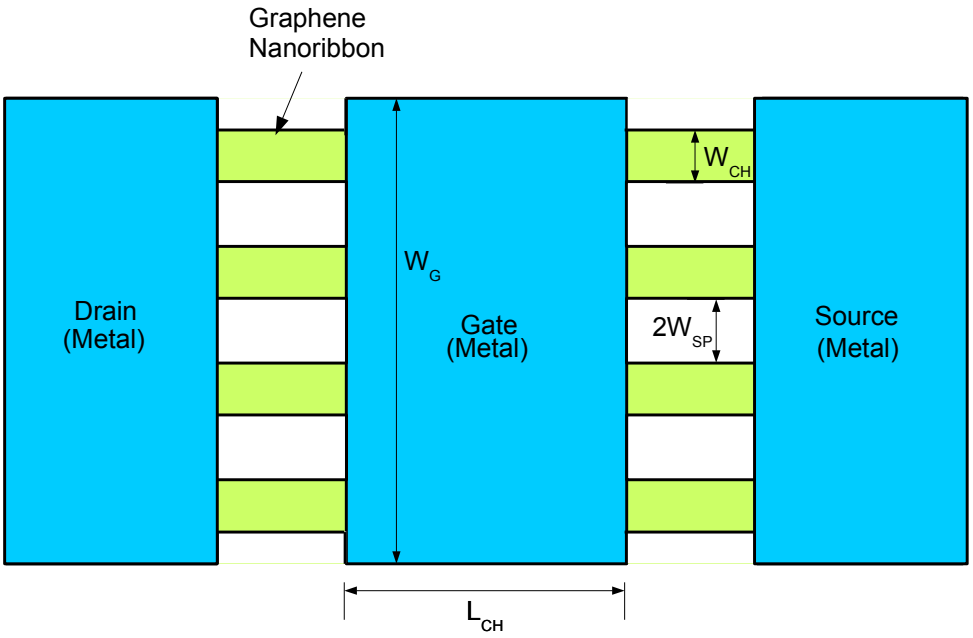


FIGURE 6.5. SB-type GNRFET

edge roughness would not be that much of problem. Since the channel length is $10nm$, which is less than the mean free path in graphene, so the carriers exhibit ballistic transport [**17**]. Table 6.1 summaries the device parameters used for the implementation.

TABLE 6.1. GNRFET device parameters.

Device Parameters	**Typical Default Values**
Physical channel length	$10nm$
Substrate oxide thickness	$20nm$
Tog-gate dielectric material thickness	$0.95nm$
Spacing between adjacent GNRs	$2.0nm$
Number of GNRs	6-10
Number of dimer lines in GNR lattice	12
Edge roughness percentage	0 (Ideal)

6.4. SRAM Design Verification

For the verification of SRAM, it is necessary to ensure the proper operation of inverter. As shown in the Fig. 6(a), for the given input waveform (top), the inverter produces the output waveform (bottom), which is the complementary of the input. Similarly the voltage transfer characteristic for the designed inverter is shown in Fig. 6(b), which shows the trip voltage of 0.5 V.

An important distinction of GFET based inverter to that of the conventional silicon based inverter is that the width of the n-type GFET and p-type GFET are same. This is due to the fact that the holes and electrons mobility is identical in graphene. However in the case of silicon, the hole mobility is almost twice less than that of the electron mobility. So to make p-type silicon transistor conduct as good as n-type silicon transistor, the width of p-type silicon transistor is made twice the width of n-type silicon transistor. This also suggests that the graphene transistor are very useful for area constraint applications. The complete GNRFET based SRAM circuit with all necessary peripheral circuitry is as shown in the Fig. 6.7.

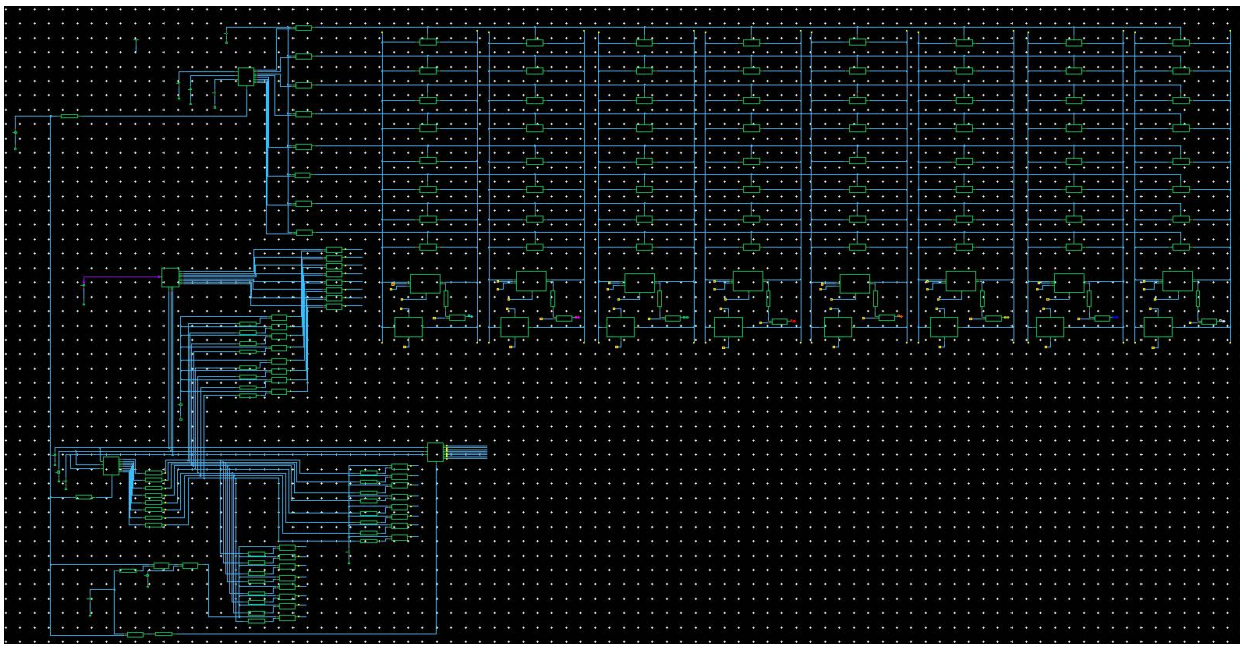
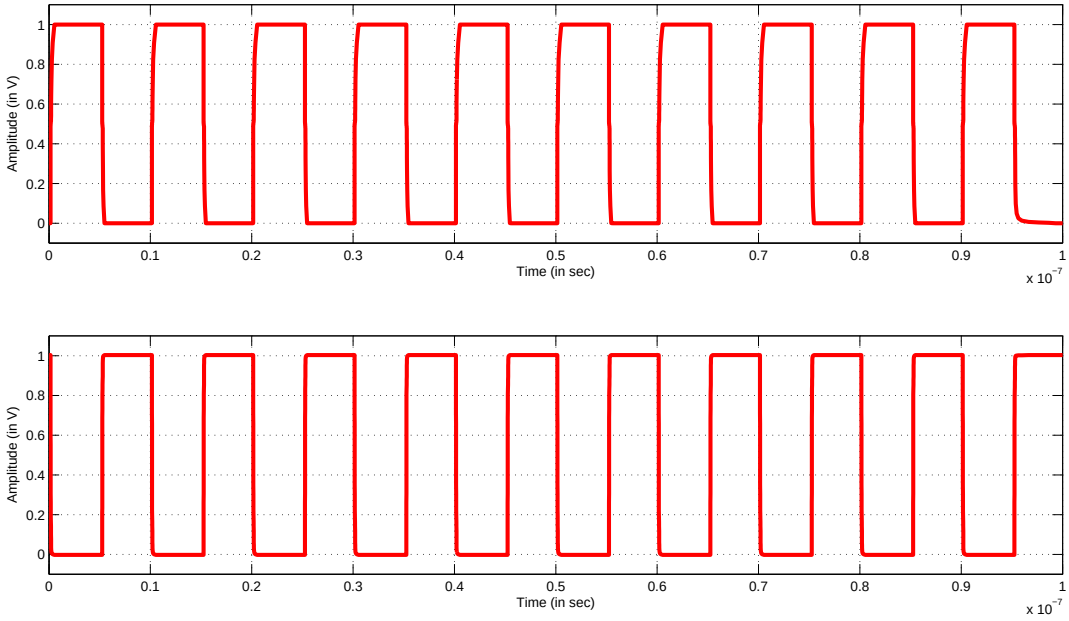
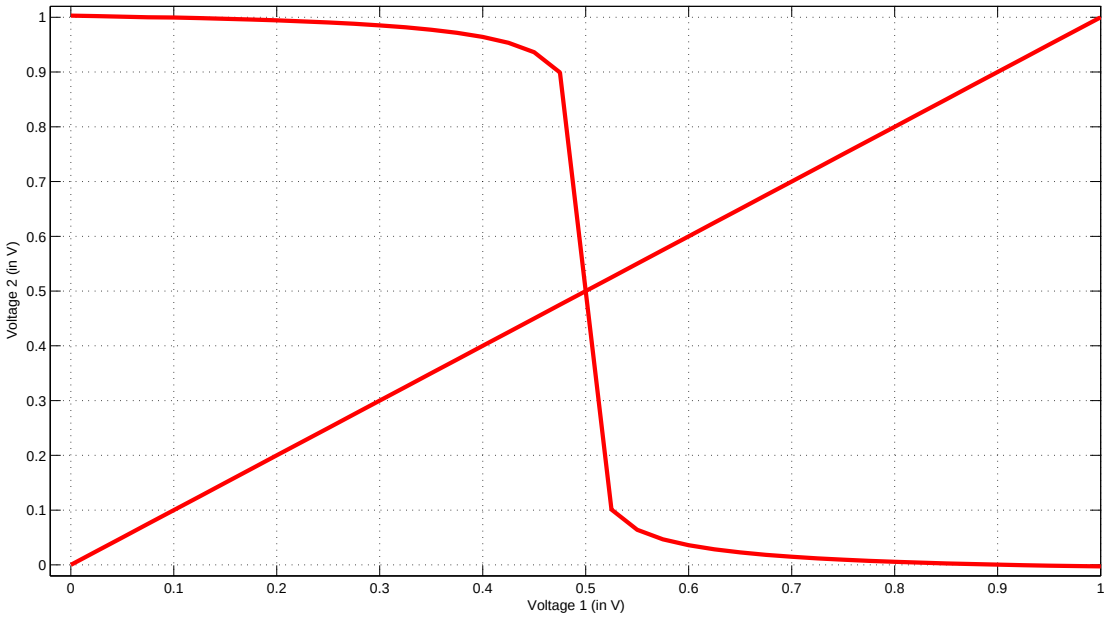


FIGURE 6.7. Complete Design of SRAM with peripherals



(a) Input-Output Waveform



(b) Voltage Transfer Characteristics

FIGURE 6.6. Graphene Based Inverter.

6.4.1. Read Stability and Write ability of the SRAM Cell

To analyze the SRAM cell stability, normally Butterfly curve and N-curve are used. N-curve provides information about both read and write stability within a single plot, so it has become more preferred way of defining SRAM stability [**51**]. Aspect ratio (Beta) is the ratio of the width of the transistor to the length of the transistor.

(1) Read Stability for SRAM Cell:

The cells become less stable with technology scaling due to low supply voltage, increased leakage and increase variability. Considering the node Q is holding 0. During the read operation, the voltage at node Q rises above $0V$ to the voltage determined by the access transistor T_5 and the pull-down transistor T_4 between the Bitline(BL) and the storage node Q. The voltage at which the memory cell flips its stored state is called the cell trip point. If the voltage at node Q exceeds the trip point of the inverter T_1 and T_2 then the cell will flip its state, causing the read upset. Thus the read stability is determined by the cell ratio of the cell.

(a) Read static noise margin(RSNM)

RSNM extracted from the read voltage transfer characteristics(VTC), is often used to quantify the SRAM read stability. RSNM represents the maximum DC noise voltage tolerated at each node $(Q/\bar{Q})$ before causing a read upset.

The equivalent circuit for determining the RSNM is shown in Fig. 6.8, where the voltage at the storage node Q (or $\bar{Q}$) is swept, keeping WL and both bitlines (i.e. BL and BLB) to V_{DD}, and measuring the voltage at another storage node $\bar{Q}$ (or Q). The resulting curve is known as the butterfly curve. By fitting the largest square within the read VTC, RSNM can be obtained from its side length.

The points A and C in the Fig. 6.9 are the stable points, while point B is a meta-stable point. When the sweep voltage at storage node Q (or $barQ$) becomes equal to the RSNM, the points A and B coincide, and the cell is at the edge of stability and can easily cause destructive read. Since during the read operation, the internal node holding 0 rises above the ground level and the cell is most vulnerable to the

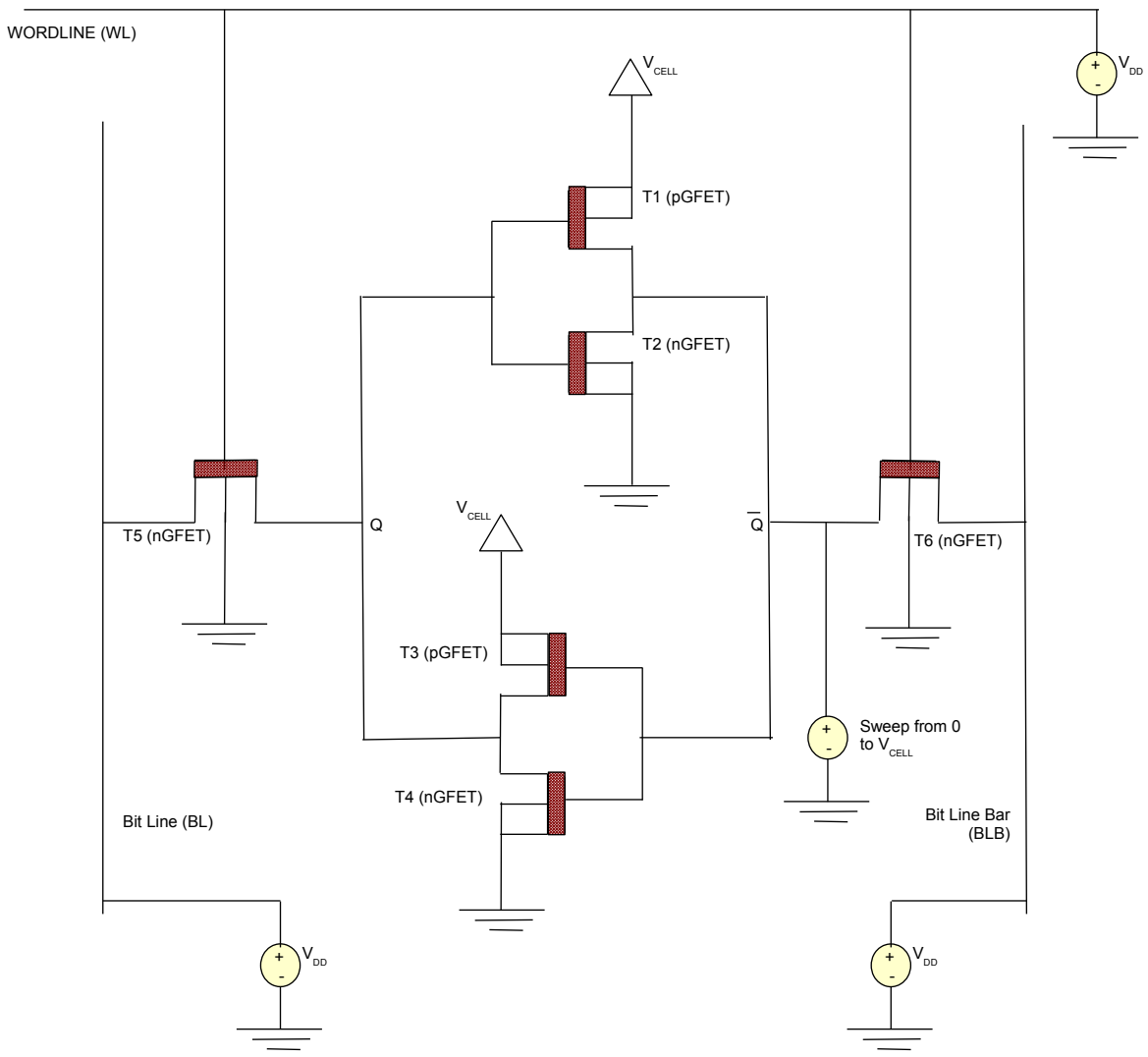


FIGURE 6.8. Circuit configuration for RSNM Calculation

TABLE 6.2. SRAM Transistor Sizing

Transistor Type	GNRFET Value	Silicon FET Value
Pullup Transistor	$n_{Rib} = 6$	100 nm (W)
Pulldown Transistor	$n_{Rib} = 10$	400nm nm (W)
Access Transistor	$n_{Rib} = 7$	150 nm (W)

noise. So the RSNM is primarily determined by the cell ratio (CR), which is defined as the ratio of aspect ratio of pull-down transistor and the aspect ratio of the access transistor. Comparing the RSNM value from Fig. 6.9, graphene based cell has RSNM

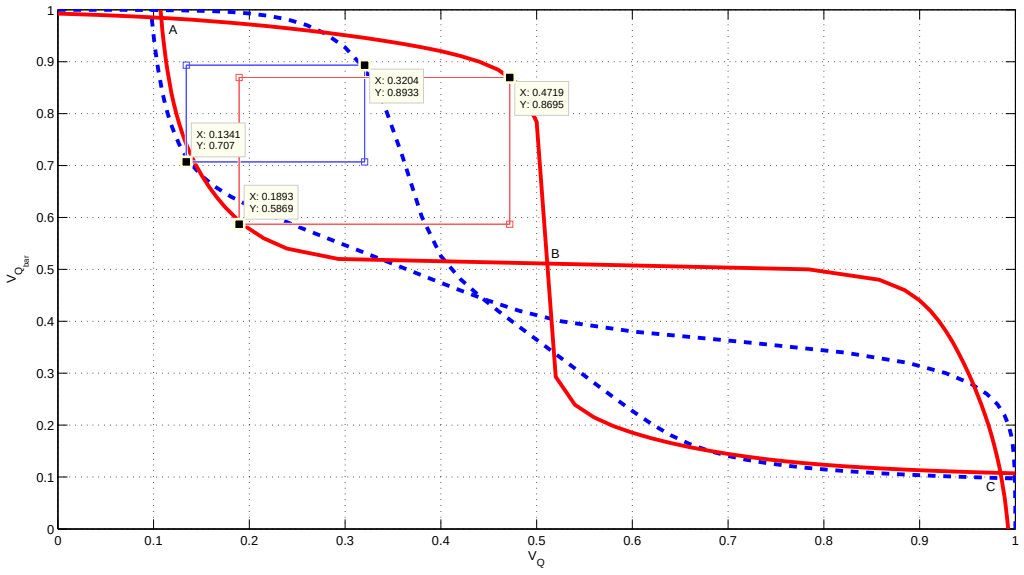


FIGURE 6.9. Simulated waveform for RSNM calculation for GEFT based SRAM (shown by solid line) and Silicon transistor based SRAM (shown by dotted line).

value of 282.6 mV as compared to 186.3 mV for silicon based transistor SRAM suggesting that graphene based SRAM offering more read noise margin as compared to conventional silicon based SRAM.

The main disadvantage of butterfly curve to determine the noise margin is that the inability to measure the noise margin by automatic inline testers and even after measuring the butterfly curve, the plot has to be post process to fit the square box.

(b) Static voltage noise margin (SVNM) and Static current noise margin(SINM)

An alternative approach to measure the SRAM stability is based on N-curve, which can be easily measured by the inline tester and provides both voltage and current information required for characterizing the read stability of the cell. The circuit configuration for N-curve is shown in Fig. 6.10.

To plot the N-curve, the voltage at the storage node Q (or $\bar{Q}$) is swept while keeping wordline and both bitlines (i.e. BL and BLB) biased at V_{DD} and measuring the external current sourced into the node Q (or $\bar{Q}$).

As can be seen from the Fig. 6.11, there are three zero-crossing points in the N-curve

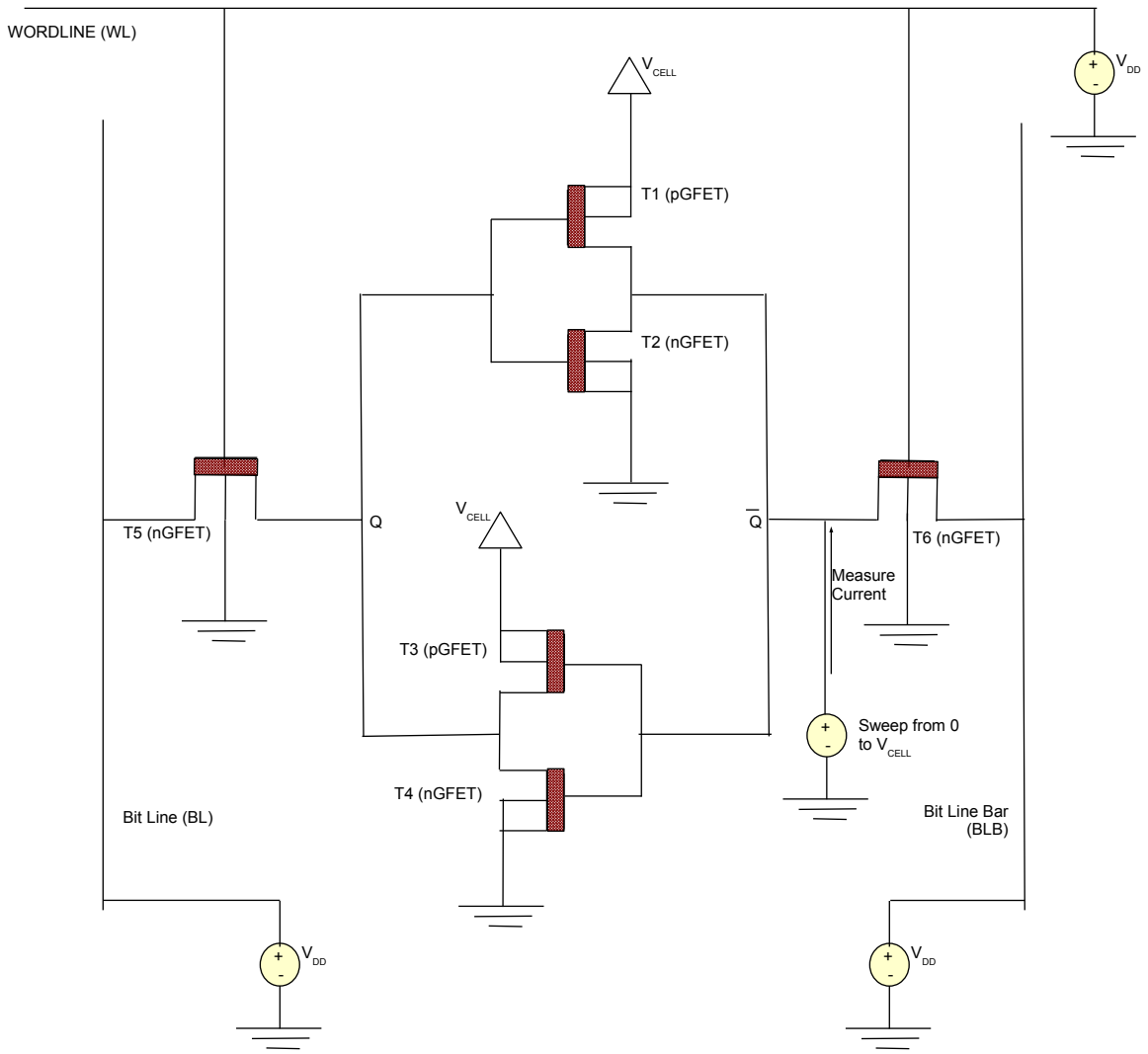
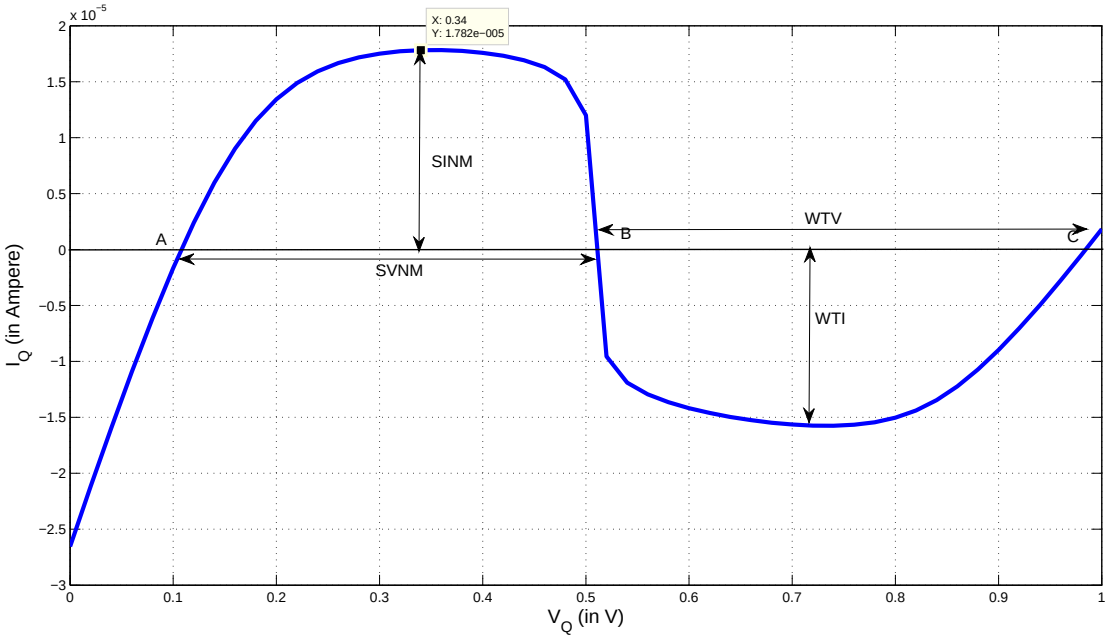
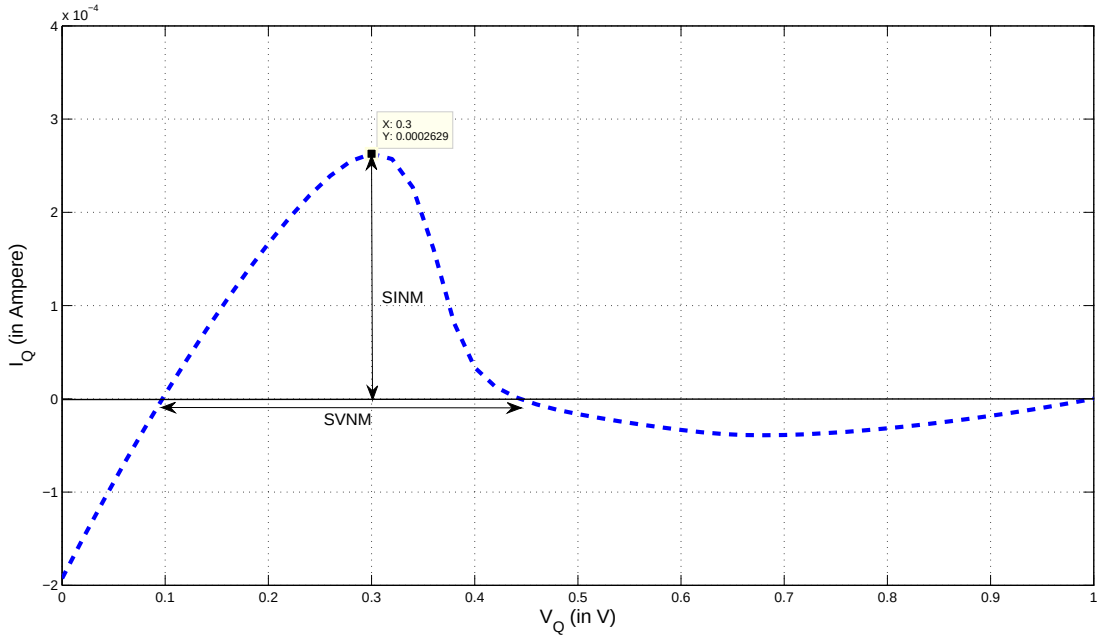


FIGURE 6.10. Circuit configuration for SINM Calculation

which corresponds to the three points (two stable points- A and C, and a meta-stable point B) as in the butterfly curve. The voltage in point A is determined by the cell ratio (CR) while the voltage in point C is determined by the pullup ratio (PR) i.e. the ratio of aspect ratio of the pull-down transistor and access transistor. The voltage in point B is determined by the pull-up and pull-down ratio [**51**]. The static voltage noise margin (SVNM) of the cell is given by the voltage difference between points A and B, which indicates the maximum tolerable DC noise voltage at the internal storage node before changing its stored information. The peak current between these



(a) Graphene based SRAM



(b) Silicon transistor based SRAM

FIGURE 6.11. Simulated waveform for SINM calculation

two points gives the maximum tolerable DC current which can be injected into the storage node of the cell before changing its content. This suffices the static current noise margin(SINM). Together with SVNM and SINM, the read stability of the cell can be properly defined. As can be seen from the Fig. 6.11 that graphene SRAM offers higher SVNM, which is around 400 mV as compared to that of the silicon based SRAM, which is around 340 mV. However the SINM value in graphene based SRAM is much smaller than that of silicon based SRAM.

(2) SRAM Cell Write-Ability:

Like read stability, it is important to guarantee the writeability in the cell without spending too much time in writing and energy to pull down the bitline voltage to $0V$. For this, a reasonable write-trip point, which is defined as the maximum voltage at the bitline required to flip the cell content, is necessary and is determined from the pull-up ratio. Similar to the read noise margin, a circuit for write noise margin is shown in Fig. 6.12.

Considering the internal storage node Q is holding 0, if the transistor pairs T_5 and T_1 pull the voltage at node $\bar{Q}$ below the trip point of the inverter, a successful write operation can be performed. Thus write noise margin(WNM) can be extracted using read VTC and write VTC, where write VTC is measured by sweeping the voltage at the storage node Q while keeping BL and WL biased at V_{DD} and BLB to ground and monitoring the voltage at node $\bar{Q}$. The side of the smallest square between the read VTC and write VTC gives the WNM. If the write VTC and the read VTC intersects each other, then the cell is not able to write correctly.

As can be seen from Fig. 6.13 the write noise margin is less in GFET based SRAM as compared to silicon transistor based SRAM. The WNM for GFET based SRAM is 366 mV while that in silicon based SRAM is 390 mV.

Similarly like N-curve for read stability, the writeability can also be characterized using N-curve. The N-curve for writeability is determined by sweeping the voltage at the internal storage node Q (or $\bar{Q}$) while biasing the WL and BLB (or BL) to V_{DD} and BL (or BLB) to ground and measuring the externally source current into the node Q (or $\bar{Q}$). If

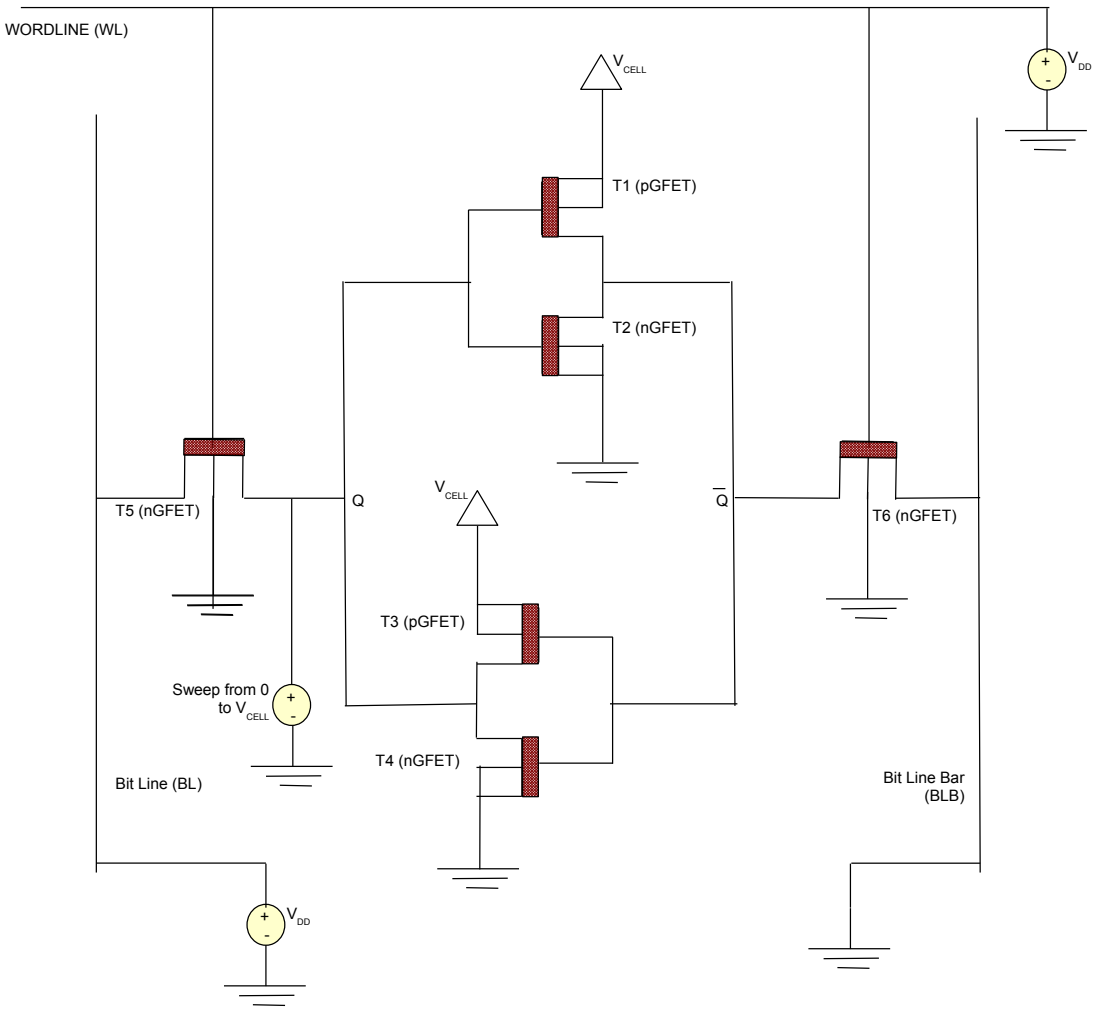
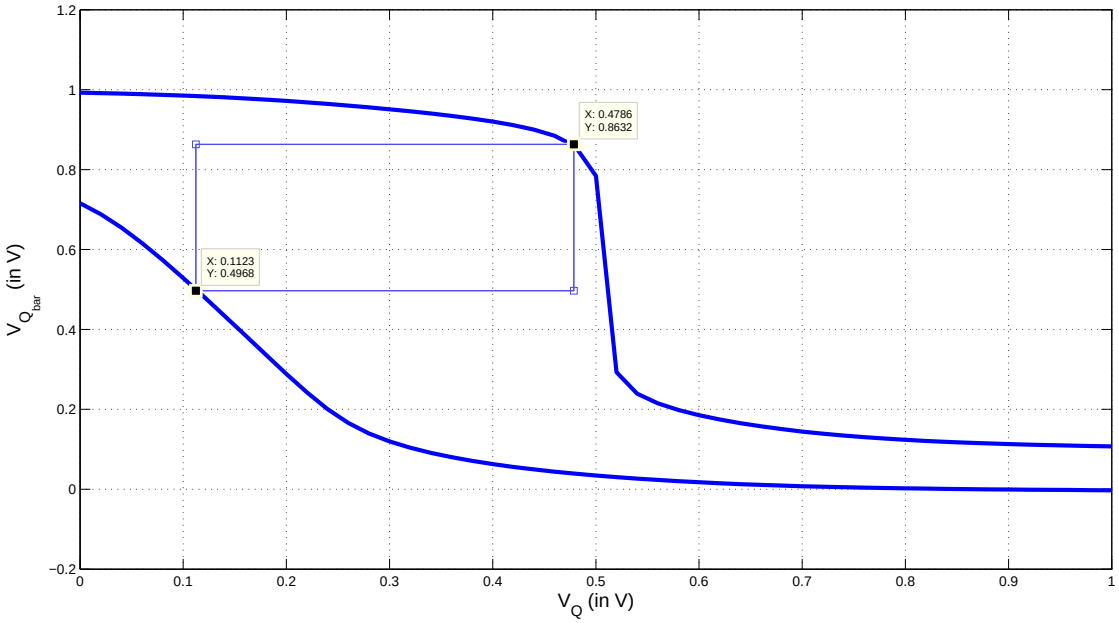
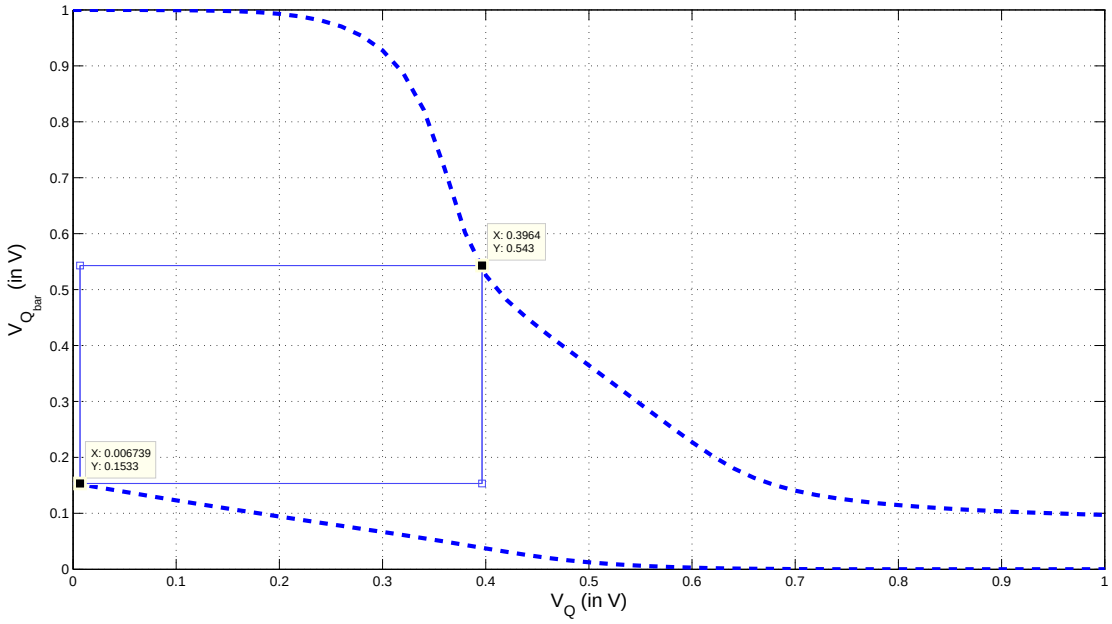


FIGURE 6.12. Circuit configuration for WNM Calculation.

the write current (IW) is less than 0, then it suggest the write failure which is equivalent to write VTC intersecting to read VTC. The simulated waveform is shown in Fig. 6.14.

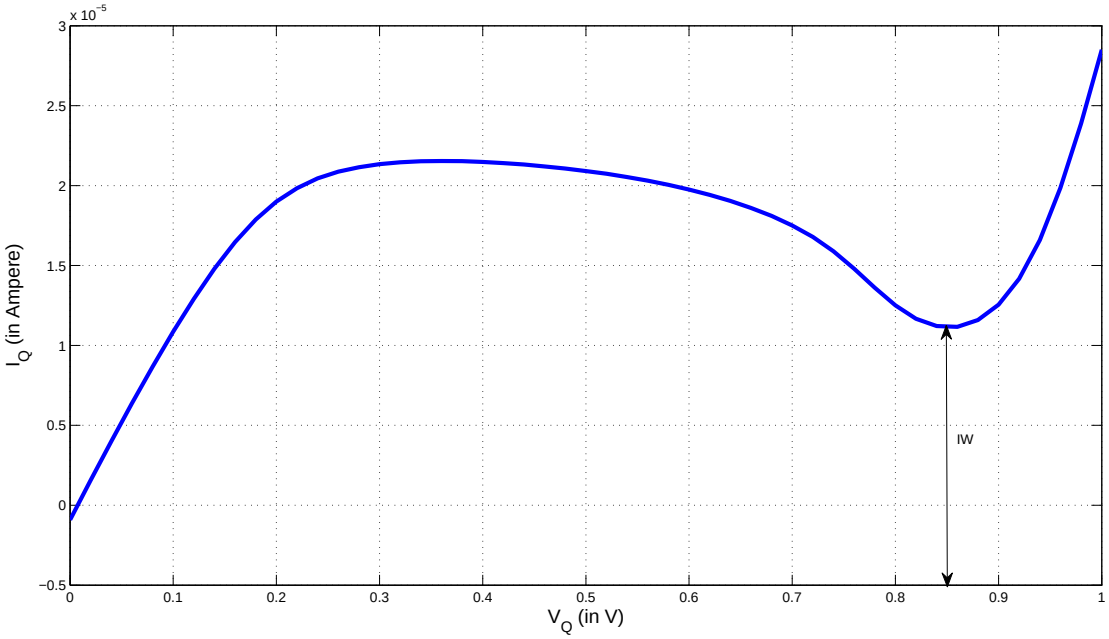


(a) Graphene based SRAM



(b) Silicon transistor based SRAM

FIGURE 6.13. Simulated waveform for WNM calculation



(a) Graphene based SRAM

FIGURE 6.14. Simulated waveform for Writeability current calculation

TABLE 6.3. Cell stability comparison

Description	GFET Based SRAM	Silicon FET Based SRAM
RSNM	282.6 mV	186.3 mV
WNM	366.4 mV	389.7 mV
SVNM	400 mV	340 mV
SINM	17.82 μA	262.9 μA
WTV	470 mV	430 mV
WTI	-16 μA	-40 μA

Table 6.3 shows the cell stability of two SRAMs. SINM (SVNM) is strongly related to read stability while WTI (WTV) is strongly related to write ability. Larger SINM ensures better read stability and smaller WTI means worse writeability. However there is a key design conflict in the design in the sense that the increase in the transistor widths of the cell degrades the write trip current while improving the SINM. Thus proper design needs to consider both read stability and

writeability.

Once the cell has been characterized, the verification of that 1-bit cell can be best described with the help of timing waveform as shown in the Fig. 6.15.

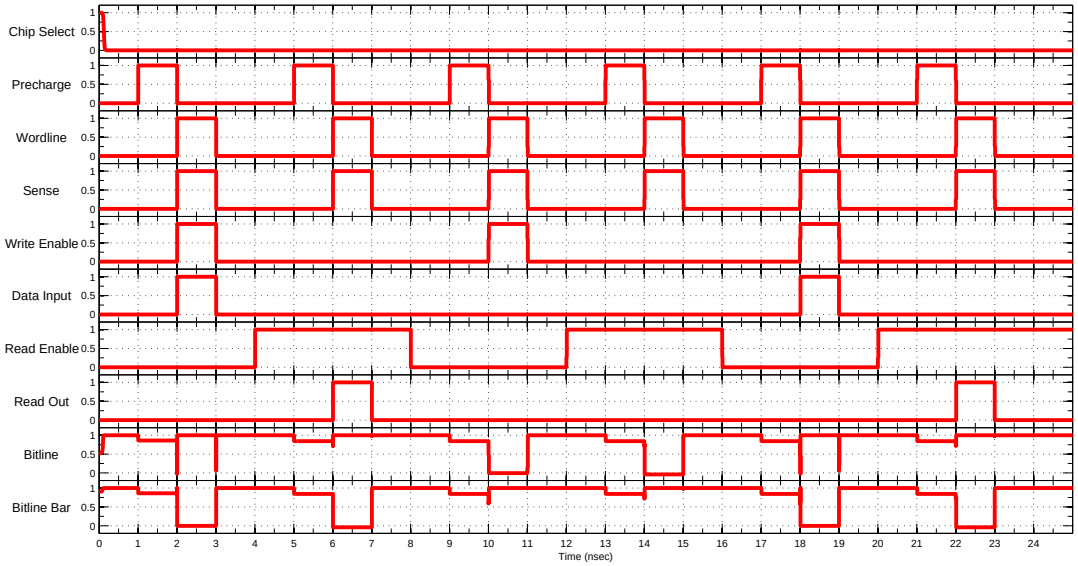


FIGURE 6.15. Timing Waveform for 1 bit SRAM Cell.

The cell has been written 1 first followed by reading the cell content. Then the state of the cell is changed to 0, in order to verify whether 0 can replace the previous content or not, followed by reading the state. Once again the cell is written with 1, followed by read operation. The output in the Fig 6.15 exactly matches to what has been expected, thus verifying the correct functionality of the 1-bit cell.

The concept is then extended to an array of size $8x8$ and the timing waveform is given as shown in the Fig. 6.16

6.5. Experimental Results

Followed by the functional verification of SRAM, it is necessary to characterize the SRAM array. Fig 6.17 shows the instantaneous power consumption scenario of the GFET based SRAM.

Comparing Fig. 17(a) and Fig. 17(b), it is obvious that the cells storing 1 consume more power than the cell storing 0. From Fig. 17(c), it is observed that the GFET based cell consume

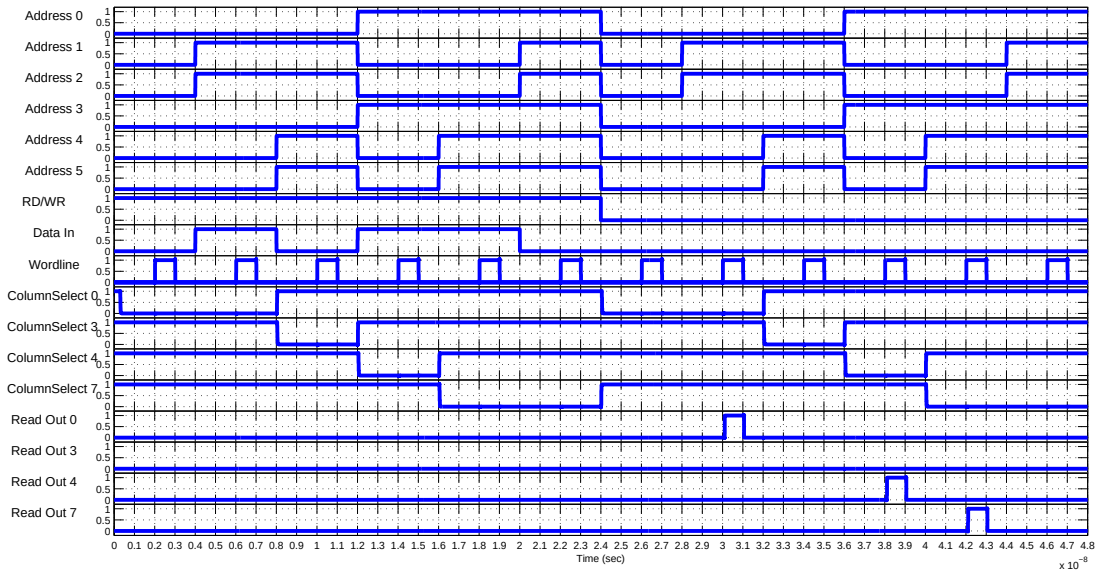


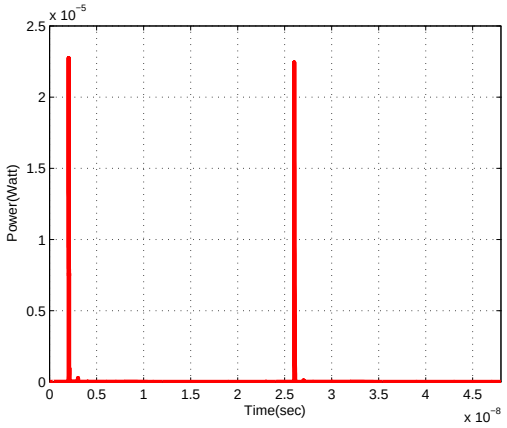
FIGURE 6.16. Timing Waveform for 8x8 SRAM Array

power even when it is not being accessed for reading and writing operation. This is due to the fact that the graphene transistor cannot be turned OFF completely, so there is a power consumption by those unaccessed cells as well. Fig. 17(d) shows the power consumption by all memory cells. Fig. 17(e) shows the power consumption by the entire design, including the peripheral circuits which are silicon transistor based. This shows that the majority of power consumption is by the silicon based transistors, while very small portion of power is consumed by the graphene based memory cells.

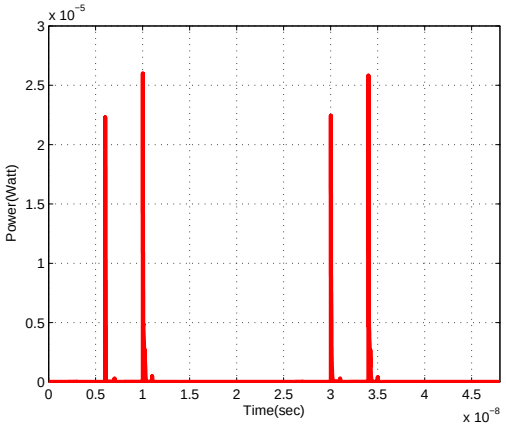
The corresponding instantaneous power consumption for silicon based SRAM under the same scenarios is shown in the Fig. 6.18.

Comparing the power consumption profile of the GFET based SRAM with the conventional silicon transistor based SRAM.

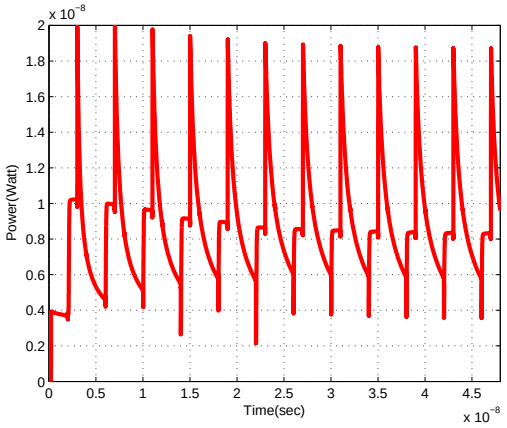
From table 6.4, it can be seen that the average power consumption of silicon based memory cell far exceeds the average power consumption by the graphene based memory cells. The use of graphene based SRAM saves the average power by 93% maintaining the read and write stability as compared to silicon based SRAM. So graphene based circuits are very much applicable in both



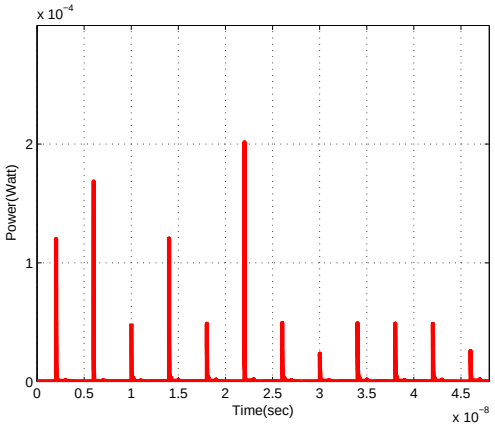
(a) Cell storing '0'



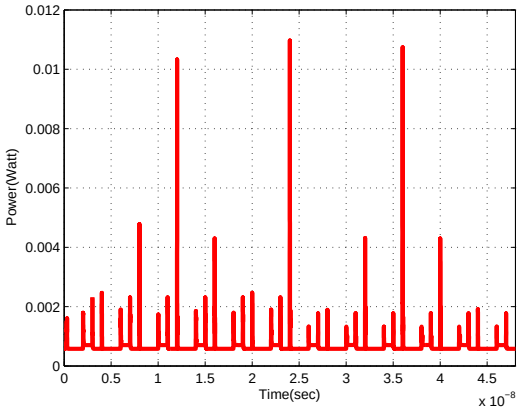
(b) Cell storing '1'



(c) Other cells

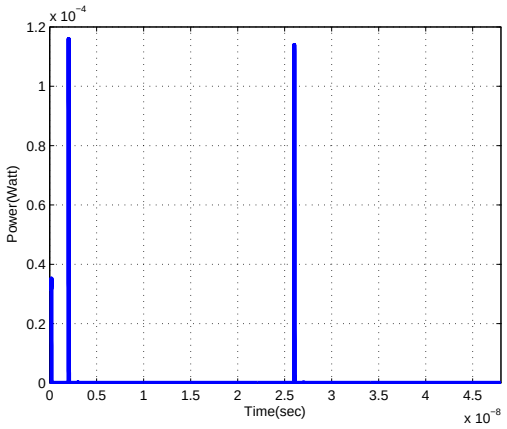


(d) All Cells

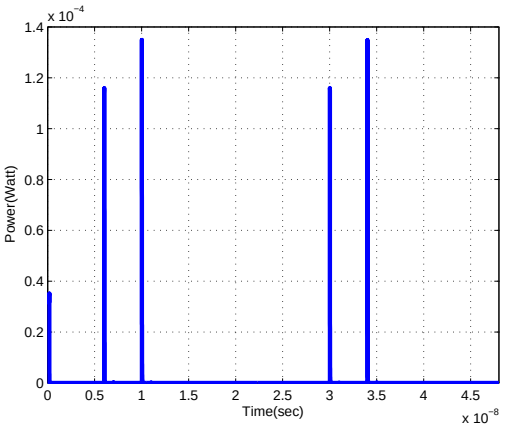


(e) All circuits

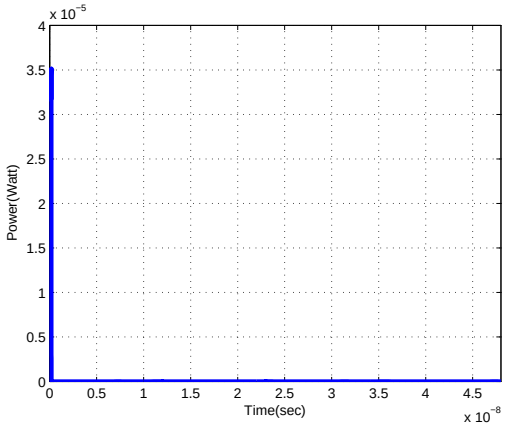
FIGURE 6.17. Instantaneous Power Consumption of GFET based SRAM.



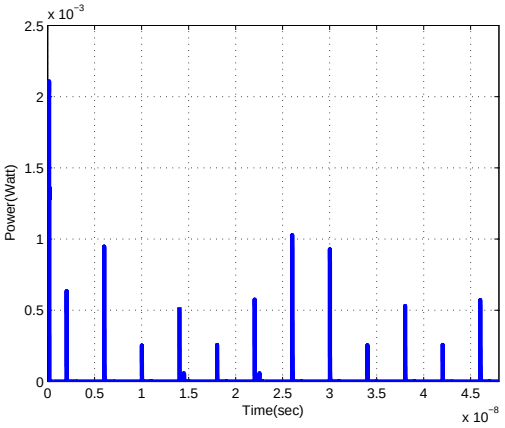
(a) Cell storing '0'



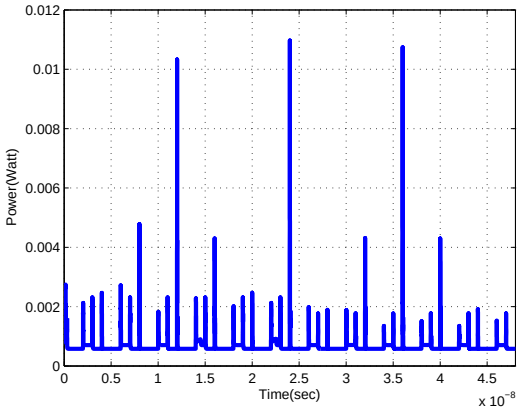
(b) Cell storing '1'



(c) Other cells



(d) All Cells



(e) All circuits

FIGURE 6.18. Instantaneous Power Consumption of Si based SRAM.

TABLE 6.4. Average Power Consumption Comparison of SRAM.

Description	GFET Based SRAM	Silicon FET Based SRAM
Cell storing 0	28.71 nW	221.3 nW
Cell storing 1	84.7 nW	330.5 nW
Other cells	8.686 nW	137.4 nW
Array	796.4 nW	11.49 μW

power constraints as well as area constraint applications.

CHAPTER 7

CONCLUSION AND FUTURE RESEARCH

7.1. Summary and Conclusion

In chapter 3, a cross coupled version of LC-VCO oscillator is successfully designed using Verilog-A modeling language. The same design has been used in chapter 5 as a baseline LC-VCO to perform optimization of the circuit. The netlist obtained from the baseline oscillator is used to apply MSO for the given objective function, design variables and constraints.The baseline LC-VCO with center frequency of 2.56 GHz was initially designed in chapter 3 and the final optimized LC-VCO shows a center frequency of 2.58 GHz in chapter 5 satisfying the design constraints of phase noise and power dissipation. The power dissipation and phase noise are 26.625% and 16.15% below their maximum values.

A Simscape® based behavioral model of graphene FETs, suitable for design exploration at high levels of abstraction, has been presented in chapter 5. The model has been verified by extensive I-V characterization of the GFET. As a case study, two circuits (LNA and LC-VCO) are considered and the results are compared with the well accepted DA models. The results obtained using Simscape® match closely with those models and hence it is shown that the Simscape® based model can be used as a substitute for more detailed but time consuming EDA simulations such as SPICE with Verilog-A and VHDL-AMS models. Thus the ability to perform mixed high-level (behavioral) and transistor-level simulations for RF systems with an integrated design environment provides RF designers with unique design exploration and verification tools.

The design of digital circuit using graphene nanoribbon has been analyzed under ideal condition. The result shows that the graphene nanoribbon has a great potential in the digital circuit design leading to significant less power consumption, which is approximately 93% as compared to $45nm$ silicon technology. The performance degrades with device imperfection like nanoribbon edge and other. However the performance gets close to the ideal, once the technology gets matured.

7.2. Future Research

In future research for chapter 4, additional functionality for noise, transfer function and non-linear RF analyses such as periodic and quasi-periodic steady state are planned to incorporate within Simscape® model. Further, it is planned to explore techniques for GFET based circuit optimization with the proposed Simscape model using particle swarm-based optimization algorithms such as artificial bee colony and ant colony optimization.

As a future work for chapter 5, an alternate design approach, surrogate model of the circuit can be created which can then be used to perform optimization instead of using netlist, in order to reduce the optimization time. In order to perform parasitic aware design, parasitic extraction can be done and multi-objective optimization will be performed to obtain the final layout.

In chapter 6, the variation of device imperfection can be incorporated to analyze the effect of variation in device parameter to the device performance.

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