Final Technical Report

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Project Title: Volmer-Weber Growth of Nanoscale Self-Assembled Quantum Dots
Project Period: August 15, 2005 – August 14, 2009

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1. Summary

Our research has focused on the fundamental understanding of the physical mechanisms and experimental methodologies to probe various growth conditions, their effects on density, size uniformity, and spatial organization of self-assembled quantum dots (SAQDs). Theoretical models and numerical simulations have been developed to understand the nonlinear dynamics of surface pattern evolution and self assembly processes. Fabrication processes of semiconductor and metal SAQDs on high-k dielectrics have been developed, which have enabled the technology development of high-speed, low-power nonvolatile memory devices for nanoelectronics applications.

Over the four years of the project, six graduate students have been trained in this research project, and four of them have graduated with PhD degrees. Our research has been reported in 11 journal articles. Both PIs and their students have given numerous presentations at national/international conferences as well as invited seminars. A list of publications and presentations is attached to the end of this report.

2. Experimental Research

We have focused on the technology and underlying science for high-speed, low power, planar and vertical Flash Electrically Erasable and Programmable Read Only Memories (EEPROMs) using high-k dielectrics and Si-Ge-C or metal SAQD floating gates. Conventional flash EEPROMs have several serious drawbacks and we investigated new memory cell structures with the goal of providing a compact, low-power, high-speed (programming, erase and read operation) semiconductor memory technology for future integrated circuit devices. The research experimentally and theoretically explored: (1) the growth of ordered arrays of Si-Ge-C and metal nanoparticles on dielectric surfaces, employing chemical/physical vapor deposition (CVD or PVD) techniques that uncouple nucleation from growth. We achieved high densities, spatial control and narrow particle size distributions, in concert with bio-nano self-assembly techniques; (2) application of high-k-based flash memory to allow for physically thicker, but electrically thinner "equivalent" oxides; (3) low band gap, high mobility Si-Ge-C heterolayers in the channel of planar flash cells to act as "cold cathodes"; (4) a novel 3D architecture with vertical flash EEPROMs incorporating nanoscale SAQDs as the floating gate; (5) first-principles modeling of nanoparticle structure evolution, including nucleation, growth, crystallization, and encapsulation within the dielectric to support experimental growth studies; and (6) modeling of hot carrier transport by hydrodynamic and Monte Carlo simulation, tunneling transport using transfer matrix methods, and quantum transport calculations of Coulomb blockade effects in the SAQDs.

The demand for high-density, low-cost, low-power/voltage, and high speed (programming, erase and read operations) semiconductor memory has led to current non-volatile

flash memories to proliferate into new approaches such as nanoparticle floating gate and single/few electron memories. This allows the tunnel oxide to be scaled down more aggressively because weakspots now erase only the nanoparticles above it. SAQDs enhance charge retention and VT stability, as well as possibly allow multi-level storage based on Coulomb blockade. High-k-based dielectrics provide high capacitive coupling, without sacrificing non-volatility, and allow for lower-voltage and/or higher-speed operation through the potential-reduction in barrier height to channel hot electron (CHE) injection and tunneling, and increased device lifetime because of the thicker tunneling barriers under low field storage conditions. Si-Ge-C planar flash cells should enhance impact ionization and CHE, for reduction of operating voltages/powers and increasing programming speed. Vertical cell structures allow the highest possible densities in a so-called cross-point architecture where the cell is located at the intersection of the wordline and bitline.

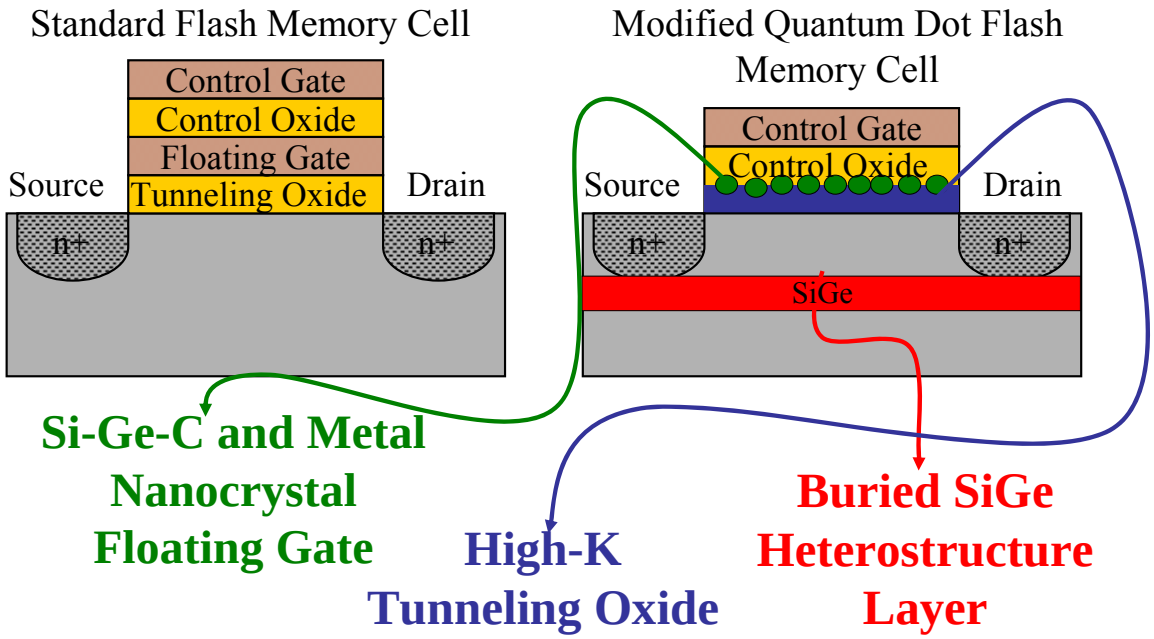

Fig. 1 Use of SiGe SAQD floating gates with high-k tunnel dielectrics in non-volatile flash memories. SiGe "cold cathodes" in substrate can enhance the hot carrier programming currents.

Our research has therefore focused on three areas to address the above issues (Fig. 1). We replaced the SiO_2 gate dielectric with high-K dielectrics to allow for thinner equivalent oxide thickness (EOT) in order to maintain the high coupling capacitance between the floating gate to the external world, without sacrificing non-volatility, and to allow for lower-voltage and/or higher-speed operation and increased device lifetime. The high-k dielectrics have a lower bandgap, but are physically thicker than SiO_2 for the same EOT. At high fields corresponding to programming or erase, the bands for the high-k dielectric bend sufficiently to cause FN tunneling through a narrow triangular barrier, while for the higher bandgap SiO_2, it stays in the direct tunneling regime. This allows programming and erase for the high-k based cells at lower voltages, as confirmed theoretically and experimentally (Fig. 2). At the same time, under

retention conditions, since the fields are low, the bandbending is less and the barriers are much wider for the high-k case, leading to reduced charge loss (Fig. 3).

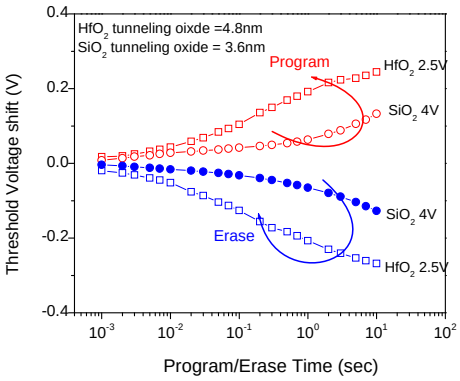

Fig. 2 Lower voltage program and erase of flash memory using SiGe self-assembled nanocrystals and high-k versus SiO_2 gate dielectric because of lower bandgaps and thicker barriers.

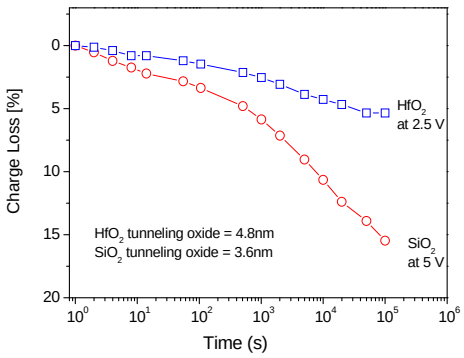

Fig. 3 Retention characteristics of HfO_2 and SiO_2 tunneling dielectric memories with SiGe nanocrystals after an initial +2.5 V and 5 V programming.

Secondly, we have investigated Si and SiGe(C) quantum dot formation on the high-k dielectrics. Since SiGe has a lower bandgap than Si, it has deeper potential wells when embedded in the gate dielectric and hence longer retention times. Preliminary data seems to confirm this though there are anomalies at longer storage times. This may be because the charge storage is not in the nanoparticle itself but at traps at the interface between the nanoparticles and the dielectric, which may be deeper for SiGe than for Si. There are concerns that Si nanoparticles embedded in SiO_2 will have too high of a charging energy as the dots are reduced in size in scaled memory cells because of reduced dot capacitance. Embedding them in a high-k dielectric and using lower bandgap SiGe dots may mitigate this concern.

The third approach we have adopted to address the scalability issue of the flash cells is to use Channel Initiated Secondary Electrons (CHISEL) instead of simply CHE, with low bandgap SiGe "cold cathodes" embedded in the channel of the MOSFET to enhance hot programming currents at lower voltages and shorter channel lengths. Monte Carlo simulations show that CHISEL programming is achieved more uniformly into the gate than CHE, which is important for the discontinuous nanoparticle floating gates. The use of low bandgap SiGe cold cathodes can enhance the gate currents by factors of ~5X compared to Si channels.

The use of SiGe SAQD floating gates on high-k gate tunneling dielectrics, with SiGe cold cathodes in the channel are proved to enhance the low voltage/power operation of flash cells, improve the speed and charge retention. Control of the dot sizes and spatial distributions may be further improved by templated growth using block-copolymers or protein-assisted assembly (Fig. 4). It may be possible to exploit Coulomb blockade and multi-level storage in single electron/ few electron charge memories.

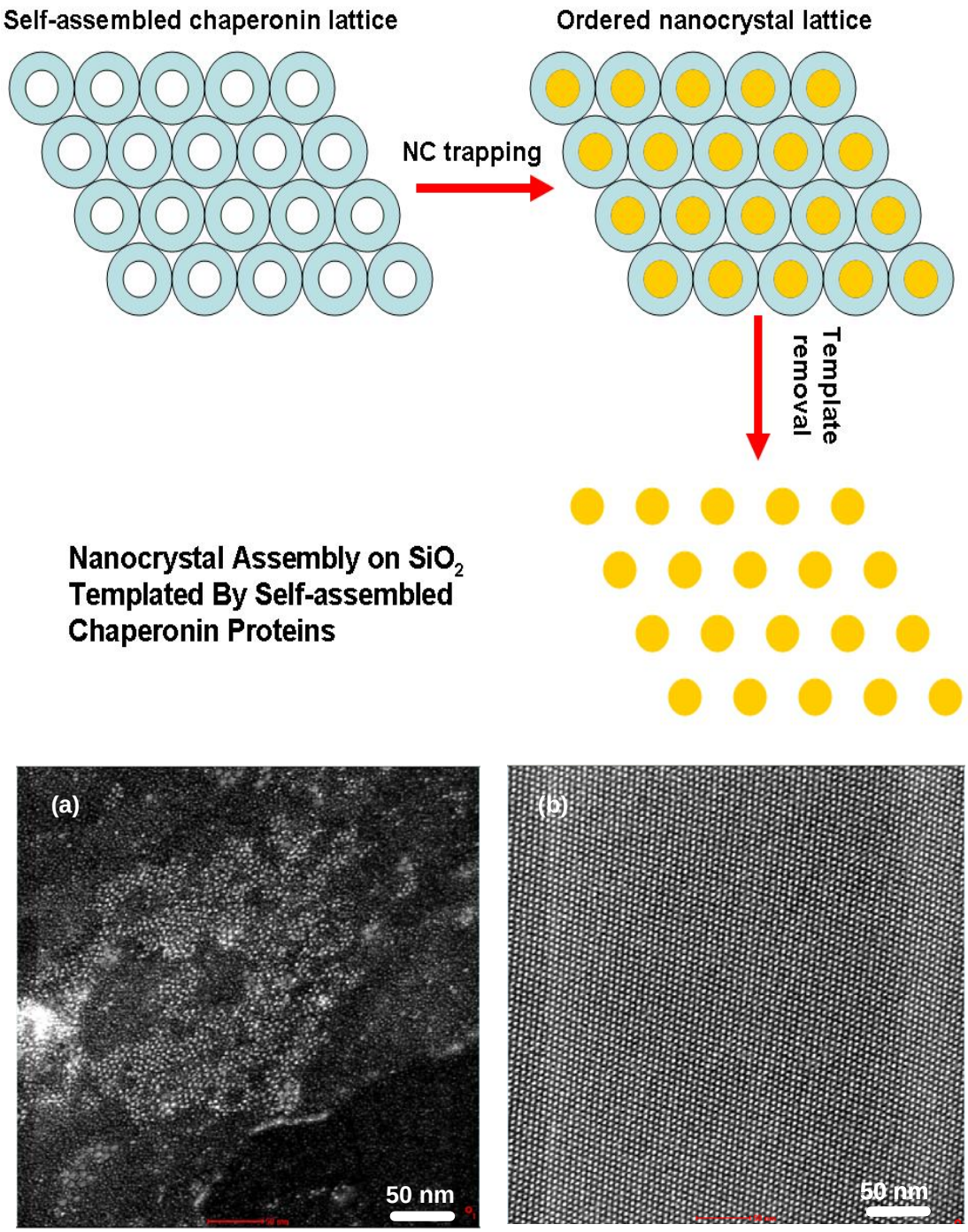

Fig. 4. Top: schematic of protein-assisted self-assembly of nanocrystals on dielectrics. Bottom: AFM images of PbSe nanocrystals without and with chaperonin-assisted self-assembly.

We have also fabricated n-type MOSFETs with PbSe nanocrystal embedded floating gate and high-K dielectric (HfO_2) on p-type Si (100) substrates. A PbSe nanocrystal matrix was self-assembled with the aid of the chaperonin protein as illustrated in Fig. 4. A 10 nm HfO_2 layer was sputtered on to form the control oxide layer in the same way as tunnel oxide deposition. To stabilize the HfO_2 stack, the wafers were annealed in nitrogen for 10 minutes at $550^\circ C$. The control gate was done by 200 nm PVD TaN deposition. Reactive ion etching with CF_4 gas and BOE etching were used to form the gates as well as the implantation mask. The source and drain implantation was done by Arsenic source with energy of 40KeV and dose of $5e^{15}$ / cm2 at 7 degree angle. After an activation annealing at $850^\circ C$ in nitrogen for 1 minute, the isolation oxide was deposited by low pressure CVD at $530^\circ C$ and Al was finally deposited and patterned as contacts. The memory characteristics were tested with tunneling program/erase, resulting in a memory window (threshold shift) bigger than SiO_2 gate even with much lower pulse voltage. Stable retention of the memory cells beyond 10^5 s at $85^\circ C$ and endurance beyond 10^4 cycles are achieved.

Self-assembly with surface chemistry control in CVD

Our research sought to develop a description of the surface chemistry that enables the precise positioning of Si and Ge quantum dots on amorphous oxide surfaces under chemical vapor deposition conditions. This requires that the process be robust at temperatures near 775 K. The key to uniform and high density nanoparticle growth on amorphous surfaces is to accumulate as many adatoms in the shortest possible time on the substrate. At the outset we considered a number of ways to block the substrate surface selectively or to deposit reactive centers. In the process we needed to understand how the adatoms form and interact with the various surfaces. Through a series of papers we described the interaction of Si and Ge with SiO_2, HfO_2 and Si_3N_4 surfaces. These papers explored the interfacial reactions and the kinetics of the reactions that lead to the accumulation of adatoms and the desorption/etching of adatoms. One outcome of these surface studies was the finding that there are temperature windows, or kinetic windows, over which adatoms etch SiO_2 and accumulate on either HfO_2 or Si_3N_4. This suggested a strategy for the selective deposition of nanoparticles on HfO_2 or Si_3N_4. A thin film (~12 nm) of SiO_2 coated on HfO_2 or Si_3N_4 could have windows (features) opened to the HfO_2 or Si_3N_4 below and then during CVD exposure, the nanoparticles would only form on the HfO_2 or Si_3N_4 and not on the SiO_2. Both e-beam lithography and lithographic patterns generated using self-assembly of diblock copolymers was employed to illustrate the limits of this method.

We have showed with Ge, that selective nanoparticle placement is possible during hot wire chemical vapor deposition (HWCVD) by employing a thin (12 nm) SiO_2 mask through which ~ 22 nm vias are etched to expose HfO_2. The more facile etching by adsorbed Ge of SiO_2 versus HfO_2, affords a kinetic window between 700 and 800 K in which the Ge adatoms can accumulate on HfO_2 and not on SiO_2, and eventually nucleate and grow into nanoparticles selectively on the HfO_2 regions. The lower limit of this window is set by a temperature required to etch SiO_2 faster than the adsorption of Ge (or more correctly GeH_x by thermally cracking GeH_4 over a filament). The upper temperature is set to minimize Ge loss from HfO_2 by etching reactions. The kinetic window for Si etching of SiO_2 versus HfO_2 is narrower (900-925 K), and as a consequence Si nanoparticle growth is not as selective as was found for Ge. Silicon nanoparticles deposited at 900 K were found on both SiO_2 and HfO_2, however, with a considerably higher density on HfO_2. Silicon nitride is not etched by adsorbed Si and is therefore ideally suited for the selective CVD growth of Si nanoparticles employing a SiO_2 sacrificial

mask. With Si on Si_3N_4 there is no upper etching limit, enabling one to work over a wider temperature range to observe the effects of adatom concentration on nucleation and growth. We demonstrated the versatility of selective nanoparticle growth within ~17 nm pores by extending it from the Ge on HfO_2 system to the Si on Si_3N_4 system. Growth is directly on the Si_3N_4 (or HfO_2) dielectric surface, possibly simplifying future incorporation of this method into device fabrication. The silica hard mask regulates nanoparticle nucleation and growth through adatoms etching the silica and evolving as gaseous SiO. The silicon deposition rate is dependent upon the balance of the adatom removal mechanism and nanoparticle nucleation and growth reactions. Maintaining a sufficient Si flux to exceed the etching rate is key to nanoparticle growth. Nanoparticle growth decreases with increasing temperature and increases with increasing incident flux of SiH_x radicals in HWCVD.

We also explored the kinetics of nucleation so one could model the processes and develop predictive models for CVD growth. The Ge/HfO2 system was selected for these studies and the mean-field nucleation theory based scaling models were employed. Germanium nanoparticle deposition kinetics were investigated on extended HfO_2 surfaces and HfO_2 confined within features etched into a 12.5 nm SiO_2 film. Electron beam lithography was used to pattern square features 200 nm to 100 μm in width. We demonstrated the ability of Ge HWCVD onto HfO_2 surfaces to investigate Volmer-Weber mode kinetics. A critical cluster size was calculated in the range of 0.3–0.4 and is estimated most likely to be zero. This implies that nucleation occurs on defect sites. The critical cluster activation energy was estimated using mean field nucleation theory as 0.6 ± 0.3 eV or 0.4 ± 0.2 eV for energetic Limits I and II, respectively. Confined deposition decreases nanoparticle density when Ge^0 desorption is significant by reducing adatom concentration in a similar manner as reducing the deposition flux on extended surfaces. Restricting the HfO_2 deposition area in the 1 to 100 μm feature dimension range had no effect on particle density with increasing flux when the flux is greater than or equal to 0.6 ML/min. Therefore, the nucleation kinetics is likely unchanged as the HfO_2 is confined by SiO_2. The results on both the extended and confined surfaces suggest the activation energies for nucleation, surface diffusion, and Ge loss from SiO_2 surfaces are close in value, and the value for Ge loss from SiO_2 has been reported as 0.42 eV.

Surface State control with core shell nanocrystals

To investigate the effect of core-shell structure, three kinds of structures were fabricated: I) bare Ge dots, II) Ge dots with top Si capping layer, III) Ge dots encapsulated in an ultrathin Si layer (Fig. 5). After 50 cycles of atomic layer deposition (ALD) of HfO_2 as tunnel oxide on P type silicon substrates, an ultrathin Si layer less than 1 nm was deposited only for sample III by thermal chemical vapor deposition (CVD) of silane. Ge dots were then grown by hot wire chemical vapor deposition (HWCVD) on bare HfO_2 (sample I & II) and on Si (sample III). After that, 2 nm of top Si capping layer was selectively grown on the Ge dots by thermal CVD for samples II and III. Low energy ion scattering (LEIS) was used to determine in situ outer layer material composition in this step. 15 nm HfO_2 control oxide was produced by reactive DC sputtering in Ar/O_2 ambient (100w, 2min) and finally 200 nm TaN was deposited on as electrodes by reactive DC sputtering (1100w, 5min). Scanning electron microscopy (SEM) and cross-section transmission electron microscopy (TEM) were used to examine the formation of Ge dots on the HfO_2 surface and the Si capping results. Fig. 6 shows that Ge dots are well formed and encapsulated in thin Si layer. X-ray photoelectron spectroscopy (XPS) was used to

investigate the Si capping effect, which proves that the Si capping layer can increase thermal stability of Ge dots.

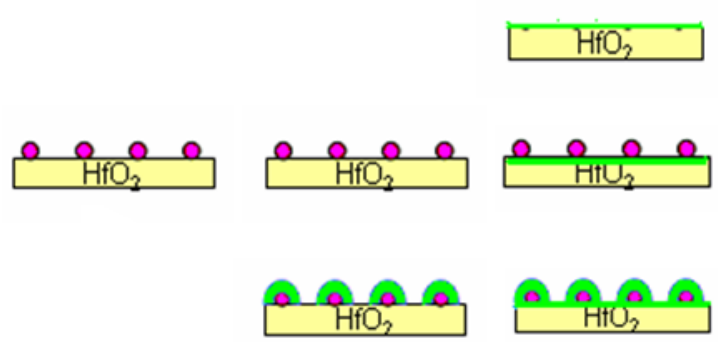

Fig. 5. Three types of dots on HfO_3: I) bare Ge dots; II) Ge dots with top Si capping; III) Ge dots capsulated in Si layer.

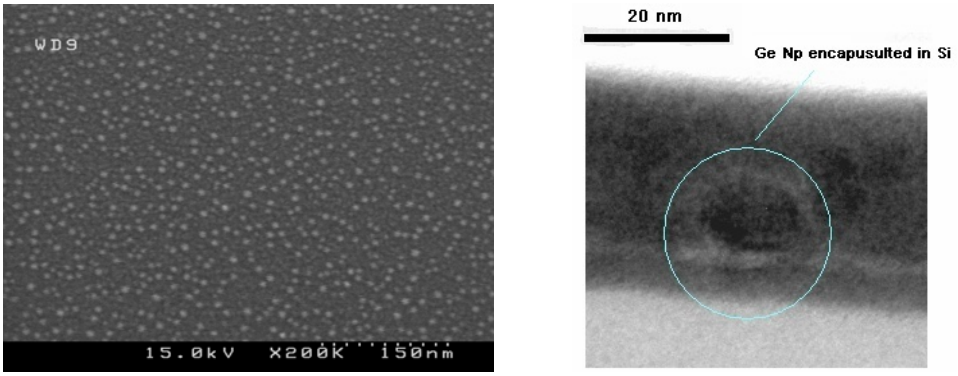

Fig. 6. a) SEM image of Ge dots grown on HfO_2 surface; b) cross-section TEM of Ge dots capped with thin Si layer

High frequency C-V measurements show that memory window of each sample is similar. The transient characteristics show that the program/erase speed for each sample is quite close, indicating that the Si capping has very little influence on programming efficiency. This is because of the ultrathin thickness of the Si layer, especially the bottom Si layer. On the other hand, the devices with core-shell structured Ge dots have better endurance performance than those with bare dots, which is believed due to fewer interfacial traps which are considered not stable under stress cycles. It is obvious that sample II and III have much better retention characteristics than sample I.

3. Modeling and Simulations

A theoretical modeling framework for surface evolution and self-assembly of nanoscale quantum dots has been developed, with a physics-based nonlinear evolution equation and a spectral method for numerical simulations. In particular, the nonlinear effects of stress and wetting interactions were examined in details. By introducing stress and elastic anisotropy, break of symmetry in the evolution process was demonstrated. Furthermore, a bifurcation in pattern formation was discovered. These results illustrate the rich dynamics of surface self-assembly,

suggesting new routes for the making of desirable patterns, and in particular, engineering-directed self-organization of nanoscale quantum dots.

The nonlinear evolution equation takes the form

$$\frac{\partial h}{\partial t} = \Omega^2 M_{\alpha\beta} \frac{\partial^2}{\partial x_\alpha \partial x_\beta} \left[\left(U_E + U_S + U_W \right) \sqrt{1 + h_\chi h_\chi} \right], \tag{1}$$

where three energetic terms are considered based on a non-equilibrium thermodynamic formulation: U_E for elastic strain energy, U_S for surface energy, and U_W for interfacial wetting potential. The competition of these thermodynamic forces determines the stability and the evolution process of the epitaxial film.

The elastic strain energy is obtained by solving a nonlinear boundary value problem of elasticity with a wavy surface. It is found that the nonlinear stress field has a significant effect on the long-term evolution of surface patterns, although a linear analysis is sufficient for the determination of the critical condition and the short-term evolution at the early stage. Figure 7 shows a circular pit-like pattern from a numerical simulation, resembling the "quantum rings" and "quantum fortresses" patterns observed in experiments.

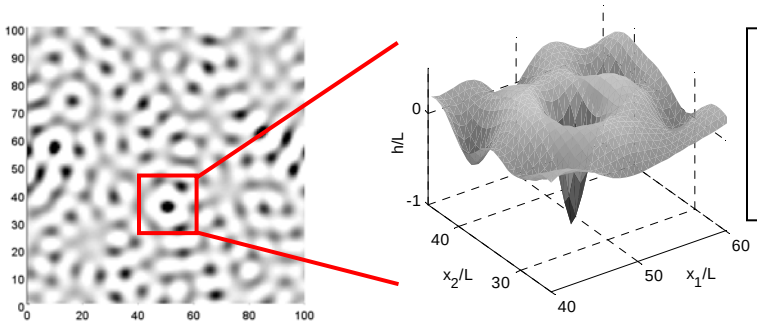

Fig. 7: A circular pit-like pattern from a numerical simulation with the nonlinear stress field.

A nonlinear wetting potential based on a transition-layer model is incorporated in Eq. (1) for the study of interfacial wetting effect. A linear analysis shows that the wetting effect can stabilize very thin films, which leads to a critical thickness for surface instability. This critical thickness depends on the mismatch stress as well as the thickness of the interfacial transition layer. This is consistent with experimental observations for the Stranski-Krastanov growth of epitaxial thin films. On the other hand, when the surface energy of the film is greater than that of the substrate, the same wetting potential leads to dewetting of the film, characteristic of the Volmer-Weber growth mode.

By combining the nonlinear stress field and the nonlinear wetting potential, our numerical simulations show self-assembly of quantum dots. In the base model, both the film and the substrate are considered to be elastically isotropic. The system is thus fully isotropic when the mismatch stress is equi-biaxial in the plane of the surface. In this case, circular quantum dots (spherical cap in

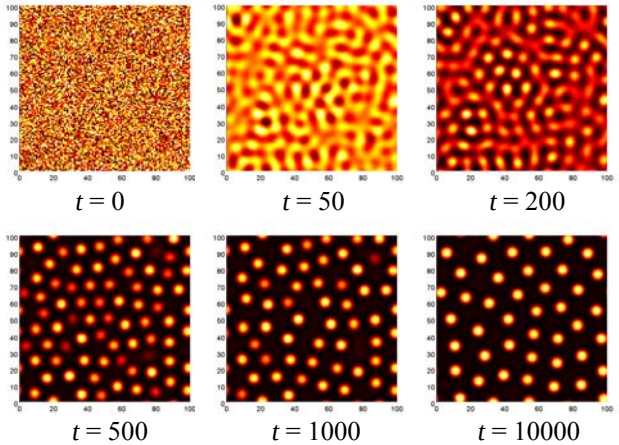

Fig. 8: Numerical simulation of self-assembled quantum dots for an isotropic system.

3D) with random spatial organization are obtained (Fig. 8), which reflects the rotational symmetry of the model system. The symmetry is broken when an anisotropy is introduced, which then leads to different shaped quantum dots (or other patterns).

Various types of anisotropy may be considered for fundamental understanding of their effects, individually and collectively, in the modeling and simulations. In a real material system, the interplay among various origins of anisotropy and ordering forces produces a rich variety of surface patterns. First, we considered the effect of anisotropic mismatch stresses. It is found that, in addition to the generic symmetry breaking, a bifurcation of surface patterns occurs in the range, $-(1-2\nu_s)^{-1} < c < -(1-2\nu_s)$, where $c = \sigma_2/\sigma_1$ is the ratio between the two principal mismatch stresses and ν_s is the Poisson's ratio of the substrate. Figure 9 shows the simulated long-term pattern evolution for $c = -1$.

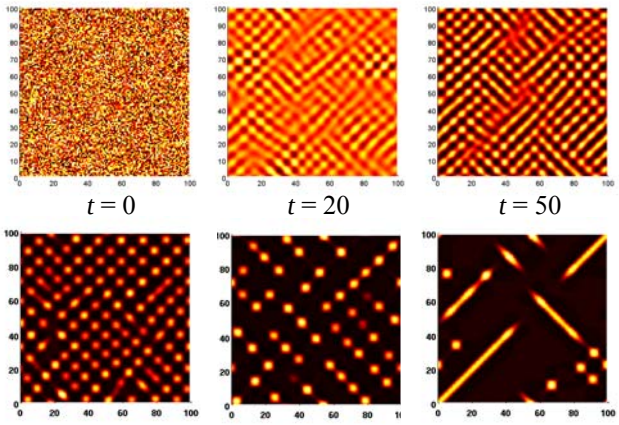

Fig. 9: Numerical simulation of surface pattern evolution under an anisotropic mismatch stress (c = -1).

Next, we consider elastically anisotropic films and substrates. The nonlinear stress field for a generally anisotropic epitaxial system is obtained by a Fourier method. To be specific, SiGe films on different Si surfaces are considered. Figure 10 shows the contours of initial growth rate on Si (001), Si (111), Si (110), and Si (113). The maximum growth rate occurs at different locations (magnitudes and orientations of dominant wave vectors), predicting different patterns at the initial growth. For long-term evolution, numerical simulations show different spatial ordering of self-assembled quantum dots and lines (Fig. 11). It is found that the underlying crystal structure of the substrate tends to improve the spatial ordering of the patterns. Variation of the Ge concentration in SiGe films leads to a change of the characteristic length scale and thus the feature size of the final pattern, ranging from over 100 nm to a few nanometers. Furthermore, a transition of the surface pattern from discrete islands to interconnected lines is revealed by the simulations for Si(001), Si(111), and Si(113) substrates when the mean film thickness increases. It is concluded that consideration of elastic anisotropy reveals a much richer dynamics of surface pattern evolution as opposed to isotropic models.

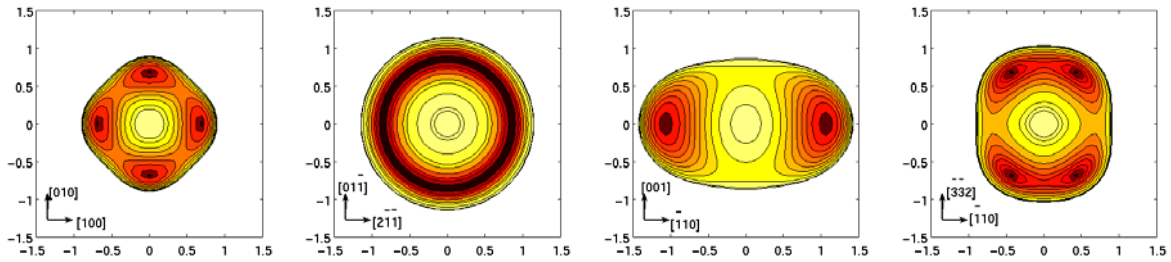

Fig. 10: Contour plots of the initial growth rate on various Si surfaces. From left to right: $\mathrm{Si}(001)$, $\mathrm{Si}(111)$, $\mathrm{Si}(110)$, and $\mathrm{Si}(113)$. Dark color indicates high growth rate.

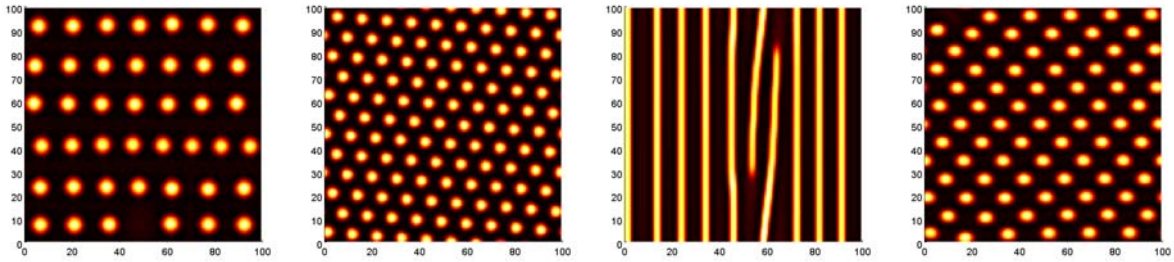

Fig. 11: Self-assembled surface patterns after long-term evolution on various Si surfaces. From left to right: $\mathrm{Si}(001)$, $\mathrm{Si}(111)$, $\mathrm{Si}(110)$, and $\mathrm{Si}(113)$.

4. List of Journal Publications

- H. Liu and R. Huang, Effect of a cap layer on morphological stability of a strained epitaxial film. J. Applied Physics 97, 113537 (2005).
- Y.R. Liu, S. Tang, S.K. Banerjee, Tunnel oxide thickness dependence of activation energy for retention time in SiGe quantum dot flash memory. Appl. Phys. Lett. 88, 213504 (2006).
- Y.R. Liu, S. Dey, S. Tang, D.Q. Kelly, J. Sarkar, S.K. Banerjee, Improved performance of SiGe nanocrystal memory with VARIOT tunnel barrier. IEEE TRANSACTIONS ON ELECTRON DEVICES 53, 2598-2602 (2006).
- S. K. Stanley, S. V. Joshi, S. K. Banerjee, and J. G. Ekerdt, Ge interactions on HfO_2 surfaces and kinetically-driven patterning of Ge nanocrystals on HfO_2. Journal of Vacuum Science and Technology A 24, 78-83 (2006).
- S. K. Stanley, S. Joshi, S. K. Banerjee, and J. G. Ekerdt, Surface reactions and kinetically-driven patterning scheme for selective deposition of Si and Ge nanoparticle arrays on HfO_2. Surface Science Letters 600, L54-L57 (2006).
- Y. Pang and R. Huang, Nonlinear effect of stress and wetting on surface evolution in epitaxial thin films. Physical Review B 74, 075413 (2006).
- Y. Pang and R. Huang, Bifurcation of surface pattern in epitaxial thin films under anisotropic stresses. J. Applied Physics 101, 023519 (2007).
- S. Tang, C.B. Mao, Y.R. Liu, D.Q. Kelly, S.K. Banerjee, Protein-mediated nanocrystal assembly for flash memory fabrication. IEEE TRANSACTIONS ON ELECTRON DEVICES 54, 433-438 (2007).
- J. Sarkar, S. Dey, D. Shahrjerdi, S.K. Banerjee, Vertical Flash memory cell with nanocrystal floating gate for ultradense integration and good retention. IEEE ELECTRON DEVICE LETTERS 28, 449-451 (2007).
- J. Sarkar, S. Tang, D. Shahrjerdi, S.K. Banerjee, Vertical flash memory with protein-mediated assembly of nanocrystal floating gate. APPLIED PHYSICS LETTERS 90, 103512 (2007).
- Y. Pang and R. Huang, Effect of elastic anisotropy on surface pattern evolution of epitaxial thin films. Int. J. Solids and Structures 46, 2822-2833 (2009).

5. List of Conference and Invited Seminar Presentations

- R. Huang, Dynamics of Surface Pattern Evolution in Thin Films. Max-Planck Institute for Metals Research, Stuttgart, Germany, Aug. 18, 2005 (invited).
- R. Huang, S. H. Im, and Y. Pang, UNDERSTANDING SURFACE INSTAILITY PATTERNS IN NANOSCALE THIN FILMS. Proceedings of the ASME NANO2005 Conference on Integrated Nanosystems: Design, Synthesis & Applications, Paper No. NANO2005-87046, Berkeley, CA, September 15-16, 2005.
- S. Tang, C. Mao, S. Banerjee, Nanocrystal flash memory made with protein mediated assembly. IEDM 2005, Washington D.C.
- R. Huang, Self-Assembly of Quantum Dots and the Effect of Non-uniform Strain Fields. 2005 ASME International Mechanical Engineering Congress, Orlando, FL, Nov. 11, 2005.
- D. Shahrjerdi, J. Sarkar, X. Gao, D. Q. Kelly, S. K. Banerjee**,** Fabrication of Self-Assembled Ni Nanocrystal Flash Memories Using a Polymeric Template. IEEE Device Research Conference 2006.
- J.Sarkar, S.Dey, Y.Liu, D.Shahrjerdi, D.Kelly and S.Banerjee, Vertical (3D) Flash Memory with SiGe nanocrystal Floating Gate. IEEE Device Research Conference 2006.
- Yueran Liu, Shan Tang, Chuanbin Mao and Sanjay Banerjee, SiC Nanocrystal Flash Memory Fabricated with Protein-mediated Assembly. IEEE Device Research Conference 2006.
- Y. Pang and R. Huang, Pattern Evolution of Self-Assembled Quantum Dots Under Biaxial Stresses. In: *Nanomanufacturing*, edited by F. Stellacci, J.W. Perry, G.S. Herman, and R.N. Das (Mater. Res. Soc. Symp. Proc., vol. 921E, Warrendale, PA, 2006), 0921-T07-08.
- S. S. Coffee, W. A. Winkenwerder, S. K. Stanley, S. Davood, S. K. Banerjee, and J. G. Ekerdt, Using Self-assembly and Selective Chemical Vapor Deposition for Precise Positioning of Individual Germanium Nanoparticles on Hafnia. Materials Research Society Symposium Proceedings, 921, Paper 0921-T07-09 (2006).
- D. Shahrjerdi, J. Sarkar, S. K. Banerjee, Fabrication of Dense Ordered Arrays of Metal Dots for Flash Memory Application. Materials Research Society, 2006.
- S. K. Banerjee, Materials, devices, and heterogeneous integration for new functions. GOMAC, Orlando, FL, Jan. 2007 (invited).
- S. K. Banerjee, New Materials and Structures for Transistors based on Spin, Charge and Wavefunction Phase Control, NIST, Gaithersburg, MD, March, 2007 (invited).
- S. K. Banerjee, Beyond CMOS, Brussels, April 2007 (invited).
- S. K. Banerjee, Retrospect and Prospects of Nanocrystal Floating Gate Memories, MARCO MSD e-workshop, July 2007.
- S. K. Banerjee, S. Tang, J. Sarkar, D. Shahrjerdi, C. Lee, Flash Memory with Nanoparticle Floating Gate. Toronto, Particles Aug. 2007 (invited).

- S. Tang, C. H. Lee, X. Gao and S. K. Banerjee, Flash Memory Fabricated with Protein-Mediated PbSe Nanocrystal Assembly as Floating Gate. IEEE Device Research Conference (DRC) 2007, p93-94.
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