D0 ENGINEERING NOTE

No. 3823.112-EN-447

D0 SILICON UPGRADE

THERMAL ANALYSIS OF THE D0 3 CHIP SINGLE
SIDED LADDER

June 18, 1996

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Introduction

The design of the D0 single sided 3 chip ladder is shown in figures 1-3. The SVX II chips are mounted directly opposite the cooling channel so that they are most efficiently cooled. Outboard of the cooling channel on the ladder top side is mounted a flex hybrid of copper/kapton, which is adhered to a beryllium substrate using a two part epoxy. The beryllium substrate, aside from providing a solid mounting structure for the flex circuit, provides a thermal conduction path between the components on the hybrid which dissipate heat and the cooling channel. The thickness of the top and bottom beryllium substrates is selected based on the [expected] channel temperature, the power dissipation of the SVX II chips, the power dissipation of the hybrid passive components, and the maximum acceptable silicon temperature within the ladder.

The thermal conductivity of the various materials within the ladder must be known to a fair degree of confidence in order to accurately simulate the ladder steady state cooling performance. The thermal conductivity of a number of ladder epoxy candidates was measured using a device at Lab D at Fermilab [1]. Preliminary measurements at Lab D, using a similar setup, have been performed in order to measure the thermal conductivity of beryllium, silicon, aluminum, and other ladder materials [2].

In order to simulate the cooling performance with confidence, prototype ladders were constructed using aluminum substrates (in place of beryllium), blank silicon, and non-functional prototype flex hybrid circuits. SVX II heat loads were simulated using 350 ohm strain gages which were adhered to the flex hybrid using a thin layer of epoxy. Temperatures were measured on the prototype ladders using a hand-held IR temperature probe, which has a laser focusing beam enabling simple optical focal length determination. The IR probe allows a correction to account for the surface emissivity of the material being measured.

Preliminary measurements [2] at Lab D indicate that the alloy used to construct the ladder models has a conductivity of 237 W/m-K. The assumed conductivity of the blank silicon is 149 W/m-K. Ladder prototypes with aluminum substrates were constructed using the prototype 3 chip assembly fixture at Lab D.

A two dimensional cooling simulation program was written using a simultaneous equation solver [3]. The simulation is written by dividing the 2D model into small dx and dy elements and performing an energy balance on each element based on the thermal resistance between the individual elements and their neighbors. It is otherwise known as the finite difference method. The steady state solution is obtained by solving the array of energy balance equations as a DC circuit. Convective boundaries can be added on exposed elements using appropriate equations. Following is a schematic which shows the energy balance terms in each element.

3

ALFRINT

3 chip ladder

Figure 4 Element Within the Two-Dimensional Mesh

This method of solution was tested against an ANSYS [4] solution of a similar problem submitted to Z. Tang [5] based on the CDF ladder design. Without going into details of the CDF ladder design, one can see that the two solution methods predict nearly identical temperature profiles of the silicon within the ladder. These results were presented in ref. [6]. Shown in Figure 5 is the silicon temperature from the ladder end at 0 mm to the ladder half point near 160 mm [7].

Figure 5 Silicon Temperature Profile in the CDF Ladder Design of January, 1995

Flex Hybrid Ladder Measurements

A number of prototype ladders were constructed in order to measure the silicon temperatures under a variety of designs and conditions. The first was built using a Silicon Valley Printed Circuit (SVPC) flex hybrid. Strain gages were adhered to the hybrid in the region of the SVX II chips and the transceiver region. The SVX II chip power and the transceiver power (of the final design) during ladder operation were unknown at the time of the measurements. For this reason the powers were varied over a wide range in order to (1) see the sensitivity of the temperature profile to the powers dissipated and (2) compare the temperature profile to the simulation output and gain additional confidence in the simulation technique.

Temperature measurements were taken on the silicon at the ladder end (~0-4 mm) and in-board of the cooling channel (~43-46 mm) using the IR probe. Additional measurements were taken on the transceiver strain gage surface, the SVX II strain gage surfaces, and the beryllium piece (on the underside) in-board of the cooling channel. Channel temperatures before and after the ladder were taken. The average of these two measurements (they usually did not vary by more than 1°C from one another) was used as the assumed cooling channel surface temperature for simulation purposes. Only silicon temperatures will be shown (and only a limited selection of the measurements) in order to demonstrate the results. Further results are available if requested.

For the first series of measurements on the SVPC prototype the coolant temperature had a set point of 10°C. The measured average channel temperatures were all normalized to 11°C so that simulation was simpler and results plots can be overlaid, which accounts for the minor fluctuations in the channel temperature for the various measurements. Silicon temperatures calculated inboard of the beryllium mount substrates are not shown since they are more dependent on convective conditions and do not yield useful information regarding the silicon temperature in this region during detector operation.

Later, measurements will be shown with the same ladder, using a chiller set point of 5°C, where the measured temperatures have been normalized to a 7°C channel temperature and plotted.

**Figure 6 Silicon Measurement vs. Simulation,
0 W Transceivers and 0.3 W SVX II Chips**

**Figure 7 Silicon Measurement vs. Simulation,
0 W Transceivers and 0.53 W SVX II Chips**

Figure 8 Silicon Measurement vs. Simulation,
0 W Transceivers and 0.83 W SVX II Chips

For the cases shown in Figures 6-8 the measurement points have clearly increased in temperature well in line with the simulation results. Temperatures at the ladder end (toward 0 mm) increase despite there being no power in this region, which is due to the convection assumptions on the hybrid and on the silicon, and due to the assumed air temperature in the room.

Next will be considered the temperature profiles with a fixed 0.41 W SVX II chip load and power on the transceiver.

Figure 9 Silicon Measurement vs. Simulation,
0.3 W Transceivers and 0.41 W SVX II Chips

Figure 10 Silicon Measurement vs. Simulation,
0.83 W Transceivers and 0.41 W SVX II Chips

Comparable agreement between the simulation and measurement numbers is seen for the 7°C cooling channel condition. These temperatures were obtained using the same ladder with a 5°C set point on the chiller.

Figure 11 Silicon Measurement vs. Simulation,
0.3 W Transceivers and 0.41 W SVX II Chips

Figure 12 Silicon Measurement vs. Simulation,
0.83 W Transceivers and 0.41 W SVX II Chips

Comparable measurements were performed on a prototype ladder using a LPC flex hybrid. Results were similar to those shown in Figures 6-12 so will not be shown here.

However, silicon temperatures which occur for the two hybrid types (LPC vs SVPC) are not the only consideration. The SVPC hybrids were considerably thicker than the LPC hybrids. This added thickness does not contribute considerably to an increase in the silicon temperature in the conduction region of the ladder. It does contribute, though, to an increase in the operating temperatures of any power dissipating components which are mounted on the hybrid. This higher operating temperature will result in a warmer gas temperature near the ladder end and would lead to higher silicon temperatures in this region. For this reason it is best to minimize the kapton thickness on the flex hybrids, if possible.

CVD Diamond Ladder Measurements

CVD Diamond has been considered as a substrate in the D0 ladder as a replacement for beryllium. Its expansion coefficient is much closer to that of silicon (2.6 ppm/°C for silicon, 1-2.5 for CVD Diamond, and 11-13 for beryllium) and the thermal conductivity of CVD diamond is much higher than beryllium (~1200 W/m-K for CVD Diamond vs. 190 W/m-K for beryllium). Cost per carat of CVD diamond currently precludes its use. The D0 collaboration purchased 9 CVD diamond pieces which were laser cut to dimensions which fit the 3 chip single sided ladder.

Three ladder types were constructed using CVD diamond in order to better understand thermal and mechanical issues. All three ladders had a LPC prototype flex hybrid glued to the surface and the SVX II and transceiver regions were instrumented as before using strain gages. Similar temperature measurements were performed on these three ladders as shown above. The three CVD Diamond ladder types are described below:

1. A CVD Diamond upper substrate was glued to an aluminum upper substrate using two part epoxy. The LPC hybrid was glued to this two piece substrate and a ladder was constructed using aluminum as the underside substrate piece. This will be called CVD Ladder type 1.
2. An aluminum upper substrate with LPC hybrid was used on the upper part of the ladder. The underside substrate was constructed of CVD Diamond glued to aluminum using a two part epoxy. The ladder was constructed using these pieces and will be referred to as CVD Ladder type 2.
3. A ladder was constructed using only CVD Diamond substrates on both top and bottom. No aluminum substrates were used. As with the others, the upper substrate was mounted with a LPC hybrid instrumented with strain gage heaters.

As before, many measurements were performed on these ladders but only a select few will be shown in this summary. In addition, no simulation work was done in support of the CVD diamond for this summary. Numbers shown are primarily in order to get a good comparison in the maximum temperature obtained on the ladder end, for identical conditions as reported above, using the 3 combinations of CVD diamond in the ladder.

Figure 13 CVD Ladder Types 1-3
Measurement Temperatures for 0.3 W Transceivers/0.41 W SVX II Chips

Figure 14 CVD Ladder Types 1-3
Measurement Temperatures for 0.83 W Transceivers/0.41 W SVX II Chips

CVD Ladder type 2 was the worst of the three ladder types constructed, regarding thermal performance. This is due to the added epoxy layer on the underside cooling substrate, and the associated temperature drop across this additional epoxy. CVD Ladder

type 1 is somewhat improved. What thermal performance that is lost by adding an additional layer of epoxy on the upper substrate is more than made up by the added thermal conductivity of the CVD diamond.

Lastly, CVD Ladder type 3, that of only CVD diamond on the top and bottom substrates, was considerably better thermally the other two CVD ladder types constructed.

Figure 15 CVD Ladder Types 1-3
Measurement Temperatures for 0.3 W Transceivers/0.41 W SVX II Chips

Figure 16 CVD Ladder Types 1-3
Measurement Temperatures for 0.83 W Transceivers/0.41 W SVX II Chips

Simulation of Flex Hybrids with Beryllium Substrates

Confidence in the simulation technique has been demonstrated by the agreement between the ANSYS results and the finite difference results. Confidence has also been gained when comparing the measured temperatures on the flex ladder and the accompanying results using the finite difference technique.

The benefits gained by using CVD diamond in the ladder design have been shown. Issues still open regarding the use of CVD diamond are beyond the scope of this engineering note. However, they can be summarized by stating that the cost, and perhaps the mass increase due to the diamond (in radiation lengths) must be considered against the benefits gained by the improved cooling performance.

The finite difference technique is now applied to the final ladder design by assuming a flex hybrid adhered to a beryllium substrate using a two part epoxy. The assumed thermal conductivity of beryllium is 190 W/m-K and, as stated before, work is on-going to better understand the thermal conductivity of beryllium and other substrate materials. The expected SVX II power dissipation is 0.300-0.500 W per chip, 0.500 W is used for the following simulations. The transceiver power dissipation estimates range between 0 W and 1.5, which is total power dissipation of the hybrids per ladder. A number of simulations have been performed in order to ascertain the optimum substrate thickness for the 3 chip ladder design.

The first prototype hybrids were designed with a transceiver located near the ladder end. Regarding the thermal modeling, this transceiver is nearly a point load heat source, hence the strain gage at this location for the thermal measurements. More recent understanding of the hybrid and final SVX II chip design indicate that the transceiver may be removed

from the hybrid, which would result in the point source being removed from thermal considerations. However, termination resistors on the hybrid surface will result in a higher power dissipation with the removal of the transceiver. Early estimates from the D0 hybrid design group [8] put the hybrid component power dissipation as high as, perhaps, 1.5 W. For the purposes of this analysis the hybrid power has been assumed to be uniformly distributed over the hybrid surface.

It has been suggested [9] that 0.75-1.5 W be used as the assumed range of power dissipation for the total hybrid surface mount components. The hybrid substrate thickness is 0.300 mm for both top and bottom. The assumed SVX II power is 0.500 W. The assumed thermal conductivity of beryllium is 190 W/m-K. The channel temperature immediately opposite the glue joint, where the ladder mounts to the cooling channel, is 0°C and is maintained by providing a bulk fluid cold enough to achieve this.

Figure 17 3 Chip Ladder Cooling
0.5 W SVX II Power/0.75 W Hybrid Component Power

Shown in Figure 17 is the temperature profile of the silicon within the 3 chip ladder during operation. Outboard of the cooling channel it has been suggested to adhere the hybrid to the ladder in selected regions of the ladder. This would reduce the effect of thermally induced bow within the silicon as the ladder is cooled below its construction temperature. The effect of a glue joint in this region versus an air gap is shown.

Figure 18 3 Chip Ladder Cooling
0.5 W SVX II Power/1.5 W Hybrid Component Power

In Figure 18 is shown the effect of hybrid component power dissipation at 1.5 W. Based on the above stated assumptions the ladder maximum temperature will be within the range of 10-16°C, which occurs at the ladder end.

Figure 19 3 Chip Ladder Cooling
0.5 W SVX II Power/0.0 W Hybrid Component Power

Lastly, Figure 19 shows the motivation for removing power entirely from the hybrid. With the power gone from the hybrid the ladder will experience only convective warming on the end (outboard of the cooling channel). The silicon temperature remains nearly uniform over the entire ladder length and rises at the ladder end due to the warmer gas temperature and the natural convection that will occur on the ladder in this region.

[1] Gillespie, G., Jostlein, H., and Ratzmann, P., Thermal Conductivity Measurements of a Variety of Epoxies and Greases used for CDF/D0 Silicon Ladder Construction, January 23, 1996, Revision 1.

[2] The work is on-going through the summer of '96, being conducted by P. Ratzmann and T. Scott.

[3] EES, Engineering Equation Solver, F-Chart Software, written by S. A. Klein and F. L. Alvarado.

[4] ANSYS Finite Element Analysis software by ANSYS, Inc., Houston, Pa.

[5] Of the Analysis Group under Bob Wands at Fermilab.

[6] Ratzmann, P., Thermal Analysis of the CDF SVX II Silicon Vertex Detector submitted to Nuclear Instruments and Methods A, March, 1996, and Fermilab pre-print FERMILAB-Pub-96/031-E CDF.

[7] The CDF ladder design used for this solution is dated and has changed since it was submitted in January of 1995.

[8] A summary sheet provided by Mike Matulik of D0 dated 8 March, 1996.

[9] From a conversation with Bill Cooper.