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Enhancing the CDF's B physics program with a faster data acquisition system

Petar Maksimović
Department of Physics and Astronomy
The Johns Hopkins University
3400 N. Charles St.
Baltimore, MD 21218

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1 Introduction

The physics program of Run II at the Tevatron includes precision electroweak measurements such as the determination of the top quark and W boson masses; bottom and charm physics including the determination of the B_s and D^0 mixing parameters; studies of the strong interaction; and searches for the Higgs particle, supersymmetric particles, hidden space-time dimensions and quark substructure. All of these measurements benefit from a high-resolution tracking detector. Most of them rely heavily on the efficient identification of heavy flavored B hadrons by detection of displaced secondary vertices, and are enhanced by the capability to trigger on tracks not coming from the primary vertex. This is uniquely provided by CDF's finely-segmented silicon detectors surrounding the interaction region. Thus CDF experiment's physics potential critically depends on the performance of its silicon detectors.

The CDF silicon detectors were designed to operate up to $2\text{-}3\text{ fb}^{-1}$ of accumulated $p\bar{p}$ collisions, with an upgrade planned thereafter. However, the upgrade project was cancelled in 2003 and Run II has been extended through 2011, with an expected total delivered integrated luminosity of 12 fb^{-1} or more. Several preventive measures were taken to keep the original detector operational and maintain its performance. The most important of these are the decrease in the operating temperature of the detector, which reduces the impact of radiation exposure, and measures to minimize damage due to integrated radiation dose, thermal cycles, and wire bond resonance conditions. Despite these measures the detectors' operating conditions continue to change with issues arising from radiation damage to the sensors, aging infrastructure and electronics. These, together with the basic challenges posed by the inaccessibility of the detector volume and large number (about 750 thousand) of readout channels, make the silicon detector operations the single most complex and high priority job in the CDF experiment.

Behari has been the silicon group sub-project leader (SPL) between 2008-2009 and continues to act as the backup SPL for the group, in addition to taking responsibilities in silicon power supplies, DAQ operations and maintaining the monitoring tools infrastructure. During the 2010 shutdown he was part of a crew which carried out repair / replacement of malfunctioning power supplies as well as the DOIM receiver modules which collect optical signal from the detector before they are converted to electrical signals and transmitted downstream in the DAQ system. Due to his expertise with the whole system he is frequently consulted for help on unusual problems and occasionally assigned the on-call pager.

2 Silicon Power Supply Maintenance

The CDF silicon detector uses custom-built power supply modules manufactured by the CAEN Inc., Italy. A total of 111 modules are housed in 16 SY527 crates located in the 4 corners of the CDF collision hall. The crates are elevated 8-25 feet off the floor due to space constraints. These locations have some distinct disadvantages. The supplies and crates are continuously exposed to radiation,

which not only shortens the life of their electronic components, but also results in single event upsets (SEUs) that require crate resets and single event burnouts that necessitate additional hardware protection for the detector. Investigation and/or replacement of a problematic power supply requires beam downtime with access to a radiation controlled area for 1-2 hours, and the use of ladders or man-lifts, once inside.

Behari has acted as the PS expert for the group since late-2006 and has spear-headed many projects (as part of this proposal) which have dramatically improved the operation and maintenance of the supplies. Specifically, he built a replica of the VME-based PS teststand at the Fermilab ESE department, where the modules are repaired. This speeded up the test procedure immensely, in addition to letting the CDF expert work closely with the repairing technician.

For power supply testing a multi-channel loadbox is used to mimic real detector load. Behari pushed for a new loadbox design along with other experts which reduces the test procedure for a repaired module from 2 hrs to 15 mins. Since this task is performed in the collision hall, requiring beam downtime, this improvement is regarded as a tremendous success for CDF operations. This device, developed by the Fermilab ESE department, incorporates both L00 and SVX/ISL type loads, which are different, and switches between them via electronic relays. It utilizes an ADC to automatically measure the voltages on each channel, which are displayed via a bright LCD screen and lets the test data be saved by push of a button for future retrieval. This makes measuring the voltages fast, safe and easy. To carry out these tasks, the loadbox has a small microprocessor, internal memory, a USB port (for connection to a laptop), RS-232 port (for connection to the CAEN mainframe), an internal battery and clock, and several safety features.

In 2006 some power supplies started developing gradual decline in the low voltages they provide to the detector readout electronics. This was traced to specific filter capacitors in the supplies degrading over time due to electrical ageing. The drop rate of the affected voltage is such that if left unattended the powered electronics stops working within a period of about 3 months. The solution is to replace all of the filter capacitors on the supply by a Fermilab technician. Although the repair takes a day but the procedure of extraction of the supply from the collision hall and post-repair check procedures add up to 3 days. A major complication, in addition, is that during normal detector operations up to 5 supplies can be replaced depending on available pool of spares. During 2007 Tevatron shutdown Behari led a massive effort to replace capacitors on 52 supplies. Eversince he is helping coordinate such operations during yearly shutdowns. Figure ?? shows the Avdd voltage for the ladder SB2W8L3 recovering after the replacement of the aged capacitors on the power supply.

Due to radiation ageing sensors progressively become under-depleted. Their bias voltages are increased to restore full depletion for optimal charge collection. This occasionally leads to coupling capacitor shorts on individual strips on the sensors, known as pinholes. The bias current of the ladders with pinholes eventually hit the power supply limit, rendering them inoperable. To fix this one needs to adjust the voltage divider resistances on the power supply. This process is complicated due to the following reasons:

Figure 1: Avdd voltage for the ladder SB2W8L3 recovers after the replacement of the aged capacitors.

- Due to complicated electrical noise behavior of the ladder as a whole, the strip suffering a pinhole is mostly not identifiable.
- The procedure to identify the bias splitting needs to be done on the detector ladder in question, and hence in the collision hall using access time.
- Intrusive modification is needed on the supply for the procedure which requires pulling out the supply for modification before the procedure.
- Bias splitting works differently for the symmetrically (Hamamatsu) and asymmetrically (Micron) biased ladders.

Prior to the 2010 yearly Tevatron shutdown Behari devised a plan to perform bias splitting on 3 leading pinhole candidates. His plan was implemented in modifying a test supply with a pair of potentiometers to measure bias currents in the collision hall quickly at various bias splitting settings. This test device was tried out successfully on the teststand before the shutdown. As customary, a detailed procedure for the task was written and was approved by the CDF operations head. After the procedure bias currents of all the 3 supplies returned to their operable limits. Figure ?? shows the bias current for the ladder SB0W6L4 recovering after the bias splitting procedure. The bias current profile was measured on the 3 candidates. To be conservative, the splitting ratios were changed from their original configuration of 100:0 to 90:10, not to expose the ladders to large changes in biasing. Before treating future pinhole candidates, as a precautionary measure, any change in S/N ratio and hit efficiency due to this procedure would be evaluated on the 3 pilot candidates.

Figure 2: Bias current for the ladder SB0W6L4 showing recovery after the bias splitting procedure.

3 Silicon DAQ Enhancements

A major goal of this OJI grant was to explore possible ways to improve CDF silicon DAQ speed and thereby gaining extra bandwidth for CDF's B physics program which depends critically on the Secondary Vertex Trigger (SVT) operating in Level-2 of the CDF trigger system.

The Silicon Readout Controller (SRC) board is at the heart of the silicon DAQ system. Maksimović was one of the key designers and implementors of its firmware. The SRC receives clocks and Tevatron bunch crossing information from the CDF clock system and trigger decisions from the trigger supervisor, processes them and fans them out to the remainder of the silicon DAQ system, namely the Fiber Interface Boards (FIBs) which transmit them to the SVX3d chips, and VME Readout Boards (VRBs) which receive event data from the FIBs. A copy of the data from the FIBs is sent to the SVT system. A synchronous readout scheme is employed in the silicon DAQ system which makes the processing time of an event dependent on the slowest ladder in the system.

Prior to 2007, several options were considered to speed up the silicon DAQ. Initially all silicon subdetectors, L00, SVXII and ISL, were operated using a single SRC. Since L00 is read out in READ-ALL mode, it dominated the Level2 trigger decision and caused significant deadtime, in addition to exposing the detectors to wirebond resonance conditions (described below). In 2004 the silicon DAQ was split between two SRCs, one operating SVXII in the normal mode (takes part in Level2 decision) and the other operating ISL and L00 in the tracer mode, acting only after a Level2 accepts. Another way of speeding up the DAQ is shortening the digitization time by employing a 7-bit as opposed to the 8-bit digitization. An offline study using real data events finds no peceivable effect of 7-bit digiti-

zation on the silicon hit resolution. However its hardware implementation is not considered yet.

To keep up with increased luminosity in the Run IIB phase, CDF DAQ was upgraded to be able to handle Level1 accept rate of 100 kHz. This was expected to cause bottle-neck for the silicon DAQ which operates below 55 kHz. We explored the possibility to improve the SRC firmware logic to run silicon DAQ at a faster rate. The length of the silicon readout is one of the bottlenecks of the “Level1 Accept Loop”, since the silicon data from the SVXII detector is needed by the SVT in order to form a Level2 decision. The length of the silicon detector’s readout cycle can be shortened by an *asynchronous readout* (via the *pre-send Digitize* commands), where the “Digitize” command for the next event can be sent from the SRC without waiting for the completion of the current event’s readout. This feature requires a duplication of the readout state machine, as well as substantial changes in the bookkeeping for the coordination between the two. In addition, several other firmware improvements involving gaining back 1-2 132 ns clocks in Level1 decision cycle, speeding up a certain logic which determines whether chips need to be refreshed by sending the PRD2 signal, were planned.

As a first step to the firmware R&D a test PC was created with all the necessary software. The SRC boards are populated with Xilinx XC4000E family FPGAs, each of which have about 180,000 usable gates with improved routing capabilities. WorkView Office 7.53 software suite by ViewLogic Corp. is used for compiling the SRC firmware. The Xilinx Foundation Series 2.1i software is used for design, timing analysis, synthesis and PROM bitstream production. Both these program suites are very old and are supported on old Windows operating systems, the latest of which is Windows98. When a new test version is synthesized and is ready for testing, the code is written onto an Amtel AT17LV512 PROM using a PROM Writer, EMP-21, by Needhams Electronics Inc. This PROM is then plugged into the SRC board on a DAQ teststand.

The CDF silicon group maintains two network capable VME-based teststands for test/development of the component boards. Each of these comprises of a full silicon DAQ chain for a realistic test environment. The one in the B0 detector building has access to Tevatron clock and bunch crossing information for fully realistic tests (including parasitic running with the real system) while the one at the Feynmann Computing Center building uses SRC on-board trigger emulator to do the job. As a sanity check, benign logic elements modifications were introduced into the SRC firmware, the PROM reprogrammed on the test PC was plugged into the B0 teststand SRC and operated successfully. The added elements were visualized using a logic analyzer. Despite much progress in this respect, the CDF management and the silicon group experts didn’t consider the SRC firmware upgrade as necessary, compared to the amount of effort needed to debug and commission the new system. So this project was deferred until a need arises in future.

In 2008, Behari used the test system to rejuvenate all the 5 spare SRCs. Some of them had older or non-standard firmwares or had non-standard jumper settings. The silicon DAQ software *svxdaq* was run in the “High Speed Test” mode to diagnose the problems. After this work the SRC online DB was updated for future ease of operations. Behari is currently the only onsite SRC expert and has experience

on the complicated and lengthy SRC checkout procedure.

During installation and commissioning phase of the CDF silicon detectors, an unintended feature of SVX3d chips was uncovered. If an SVX3d chip does not receive any periodic commands from the DAQ, it transitions into an undefined state in which digital end of the chip draws significantly larger amount of current than during normal operation. This eventually causes a trip of the affected ladder. A solution was implemented into the SRC firmware which sends periodic “keep-alive” commands every $270\ \mu\text{s}$ in the absence of any other command. This proved to be an effective and robust mode of operation for the SVX3d chips. However, occasionally majority of the chips in the SVXII system go into undefined state, causing a trip of almost the whole subdetector. In 2009 winter there were growing number of these incidents and Behari and his co-SPL investigated its cause using the above test DAQ system and a pair of logic analyzers. One of the logic analyzers was attached to the SVXII SRC spare output (parasitically) to trigger on any unexpected command or lack of “keep-alive” commands from the SRC, while the other one was setup to look for unexpected commands on the FIB J3 backplane and trigger the first logic analyzer. Unfortunately, these events subsided before a clear diagnosis and the setup was retained for future investigation.

Resonance conditions occur in SVXII when readout commands are executed at a fixed rate and higher than a threshold of $15\ \text{kHz}$. This sets the wirebonds, which connect r-phi with r-z side of the sensors, in motion. If not stopped they cause breakage of the wirebonds, making the z-side of the sensor unusable. This can be caused by certain noisy Level1 trigger element which drives the Level1 accept rate unreasonably high. A hardware solution (ghostbuster board) was implemented to monitor and stop data taking when a resonance condition is reached. The ghostbuster board was designed for SVT to suppress duplicates from the extremely Fast Tracker (XFT) board of Level1 and has been modified for use with the silicon system. It is fed by the SRCTM mezzanine card. SRCTM mezzanine card picks up readout acknowledgement signals from FIB fanout boards and passes them on to the ghostbuster board. The latter then counts the time between two consecutive readout commands. If they become synchronous a counter is started and if the counts (ticks) exceed a threshold a brake signal is fired (causing an SRCERR) to stop data taking. Currently the SVX and ISL systems are operated with a 13 ticks threshold. Resonance conditions occur also when noisy or misconfigured SVXII ladders give rise to large event size, causing the occupancy of all available Level2 buffers waiting for decision. This situation leads to subsequent continuous Level2 rejections. Behari has developed automated web-based tools for monitoring both types of resonant conditions. Figure ?? shows number of resonant events per week for the cases arising due to high (a) Level1 accepts and (b) Level2 rejects. The former is typically isolated by looking for noisy Level1 elements and fixing or suppressing them. The latter, on the other hand, is mostly due to chip errors which are dealt with case-by-case.

The CDF Run Control state machine spends 10 secs to recover from a halt, induced by a problem in a subsystem. The time taken is mainly due to commands / acknowledgement handshakes transmitted via smartsocket messages. There is a feature of the Run Control GUI which bypasses this messaging and resets the sub-

Figure 3: Realtime monitoring of the resonant conditions due to high Level1 accepts or Level2 rejects.

systems via dedicated lines, called *TurboHRR*. This reduces the recovery time to several milliseconds. From a study Behari found that the silicon subsystem is not the source of the Run Control turn-around time of 10 secs. Also, that silicon DAQ is capable of running in *TurboHRR* mode. However, due to lack of preparedness on other fronts, e.g. central outer tracker TDCs, this feature is not implemented yet. To be noted that *TurboHRR* causes the trigger supervisor to send RECOVER command to SRC via a dedicated line which in turn sends CHIP RESET to all the relevant chips. This is quite different from the CONFIG of the chips done by the FIBs over VME. Unfortunately it is not possible to know apriori how the SVX3d chips perform with just CHIP RESETs as opposed to CONGIFs, without commissioning the *TurboHRR* feature. Enabling of this capability is deferred to a future decision by the CDF operations management.

4 Calibration Taskforce Study

The offline silicon calibration framework analyzes data taken during dedicated calibration runs in which every silicon channel is read out. These data are processed to extract calibration constants (pedestals, noise, and target thresholds) for each channel on every chip. Keeping track of all of this information is a daunting task, which is accomplished through the use of scripts and lightweight servers which constantly check for new calibration jobs, new data runs, and new silicon configurations. Accuracy of the calibration data is crucial for pedestal subtraction from the raw data before they can be used for event reconstruction and subsequent physics analyses.

In 2008 a drop of silicon hit efficiency was observed in a significant portion of the data. It was traced to faulty calibration data. CDF spokespersons appointed a taskforce to resolve this issue. As a member of this small group of experts, Behari diagnosed the problem to be due to a malfunctioning SVX FIB crate, during the

affected calibration run, which misconfigured the chips controlled by it to sparse mode. During calibration runs all the chips must be read out in read-all mode. The drop in efficiency was recovered by reprocessing the affected data using a valid pair of calibration runs. Utilising his experience in maintaining the silicon online monitoring tool, SVXMon, Behari developed and optimized a parameter set to be used during calibration runs to catch similar problems in future. This setup is now part of the CDF operations procedure. Figure ?? shows the SVXMon status map

Figure 4: The SVXMon chip status map for calibration run 263032, where the affected chips controlled by the FIB02 crate appear red.

for the SVX chips in run 263032. The chips controlled by the malfunctioning FIB02 appear red.

5 Operations Tools Upgrade and Maintenance

Following a security compromise of one of the silicon computers in 2008, Behari migrated all the silicon operations softwares to the secured CDF online cluster and completely reorganized them for easier maintenance. He continues to maintain most of the operations software tools and helps out with data mining and analysis using them, as need arise.

He is one of the very few experts on the silicon online tool, *SVXMon*, which ensures silicon data quality in realtime as the data are being acquired, and issues reset requests to the CDF DAQ software.

He has also made several crucial upgrades of the power supply test software making it more automated and speeding up the tests. In addition, his *PSmap* web-based tool is regarded essential in most of the PS expert procedures and lets conveniently monitor the declining low voltages in power supplies.

6 Study of Radiation-induced Effects on Silicon DAQ

During commissioning of the silicon detectors an occasional issue encountered was the loss of analog power to one or more chips of a ladder. This is sometimes caused by abnormal beam aborts, thermal cycles or when the detector encounters resonant conditions. The main symptoms are; one or more chips become unresponsive, an observed decrease in the total analog chip current for a ladder, failed initialization, chips downstream from the affected chip missing from the data. This is the so called “AVDD2 failure”, named after the lost wirebond channel. Since the affected chips are not recoverable, steps were taken to protect the detector from sudden beam incidents, minimize thermal cycles and control resonant events using the ghostbuster board. Behari investigated the past failure events to identify operational parameters which caused them and to be able to predict future failures from the available data. The known cases were profiled according to year of occurrence and detector geometry. Due to employing safety measures described above, especially installation of the ghostbuster board in 2005, there is a drastic reduction of these cases, to just a few per year. In data on and before 2005, no conclusive trends were observed with respect to their location in the detector.

As described earlier, the Fiber Interface Boards (FIBs) transmit clocks and commands from SRC to the SVX3d chips and transmit the data from the chips to the VRBs. Each SRC command corresponds to a command sequence in the FIB. These command sequences are stored in an onboard EEPROM (Static RAM). On power ON they are loaded onto a Micro Sequencer RAM (MSRAM) and are accessed at runtime. Due to bad beam conditions the FIB crates, located in the CDF collision hall, may be sprayed with particles which cause SEUs in the MSRAM. At every CONFIG, FIB checks the consistency of the MSRAM. If it fails, FIB issues a warning message and rewrites MSRAM from the EEPROM. Occasionally the EEPROM content may also become corrupt due to SEU which leads to a series of MSRAM corruptions. Behari has an automated tool to monitor the FIB SEUs with respect to the crate location and instantaneous luminosity. Figure ?? shows the FIB SEU events in the 8 crates in 4 corners of the CDF collision hall. The growth of the rate of SEUs is consistent with the Tevatron integrated luminosity. In addition, the upper crates on the north side and the lower crates on the south side are significantly more affected by the rest. This is consistent with the radiation profile in the collision hall measured from an independent measurement.

Like the FIB crates, 16 CAEN power supply crates are located in 4 corners of the CDF collision hall, 2 each in the upper and lower racks. On getting hit by SEU events, CAEN crates lose communication with the silicon DAQ. The DAQ software issues crate reset, the so called “AutoHocker”, on a dedicated line when it is unable to establish connection for 3 consecutive DAQ cycles. Behari has developed a tool to monitor the AutoHocker rate in realtime, according to their crate location. Figure ?? shows the CAEN SEU (AutoHocker) events in the 4 corners of the CDF collision hall. The the north and the west sides are clearly more hit than the rest. The rate is consistent with the Tevatron integrated luminosity, same as the FIBs.

In addition to monitoring and dealing with the silicon detector hardware is-

Figure 5: Plots showing FIB SEU events distributed over upper and lower location in the 4 corners of the CDF collision hall.

sues, the silicon group has traditionally monitored low level reconstruction parameters such as, hit efficiency in track reconstruction, which directly affect physics analyses. This has enabled the silicon group to identify gross problems in silicon hardware or provide feedback to reconstruction groups on problems. Behari has been a lead developer and maintainer of the *SiHitAnalyzer* package which runs daily on 3 physics runs from the online area and produces hit efficiency for various detector segments, e.g. bulkheads, wedges, layers, chips etc. and produces historical plots. The efficiency is calculated by checking if a reconstructed track intersects a ladder (denominator) and if so, if there is an associated hit in the ladder (numerator). In 2009, about 11 ladders made by Micron Inc. (L2 and L4 of SVXII) were found to lose hit efficiency due to underdepletion. So were a few L00 ladders. Increasing their bias voltages to values estimated from bias scans, restored their efficiencies. Figure ?? shows recovery of the offline hit efficiency of the ladders SB2W2L2 and LB1W3L2 after increasing their bias voltages. In addition to helping out with monitoring hit efficiency, the *SiHitAnalyzer* data is used to study several things, including the number of strips hit per chip per event. This number's dependence on applied ADC threshold is used to mask noisy chips, e.g. those which are suspected to contribute to SVXII resonances.

Behari has coordinated writing a paper containing operational experiences

Figure 6: Plots showing CAEN SEU events distributed over the 4 corners of the CDF collision hall.

accumulated over the past 5 years of CDF silicon detectors running at their peak efficiency, and the performance results thereof. Most of the work presented in this report are elaborated in it. It is ready for collaboration internal review, before submission to the Nuclear Instrumentation Methods journal for publication.

Figure 7: Plots showing recovery of hit efficiency after increasing bias voltages of SVXII ladder SB2W2L2 and L00 ladder LB1W3L2.