SiC Power MOSFET with Improved Gate Dielectric

STTR Phase II Progress Report

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A: Overview and Summary:

A.1 Executive Summary

In this STTR program, Structured Materials Industries, Inc. www.structuredmaterials.com (SMI), and Cornell University www.cornell.edu are developing novel gate oxide technology, as a critical enabler for silicon carbide (SiC) devices. SiC is a wide bandgap semiconductor material, with many unique properties. SiC devices are ideally suited for high-power, high-voltage, high-frequency, high-temperature and radiation resistant applications. The DOE has expressed interest in developing SiC devices for use in extreme environments, in high energy physics applications and in power generation. The development of transistors based on the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) structure will be critical to these applications.

Presently, a key limiting factor for SiC MOSFET development is the material and the process technology for reliable gate oxide films. In this STTR program, SMI and Cornell are developing novel gate oxide technology for SiC devices, based on high dielectric constant (high-k) materials. In Phase I, we demonstrated technical feasibility of a composite gate dielectric stack, based on hafnium oxide (HfO₂) and silicon oxide (SiO₂). During this Phase II Project, the objectives were to;

1. Further optimizing the materials and the process technology for the high-k gate dielectric materials.
2. Develop the technology to implement the materials and processes in actual SiC device manufacturing.
3. Design optimized tools for gate dielectric film deposition in commercial SiC device production.

SMI and Cornell University have successfully completed all Phase II Objectives. We have developed and optimized processes for high-k gate dielectric films based on HfO₂/SiO₂ gate stacks. We demonstrated effective dielectric constants for our gate stacks which are close to the bulk dielectric constant for HfO₂. We developed the process integration technology and demonstrated SiC devices structures with excellent transistor parameters. We also developed the computer modeling tools for use in SiC device development. SMI has designed production ALD/CVD tools for SiC gate dielectric deposition, which have become part of SMI product line of advanced materials processing tools. Complete details of our technical progress are included in Section C of this Report.

SMI has also formed relationships with several other companies involved in SiC device development. This work is part of our effort to commercialize the technology resulting from this STTR project, since these companies represent potential customers. Since many of these companies are also located near central New Jersey, the potential exists for a concentrated technology base for SiC device development. Details of SMI's efforts toward commercialization and collaborative development are included in Section D of this Report.

A.2 Technical Background and Program Objectives

Silicon Carbide (SiC) is a very attractive semiconductor material for high temperature, high power, high frequency, high voltage and radiation hard applications. SiC has many unique properties which make it particularly attractive for a variety of semiconductor applications. The wide bandgap of SiC enables electro-optical devices that operate in the blue to ultraviolet range. The wide bandgap also enables transistor devices that can operate at high temperatures and handle high power. SiC's high carrier saturation velocity and high thermal conductivity make it particularly suited for RF and high power device applications. SiC is second only to gallium nitride, for its ability to handle high power and high frequencies. In many future applications, particularly those involving high-temperatures and high power levels, SiC is expected to challenge and replace gallium nitride.

To date, SiC MOSFET device technology has been hampered by several device limitations, such as a low electron mobility and an unstable threshold voltage, but predominantly because of poor gate oxide reliability. Great strides have been made in improving SiC MOSFET performance through enhanced processing, such as post-oxidation annealing and nitridation of the silicon dioxide gate dielectric.

However, recent reports have indicated that the use of an alternative gate dielectric such as aluminum oxide (Al_2O_3) or hafnium oxide (HfO_2) results in SiC MOSFET's with much higher electron mobilities, increased oxide reliability and a stable threshold voltage. The advantage of the high-k dielectrics are that thicker gate dielectric films can be utilized, while still maintaining the same effective capacitance. The thicker gate dielectric layer allows the SiC transistors to operate at higher voltage and higher power levels, without increasing gate leak current, increasing gate tunneling or increasing the risk of dielectric breakdown.

Figure 1: Schematic of a MOSFET. In this STTR program, the gate oxide (presently SiO_2) is being replaced by an alternative high-k gate dielectric.

In this STTR program, SMI and Cornell are developing gate oxide technology for SiC power devices, based on high-k dielectric materials. Our technical approach utilizes Metal Organic Chemical Vapor Deposition (MOCVD) for the high-k film deposition. The SiC MOSFET technology will directly benefit all future SiC electronic systems, including those specific to high energy physics applications, such as digital signal processors (DSPs), pulse processors and pulse-shape discriminators. The resulting SiC device technology will also fulfill needs in high-power, high-voltage, high-frequency and high-temperature applications, including power distribution, power generation, automotive, space exploration and military markets.

The team of SMI and Cornell University is ideally suited to develop and commercialize SiC MOSFET technology. SMI is a leading US based supplier of CVD equipment for advanced materials and devices. SMI has extensive experience in deposition of a wide range of materials, including compound semiconductors, oxides, nitrides, carbides, diamond and graphene. Our STTR partner, Dr. Michael Spencer at Cornell University, is a leading expert in SiC materials and devices. Dr. Spencer's work on SiC power transistors and SiC epitaxial

film growth has been responsible for several (patented) advancements in SiC device technology. SMI is also establishing relationships with several other companies involved in SiC device development, as will be detailed in Section D of this Report.

In Phase I, SMI and Cornell investigated high-k dielectric films, based HfO_2 . While we found we could produce films with high dielectric constants and low leakage currents (as measured by AC conductance), the films suffered from significant hysteresis in their capacitance/voltage (C-V) behavior, owing to traps at the non-native hafnium oxide/silicon interface. We demonstrated that a thin layer of SiO_2 native oxide, thermally grown on the SiC surface prior to HfO_2 deposition, preserved the quality of the SiC/ SiO_2 native oxide interface and significantly improved the C-V behavior. Since this thermal SiO_2 layer could be very thin (approximately 10 nm) there was minimal impact on the overall dielectric constant of the stack.

In Phase II, SMI and Cornell built on these results to develop production worthy technology for fabrication of SiC MOSFET devices. This included the process technology for the high-k dielectric film stack, the integration technology for the high-k gate stacks into SiC device fabrication, and the hardware designs for production tooling. Details of the Phase II results are included in Part C of this Final Report. Additional activities to initiate commercialization of the technology developed in this STTR are described in Part D of this Final Report.

B: Phase II Objectives and Work Plan:

The Phase II objectives and work plan are summarized in the following Tables. In Section C, we provide a detailed description of our technical results.

<i>Phase II Objectives:</i>		
<i>Objective</i>	<i>Description</i>	<i>Status</i>
1	Optimize the high-k gate dielectric films and structures for SiC MOSFET's and other devices.	Complete
2	Integrate the optimized dielectric film materials and deposition processes into commercial SiC device fabrication.	Complete
3	Design the optimum MOCVD hardware and process technology for routine commercial production of high-k gate dielectrics for SiC devices.	Complete

<i>Phase II Work Plan:</i>			
<i>Task Number</i>	<i>Task Description</i>	<i>Month</i>	<i>Status</i>
1	Install modifications to optimize and streamline the ALD/MOCVD tool performance, as identified in Phase I.	1 - 3	Complete
2	Perform computer modeling and simulation of SiC device performance, with the proposed gate dielectric materials and structures.	1 - 7	Complete
3	Optimize the film properties for the single layer and multilayer dielectric film structures.	3 - 12	Complete
4	Integrate the optimized dielectric films and multilayer structures into SiC power device fabrication.	5 - 15	Complete
5	Optimize the film growth processes in the modified ALD/MOCVD tool, for highest yield and throughput, and for minimal cost of ownership.	9 - 19	Complete
6	Evaluate additional process enhancements to the dielectric film ALD/MOCVD process.	15 - 21	Complete
7	Demonstrate high performance SiC power devices fabricated using the optimized materials and deposition processes.	14 - 23	Complete
8	Perform materials characterization in support of all Tasks.	2 - 23	Complete
9	Perform device characterization in support of all Tasks.	15 - 23	Complete
10	Design the optimum MOCVD hardware and process technology for commercial production of high-k dielectric films for SiC devices.	21 - 24	Complete
11	Reporting.	1 - 24	Complete

C: Detailed Description of Phase II Results:

C.1 Computer modeling and simulation of SiC device performance

Design of the dielectric stack

The most commonly cited degradation mechanism in SiC MOS devices is based on Fowler-Nordheim (FN) tunneling. This mechanism has been thoroughly investigated in Si technology. The work of DiMaria et. al. of IBM analyzing reliability data taken over 15 years attempts to develop simple models to explain the trends. A reliability figure of merit can be obtained from the charge to breakdown parameter described and calculated in the IBM work¹. The charge to breakdown is the total amount of charge that is injected in the dielectric before breakdown. The charge to breakdown is a function of the charge injection rate, and the time to breakdown, both of which are related to the electric field across the oxide. Figure 2 plots the charge to breakdown as a function of the electric field applied across the oxide, the higher the charge to breakdown, the more reliable the dielectric. In reviewing these results there are several important points to make.

- There are two oxide breakdown mechanism, trap generation and electron hole recombination due to avalanche currents.
- Trap generation is significantly reduced in thin oxides, for example for oxides which are 5 nm thick there is no significant trap generation for fields less than 8 MV/cm. This implies that our design criteria for the SiO₂ layer should be ~5 nm.
- For 50 nm thick oxides fields less than 5 MV/cm are required to eliminate significant electron-hole recombination currents. While fields less than 14 MV/cm can eliminate significant electron-hole recombination current in a 5 nm thick film. This implies that we should have fields of 5 MV/cm or less across our HfO₂ in the worst case.

Figure 2: Normalized Charge to Breakdown as a function of Electric Field. From Reference [1].

By utilizing a dielectric stack of SiO_2 and HfO_2 , we are able to reduce the field across the SiO_2 dielectric while maintaining the high field required to bias the gate of a SiC MOS transistor. The gate voltage will appear across the entire dielectric stack in such a way as to produce the optimum low resistance on-state while increasing reliability. In our solution a thin layer of high quality SiO_2 is in intimate contact with 4H-SiC, while most of the thickness of the gate is composed of the high-k HfO_2 . During forward bias FN tunneling can be lowered because a low electric field is achieved through the use of a much thicker HfO_2 for the same channel resistance R_{ch} . Figure 3 shows a computer simulation of the total capacitance of the dielectric stack as a function of the HfO_2 thickness. For comparison, the capacitance of two different thicknesses of SiO_2 (45 and 60 nm) are shown in the graph. Typical SiO_2 gate dielectric thicknesses are ~50 nm for most SiC DMOS designs. Our simulations show that for 5 nm of SiO_2 , 220 to 280 nm of HfO_2 are required to produce an over capacitance which is comparable to the SiC DMOS designs, and which therefore will maintain the same overall on-state resistance for a comparable gate turn on voltage.

Based on the design values for the dielectric stack that we have chosen as discussed above, we now calculate the electric field in the SiO_2 layer as a function of the HfO_2 thickness at a gate voltage of 30 V. The value of 30 V was chosen because this is a worse case condition (based on literature designs) for the gate turn-on voltage. In all cases considered the electric field across the oxide is less than the value which would degrade the reliability. See Figure 4.

Figure 4: Electric field across the SiO₂ layer as a function of the HfO₂ thickness at a gate voltage of +30 V. Note the field across the SiO₂ in all cases is in a region of high reliability, defined in Figure 4.

Implementation of the dielectric stack in a DMOS design

We designed our SiC DMOS FET in such a way as to ensure that when the device is in the off-state, the applied fields are well below those which would reduce the reliability by electron hole recombination currents as defined in Figure 2. In Figure 5a, we show the associated leakage currents due to forward bias FN tunneling for a 5 nm oxide as a function of HfO₂ thickness. There is strong dependence of the leakage current on the HfO₂ thickness. In Figure 5b, we calculate the effect of increased temperature on these leakage currents.

2D Simulation of DMOS design with dielectric stack

We have also performed the 2D simulation of a SiC DMOS using Silvaco software. The goal of the 2D simulation is to predict the on-resistance of the device as well as the maximum field seen by the dielectric in the off condition. These parameters were monitored and optimized based on the device geometry. In particular the gate length was examined in light of the trade offs between the on resistance and the reverse electric field across the oxide.

An example of the DMOS cell which we was modeled is shown in Figure 6. The N+ source, the P-base and the N-Drain are all indicated in the Figure. In addition the gate electrode and gate oxide are also shown.

Figure 5a: Leakage current across the gate, during the application of +30 V across the oxide, as a function of the total gate oxide thickness. Note the strong dependence on the HfO₂ film thickness.

Figure 5b: Normalized leakage current as a function of temperature.

Figure 6: Model geometry for the SiC DMOS FET transistor. Source, base, gate and drain contacts are shown.

References

1. *Impact ionization, trap creation, degradation and breakdown in silicon dioxide films on silicon*, D.J. DiMaria, E. Carter, and D. Arnold, Journal of Applied Physics, 73 (7) p. 3367-3384 (1993).

C.2 Optimization of film properties for single and multilayer dielectric film structures.

In Phase I, SMI and Cornell demonstrated deposition of HfO_2 films with high dielectric constants and low leakage currents. However, HfO_2 films deposited directly on semiconductor materials such as silicon and silicon carbide films suffered from significant hysteresis in their capacitance/voltage (C-V) behavior, owing to traps at the interface. In Phase I, we demonstrated that a thin layer of SiO_2 native oxide, thermally grown on the SiC surface prior to HfO_2 deposition, preserved the quality of the SiC/ SiO_2 native oxide interface, and significantly improved the C-V behavior. Since this thermal SiO_2 layer could be very thin (approximately 10 nm) there was minimal impact on the overall dielectric constant of the stack. Therefore for the Phase II effort, we are concentrating on composite gate dielectric stacks, consisting of MOCVD or ALD deposited HfO_2 on thermally grown SiO_2 films. Since both silicon and silicon carbide form high quality native oxides of pure SiO_2 , we used silicon substrates for the initial process development, prior to demonstration on actual silicon carbide device substrates. The use of inexpensive silicon substrates was done to conserve project materials and expenses, and is completely valid since both silicon and silicon carbide are known to produce low defect interfaces with SiO_2 .

For the process development work of this project period, we used 100 mm silicon wafers, (100) orientation, p-type, boron doped, 5 - 10 $\Omega\cdot\text{cm}$. An SiO_2 native oxide was thermally grown on some of the silicon wafers, to a thickness of 10.0 nm. All other film deposition was done in the

Table I: MOCVD process parameters investigated for HfO_2 film deposition on Si and SiO_2 substrates.

Substrate Temperature	300 C - 500 C
Total Chamber Pressure	10 Torr
Hf TEMA Bubbler Pressure	300 Torr
Hf TEMA Bubbler Temperature	110 C
Gas Line Temperature	135 C
Carrier Gas (Ar) Flow Rate	100 sccm
Process Run Line Push Gas (Ar) Flow Rate	1000 sccm
Uniform Argon Flow Rate	0 sccm - 700 sccm
Uniform Oxygen Flow Rate	0 sccm - 700 sccm
Deposition Time	45 minutes - 60 minutes

ALD/MOCVD test reactor at SMI. The Hf precursor was hafnium tetrakis ethylmethanamide (TEMA). The other process gases were ultra-high purity argon and oxygen. For all deposition trials described in this report, the reactor was run in MOCVD mode. The process parameters used are listed in Table I. As presently configured, the research reactor can process up to three 100 mm wafers per run. Although we demonstrated that we could produce uniform HfO_2 films on whole 100 mm wafers, as shown in Figure 7, we typically worked with quarter wafer sized samples, as shown in Figure 8. Again, this was done to conserve materials, and presented no problem since there is easily sufficient material on one quarter of a 100 mm wafer for all of the materials and electrical characterization. Typically we would load two or more quarter wafer samples per run, of both bare silicon and silicon wafers with the 10 nm of thermal oxide.

Figure 7: Uniform HfO_2 film deposited on a 4 inch silicon wafer by MOCVD at SMI.

Figure 8: Uniform HfO_2 film deposited on a 4 inch silicon wafer quarter by MOCVD at SMI.

Figure 9: Typical XRF results for HfO_2 films in this study. The silver peak is due to the backscattered signal from the x-ray source.

As an initial characterization of all samples, we performed x-ray fluorescence (XRF) analysis at SMI. Typical results are shown in Figure 9, in which the $\text{Hf } L_\alpha$ and L_β peaks are readily observed. Since our XRF system uses an x-ray tube with a silver target, the backscattered Ag emission peak is a convenient reference. We found the ratio of the $\text{Hf } L_\alpha$ peak to the $\text{Ag } L_\alpha$ peak to correlate well with the film thickness, as shown in Figure 10. This became a convenient method to judge thickness of the deposited films, and will prove valuable in later work with multilayer film stacks. However, for all of the results reported here, we verified the HfO_2 film thickness by optical reflectance

spectroscopy at SMI. This analysis also yielded measurements of the optical properties of the films, including the index of refraction (n). For selected samples, additional confirmation of film thickness was obtained by Scanning Electron Microscopy (SEM) of sample cross sections, performed at Cornell University. Also at Cornell, capacitor structures were fabricated in the films, in order to measure leakage current, dielectric constant and C-V behavior.

Figure 11 shows the measured HfO_2 deposition rate as a function of substrate temperature. We observed peak deposition rate at around 350 C to 375 C, with a rapid decrease in deposition rate at higher temperatures. At this time, we do not have an explanation for the

Figure 10: Correlation of XRF results with the HfO₂ film thickness for films deposited by MOCVD at SMI.

Figure 11: Measured HfO₂ deposition rate as a function of substrate temperature, for films deposited by MOCVD at SMI.

drop off of deposition rate at higher temperatures, but it may be related to pre-reaction of the precursors. As shown in Figures 12 and 13, we also observed the highest index of refraction and highest dielectric constant for HfO_2 films deposited at 350 C. We observed values for the index of refraction very close to the bulk value for HfO_2 ($n_{\text{HfO}_2} = 2.05$). We also observed values for the HfO_2 dielectric constant over 15, which is nearly four times that for present technology SiO_2 gate dielectric films. It turns out to be quite convenient that we observe the best film properties at the same temperature which gives the highest deposition rate. Therefore, there may be no need for post deposition annealing of the films to achieve optimum properties. The advantages for the process economics and for reducing the device thermal budget are obvious.

Figure 12: Measured refractive index for HfO_2 films deposited by MOCVD at SMI, as a function of substrate temperature.

Figure 13: Measured dielectric constant for HfO_2 films deposited by MOCVD at SMI, as a function of substrate temperature.

In Figure 14, we show that the film thickness increases linearly with deposition time, indicating no incubation period for the deposition process. Figures 15 and 16 show that the index of refraction and the dielectric constant are insensitive to deposition time, indicating no transitions occur during the HfO_2 growth process. Both observations are encouraging for implementing the HfO_2 film deposition process in SiC device production. In agreement with the Phase I work, we observed similar dielectric constant and index of refraction for HfO_2 films on Si and SiO_2 substrates, as illustrated in Table II. However, flat band voltage and C-V hysteresis were both higher for capacitors fabricated from HfO_2 films on silicon

Figure 14: HfO_2 film thickness as a function of deposition time, for HfO_2 films deposited by MOCVD at SMI.

Figure 15: Measured refractive index for HfO_2 films deposited by MOCVD at SMI, as a function of deposition time.

Figure 16: Measured dielectric constant for HfO₂ films deposited by MOCVD at SMI, as a function of deposition time.

Table II: Property comparison for HfO ₂ films deposited on Si and SiO ₂ substrates.		
	Si	SiO₂
Index of Refraction (<i>n</i>)	1.90	1.90
Dielectric Constant (<i>k</i>)	17.5	15.5
Flatband Voltage (<i>V_f</i>)	+ 5.1 V	-3.3 V
C-V Hysteresis (volt)	0.3 V	0.0 V

Oxygen partial pressure also appeared to influence the HfO₂ film deposition process and the resulting film properties. Figure 17 shows that the HfO₂ film deposition rate increases significantly with the static oxygen partial pressure. (Static partial pressure is defined as the partial pressure calculated from the gas flow rate ratios, assuming no material is consumed during processing.) Figures 18 and 19 show that the HfO₂ film index of refraction remains relatively constant with oxygen partial pressure, while the dielectric constant appears to increase significantly. In the best case, we observe a dielectric constant of $k > 20$ for our HfO₂ films, which is approaching the value for bulk HfO₂. This effect needs to be investigated more thoroughly. The possibility exists to increase deposition rate and film properties for HfO₂ films even further, through MOCVD process optimization.

X-ray diffraction (XRD) analysis of the as-deposited films showed no diffraction peaks, as shown in Figure 20, indicating the as-deposited films to be amorphous. The films could be crystallized by post-deposition annealing, as shown in Figure 21. However, the HfO₂ film

properties did not improve with annealing, as indicated in Table III. In addition, the increase in the C-V hysteresis indicates formation of defects or interface traps, during annealing of the $\text{HfO}_2 / \text{SiO}_2$ gate stack films. In light of this information, we will most likely utilize the high- k films in the as-deposited condition, and optimize the film properties through the process parameters. This eliminates the need for post processing to achieve optimum film properties.

Figure 17: Deposition rate for HfO_2 films deposited by MOCVD at SMI, as a function of oxygen partial pressure.

Figure 18: Measured refractive index for HfO_2 films deposited by MOCVD at SMI, as a function of oxygen partial pressure.

Figure 19: Measured dielectric constant for HfO₂ films deposited by MOCVD at SMI, as a function of oxygen partial pressure.

Figure 20: Typical x-ray diffraction results for the as-deposited HfO₂ films deposited on oxidized silicon by MOCVD at SMI. Cu K_α x-ray source.

Figure 21: X-ray diffraction results for HfO_2 films deposited on oxidized silicon wafer and annealed in oxidizing environments for 30 minutes at various temperatures.

Table III: Property comparison for HfO_2 films on SiO_2 coated substrates, in the as-deposited condition versus annealed for 30 minutes at 700 C.

	As-Deposited	Annealed at 700 C
Dielectric Constant (k)	16.7	16.2
Flatband Voltage (V_f)	- 4.0 V	-6.3 V
C-V Hysteresis (volt)	0.1 V	0.5 V

C.3 Integration of the materials and process technology into SiC device fabrication

SiC Homoepitaxy by Chemical Vapor Deposition

Figure 22: Measured refractive index for HfO_2 films deposited by MOCVD at SMI, as a function of oxygen partial pressure.

Force Microscopy (AFM) image, illustrating the smooth morphology of the grown films with low roughness. Steps are not visible in the AFM image because at the 8 degree offcut, the terrace widths are approximately 5 nm, which is below the resolution of the AFM. Figure 24 shows the doping concentration obtained by mercury probe capacitance-voltage scans. N-type doping levels of $1 \times 10^{16} \text{ cm}^{-3}$ were obtained using nitrogen as the doping source. Figure 25 shows the FTIR spectrum, revealing clear periodic Fabry-Perot oscillations from the epi/substrate interface. Analysis of these oscillations yields a thickness of 6 μm .

SiC was grown by chemical vapor deposition on n+ 8 degree off-axis $\langle 0001 \rangle$ 4H-SiC substrates at a temperature of 1600 C and pressure of 150 Torr. Figure 22 shows the cold wall CVD reactor used for the Phase II work. Silane, propane and HCl were used as the reactants in a hydrogen carrier gas at concentrations of 0.1% each in a vertical cold-wall spinning disk reactor. Nitrogen was used as the n-type dopant. An in-situ pre-growth etch in HCl at 1500 C was performed to prepare the surface for the growth. Growth rates of 3 $\mu\text{m/hr}$ were obtained. Doping densities of $1 \times 10^{16} \text{ cm}^{-3}$ were determined by capacitance voltage measurements. Layers were grown for 2 hours to obtain 6 μm thick layers suitable for investigation of both traditional PMOS capacitors as well as NDMOS structures for 1000 V breakdowns. Figure 23 shows a representative Atomic

Figure 23: AFM micrograph illustrating the smooth morphology of the CVD deposited SiC films.

Figure 24: Doping concentration obtained by mercury probe capacitance-voltage scans. N-type doping levels of $1 \times 10^{16} \text{ cm}^{-3}$ were obtained using nitrogen as the doping source.

Figure 25: FTIR spectrum, revealing clear periodic Fabry-Perot oscillations from the epi/substrate interface. Analysis of these oscillations yields a thickness of 6 μm .

Fabrication of SiC device requires the growth of thick SiC epitaxial layers as the voltage blocking layers. These layers have to be very pure, with carrier concentrations less than $1 \times 10^{17} \text{ cm}^{-3}$. Furthermore, they need to be very thick, requiring fast growth rates to be practical. Growth is typically done in a cold wall SiC CVD system, under mass-transport limited conditions with growth rates of around $2 \mu\text{m/hr}$. The addition of HCl to the chemistry breaks the mass-transport limited constraint, allowing faster growth rates to be obtained. However, the addition of HCl also significantly changes the optimal C/Si ratio provided at the inlet, since HCl preferentially enhances Si-transport over C-transport. This is complicated by the fact that at growth temperatures around 1600 C , HCl etches the SiC surface, potentially destroying the surface morphology and making the SiC film unsuitable for device fabrication. Thus, the HCl use must be judicious. In Phase II, we developed SiC CVD process using HCl additions, and demonstrated SiC growth rates up to $5 \mu\text{m/hr}$. The optimum HCl/SiH₄ ratio was found to be around 2. The SiC film morphology was specular, with background doping levels below 10^{15} cm^{-3} . By adding nitrogen, carrier concentrations up to 10^{18} cm^{-3} were obtained controllably. Using temperatures in the range of 1600 C to 1650 C improved the surface morphology by preventing Si-droplets from condensing on the surface.

P-type Dopant Implant and Activation for SiC

The DMOS structure considered in this Phase II requires 2 implants that must be activated. N-type dopants such as nitrogen and phosphorus are fairly shallow donors (~ 60 meV below the conduction band), and can be activated at low temperatures without significant degradation of material quality. On the contrary, p-type dopants (aluminum being the shallowest), are much deeper (250 meV above the valence band). At room temperature, even with 100% activation, only 1% of the dopants are *ionized*, requiring much higher doping levels. This is far from ideal, particularly considering that the p-type implant region is the channel in the MOSFET. To learn how to activate p-type dopants in our SiC devices, we did a study on various implant activation strategies.

Ion	Energy	Range	Straggle
(keV)	(Å)	(Å)	(Å)
190	2141	237	
180	2029	565	
170	1918	545	
160	1806	524	
150	1693	502	
140	1581	480	
130	1467	457	
120	1354	433	
110	1241	408	
100	1127	382	
90	1013	356	
80	899	328	
70	786	299	
60	673	269	
50	560	237

Figure 26: Calculated ion implant profiles to produce n-type (Al) doped SiC layers for the MOSFET devices.

Prior to ion implantation, a 20 nm cap of SiO₂ was grown on the SiC surface by thermal oxidation. The purpose of the protective cap is to preserve the p-type dopant concentration during the high temperature implant and annealing steps. The standard industry practice is to use implanted p-wells for NMOS SiC transistors. During this Phase II, we used TRIM software to design a test structure implant schedule to produce workable p-n junctions. Figure 26 shows the final schedule to produce 200 nm deep junctions in n-type SiC epitaxial layers. The implants were done at Kroko Ion Implantation services in Tustin, CA. Aluminum ion implants of 2×10^{20} cm⁻³ were done over a depth of 200 nm, using 4 implant steps to give a box profile in the lightly doped ($\sim 3 \times 10^{15}$ cm⁻³)

Figure 27: AFM micrographs of the SiC surface before and after ion implantation and annealing. The results show negligible increase in surface roughness.

Figure 28: IV characteristic of a typical SiC p-n junction fabricated in Phase II. The results show excellent junction behavior.

n-type SiC epilayer. This number was chosen to be just below the solubility limit in SiC, to achieve $\sim 2 \times 10^{18} \text{ cm}^{-3}$ holes at room temperature.

The implants were done at an elevated temperature of 1,000 C, to maximize the eventual activation of the p-type dopants. The high temperature allows self-annealing of implant damage. After implanting, the protective window was removed, and a new 2 μm thick protective SiO₂ mask was used. The samples were then annealed under various conditions in the SiC CVD chamber, at temperatures ranging from 1500 C to 1700 C. Following the activation anneal, the oxide was removed using HF, and the

underlying surface characterized by AFM. The samples were finally fabricated into diode structures of sizes from 0.5 mm to 2 mm squares with contacts. Current-Voltage (IV) curves for the diodes were then taken to characterize the activation.

Vacuum annealing did not accomplish any activation, resulting in highly insulating SiC layers. This was probably due to the oxide caps, as well as the difficulty in attaining the high temperatures in vacuum. Activating in 200 Torr of argon with a 0.1% silane overpressure at 1500 C resulted in complete activation, with no observable roughening of the surface, as seen in the AFM micrographs of Figure 27. The resulting p-n junction performs very close to the best epitaxial SiC junctions in the literature. Figure 28 shows the IV characteristic of a typical p-n junction fabricated by mesa-isolation.

Figure 24: Increasingly more negative flatband voltage with increasing HfO₂ thickness indicates that the turn-on voltage is determined by the film thickness rather than by non-idealities associated with trapped charges at the interface.

Figure 25: Interfaces without an SiO₂ interlayer demonstrate clear hysteresis that is eliminated with the interlayer. Also, the flat band voltage shifts significantly. Both of which indicate the presence of large trapped charge at the interface, which is not desirable.

Fabrication and Characterization of HfO₂/SiC MIS Devices

Metal Insulator Semiconductor (MIS) devices were fabricated using silicon carbide crystal substrates with an HfO₂ dielectric layer on the surface. For the fabrication of test devices, top electrode structures were deposited on the HfO₂ by e-beam evaporation of aluminum through a shadow mask. The circular metal electrode diameters ranged from 250 μm to 750 μm . The electrode thickness was approximately 200 nm. Backside contact was made on the n-type SiC substrate by a second evaporation of Ti, Al, and Au. The schematic drawing of the structure is shown in Figure 26.

Figure 26: Structure of the HfO₂/SiC MIS devices fabricated during the Phase II program.

Electrical properties of HfO₂/SiC MIS structures were characterized by Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements. C-V measurements utilize a small AC bias signal superimposed on the DC bias, and are a very powerful and sensitive tool to characterize dielectric properties of insulators, charge inside the dielectric, and interface charge/states. Figure 27 shows the C-V data for a 500 μm size MIS structure. Since we know the thickness of HfO₂ and the size of the capacitor, the dielectric constant of the HfO₂ layer can be calculated using the capacitance value (~ 118 pF) of the accumulation region. A simple parallel capacitor formula gives the relative dielectric constant of 21, which agrees quite well with that of high quality HfO₂ films. The shape and shift of the C-V plot indicate the existence of negative interface charge. Compared to the ideal theoretical value for the flat-band voltage ($V_{\text{FB}} = \Phi_{\text{metal}} - \Phi_{\text{semiconductor}} = \sim 0$ V), the C-V plot is shifted to positive voltage by about 20 V. Based on Gauss's law, the interface charge density can be extracted from this equation:

$$V_{FB} = \frac{d_{HfO_2} \sigma_{HfO_2}}{\epsilon_{HfO_2}}$$

Here, Φ_{metal} = the work function of the metal, $\Phi_{\text{semiconductor}}$ = the work function of the semiconductor, V_{FB} = the flat-band voltage, d_{HfO_2} = the thickness of dielectric, σ_{HfO_2} = the interface charge density (coulomb/cm²), and ϵ_{HfO_2} = the dielectric constant of HfO₂. The shift of flat-band voltage (~20 V) corresponds to an average interface charge of $\sim 7.5 \times 10^{12}$ cm⁻². This is larger than the typical interface charge ($\sim 1.0 \times 10^{12}$ cm⁻²) between SiC and SiO₂ [2], and could result from structural defects.

Figure 27: Results of Capacitance-Voltage scans for a 500 μm size MIS structure fabricated from HfO₂/SiC during the Phase II program.

Leakage current through the HfO_2 was measured using a DC I-V method. As shown in Figure 28, leakage current on the 500 μm size MIS structures was approximately 1 to 130 pA in the voltage range of 1 to 40 Volts. This indicates a good quality film and reliable growth of HfO_2 on SiC. No electrical breakdown was observed up to an electric field of 1.3 MV/cm.

Figure 28: Results of Current-Voltage scans for a 500 μm size MIS structure fabricated from HfO_2/SiC during the Phase II program.

References

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C.4 Design of the optimum MOCVD hardware for commercial production of high-k dielectric films for SiC devices

The objective for this part of the Phase II project was to design a reactor which is capable of efficiently depositing high-k gate dielectric films in both ALD and MOCVD modes. Our starting point was the rotating disc reactor shown in the solid models of Figures 29 and 30 below. This system was previously developed by SMI for commercial scale deposition of complex oxide and ferroelectric thin films, and is representative of SMI's oxide film deposition products. Two separate gas inlet systems are provided. The "Uniform" gas inlet system distributes inert and oxidizing gases uniformly over the substrate platter, as illustrated in Figure 29. The "Process" gas inlet system injects the precursor gases from a linear array of injectors, as illustrated in Figure 30. Substrate rotation is provided to uniformly distribute these gases over the entire wafer platter.

Figure 29: Computational fluid dynamics model for the "Uniform" gas flow in the ALD/MOCVD test reactor at SMI. The arrows indicate gas flow trajectory. The colors indicate gas temperature.

Figure 30: Computational fluid dynamics model for the "Process" gas flow in the ALD/MOCVD test reactor at SMI. The arrows indicate gas flow trajectory. The colors indicate gas temperature.

Developing an optimized design for both ALD and MOCVD deposition will require optimizing the reactor materials, the showerhead design and the reactor geometry. This would be an extremely daunting task to do empirically. Fortunately, SMI has modern computational fluid dynamic tools to aid in the design. In the following discussions, we illustrate results of testing various reactor configurations, under a range of experimental conditions consistent with the HfO_2 film deposition parameters. The analysis is not only useful in the design of the optimized ALD/MOCVD reactor, but is also a valuable aid for interpreting experimental results.

During Phase II, SMI established an initial design for the ALD/MOCVD reactor chamber, based on a small chamber volume and a short substrate to showerhead distance, as illustrated in Figure 31. The advantages of the small chamber volume are rapid cycle times for the ALD mode of film deposition, and improved precursor utilization. SMI investigated a

number of chamber geometry parameters, and tested these computationally under various process conditions. In Figure 31, we show a reactor design tested under a range of chamber pressures. The Figures show the process gas trajectories and temperature distribution. Note that uniform process gas delivery and gas temperature is provided over the entire 14 inch wafer platter. We show only the process gas flow results in Figure 31 for brevity. Similar results were obtained for the uniform gas inlet. Both uniform gas delivery and uniform temperature are imperative for uniform film growth over large wafers, or over large batches of small wafers. The following results show our design is capable of achieving both.

Figure 31: Computational fluid dynamics model for the "Process" gas flow in the new ALD/MOCVD chamber design. (Left) Pressure = 10 Torr. (Right) Pressure = 2 Torr. Other parameters are: Platter diameter = 14 inches. Showerhead height = 0.8 inches. Total gas flow = 2200 sccm. Rotation = 600 RPM. Substrate temperature = 400 C.

Figure 32 shows a similar set of experiments investigating total uniform and process gas flow rates. For the trials illustrated in Figure 32, we investigated total gas flows ranging from 1100 to 4400 standard cubic centimeters per minute (sccm). Again we show that we can achieve both uniform gas delivery and uniform temperatures over the entire range of gas flow rates anticipated for the process. In Figure 33, we show similar investigations of the effect of substrate temperature. One of the factors that helps us achieve this level of uniformity over a wide range of process conditions in our reactors is the high speed rotation of the substrate platter. Figure 34 shows an illustration of this effect. Substrate rotation at 600 RPM results in excellent uniformity. However, uniformity falls off dramatically with no substrate rotation.

Figure 32: Computational fluid dynamics model for the "Process" gas flow in the new ALD/MOCVD chamber design. (Left) Total gas flow = 1100 sccm. (Top) Total gas flow = 2200 sccm. (Right) Total gas flow = 4400 sccm. Other parameters are: Platter diameter = 14 inches. Showerhead height = 0.8 inches. Pressure = 10 Torr. Rotation = 600 RPM. Substrate temperature = 400 C.

Figure 33: Computational fluid dynamics model for the "Process" gas flow in the new ALD/MOCVD chamber design. (Left) Substrate temperature = 400 C. (Right) Substrate temperature = 800 C. Other parameters are: Platter diameter = 14 inches. Showerhead height = 0.8 inches. Total gas flow = 2200 sccm. Pressure = 10 Torr. Rotation = 600 RPM.

Figure 34: Computational fluid dynamics model for the "Process" gas flow in the new ALD/MOCVD chamber design. (Left) Rotation = 600 RPM. (Right) Rotation = 0 RPM. Other parameters are: Platter diameter = 14 inches. Showerhead height = 0.8 inches. Total gas flow = 2200 sccm. Pressure = 10 Torr. Substrate temperature = 400 C.

D: Commercialization and Collaborative Developments:

Presently, Structured Materials Industries is pursuing several opportunities to transition SiC device manufacturing technology to the market place. This market is well defined, as shown in Figure 35, with dramatic growth potential (60-70% for next several years). However, the market is still not well served, with only one significant competitor for the SiC tool market, and no domestic

providers. SMI has developed core CVD technology that spans an array of technologies for SiC devices. SMI already has a long term relationship with our present STTR partners - Cornell University and Widetronix - to demonstrate SiC epitaxial films. SMI is presently in discussions with the State of New Jersey "Edison Fund", to develop a commercial SiC epi tool. SMI will work with Veeco in this proposed effort. Widetronix intends to be the first production tool purchaser. SMI is also teaming with Penn State University (PSU), to develop CVD tools for bulk SiC growth. The successful development of a high-k gate oxide

Figure 35: Market for SiC devices in various applications.

deposition system in the present STTR program will complement SMI's product line for SiC tools, and enable SMI to offer the complete package to SiC device manufacturers.

SMI has also begun to aggressively build interactions with a wide range of other SiC research groups and device producers (within New Jersey and around the world) that will support sales in the future. As illustrated in the following graphic, there is a concentration of organizations active in SiC development, close to SMI in the Central New Jersey area. The potential exists for a technology base for SiC device development, in close proximity to SMI. SMI has already established relations with many of these companies, most notably II-VI, Princeton and United SiC. We will continue to expand and build these relations in the future. The advantages to the present STTR effort are two fold, to provide technical input to our development effort, and to begin marketing our technology to potential customers.

Figure 36: The high concentration of organizations actively involved in SiC devices development near SMI in Central New Jersey.