Design of Low-Noise Output Amplifiers for P-channel Charge-Coupled Devices Fabricated on High-Resistivity Silicon

S. Haque[a], F. Dion[b], R. Frost[b], R. Groulx[b], S.E. Holland[a], A. Karcher[a], W.F. Kolbe[a], N. A. Roe[a], G. Wang[a], and Y. Yu[c]

[a]Lawrence Berkeley National Laboratory, 1 Cyclotron Road, Berkeley, CA, USA 94720;
[b]Teledyne DALSA Semiconductor, 18 Boul. de l'Aéroport, Bromont, Québec, Canada J2L 1S7;
[c]Stanford University, 450 Serra Mall, Stanford, CA, USA 94305

ABSTRACT

We describe the design and optimization of low-noise, single-stage output amplifiers for p-channel charge-coupled devices (CCDs) used for scientific applications in astronomy and other fields. The CCDs are fabricated on high-resistivity, 4000–5000 Ω-cm, n-type silicon substrates. Single-stage amplifiers with different output structure designs and technologies have been characterized. The standard output amplifier is designed with an n^+ polysilicon gate that has a metal connection to the sense node. In an effort to lower the output amplifier readout noise by minimizing the capacitance seen at the sense node, buried-contact technology has been investigated. In this case, the output transistor has a p^+ polysilicon gate that connects directly to the p^+ sense node. Output structures with buried-contact areas as small as 2 μm × 2 μm are characterized. In addition, the geometry of the source-follower transistor was varied, and we report test results on the conversion gain and noise of the various amplifier structures. By use of buried-contact technology, better amplifier geometry, optimization of the amplifier biases and improvements in the test electronics design, we obtain a 45% reduction in noise, corresponding to 1.7 e^- rms at 70 kpixels/sec.

Keywords: Charge-coupled device, buried contact, noise, source follower, high-resistivity silicon

1. INTRODUCTION

Charge-coupled devices (CCDs) are the detectors of choice for demanding scientific applications such as astronomy and astrophysics. Large format, back-illuminated devices with high quantum efficiency and low noise form the basis for existing and planned large camera systems on astronomical telescopes such as the VLT Survey Telescope OmegaCAM[1] (268 Megapixels), the Dark Energy Survey camera[2,3] (520 Megapixels), the Subaru HyperSuprime camera[4,5] (872 Megapixels), the University of Hawaii Pan-STARRS camera[6,7] (1.4 Gigapixels), and the camera for the planned Large Synoptic Survey Telescope[8] (LSST, 3.2 Gigapixels).

Ideally the CCD read noise will be small in comparison to the shot noise from the background light levels in imaging applications. Given the desire to minimize the total time needed to read out the CCDs, e.g. 2 seconds for LSST,[8] it is necessary to reduce the CCD read noise in order to maintain shot-noise limited imaging at high readout rates since the CCD read noise increases as the square root of the pixel rate.[9] In addition, the signal can be photon-starved in spectroscopic applications in which case the read noise of the CCD output amplifier can be the major noise source. The emphasis of this paper is on the investigation of methods to reduce the CCD amplifier read noise for p-channel CCDs that are fabricated on high-resistivity silicon substrates.

The organization of the paper is as follows. The background theory of CCD amplifier noise is presented, followed by a discussion of device design and technology developments that are investigated to improve the noise. This is followed by the description of experimental results measured on CCDs with varying amplifier designs.

Further author information: (Send correspondence to S.H.)
S.H.: E-mail: SHaque@lbl.gov, Telephone: 1 510 495 2965

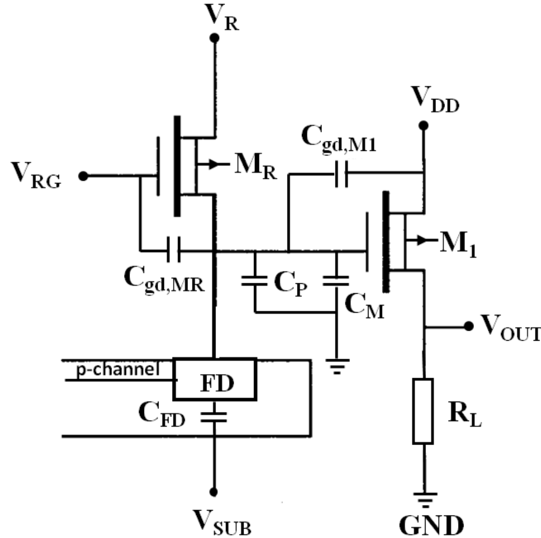

Figure 1. Schematic of a single-stage, source-follower amplifier. M_1 and M_R are the source-follower and reset transistors, respectively. The pertinent device and parasitic capacitances are shown, as well as a simplified cross-section showing the p-channel and floating diffusion (FD) in the n-type silicon substrate. The load resistor R_L is external to the CCD.

2. NOISE THEORY FOR SINGLE-STAGE, SOURCE-FOLLOWER AMPLIFIERS

For the CCDs considered in this work the output amplifier consists of a source-follower transistor M_1 that is connected to the floating diffusion as shown in Fig. 1. The floating diffusion is reset to the potential V_R by transistor M_R. In this work we only consider the noise from the source-follower MOSFET M_1.

For the case where the white noise of M_1 dominates, the read noise in electrons is given by[9]

$$Q_n = \frac{V_{W,M1}}{S_V A_v} \tag{1}$$

where $V_{W,M1}$ is the input-referred voltage noise of the source-follower transistor M_1 in units of volts rms, S_V is the conversion gain in units of volts/electron at the floating diffusion, and A_v is the voltage gain of the source follower. The conversion gain is

$$S_V = \frac{q}{C_T} \tag{2}$$

where q is the electronic charge and C_T is the total capacitance at the input of the source-follower transistor, given by the sum of all the capacitances shown in Fig. 1. From equations 1 and 2 it is clear that for low noise the total capacitance C_T at the input of M_1 should be minimized. The equivalent capacitances that are of interest are shown in Fig. 1, and are the floating-diffusion capacitance C_{FD}, the gate-drain overlap capacitances of M_1 and M_R, i.e. $C_{gd,M1}$ and $C_{gd,MR}$ respectively, the parasitic capacitance C_P due to the wiring between the floating diffusion and M_1, and the equivalent capacitance to ground of M_1. The latter is the Miller-effect capacitance of M_1 and is given by[10]

$$C_M = (1 - A_v) C_{gs,M1} \tag{3}$$

where $C_{gs,M1}$ is the gate-to-source capacitance of M_1. For a surface-channel MOSFET $C_{gs,M1}$ is to first order given by $\frac{2}{3} C_{ox} W L$.[11] The capacitance for a buried-channel MOSFET as used here will be substantially less, and is voltage dependent due to the varying depletion of the buried channel along the length of the transistor.[12,13] C_{ox} for a SiO_2 gate insulator is $\epsilon_{\text{SiO}_2}/x_{\text{SiO}_2}$ where ϵ_{SiO_2} and x_{SiO_2} are the permittivty and thickness of the SiO_2. W and L are the channel width and length of the source-follower transistor.

The small-signal voltage gain of the source follower is given by

$$A_v = \frac{g_m R_{eq}}{1 + g_m R_{eq}} \quad (4)$$

where g_m is the small-signal transconductance of the source-follower transistor M_1 and R_{eq} is the parallel combination of the external load resistor R_L and the small-signal output resistance of M_1.

For long-channel MOSFETs the input-referred voltage noise squared of M_1 is[14]

$$V_{W,M1}{}^2 = 4kT\frac{2}{3}\frac{1}{g_m}\Delta f \quad (5)$$

where k is Boltzmann's constant, T is the temperature in Kelvin, and Δf is the bandwidth in Hz. g_m is given by[14]

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2 I_D \mu_p C_{\rm ox} W/L} \quad (6)$$

I_D and V_{GS} are the drain current and gate-to-source voltage of M_1, and μ_p is the hole mobility in the buried channel.

Besides C_T, the other key parameter that affects the noise is the transconductance of M_1 as seen from Eqs. 1 and 5. Ideally the output transistor will have both high g_m and small area to reduce $C_{gd,M1}$ and C_M. There are tradeoffs, however. For example, g_m can be increased by increasing W but that in turn causes an increase in $C_{gd,M1}$ and possibly C_M. Ideally an optimization process similar to that reported for CMOS image sensors would be performed,[15] but this would require accurate device models for the output transistor that are not presently available. Nonetheless, the first-order models presented above provide a good framework for the development work described in this paper.

The analysis presented so far has neglected $1/f$ noise. The input-referred noise voltage squared due to $1/f$ noise is given by[14]

$$V_{1/f,M1}{}^2 = \frac{K_f \Delta f}{W L C_{ox} f} \quad (7)$$

where f is the frequency. K_f is a constant in units of V^2F that depends on the details of the fabrication process and can vary from device to device due to defects and contamination in the channel region of the transistor. As can be seen from Eq. 7 the $1/f$ noise increases with decreasing gate area, and this effect can be the limiting factor in terms of the benefit in capacitance reduction one achieves from reducing the size of M_1. The $1/f$ noise can also be reduced by decreasing the oxide thickness according to Eq. 7, which also increases the transconductance as seen from Eq. 6. It is interesting to note that deep submicron CMOS transistors with ultra-thin gate oxides and very small channel lengths used in CMOS image sensors can easily achieve both high transconductances and small areas. Noise levels as low as 0.78 e-[16] and 1.28 e-[17] have been reported, with the primary limitation for the aggressively scaled CMOS transistors being excess noise due to random telegraph signal.[16] For the purposes of this study we chose not to attempt a change in the gate-oxide thickness but rather explored other options to reduce the noise.

3. DEVICE DESIGN AND TECHNOLOGY DEVELOPMENT FOR READ NOISE REDUCTION

In this section we describe specific efforts aimed at improving the read noise given the basic framework presented in the previous discussion. We present 2D simulation and experimental measurements of the gate-drain overlap capacitance as well as a technology development to reduce the wiring component C_P of the capacitance at the floating diffusion.

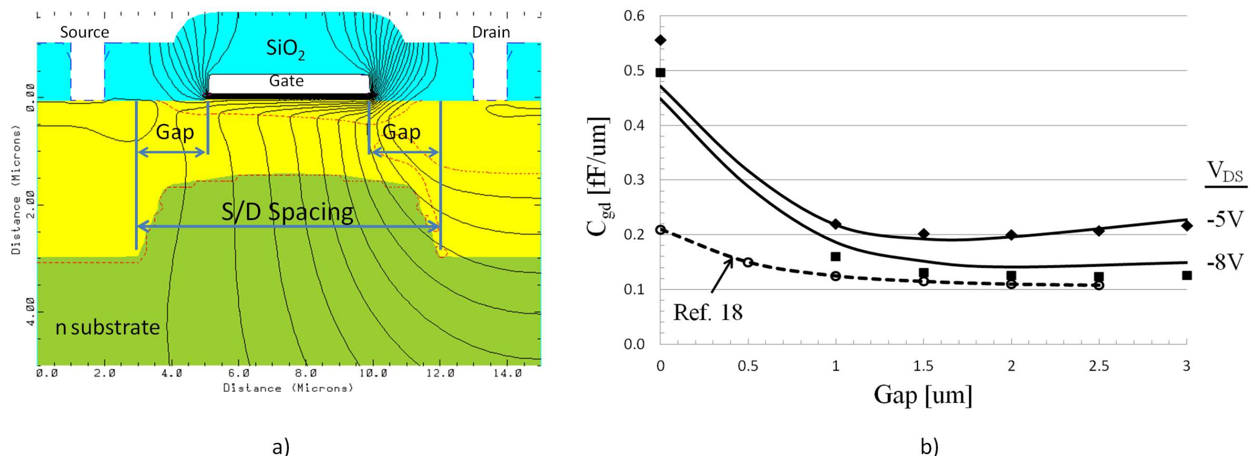

Figure 2. a) Two-dimensional simulation cross-section of a p-channel transistor. The lighter-colored region in the silicon (yellow in the on-line version) is doped p type. S/D Spacing denotes the spacing between the source and drain (channel length L) and Gap denotes the spacing between the edge of the gate and the heavily-doped source or drain. The solid lines are equipotential lines, and the dashed lines in the silicon show the edge of the depletion region. b) Comparison of the measured gate-to-drain capacitance (closed symbols) with simulation (solid lines) and with published data[18] (dashed line and open symbols). For the measurements 600 μm wide transistors were used. As described in the text an offset of 0.05 fF/μm was added to the experimental data points.

3.1 Gate-to-drain overlap capacitance

The gate-to-drain overlap capacitances of both the reset and source-follower transistors contribute to the total capacitance C_T and hence the noise. This capacitance is proportional to the transistor width W, but as pointed out in Section 2 other considerations affect the choice of W. In terms of transistor design, a standard method to reduce the overlap capacitance is to offset the heavily-doped drain region from the edge of the polysilicon-gate electrode.[18] The buried-channel implant connects the channel of the transistor to the drain region. This method relies on photolithographic registration to set the gap spacing between the gate edge and the heavily-doped drain region, and is easily implemented in a standard scientific CCD process technology.

In order to improve our understanding of the overlap capacitance we have performed 2D simulations and compared the results to experimental measurements. Figure 2 a) shows a 2D simulation cross-section with a symmetric gap between the gate edge and the heavily-doped source and drain regions of the transistor. A gap on the source side tends to reduce the transconductance of the transistor but also reduces the punchthrough current,[19, 20] which is a consideration for transistors fabricated on high-resistivity silicon substrates as is the case in this work.[21, 22] The process simulator TSUPREM4 was used to generate the cross-section shown in Fig. 2 a), and the 2D device simulator MEDICI was used to study the overlap capacitance.

Figure 2 b) compares the simulation results to measurements on $W = 600$ μm transistors with n-type polysilicon gates that are included as part of the process monitor test devices on the CCD wafer layout. Published data are included for comparison.[18] The transistors used for the measurement were prescreened by measuring their current-voltage characteristics with source and drain interchanged. Only transistors with nearly identical characteristics in both configurations were used for the capacitance measurements. In this way we were able to avoid transistors with photolithographic misalignment that would have resulted in an incorrect estimate of the gap spacing.

The capacitance measurements were taken with a Hewlett Packard 4284A LCR meter. The transistor gate was grounded for the measurements. Even with the 600 μm-wide transistors the measurements were challenging due to the small magnitude of the overlap capacitance. After careful calibration and subtraction of the cable capacitance, we observed a more or less constant offset between the measurements and simulations. We have added a slight offset of 30 fF (0.05 fF/μm) to the data that is shown in Fig. 2 b). With the addition of this offset we find reasonably good agreement between the measurements and simulations.

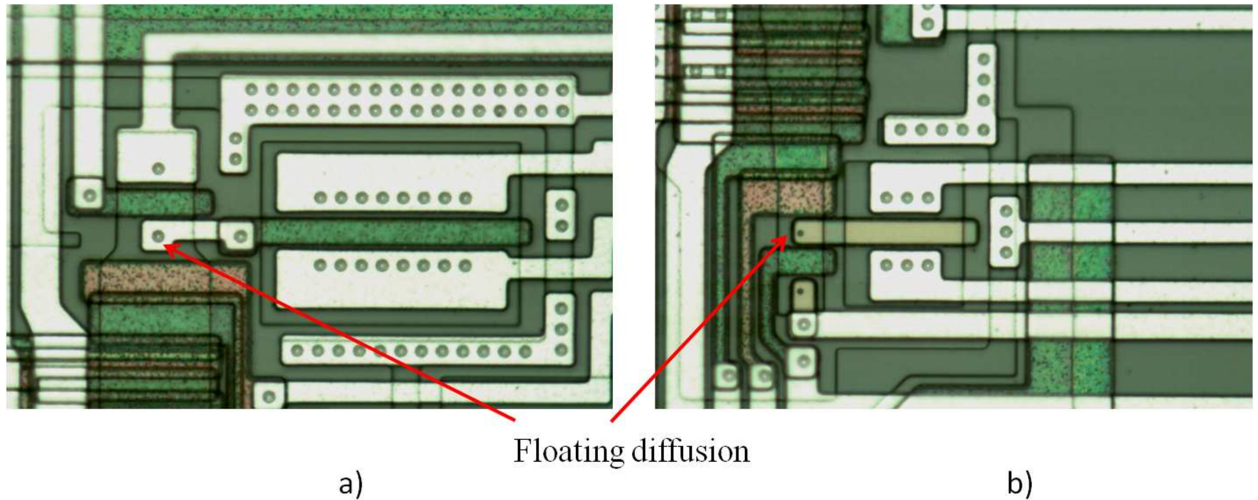

Figure 3. Photographs of the amplifier region showing a) a metal contact between the floating diffusion and the polysilicon-gate electrode of the standard $W/L = 47/6$ output transistor with a floating-diffusion area is 9 μm $\times$ 9 μm and b) a direct connection of dimensions 2 μm $\times$ 2 μm between the floating diffusion and the polysilicon-gate electrode of the $W/L = 20/6$ output transistor.

There are two interesting trends observed in Fig. 2 b). The reduction in overlap capacitance is a strong function of the gap spacing for spacings of about 2 μm and below, but for larger gap sizes there is little improvement and even some degradation. The transistors used in this study had a gap spacing of 1.5 μm at both the source and drain sides. Secondly, the overlap capacitance is a function of the drain voltage and decreases as more voltage is dropped across the drain region. In section 4.3 we describe the methods available to bias the source-follower transistor in order to increase the voltage drop across the drain region, and the resulting effects on the noise.

The dashed lines in Fig. 2 a) show the edge of the depletion regions. The depletion depth at the surface beneath the gate is much greater than the oxide thickness, and therefore it is the surface depletion that mainly determines the gate-to-source capacitance C_{gs}.[12,13] The dependence of C_{gs} on the depletion depth causes the Miller-effect capacitance to be a function of the bias conditions of the source-follower transistor.

3.2 Buried-contact development

In this section we describe a technology development intended to reduce the interconnect capacitance between the floating diffusion and the polysilicon-gate electrode of the output transistor, as well as the floating-diffusion capacitance itself. Figure 3 a) shows a conventional metal connection between the floating diffusion and the polysilicon-gate electrode of the output transistor. The connection to the floating diffusion in this case is aluminum that contacts the floating diffusion through an opening etched in the SiO_2 insulator between the aluminum and the silicon substrate. The contact opening must be smaller than the implanted floating-diffusion area in order to guarantee an ohmic contact to the floating diffusion when taking into account registration errors in the photolithography process. As a result the floating-diffusion area is larger than the minimum area allowed by the process design rules. For the particular process used the floating-diffusion implant must extend beyond the contact by at least 1.5 μm. In addition, the metal must similarly contact the polysilicon-gate electrode. For the conservative design shown in Fig. 3 a) the floating-diffusion size is 9 μm $\times$ 9 μm.

Fig. 3 b) shows a direct contact between the polysilicon-gate electrode and the floating diffusion, which is referred to in this work and elsewhere as a buried contact. The buried contact allows for a minimum sized floating-diffusion area, thereby reducing C_{FD}. The area that would otherwise be needed for a conventional connection to make contact to the polysilicon-gate electrode is eliminated. The latter allows the output transistor to be placed closer to the floating diffusion, which reduces the interconnect capacitance C_P. The benefit of the buried contact is a reduction in the floating-diffusion and interconnect capacitance, and has been shown to yield excellent results in terms of noise for n-channel CCDs.[23]

The challenge to implement buried contacts in the p-channel technology described here is the need to contact a p-type floating diffusion. The three polysilicon layers are doped n type, and therefore cannot make a direct connection to a p^+ floating diffusion. The choice of n-doped polysilicon is due to the smaller sheet resistance that can be achieved with n-type doping when compared to p-type. As a result a fourth polysilicon layer that is implanted with boron to form p-type polysilicon is used for the buried contact and gate electrode of the output transistor. The buried-contact opening is formed by etching of the SiO_2 layer over the floating-diffusion region. The same photoresist mask that defines the etched region is then implanted with boron, resulting in a self-aligned implant. The fourth polysilicon layer is then deposited, making direct contact to the implanted floating diffusion. The polysilicon is in turn implanted with boron and subsequently patterned to form the gate electrode and connection to the floating diffusion. The implants are then annealed, and the remaining process steps are conventional.

The two buried-contact sizes were 9 μm $\times$ 2 μm and the minimum-sized 2 μm $\times$ 2 μm. The latter required a gradual reduction in the serial-register width in the extended pixel region as can be seen in Fig. 3 b).

4. MEASUREMENT RESULTS

The CCDs used in this study are 1022 $\times$ 1252 and 1022 $\times$ 682 (15 μm pixel)^2 frame-transfer devices with amplifiers of varying design located at each of the four corners. The p-channel CCDs were fabricated on high-resistivity, float-zone refined, 4000–5000 Ω-cm silicon substrates that are approximately 650 μm thick. At the typical 40V substrate bias used in this work the substrates are only partially depleted, with an estimated depletion depth of 200–300 μm. Traditional floating diffusions and single-stage, source-follower amplifiers are used. The load resistors of the source followers are located external to the CCD. The CCD vertical and horizontal registers have three-phase clocks that are designed for split readout. An independently clocked transfer gate is used to transfer signal charge from the vertical register into the horizontal register. Each horizontal register is followed by a summing well, output gate, floating-diffusion sense node, and a single-stage, source-follower amplifier.

All tests were conducted at -140° C at a read out rate of 70 kpixels/sec. The CCD output signal was digitized to 16 bits. The CCD system gain was calibrated using a ^{55}Fe x-ray source[9] that generates a charge signal corresponding to approximately 1570 e^- at -140° C. To obtain the total deposited charge for each incident x-ray, an array of 3 $\times$ 3 pixels was summed. The read noise was determined by measuring the Gaussian width of the overscan signal and correcting by the measured system gain. The gain components of the test system consist of the charge conversion gain S_V of the sense node, the on-chip, source-follower amplifier gain, the off-chip JFET source-follower gain where applicable, and the gains of the external pre-amplifier and signal-processing circuitry of the commercial CCD controller used in this work.[24]

For this study the source-follower transistor channel dimensions were varied as well as the method to make contact to the floating diffusions. The standard source-follower amplifier MOSFET that was included as a reference on both CCDs has an n-type polysilicon gate of width $W = 47$ μm and length $L = 6$ μm. The n-type polysilicon gate makes contact to the p^+ floating diffusion via a metal connection as described in the previous section. The other three source-follower amplifier configurations on each CCD have p^+ polysilicon gates that make contact to the p^+ floating diffusion via the buried contact. The dimensions of the buried contacts were 9 μm $\times$ 2 μm and 2 μm $\times$ 2 μm for the 1022 $\times$ 1252 and 1022 $\times$ 682 CCDs, respectively. For the transistors with p^+ polysilicon gates the W/L ratios were 47/6, 20/6 and 12/3 resulting in 6 combinations of W/L and buried-contact size.

The 12/3 transistor was observed to suffer from short-channel effects and degraded read noise when compared with the standard amplifier despite the reduction in capacitance. Simulation studies do predict possible performance improvements for a 3 μm gate length if the gate-insulator thickness is substantially reduced, and that could be the subject of a future study. Also, the read noise measured on the 47/6 amplifier with the p^+ polysilicon gate and buried contacts showed marginally improved results when compared with the standard 47/6 amplifier with the metal connection to the floating diffusion. We were able to demonstrate significant improvement in the noise performance of the amplifiers with the 20/6 output transistor, and the measured noise results are summarized in Fig. 4. Table I contains the details on the corresponding DC biasing conditions and the source-follower and floating diffusion conversion gains A_v and S_V, respectively. In the following we will focus on

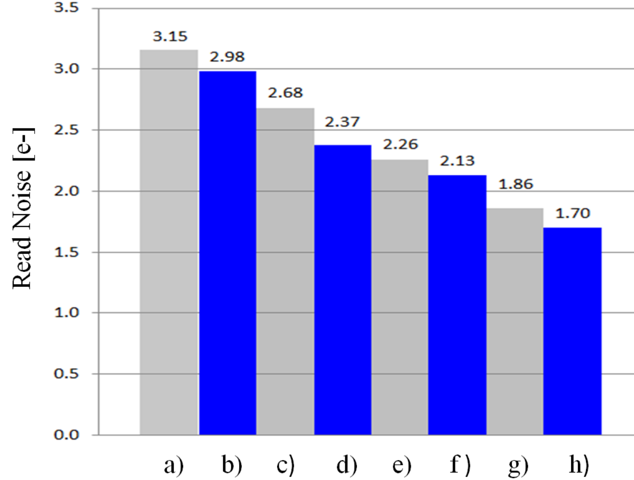

Figure 4. Bar chart showing the read noise at an operating temperature of -140° C, readout speed of 70 kpixels/sec and substrate bias voltage of 40V comparing a) the standard 47/6 output amplifier with b)–h) the 20/6 version with buried contacts. Entries b) through f) are for the 9 μm $\times 2$ μm buried contact. Key: W/L, $R_L/V_{DD}/V_R$. a) 47/6, 20 k$\Omega/-22$ V$/-12.5$ V. b) 20/6, 20 k$\Omega/-22$ V$/-12.5$ V. c) 20/6, 30 k$\Omega/-22$ V$/-12.5$ V. d) 20/6, 30 k$\Omega/-22$ V$/-9$ V with JFET. e) 20/6, 30 k$\Omega/-25$ V$/-9$ V. f) 20/6, 30 k$\Omega/-25$ V$/-9$ V with JFET. g) 20/6, 30 k$\Omega/-25$ V$/-9$ V and 2 μm $\times$ 2 μm buried contact. h) 20/6, 30 k$\Omega/-25$ V$/-9$ V with JFET and 2 μm $\times$ 2 μm buried contact.

Table 1. DC operating conditions, source-follower voltage gains A_v, floating diffusion conversion gains S_V and measured noise corresponding to 5 of the data points shown in Fig. 4. For the first three 20/6 entries the buried-contact size was 9 μm $\times$ 2 μm. The last entry in the table is for a 2 μm $\times$ 2 μm buried contact. The V_{GS} values are calculated from the externally-applied voltages and do not account for clock feedthrough effects when the reset transistor is turned off.

Amplifier W/L	R_L [kΩ]	V_{DD} [V]	V_R [V]	V_{OUT} [V]	V_{GS} [V]	V_{DS} [V]	I_{DS} [mA]	A_v [V/V]	S_V μV/e$^-$	Noise [e$^-$]
47/6 Standard	20	-22	-12.5	-17.7	5.2	-4.3	-0.89	0.67	4.3	3.15
20/6	20	-22	-12.5	-16.0	3.5	-6.0	-0.80	0.61	5.8	2.98
20/6	30	-22	-12.5	-17.5	5.0	-4.5	-0.58	0.58	6.4	2.68
20/6	30	-25	-9.0	-15.4	6.4	-9.6	-0.51	0.66	7.0	2.26
20/6 2×2 μm^2	30	-25	-9.0	-15.0	6.0	-10.0	-0.50	0.70	9.3	1.86

the read noise performance of the amplifier with $W/L = 20/6$ and will describe the methods used to achieve the noise reductions seen in Fig. 4.

4.1 20/6 with buried contact at standard biasing conditions

The goal of the initial study was to compare the 20/6 transistor amplifier to the standard version under the same external biasing conditions. The standard conditions are at a power supply voltage $V_{DD} = -22$ V, a reset level of $V_R = -12.5$ V and a load resistor value of $R_L = 20$ k Ω. As seen from Fig. 4 the read noise for the amplifier with the 20/6 transistor and buried contact is 2.98 e$^-$ as compared to 3.15 e$^-$ for the standard amplifier. As seen in Table I, this small reduction in read noise is attributed to a lower total capacitance and correspondingly larger conversion gain S_V due to the buried contact with reduced C_P and smaller transistor width. The read noise is improved despite the smaller transconductance and source-follower voltage gain for the 20/6. For Table I the output voltage is measured directly with the output current inferred from V_{OUT} and R_L. The source-follower voltage gain A_v is measured via injection of a sinusoidal signal into the reset-drain node, and the conversion gain is calculated from the measured ^{55}Fe conversion gain taking into account the total voltage gain in the electronics

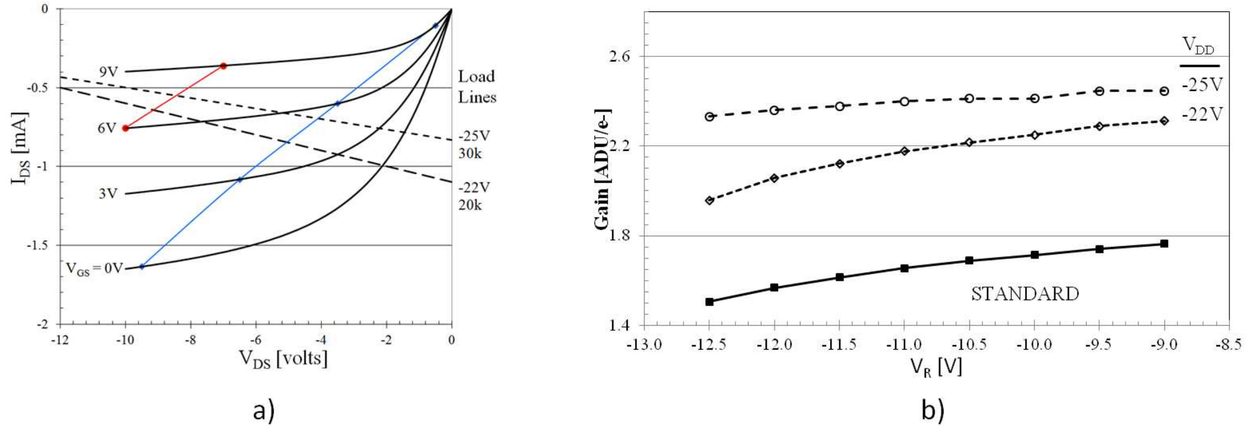

Figure 5. a) 20/6 source-follower transistor current-voltage characteristics measured at -140° C. The substrate-bias voltage was 25V. The upper dashed line is the load line for V_{DD}/R_L of -25 V/30 kΩ, and the lower dashed line is for -22 V/20 kΩ. The smooth curves with points intersecting the transistor curves are the loci of points satisfying Kirchhoff's voltage law given the bias voltages V_R and V_{DD}. The leftmost curve is for V_R/V_{DD} values of -9 V/-25 V, and the rightmost curve is for -12.5 V/-22 V. b) Gain in ADU/e$^-$ versus reset-drain voltage comparing the 47/6 amplifier (solid line and symbols) at standard conditions of V_{DD}/R_L of -22 V/20 kΩ with the 20/6 amplifier with 30 kΩ load resistor and buried contact of size 9 μm × 2 μm (dashed lines and open symbols). The effect of V_{DD} on the gain for the 20/6 is also shown. The measurements were done at a readout speed of 70 kpixels/sec, temperature of -140° C and substrate-bias voltage of 40V.

chain. The gate-to-source voltage is calculated, and does not take into account the reset-clock feedthrough that raises the floating-diffusion potential when the reset transistor is turned off.

4.2 Effect of the load resistor

A further reduction in noise from 2.98 e$^-$ to 2.68 e$^-$ was realized by increasing the value of R_L from 20 kΩ to 30 kΩ as seen when comparing the 2nd and 3rd bars from the left in Fig. 4. As seen in Table I the drain current was reduced from -0.80 mA to -0.58 mA, resulting in a decrease in the output-transistor transconductance according to Eq. 6. This was offset by an increase in the equivalent output resistance R_{eq} of the amplifier for R_L of 30 kΩ with the voltage gain remaining about the same. The larger V_{GS}, i.e. 5.0V versus 3.5V from Table I, will increase the depletion depth under the gate. This change in V_{GS} is consistent with the reduction in the output current noted above. The increased surface depletion reduces $C_{gs,M1}$ as discussed in Section 3.1. This reduces the Miller-effect capacitance (Eq. 3) even though the gain is unchanged to first order, and therefore we attribute the lower noise to the reduced capacitance. It is interesting to note that this effect overcomes the increase in noise due to the thermal noise contribution of R_L that is given by ${V_{R_L}}^2/\Delta f = 4kTR_L$.

4.3 Effect of V_{DD} and V_R

In order to investigate further improvements in noise, the effect of the DC bias voltages was studied. To aid in the understanding we have performed current-voltage measurements on source-follower transistors. The reset transistor shown in Fig. 1 was biased to its on state. This allows for the application of the source-follower gate voltage via the conducting channel of the reset transistor. The drain and source connections are the V_{DD} and source-follower output connections. The measurements were done with a Hewlett Packard 4145B Semiconductor Parameter Analyzer.

Figure 5 a) shows the current-voltage characteristics of a 20/6 source-follower transistor measured at -140° C. The drain current versus drain-to-source voltage is shown for different gate-to-source voltages. Also shown are load lines for V_{DD}/R_L values of -22 V/20 kΩ and -25 V/30 kΩ, as well as the loci of V_{GS} and V_{DS} voltage values that satisfy Kirchhoff's voltage law for the bias conditions, i.e.

$$V_{GS} = V_R + V_{DS} - V_{DD} \tag{8}$$

The two bias conditions that are represented in Fig. 5 a) are for $V_R/V_{DD}/R_L$ values of -12.5 V/-22 V/20 kΩ and -9 V/-25 V/30 kΩ. The operating point of the transistor occurs at the intersection of the load line and the current-voltage characteristics where in addition Kirchhoff's voltage law is satisfied. Interpolation is used to draw the smooth curves connecting the loci of points corresponding to Eq. 8. As noted earlier the gate voltage will be higher than V_R due to clock feedthrough when the reset transistor is turned off.

As can be seen in Fig. 5 a), the $V_R/V_{DD}/R_L$ values of -9 V/-25 V/30 kΩ result in the transistor being biased deeper into the saturation region with more negative V_{DS} than for the -12.5 V/-22 V/20 kΩ case. Referring to Table I, the reverse bias between the gate and channel is also larger for the -9 V/-25 V/30 kΩ combination. The gate-to-drain overlap and gate-to-source capacitances are reduced, leading to an improvement in the conversion gain S_V from 5.8 to 7.0 μV/e$^-$ according to Table I. The source-follower voltage gain is also improved from 0.61 to 0.66, and the measured gain is consistent with first-order calculations based on the data in Fig. 5 a).

To study in more detail the effects of V_R and V_{DD} on the output-amplifier read noise we varied V_R from the standard -12.5 V to -9.0 V in steps of 0.5 V. To prevent hole injection from the floating diffusion and for proper CCD performance we were required to shift the CCD clocks and bias voltages accordingly. The total clock excursions were kept constant at 10 and 8 V for the serial and vertical clocks, respectively.

Figure 5 b) shows the gain in analog-to-digital units (ADU) per electron versus V_R comparing the 47/6 at standard operating conditions of V_{DD}/R_L of -22 V/20 kΩ with the 20/6 with 30 kΩ load resistor at V_{DD} values of -22 and -25 V. The effect of reducing in magnitude V_R is to increase the gain, and the same is true for an increase in magnitude of V_{DD}. The latter is limited by hot-electron effects that initially manifest themselves as amplifier glow.[9] Also, as noted earlier the change of V_R from -12.5 V to -9.0 V causes a larger gate-to-drain voltage as seen in Table I and Fig. 5 a), and threshold voltage shifts due to hot-carrier trapping will be a concern for sufficiently large values of V_{GD}.

The net effect of changing V_{DD} from -22 to -25 V and V_R from -12.5 to -9 V for the 20/6 with 30 kΩ load is a reduction in the read noise of 0.42 e$^-$ to a level of 2.26 e$^-$. As seen in Fig. 4, when compared to the 47/6 amplifier read noise of 3.15 e$^-$ at standard conditions the total read noise reduction is 0.89 e$^-$. This improvement is due to the cumulative effects of reduced capacitance due to the buried contact, smaller transistor width with reduced Miller effect, and increased voltage drops across the transistor electrodes that reduce the gate-to-drain and gate-to-source capacitances.

4.4 Effect of buried-contact size

The measurement results presented in the previous sections were for a buried-contact size of 9 μm × 2 μm. As mentioned previously, CCDs were also fabricated with a minimum-sized buried contact of 2 μm × 2 μm in order to reduce the floating-diffusion capacitance even further.

Figure 6 shows the gain and noise as a function of V_R with V_{DD} as a parameter comparing the standard transistor and the 20/6 with 9 μm × 2 μm and 2 μm × 2 μm buried contacts. The y-axis scales are the same in Fig. 6 a) and b) in order to emphasize the increase in conversion gain due to the smaller buried contact. From Table I the smaller buried contact results in a conversion gain improvement of more than 30% at $V_R/V_{DD}/R_L$ values of -9 V/-25 V/30 kΩ. The corresponding noise reduction is nearly 20%, from 2.26 e$^-$ to 1.86 e$^-$. The last row in Table I shows the DC operating point of the transistor with the 2 μm × 2 μm buried contact. The bias points are slightly different than for the 9 μm × 2 μm case under the same conditions due to wafer to wafer variations.

There are three additional entries in Fig. 4 that show the noise improvements realized with a JFET source-follower buffer inserted between the CCD output and the preamplifier. The JFET model number is J176. The circuit is located on a flex circuit near the CCD to reduce the wiring capacitance. The load resistor is operated cold at a temperature comparable to the CCD. The load resistor was at room temperature when the JFET buffer was not used. The JFET buffer has a smaller effective input capacitance than the preamplifier. The latter is located outside the cryostat with correspondingly larger wiring capacitance. The reduced capacitive load on the CCD amplifiers allows for faster on-chip transition times where the dominant RC time constant for the on-chip amplifier is the product of $1/g_m$ of the output transistor and the load capacitance of the following

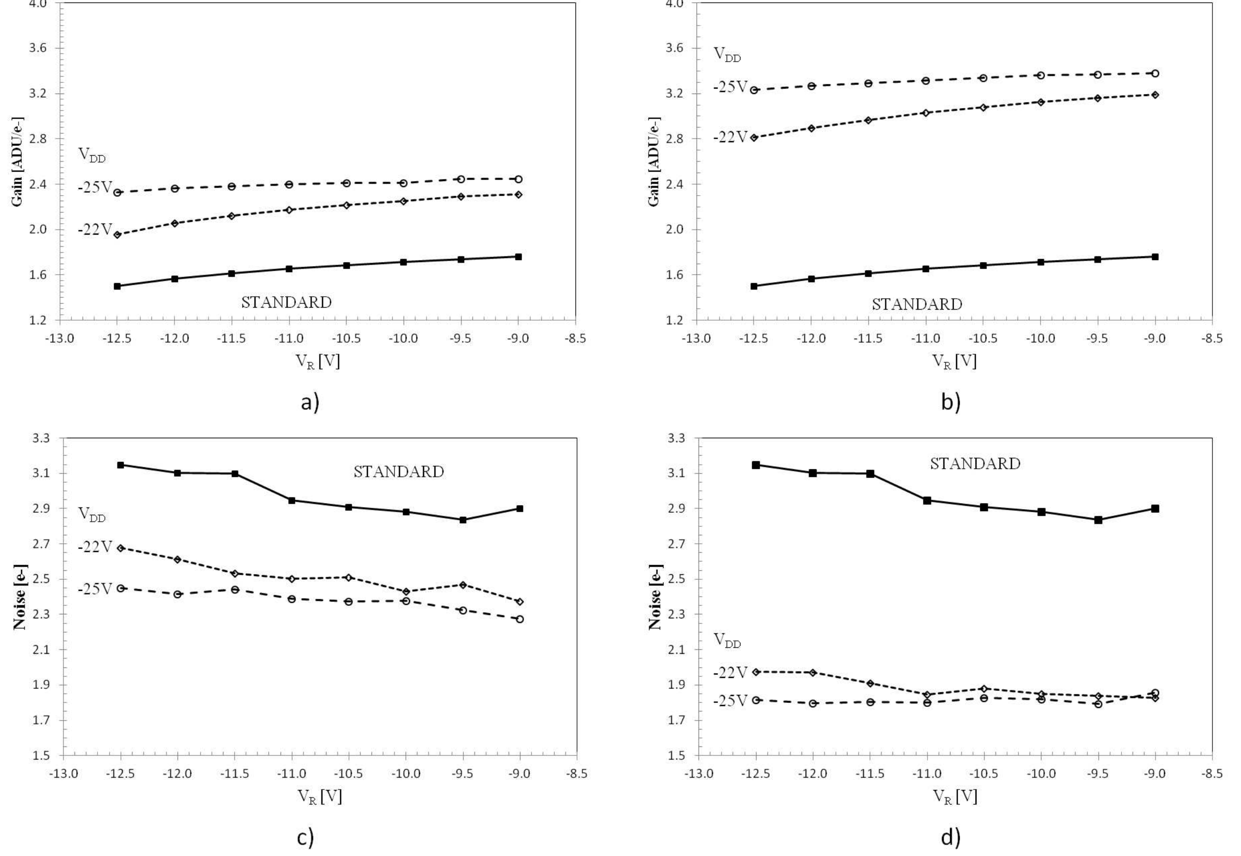

Figure 6. Gain in ADU/e$^-$ versus reset-drain voltage at $V_{DD} = -22/-25V$ (open symbols and dashed lines) comparing the 20/6 amplifier with buried contacts of sizes a) 9 μm $\times$ 2 μm and b) 2 μm $\times$ 2 μm. Corresponding noise versus reset-drain voltage at $V_{DD} = -22/-25V$ (open symbols and dashed lines) comparing the 20/6 amplifier with buried contacts of sizes c) 9 μm $\times$ 2 μm and d) 2 μm $\times$ 2 μm. The 20/6 measurements were done with a load resistor of 30 kΩ at a readout speed of 70 kpixels/sec, temperature of -140° C and substrate-bias voltage 40V. The results for the 47/6 at standard operating conditions of V_{DD}/R_L of -22 V/20 kΩ are also shown for comparison (solid lines and closed symbols).

stage. We attribute the improvements in noise with the JFET buffer to be due to improved noise rejection from the correlated double signal processing circuitry with the faster waveforms. The minimum noise achieved using the JFET buffer and the 20/6 with 2 μm $\times$ 2 μm buried contact is 1.70 e$^-$, which is a 45% improvement over the 47/6 amplifier operated at standard conditions.

5. DISCUSSION

The noise improvements described in the previous sections arise primarily from reductions in the total capacitance at the floating diffusion. In addition to the key technology development of the buried contact, a major part of the noise-reduction effort had to do with determining the DC operating conditions that reduce the voltage-dependent capacitances C_{gd} and C_{gs}. The floating-diffusion capacitance is also voltage dependent, and we intend to repeat the noise study on fully depleted devices. As pointed out earlier, the devices used in this study are fabricated on thick substrates that are partially depleted. The floating-diffusion component of the capacitance in this study could be smaller than what will be observed on a 200–250 μm thick, fully depleted device.

The results presented here are for a small number of devices from one fabrication lot of wafers. We plan to repeat this effort on additional lots to determine the reproducibility of the buried-contact processing as well as to study in more detail the effect on noise due to wafer-to-wafer variations.

Improvement in the device design of the output transistor is an avenue for future noise reduction. Given that the output transistor with the buried contact uses a fourth layer of polysilicon, one can consider a gate dielectric thickness and channel doping that is different than that used in the CCD channels. We have performed preliminary 2D simulations where the output-transistor gate dielectric thickness and gate length were decreased, and have studied the effects of these changes on the device g_m, output resistance, and capacitances with encouraging results.

6. SUMMARY

We have presented the results of an experimental study aimed at improving the noise performance of p-channel CCDs that are fabricated on high-resistivity silicon substrates. The development of a buried contact to reduce the interconnect and floating-diffusion capacitance has been described as well as the effect of the DC operating point of the output transistor on the read noise. The noise was reduced from 3.15 e^- for the standard amplifier to as low as 1.70 e^- at 70 kpixels/sec for a smaller amplifier utilizing a buried contact and optimized biasing.

7. ACKNOWLEDGEMENTS

The CCDs used in this work were packaged by John Emes. This work was supported by the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231. The U.S. Government retains, and the publisher, by accepting the article for publication, acknowledges, that the U.S. Government retains a non-exclusive, paid-up, irrevocable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for U.S. Government purposes.

8. DISCLAIMER

This document was prepared as an account of work sponsored by the United States Government. While this document is believed to contain correct information, neither the United States Government nor any agency thereof, nor the Regents of the University of California, nor any of their employees, makes any warranty, express or implied, or assumes any legal responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by its trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof, or the Regents of the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof or the Regents of the University of California.

REFERENCES

[1] O. Iwert *et al.*, "The OmegaCAM 16K x 16K CCD Detector System for the ESO VLT Survey Telescope (VST)," *Proc. of SPIE*, **6276**, 62760A-1, 2006.

[2] B. Flaugher *et al.*, "The Dark Energy Camera (DECam)," *Proc. of SPIE*, **7014**, 70140E-1, 2008.

[3] J. Estrada *et al.*, "Focal Plane Detectors for Dark Energy Camera (DECam)," *Proc. of SPIE*, **7735**, 77351R-1, 2010.

[4] Y. Komiyama *et al.*, "Hyper Suprime-Cam: Camera Design," *Proc. of SPIE*, **7735**, 77353F-1, 2010.

[5] Y. Kamata, S. Miyazaki, H. Nakaya, H. Suzuki, Y. Miyazaki and M. Muramatsu, "Characterization of Performance of Hyper Suprime-Cam CCD," *Proc. of SPIE*, **7742**, 774229-1, 2010.

[6] N. Kaiser *et al.*, "The Pan-STARRS wide-field optical/NIR imaging survey," *Proc. of SPIE*, **7733**, 77330E-1, 2010.

[7] B. Burke *et al.*, "Orthogonal Transfer Arrays for the Pan-STARRS Gigapixel Camera," *Proc. of SPIE*, **6501**, 650107-1, 2007.

[8] S. Kahn *et al.*, "Design and Development of the 3.2 Gigapixel Camera for the Large Synoptic Survey Telescope," *Proc. of SPIE*, **7735**, 77350J-1, 2010.

[9] J.R. Janesick, "*Scientific Charge-Coupled Devices*," SPIE Press, 2001.

[10] P. Centen, "CCD On-Chip Amplifiers: Noise Performance versus MOS Transistor Dimensions," *IEEE Trans. Elec. Dev.*, **38**, 1206, May 1991.

[11] Y.P. Tsividis, "*Operation and Modeling of the MOS Transistor*", McGraw-Hill, 1987.

[12] K. C.-K. Weng, P. Yang and J-H. Chern, "A predictor/CAD model for buried-channel MOS transistors," *IEEE Trans. on Computer Aided Design*, **6**, 4, 1987.

[13] M.J. Van der Tol and S.G. Chamberlain, "Buried-channel MOSFET model for SPICE," *IEEE Trans. on Computer Aided Design*, **10**, 1015, 1991.

[14] P.R. Gray and R.G. Meyer, "*Analysis and Design of Analog Integrated Circuits, Second Edition*," John Wiley & Sons, Inc., 1984.

[15] B. Fowler, "Single photon CMOS imaging through noise minimization," in "*Single-Photon Imaging*," Springer Series in Optical Sciences, 2011.

[16] J. Janesick, J. Pinter, R. Potter, T. Elliott, J. Andrews, J. Tower, M. Grygon, and D. Keller, "Fundamental performance differences of CMOS and CCD imagers: Part IV," *Proc. of SPIE*, **7742**, 77420B-1, 2010.

[17] B. Fowler, C. Liu, S. Mims, J. Balicki, W. Li, H. Do, J. Appelbaum, and P. Vu, "A 5.5Mpixel 100 Frames/sec Wide Dynamic Range Low Noise CMOS Image Sensor for Scientific Applications," *Proc. of SPIE*, **7536**, 753607-1, 2010.

[18] B.E. Burke, R.W. Mountain, D.C. Harrison, M.W. Bautz, J.P. Doty, G.R. Ricker, and P.J. Daniels, "An abuttable CCD imager for visible and x-ray focal plane arrays," *IEEE Trans. on Electron Devices*, **38**, 1069, May 1991.

[19] K. Yamaguchi and S. Takahashi, "Submicron gate MOSFET's with channel-doped separate gate structures (SG-MOSFET's)," *IEEE Trans. Elec. Dev.*, **28**, 888, July 1981.

[20] K. Yamaguchi, S. Takahashi, and H. Kodera, "Theoretical study of a channel-doped separate gate Si MOSFET (SG-MOSFET) by two-dimensional computer simulation," *IEEE Trans. Elec. Dev.*, **28**, 117, January 1981.

[21] G. Vanstraelen, I. Debusschere, C. Claeys, and G. Declerck, "Fully integrated CMOS pixel detector for high energy particles," *Nuclear Instrum. Methods in Physics Research A*, **275**, 574, March 1989.

[22] S.E. Holland, D.E. Groom, N.P. Palaio, R.J. Stover, and M. Wei, "Fully depleted, back-illuminated charge-coupled devices fabricated on high-resistivity silicon," *IEEE Trans. Elec. Dev.*, **50**, 225, 2003.

[23] B.E. Burke, J.A. Gregory, M.W. Bautz, G.Y. Prigozhin, S.E. Kissel, B.B. Kosicki, A.H. Loomis, and D.J. Young, "Soft-X-Ray CCD Imagers for AXAF," *IEEE Trans. Elec. Dev.*, **40**, 1633, 1997.

[24] Astronomical Research Cameras, Inc., San Diego, CA.