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Signal Conditioning Circuitry Design For Instrumentation Systems

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Abstract

This report details the current progress in the design, implementation, and validation of the signal conditioning circuitry used in a measurement instrumentation system.

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Nomenclature

ADC Analog-to-Digital Converter

DAC Digital-to-Analog Converter

PGA Programmable Gain Amplifier

FPBW Full Power BandWidth

MFB Multiple FeedBack

SK Sallen-Key

LPF Low-Pass Filter

CMRR Common-Mode Rejection Ratio

IRR Infinite Impulse Response.

Q or Q-Factor Quality Factor.

ksps kilo-samples per second.

SPI Serial-Programmable Interface.

DSP Digital Signal Processing.

Chapter 1

Signal Conditioning

1.1 Introduction

The purpose of this text is to document the current progress of a particular design in signal conditioning circuitry in an instrumentation system. The input of the signal conditioning circuitry comes from a piezoresistive transducer and the output will be fed to a 250 ksp/s, 12-bit analog-to-digital converter (ADC) with an input range of 0-5 V. It is assumed that the maximum differential voltage amplitude input from the sensor is 20 mV with an unknown, but presumably high, sensor bandwidth. This text focuses on a specific design; however, the theory is presented in such a way that this text can be used as a basis for future designs.

1.2 System Requirements

The specified system requirements were given as follows:

Passband Frequency:	0 to 50 kHz.
Sample Rate:	250 ksp/s.
Maximum Amplitude Distortion:	5%.
Maximum Phase Nonlinearity:	5°.
Aliasing Allowed in Transition Region:	Yes.
Voltage Supply:	5V, Rail-to-Rail, Single-Sided.
Gain:	1-128 binary, SPI programmable.
Offset Voltage:	0-5 V, SPI Programmable.
Max. Power Consumption:	21 mA.
Number of Channels:	4.
Component Area:	4.94 in ² .

Further discussion is required to fully understand the rationale for several of the requirements given. The 50 kHz passband frequency was determined to be the region in which the system produces frequency content of interest. The maximum amplitude distortion of 5% comes from limitations of the transducer. According to the data sheet of the transducer, it is

only guaranteed to be calibrated to within 5% of the actual value within the entire frequency range. The maximum phase nonlinearity of 5° is a rule of thumb value determined through discussions with Dr. Pat Walter of Texas Christian University in which, in his experience, distortion does not alter the signal shape significantly. The definition of phase nonlinearity for a second-order low-pass transducer model, such as the one being used, is given by the following set of equations [1]

$$\text{Initial Slope Line } (w) = \phi(0) + \left(\frac{d\phi(w)}{dw} \bigg|_{w=0} \right) w \quad (1.1)$$

$$\text{Phase Nonlinearity } (w) = \phi(w) - \text{Initial Slope Line } (w). \quad (1.2)$$

It is important to understand the 5% variation does NOT mean there will be a variation of 5% in the data recorded. This variation will only occur in the upper frequencies, as such the total wave-shape is distorted significantly less than 5%. The same argument applies to the 5° phase nonlinearity requirement.

In this application, aliasing is allowed into the filter's transition region, but not the passband region. This aliasing does not affect the signal because the transition region, where aliasing is allowed, will later be removed by applying a high order digital low-pass filter after digitization (Figure 1.1). It will be shown later that this requires an attenuation of 72 dB at 200 kHz. Minimal power consumption is desired as this device will be battery powered. The number of channels is four channels: Three data channels and one check channel. Check channels are important to determine the quality of the data recorded by ensuring the circuitry itself is not producing significant noise content. Finally, note that the board area is for a double sided board.

Figure 1.1. Allowed aliasing in transition region.

1.3 Analog Circuit Design

The following section discusses the considerations and assumptions used in designing the analog circuitry.

1.3.1 System Overview

The system topology for the signal conditioning circuitry is presented in Figure 1.2. A transducer provides the input signal, which is then buffered by an instrumentation amplifier. A (inverting) gain is provided to amplify the signal in order to provide full ADC resolution. Sampling aliasing is prevented through using an anti-aliasing, low-pass filter on the signal before it is sent to the ADC for digitization and storage. Upon retrieval from memory, the data is un-inverted, the offset voltage removed, and further filtered before the data is presented to the engineer for analysis. Each of the stages will be explained in further detail throughout this section and the next.

Figure 1.2. Analog system overview.

1.3.2 Transducer

In this application, a piezoresistive transducer is used with a Wheatstone bridge built-in to the transducers packaging. The output of the transducer circuit will be a differential signal with an assumed maximum amplitude of 20 mA and unknown frequency content. In addition, the transducer will present an input load of 650 ± 300 ohms to the following circuitry.

1.3.3 Instrumentation Amplifier

Prior to the instrumentation amplifier, the signal is first filtered using a single, shunt-capacitor pole. This passive pole is the first pole of seven of the 60 kHz Butterworth anti-aliasing filter and is implemented using a resistor-capacitor combination in a balanced C half-section topology (Refer to Appendix B and Figure 1.3). By placing this passive filter before the instrumentation amplifier, high frequency signals are attenuated — thereby preventing nonlinearities being introduced due to slew rate limitations in the instrumentation amplifier [2, 3]. A differential, instrumentation amplifier is then used on the signal to provide a high-impedance buffer and to remove unwanted common-mode noise in the signal [2]. Instrumentation amplifiers are desirable in this application due to their high DC precision, low op-amp noise, high common-mode rejection ratio, and a high input impedance which prevents a significant load being presented to the transducer [4]. In addition, the instrumentation amplifier can provide an early-stage gain to the signal.

The AD8224B instrumentation amplifier shown in Figure 1.3 was chosen for this design. A gain of approximately 5 (4.98387 ± 0.040241) is implemented to provide an initial gain stage. To determine whether this amplifier provides sufficient bandwidth under these conditions, the full-power bandwidth (FPBW) is calculated using (1.3) [4, 5, 6]. The slew rate (SR) of this amplifier is $2 \text{ V}/\mu\text{s}$ and the maximum output peak-to-peak voltage is assumed to be 100 mV (gain of 5 times 20 mV). Using these assumptions, the full-power bandwidth of the op-amp can be calculated

$$FPBW = \frac{SR}{2\pi V_p} = \frac{2 \text{ [V}/\mu\text{s}]}{2\pi \times 0.1 \text{ [V]}} \times \frac{10^6}{10^6} = 3.18 \text{ [MHz]}. \quad (1.3)$$

Since the initial real pole of the 60 kHz low-pass filter is placed before the instrumentation amplifier, any signals above 60 kHz will be greatly attenuated. Therefore it is concluded that even with conservative estimates slew rate limitations should not affect the instrumentation amplifier.

Figure 1.3. First filter pole and instrumentation amplifier.

Another important factor to consider is how the load of the transducer will effect the pole of the shunt capacitor filter. According to the data sheet of the transducer, it will provide an load of 650 ± 300 ohms. This means the initial pole will range from 54 to 57.5 kHz, instead of the designed value of 59.8 kHz. Figure 1.4 shows that this small variation in the initial pole has a minimal effect on the circuit performance.

Figure 1.4. Frequency response with additional 649 ohm source load.

1.3.4 Programmable Gain and Offset Voltage

Despite the gain provided by the instrumentation amplifier, additional gain is required in order to bring the signal within full scale range of the ADC. As per the design requirements, the additional gain must be SPI programmable to 1 through 128 in binary steps. The PGA112 programmable gain amplifier was chosen to accomplish this task. In addition, the PGA112 provides the advantage of being able to be calibrated with the ADC in order to reduce the gain and offset errors of the ADC (Refer the PGA112 data sheet for details). The gain will be programmed by the systems microcontroller prior to use and will not be adjusted during application. Note that the inputs of the op-amps used in the low-pass filter are limited to 4 V. Therefore, the PGA can only be used to bring the signal up to 4 V, with the filter providing the last gain of $\frac{5}{4}$ to achieve the full 5 V range of the ADC. The PGA112 circuit is shown in Figure 1.5 with the ideal total gain calculated as

$$\text{Gain} = 5 \times \text{PGA} \times 1.25. \quad (1.4)$$

In addition, the circuit contains an SPI programmable onboard digital-to-analog converter (DAC) to provide an offset voltage. An offset voltage allows for removal of the zero measurand offset voltage or adjusting the data range to better fit the application. The transducer being used has a maximum zero measurand offset of ± 100 mV. The device chosen for this design was the 14-bit AD5641. With an input range of 0-5 V, the DAC should be programmable to a resolution of $305.176 \mu\text{V}$. A buffer amplifier is used on the output to ensure

Figure 1.5. Programmable gain circuit.

the correct voltage being driven to each device. The voltage offset circuitry is presented in Figure 1.6.

Figure 1.6. Programmable voltage offset circuitry.

An advantage of including a programmable gain and offset into the system is to allow the system to be used in multiple applications without modification. In addition, it allows for recalibration of the device if the transducer has a zero measurand shift during use or due to environmental conditions.

1.3.5 Low-Pass, Anti-Aliasing Filter

In this design, it was deemed acceptable (and necessary to meet the 50 kHz passband frequency) to allow aliasing into the filters transition region since the data would be stored and later digitally filtered. To prevent any aliasing, an ADC requires a minimum of 6 dB attenuation per bit at the Nyquist frequency [7, 2]. A 12-bit ADC thus requires 72 dB attenuation. When allowing aliasing into the filter's transition region, the 72 dB attenuation is required at the sampling frequency minus the highest non-aliased frequency desired. For this design, the highest non-aliased frequency desired is 50 kHz with a sampling rate of 250 kHz, thus requiring 72 dB of attenuation at 200 kHz. The minimum filter order can be determined using the following equation [7, 2].

$$M \geq \frac{3N}{10 \log_{10} \left(\frac{f_s}{f_c} \right)} = \frac{3 \times 12}{10 \log_{10} \left(\frac{250k}{50k} \right)} \Rightarrow M \geq 6 \quad (1.5)$$

where M is the minimum filter order required, $N = 12$ is the number of bits in the ADC, $f_s = 250$ kHz is the sampling frequency, and $f_c = 50$ kHz is the passband frequency. Thus, allowing

aliasing in this system down to 50 kHz, a minimum filter order of six is required. As discussed in Section 1.3.3, an additional passive filter pole was added before the instrumentation amplifier to prevent distortion from slew rate limitations of the instrumentation amplifier. Therefore, the resulting filter in this design has a total of seven poles. Higher order filters are undesirable due to space and power constraints, in addition to decreased stability that often occurs in higher order filters. After performing a comparison among Bessel, Butterworth, and Transitional implementations, it was found that a Butterworth filter was more effective in achieving the design requirements (see Appendix A). After an in depth analysis, it was determined that a seven pole, 60 kHz corner frequency (-3dB point) Butterworth filter is needed to allow for less than 5% magnitude attenuation to over 50 kHz and less than 5°s of nonlinear phase over 30 kHz, meanwhile providing over 72 dB of attenuation at 200 kHz. Phase compensator filters are being investigated (see Section 1.5) which can extend the range in which the phase is linear.

The seventh-order, low-pass, analog Butterworth IIR filter used in this design has a transfer function of the following form:

$$G(s) = \frac{b_7}{a_0s^7 + a_1s^6 + a_2s^5 + a_3s^4 + a_4s^3 + a_5s^2 + a_6s + a_7}. \quad (1.6)$$

The filter coefficients are easily solved for using the `butter` function contained in the Signal Processing Toolbox in MATLAB with the values presented in Table 1.1 to fifteen decimal places.

Table 1.1. Butterworth filter coefficients.

b_0 :	0	a_0 :	1
b_1 :	0	a_1 :	1.694182707793176e+006
b_2 :	0	a_2 :	1.435127523692709e+012
b_3 :	0	a_3 :	7.818114790185271e+017
b_4 :	0	a_4 :	2.947359838772130e+023
b_5 :	0	a_5 :	7.689247673091203e+028
b_6 :	0	a_6 :	1.290077611462991e+034
b_7 :	1.082225670413983	a_7 :	1.082225670413983e+039

The free Texas Instruments FilterPro Desktop tool [5] was used to aid in choosing components after a filter design was selected. The amplifier stages are ordered in increasing Q to avoid peaking due to high Q sections potentially overloading the following op-amps.

Both the multiple feedback (MFB) and Sallen-Key (SK) filter topologies were considered. Advantages of the MFB topology is a low sensitivity to component variations, excellent stop band rejection, simplicity in adding gain to the last stage [8, 9]. A disadvantage is that MFB topologies with an odd number of stages will invert the signal; however, in this application the data can be corrected digitally upon retrieval. The Sallen-Key topology has the advantage of being non-inverting, has least dependance on the amplifier characteristics, and should only

be selected when gain accuracy is important, in unity-gain configuration, and pole-pair Q is low ($Q < 3$) [10, 5]. The disadvantages of the Sallen-Key configuration is that it does not provide as much high frequency attenuation and it is sensitive to component variations. The Sallen-Key uses less resistors, however this advantage is nullified when using single-side supplies due to the resistors required to properly bias the circuit.

The gain bandwidth required for each filter type is debatable. According to [8], the SK may require less gain bandwidth product than the MFB Implementation. However, the gain bandwidth calculations for MFB (1.7) and for SK (1.8, 1.9) given by [5, 6] indicate that the MFB topology requires less gain-bandwidth (for information on calculating the Q of an MFB filter, refer to [10]). The gain bandwidth (GBW) required for the MFB topology is

$$GBW_{MFB} \geq 100 \times \text{Gain} \times Q \times f_n, \quad (1.7)$$

and for the SK topology

$$GBW_{SK} \geq 100 \times \text{Gain} \times Q^3 \times f_n, Q > 1, \quad (1.8)$$

$$GBW_{SK} \geq 100 \times \text{Gain} \times f_n, Q \leq 1. \quad (1.9)$$

The MFB topology was chosen for this design mainly due to its insensitivity to component variations, increased high frequency attenuation, and the need for implementing a gain in the last stage. Although it is possible to combine stages from different topologies, this was not considered advantageous here. The final filter design can be seen in Figure 1.8.

The OP462 op-amp was chosen for the filter's internal op-amps. Due to the high gain previously in the circuit, slew rate concerns must again be evaluated. The OP462 op-amps have a slew rate of $10 \text{ V}/\mu\text{s}$. Using (1.3), with a max peak-to-peak voltage of 5 V , the FFBW of the OP462 is over 397 kHz . Since values over 60 kHz have already been attenuated, and will continue to be attenuated further, it can be safely concluded that slew rate limitations will not be a problem in this circuit. It is important to note that the input to the OP462 op-amps are limited to 4 V , therefore the last filter stage provides a gain of 1.25 (1.25532 ± 0.024981) to provide the full 5 V ADC input range. The ideal frequency response of the filter can be seen in Figure 1.13.

A single, passive RC pole placed after the filter is used to bandlimit the noise of the op-amps. Depending on the ADC type, this circuit may present an adverse load to the ADC [8]. However, in this application, the Texas Instruments ADS7865 successive-approximation register (SAR) ADC is used. For SAR ADC's, the RC pole can bandlimit op-amp noise and the input of the ADC, isolates filter op-amps from the dynamic load presented by the ADC, and minimizes the effects of the internal ADC capacitors [11, 12, 13, 14]. However, several important timing considerations must take place to ensure the acquisition time required to charge the ADC's input capacitor is less than one-half a significant bit. According to the data sheet, the corner frequency of the input filter can be calculated by

$$f_{FILTER} = \frac{\ln(2) \times (n + 1)}{2 \times \pi \times R \times C} \quad (1.10)$$

where n is the number of ADC bits, and R and C are the external input components. The data sheet also specifies C must be greater than 20 pF and

$$R \leq \frac{t_{acq}}{\ln(2) \times (n + 1) \times C}. \quad (1.11)$$

Derivations of (1.10) and (1.11) can be found elsewhere [12].

Upon evaluation of the filter (refer to Section 1.6), it was found that capacitance feed-through on the op-amps created a deviation from the theory and resulted in insufficient attenuation to prevent aliasing in the passband region [15]. The value of the final RC pole was changed to create a pole at 135 kHz to provide the required additional attenuation. In moving the pole down to 135 kHz, the condition in (1.11) is not satisfied. A trade-off is required, however further investigation is needed.

1.3.6 Passive Component Selection

Several considerations must be taken into account when choosing passive components for filters. Besides wanting minimal variation in components (less than 1% was selected when possible), it is desired to minimize variations due to environmental effects. Since a piezo-electric transducer is being used, capacitors that have minimal piezo-electric effects must be chosen. In addition, components with minimal temperature coefficients are desirable. When possible, C0G capacitors are desirable as they have a minimal temperature coefficient are known to have minimal piezo-electric effects, unlike other ceramic capacitor types such as X7R and Y5V. For higher value capacitors unavailable in C0G, tantalum is desired [16].

1.3.7 Analog Design Summary

The final designed values for the ideal analog signal conditioning circuitry are listed below in Table 1.2. Figures 1.7 and 1.8 present the signal conditioning circuitry per channel and the Butterworth filter circuit, respectively.

Figure 1.7. Signal conditioning per channel.

Figure 1.8. 60 kHz Butterworth anti-aliasing filter.

Table 1.2. Analog signal conditioning design summary.

Property:	Value
Filter Type:	Active Low-Pass
Design Methodology:	Butterworth
Filter Order:	7
Number of Stages:	4
-3dB Attenuation:	60 kHz
5% Attenuation:	50 kHz
5° Phase Nonlinearity:	30 kHz
-72 dB Attenuation:	200 kHz
Filter Topology:	MFB
Min. Gain:	6.25
Max. Gain:	800
Gain Step:	Binary
Offset Voltage Range:	0-5V
Offset Voltage Resolution:	305.2 μ V
Max. Q-Factor:	2.25

1.4 Digital Post-Processing

After the data is retrieved from the onboard storage it is post-processed before being presented for analysis. Two post-processing steps are required: 1) Un-inverting the signal and removing the bias voltage introduced in the analog circuitry and 2) Digital low-pass filtering. A third step of digital phase compensation can be included to linearize the phase in the passband in order to minimize phase distortion at higher frequencies. An overview of the digital processing is presented in Figure 1.9 and each step will now be discussed.

Figure 1.9. Digital post-processing system overview.

1.4.1 Digital Low-Pass Filtering

Digital low-pass filtering is an essential step to remove the allowed aliasing in the transition region within the analog circuitry. Digital filters provide the advantage of sharper roll-off and increased stability over analog filters. In addition, since the processing is not done in real time, a non-causal, zero-phase digital low-pass filter can be used. This filter does not affect the phase of the system because it runs the data through forward and in reverse-time, however the amplitude effects from the filter are doubled [2]. A digital, low-pass Butterworth filter can be designed in MATLAB using the `butter` command and applied to the data using the `filtfilt` command, both of which are contained in the Signal Processing Toolbox.

1.4.2 Reducing Digital Distortion Effects

As with any filtering operation, digital filtering can introduce unwanted distortions if proper care is not taken in applying the filter. Of largest concern is digital filter startup effects which create distortions on the edges of the filtered data. Startup effects can be minimized by zero-padding the data by at least $\frac{1}{f_c}$ seconds on both sides, where f_c is the cutoff frequency of the filter [17, 2].

1.5 Phase Compensation Filters

Phase compensation filters are used on existing filters that have an acceptable magnitude response but a less than desirable phase response. Benefits of increased time domain response comes with the disadvantages of additional required design, increased complexity in implementation due to higher transfer function order of the system, and increased signal delay [18]. Phase compensation, also known as group delay equalization, is commonly used in telecommunication systems to remove distortion caused by unequal group delay. Group delay is another often used method of measuring the linearity of the phase response. The group delay is defined as

$$\tau_g = -\frac{d\phi}{dw}. \quad (1.12)$$

Since the group delay is the slope of the phase, a constant group delay indicates the system is linear phase. Group delay equalization techniques use all-pass filters to linearize the phase without affecting the amplitude [19, 20, 2].

The design objective of the following phase compensation filters is to linearize the phase of the Butterworth filter described in Section 1.3.5 to meet the less than 5° phase nonlinearity requirement for the entire 50 kHz range. Both analog and digital phase compensation filters are being investigated, with the design for each described in the following sections.

1.5.1 Analog Phase Compensation Filter

An evaluation of first- and second-order phase compensation filters is presented in Appendix C, with the first-order filter determined as the better option in this application. This compensation filter can theoretically extend the frequencies containing less than 5° nonlinearity over the desired 50 kHz range. The filter implementation is shown in Figure 1.10 and the simulated system response is shown in Figure 1.11. Further validation of the design will be performed before being implemented in the final system.

Figure 1.10. Analog, first-order phase compensation filter.

1.5.2 Digital Phase Compensation Filter

Digital post-processing methods, such as deconvolution techniques, have been shown to reduce distortion in measurement system applications [21, 2]. In this application, a digital filter is used to compensate for the nonlinear phase of the Butterworth filter. Using the `iirgrpdelay` function in the MATLAB DSP Systems Toolbox, a group delay equalization filter can be easily constructed. The compensator filter designed for this application is a fourth-order digital all-pass filter

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4}}{a_0 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + a_4 z^{-4}}, \quad (1.13)$$

where the coefficient values calculated using the `iirgrpdelay` function are given to fifteen decimal places in Table 1.3.

Figure 1.11. Analog, first-order phase compensation filter response.

Table 1.3. Phase compensation filter coefficients

b_0 :	0.161903055732724	a_0 :	1.0000000000000000
b_1 :	-0.930904063315975	a_1 :	-2.299189244552675
b_2 :	2.126510036540996	a_2 :	2.126510036540996
b_3 :	-2.299189244552675	a_3 :	-0.930904063315975
b_4 :	1.0000000000000000	a_4 :	0.161903055732724

The results of applying the compensating filter to the response is presented in Figure 1.12. In this application, only wave shape is a concern, therefore it is irrelevant that the total group delay of the system increases and therefore the offsets have been removed to ease comparison between the two signals. In Figure 1.12, the blue line is the response of the analog circuitry and the red line is the response of the analog circuitry post-processed by the digital compensator filter. Further work is needed to characterize the practical applicability of digital phase compensation to the current application.

Figure 1.12. Theoretical digital compensation results.

1.6 Performance Analysis

The performance of the signal conditioning system in this section does not include the phase compensation filters discussed in Section 1.5. The frequency response of the theoretical system and the measured system can be compared in Figure 1.13. Due to capacitance feed-through in the op-amps, the filter is not able to give sufficient attenuation of 72 dB at 200 kHz. To fix this problem, the post-filter RC pole was moved to 135 kHz to provide the extra attenuation required [15]. Note that after adding an additional RC pole of 135 kHz the circuit provides the needed 72 dB attenuation at 200 kHz.

In addition, the step pulse response of the system is presented in Figure 1.14 to portray the time domain distortions that may occur as simulated using MATLAB. The red line indicates the input signal, the blue line the result after applying the analog anti-aliasing filter, the maroon line shows the results after being sampled and digitized (scaled), and the

Figure 1.13. Theoretical vs. measured frequency response.

cyan line shows the effect of digitally post-processing the data. As a real world signal will not have the nonlinearities of the step response shown, this represents an upper limit to how the signal may be distorted.

Figure 1.14. Simulated system step response.

1.6.1 Two Channel Prototype Board Results

Below is a list of the measurement results from testing a two channel prototype board. The following results were obtained using a power supply of 5 V, a bias voltage of 2.5 V and at room temperature.

Supply Current: .

Shutdown = 5 mA

Typical = 6-7 mA

Max. = 15 mA

Passband 5% Magnitude Drop: 55 kHz

-3 dB Frequency: 60 kHz

-72 dB Frequency: 250 kHz

-72 dB Frequency (w/ 135 kHz RC Pole): 190 kHz

1.7 Conclusions and Future Work

Throughout this document, the design of signal conditioning circuitry for an instrumentation application is presented. The system proposed meets all the specified requirements, however further validation of phase compensation filters in this application will need to be evaluated.

In addition, further investigation is required to ensure proper interfacing with the ADC and noise characteristics of the filter will be evaluated. Finally, a full-channel, form factor board will be developed and analyzed before being included into the final system.

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Appendix A

Comparison of Filter Types

Three filter types were evaluated and considered in the selection of the filter: Bessel, Butterworth, and Transitional low-pass filters [18]. Bessel filters are desirable for their linear phase characteristic in the passband; however, they have the worst amplitude response of all. Butterworth filters have a flat magnitude response in the passband, but are not linear phase. Butterworth filters are generally provide a good compromise between amplitude and phase responses. Finally, using a transitional filter, created by cascaded sections of both Butterworth and Bessel filters, was evaluated. Transitional filters are so called because they give a response that is in between the two filter types [18]. Each filter type was designed as a 7-pole low-pass filter. Aliasing was allowed, up to 50 kHz or the highest non-distorted frequency, whichever was less. At the stopband frequency, 72 dB attenuation was required. The filters were designed in MATLAB and the filter design that meets the requirements given closest for each type is given in Table A.1. The transitional filter that had the best result used a two-pole Bessel and a five-pole Butterworth. Figure A.1 presents the frequency response, group delays, and phase nonlinearity of each filter type. In the figures, red is the Bessel filter, blue is the Butterworth, and green is the transitional filter's response. Also note that for the Butterworth filter, the corner frequency is defined as the -3dB or half-power point. For the Bessel filter, the corner frequency is the frequency up to which the phase response is remains linear. The filters were implemented in MATLAB using the `butter` (with the analog 's' option), `besself`, and using the `conv` function to cascade the two sections in the Transitional filter.

Table A.1. Bessel, Butterworth, and Transitional Filter Comparisons

Filter Type	Bessel	Butterworth	Transitional
Corner Frequency (kHz)	72.4	60	84.5 (Bes) / 64 (BW)
5% Mag. Attn. Freq. (kHz)	15.1	51.21	25.88
5° Nonlin. Phase Freq. (kHz)	78.71	31.4	36.3
Stopband Freq. (kHz)	234.9	200	224.1
Stopband Attenuation (dB)	-72	-73.2	-72.04

From this analysis, it was concluded that the Butterworth filter was the best design for the current application. The Bessel filter was unable to meet even the minimum requirements

Figure A.1. Filter response comparisons.

of 20 kHz. Note that if we allowed aliasing down to the 5 degree nonlinearity requirement, we could potentially move the corner frequency of the Butterworth filter to 65.5 kHz, allowing us a 5 degree phase nonlinearity up to 34 kHz. This was not implemented because 1) It was a small and barely significant increase and 2) phase compensation methods of linearizing the response of the Butterworth filter are being investigated which may allow better results.

Appendix B

Design Reference - Filter C-Half Section

The balanced, C-half section topology is shown in Figure B.1 [22]. The pole of this filter stage is calculated as follows

$$f = \frac{1}{2\pi ZY}. \quad (\text{B.1})$$

Figure B.1. C half-section topology.

Appendix C

All-Pass Analog Phase Compensation Filter Design

The analog phase compensation filters investigated in this text are limited to first and second order all-pass filters. The first order filter has the transfer function

$$H(s) = \frac{s - a}{s + b}, \quad (\text{C.1})$$

where $a = b = \frac{1}{RC}$. The second order filter has the transfer function

$$H(s) = \frac{s^2 - s(\frac{\omega_0}{Q}) + \omega_0^2}{s^2 + s(\frac{\omega_0}{Q}) + \omega_0^2}, \quad (\text{C.2})$$

where $\omega_0 = 2\pi f_0$ and Q are the frequency where the phase shift is 90 degrees (i.e. the input-to-output quadrature) and the quality factor, respectively [18, 8]. One method for choosing the design values include finding the Taylor Expansion of the group delays of both the anti-aliasing filter and the compensation filter, adding them together in order to solve for the design parameters of the compensation filter that linearizes the phase [23]. A pseudo-code example of this technique using the open-source Maxima algebra system software is shown in Figure C.1.

The design values derived in Maxima were then manually optimized for this application. The resulting design values for the unity-gain, first-order all-pass are $R = 21.5 \text{ k}\Omega$ and $C = 150 \text{ pF}$ placing the pole at 50 kHz. The second-order values were $f_0 = 46 \text{ kHz}$ and $Q = \sqrt{\frac{1}{3}}$ with a filter gain of $0.25 \frac{\text{V}}{\text{V}}$. Using MATLAB to simulate the system, Table C.1 lists the effects of adding ideal first- and second-order all-pass compensator to the seven-pole Butterworth filter design. It is apparent from Table C.1 that the all-pass filter sufficiently linearizes the phase of the anti-aliasing filter to meet the specified design requirements.

Since the specified design requirements could be met using a first-order all-pass pole, and the increased complications of the second-order filter (non-unity gain of $0.25 \frac{\text{V}}{\text{V}}$), the single-pole filter was chosen for further investigation. For more information on the design and physical implementation of an all-pass equalizer filter, refer to [8, 23, 18].

```

{Define Coefficients values (b8,a1-a8)}
\\ 7-pole Butterworth Group Delay Derivation
s : %i*w;
G : b7 / ( a1*s^7 + a2*s^6 + a3*s^5 + a4*s^4 + a5*s^3 + a6*s^2 + a7*s + a8 );
Tg : float(ratsimp(diff(atan2(imagpart(G),realpart(G)),w,1)));
T_Tg : float(taylor(Tg,w,0,4));

\\ First order All-Pass Group Delay Derivation
H : ( s - 1/(R*C) ) / ( s + 1/(R*C) );
Th : ratsimp(diff(atan2(imagpart(H),realpart(H)),w,1));
T_Th : taylor(Th,w,0,4);
\\ Add Taylor Expansion of Group Delay Derivations to solve for filter values
Tf : T_Tg+T_Th;
algsys([ {insert w^2 coefficient here} = 0 ], [R,C]);

\\ Second order Butterworth Group Delay Derivation
H : ( (s/wo)^2 - 1/Q * (s/wo) + 1 ) / ( (s/wo)^2 + (1/Q)*(s/wo) + 1 );
Th : ratsimp(diff(atan2(imagpart(H),realpart(H)),w,1));
T_Th : taylor(Th,w,0,4);
\\ Add Taylor Expansion to solve for second-order filter values
Tf : T_Tg+T_Th;
algsys([ {insert w^2 coefficient here} = 0,
        {insert w^4 coefficient here} ], [wo,Q]);

```

Figure C.1. Maxima pseudo-code for deriving first and second order all-pass filter values.

Table C.1. Effects of analog compensator filter applied to a 7-pole, low-pass Butterworth filter.

AP Filter Order	5° Phase Nonlinearity
0	31.3 kHz
1	51.9 kHz
2	52.3 kHz

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