Xyce™ Parallel Electronic Simulator Release Notes

Release 5.1.2

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Sandia National Laboratories

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Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

■ Hardware and software requirements

■ New features and enhancements

■ Any defects fixed since the last release

■ Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at http://www.cs.sandia.gov/xyce.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 5.1.2.

Supported Platforms (Certified Support)

Xyce 5.1.2 currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms. These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 5.1.2 release.

■ Red Hat Enterprise Linux® 4 or 5, x86 and x86-64 (serial and parallel)

■ Microsoft Windows XP Professional®, x86 (serial)

■ Apple® OS X, x86-64 (serial and parallel)

■ TLCC (glory) (serial and parallel)

■ Xyce directly coupled to the Dakota optimization and uncertainty quantification library for Apple OS X and Linux platforms.

Build Supported Platforms (not Certified)

The platforms listed in this section are "not supported" in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 5.1.2 release.

■ FreeBSD 7.2 on Intel x86 architectures (serial and parallel)

Please contact the Xyce development team for platform and configuration availability.

Hardware Requirements

The following are *estimated* hardware requirements for running **Xyce**:

- 128MB memory memory minimum – *memory requirements increase with circuit size*

- 128MB disk space required for installation (does not include space needed for output files)

Software Requirements

Several libraries are required to run **Xyce** or build **Xyce** from source on a platform. Serial versions of the static **Xyce** binary have no run-time software requirements. However, parallel versions require the following software at run time:

- Open MPI (http://www.open-mpi.org/) (version 1.2.5 or higher)

- Intel (http://www.intel.com/) MKL (version 10.0) and Compilers (version 10.1)

- TLCC (glory) users can load the **xyce** module to properly set the environment

Several libraries (all freely available from Sandia National Laboratories or other sites) are always required when building **Xyce** from source. These are:

- Trilinos Solver Library version 10 (Sandia, http://trilinos.sandia.gov) . This is a suite of libraries including Amesos, AztecOO, Belos, Teuchos, Epetra, EpetraExt, Ifpack, NOX, LOCA, Sacado, Zoltan.

- SuperLU (libsuperlu.a) (http://crd.lbl.gov/ xiaoye/SuperLU/)

- UMFPACK version 4.1 and AMD version 1.0 (libumfpack.a, libamd.a) (http://www.cise.ufl.edu/research/sparse/umfpack/)

- LAPACK (liblapack.a).

- BLAS (libblas.a).

For parallel builds, the following libraries are additionally required:

- MPI (http://www.open-mpi.org) library for message passing (version 1.1 or higher). The version used to build Xyce must be the same that is used for building Trilinos.

- ParMETIS (http://glaros.dtc.umn.edu/gkhome/views/metis) library for graph partitioning (version 3.1 or higher). The MPI compiler used to compile ParMETIS must be the same that is used for Trilinos and Xyce.

Xyce Release 5.1.2 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form.

- **Xyce** Users' Guide, Version 5.1.2

- **Xyce** Reference Guide, Version 5.1.2

- **Xyce** Release Notes, Version 5.1.2

- **Xyce** Theory Document

- **Xyce** Test Plan

New Features and Enhancements

Xyce Release 5.1.2 is a minor release building on release 5.1.1.

Highlights for this release include:

- Update to the stand-alone neutron model, to better model the transition from saturation mode to forward-active mode.

- New reduced-order model (ROM) device that enables reintegration of linear ROMs into circuits.

- Significant improvements to the Vertical Bipolar Intercompany Model (VBIC).

- New preprocessing features for effectively handling supernoding and R=0 resistors.

For details of each of these new features, see the **Xyce** Users' Guide, and the **Xyce** Reference Guide. Also, a more complete listing of new features and improvements are given in the following sections.

Device Support

Table 1 contains a complete list of devices for **Xyce** Release 5.1.2.

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible) Stability improvements
Resistor (Level 1)	Semiconductor

Device	Comments
Resistor (Level 2)	Thermal Resistor
Diode (Level 1)	
Diode (Level 2)	Addition of PSPICE enhancements
Diode (Level 3)	Prompt and delayed photocurrent radiation model
Diode (Level 4)	Generic photocurrent source model
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Current Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 2)	Prompt photocurrent radiation model
Bipolar Junction Transistor (BJT) (Level 3)	Neutron-effects model
Bipolar Junction Transistor (BJT) (Level 4)	Prompt photocurrent radiation model (same as level 2)
Bipolar Junction Transistor (BJT) (Level 5)	Deveney-Wrobel Neutron model, with photocurrent
Bipolar Junction Transistor (BJT) (Level 6)	Physics-based (QASPR) Neutron model, with photocurrent
Bipolar Junction Transistor (BJT) (Level 10)	Vertical Bipolar Intercompany (VBIC) model **Updated!**
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model
Junction Field Effect Transistor (JFET) (Level 2)	Shockley JFET model
MESFET	
MOSFET (Level 1)	
MOSFET (Level 2)	Spice level 2 MOSFET

Device	Comments
MOSFET (Level 3)	
MOSFET (Level 6)	Spice level 6 MOSFET
MOSFET (Level 9)	BSIM3 model with initial condition support
MOSFET (Level 10)	BSIM SOI model with initial condition support
MOSFET (Level 11)	BSIM SOI model with Transient Photocurrent
MOSFET (Level 12)	BSIM SOI model with Transient Photocurrent
MOSFET (Level 14)	BSIM4 model
MOSFET (Level 18)	VDMOS general model
MOSFET (Level 19)	VDMOS total dose radiation model
MOSFET (Level 20)	VDMOS photocurrent model
MOSFET (Level 21)	Level 1 with photocurrent
MOSFET (Level 23)	Level 3 with photocurrent
Transmission Line	Lossless
Controlled Switch (S,W) (VSWITCH/ISWITCH)	Voltage or current controlled
Generic Switch (SW)	Controlled by an expression
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional
Digital (Level 1)	Behavioral Digital
EXT (Level 1)	External device, used for code coupling and power-node parasitics simulations
OP AMP (Level 1)	Ideal operational amplifier
ACC	Accelerated mass device, used for simulation of electromechanical and magnetically-driven machines
NEUTRON (Level 1)	Stand-alone neutron device model **Updated!**
ROM (Level 1)	Reduced-order model device for linear (RLC) circuits **New!**

Table 1: Devices Supported by Xyce

New Devices

■ There is one new device in Xyce version 5.1.2, a reduced-order model (ROM) device for linear (RLC) circuits. The ROM device for linear (RLC) circuits is an implementation of the macromodel integration presented for the Passive Reduced-order Interconnect Macromodeling Algorithm (PRIMA). The macromodel is generated external to Xyce at this time and read in during the simulation. The new ROM device in **Xyce** should be considered a trial (beta) version.

■ This release provides improvements to the Vertical Bipolar Intercompany Model (VBIC), which was released for the first time in Xyce release 5.1. Release 5.1.2 improves the support for the VBIC model by adding convergence-assisting junction voltage limiting to the implementation.

The VBIC is a bipolar junction transistor (BJT) model that was developed as a public domain replacement for the SPICE Gummel-Poon (SGP) model. VBIC is designed to be as similar as possible to the SGP model, yet overcomes its major deficiencies. VBIC improvements on the SGP model include:

  – improved Early effect modeling

  – quasi-saturation modeling

  – parasitic substrate transistor modeling

  – parasitic fixed (oxide) capacitance modeling

  – avalanche multiplication model

  – improved temperature modeling

  – base current is decoupled from collector current

  – electrothermal modeling

  – improved smoothness in the model.

The new VBIC implementation in **Xyce** should be considered a trial (beta) version.

■ The stand-alone neutron model (Neutron level 1), while not a new model, has been substantially updated for Xyce release 5.1.2. The updates primarily affect the transition from saturation mode to forward active mode. The base-collector carrier model is now more accurate on the base side of the junction.

Interface Improvements

■ Updates to the Habanero API, to support linking **Xyce** to ModelSim.

■ When **Xyce** encounters a resistor with zero resistance in a netlist, Xyce can now remove that device from the circuit to avoid numerical complications that could abort the simulation. When a resistor with zero resistance is removed the remaining nodes are combined or super-noded into one node. Any other devices that are now connected to just one node are then removed automatically. This new capability is off by default, but can be activated by adding `.options topology supernode=true` to your netlist. See the **Xyce** Users' Guide, and the **Xyce** Reference Guide for more information.

Defects of Release 5.1 Fixed in this Release

Defect	Description
bug 105, 171: Improve handling of Time Step Too Small Errors	Typically, Xyce's non-linear solver will find a solution for the next time step, but the time integrator will reject that step because an estimated error is too high. Now Xyce can be instructed to take a fixed number of steps where the non-linear solver passes, but the error control in the time integrator fails. An example use of this option is `.options timeint mintimesteprecovery=10` where Xyce will attempt 10 such steps before giving up.
bug 177: Modify resistor device to handle R=0 correctly	Xyce can now remove such resistors from a circuit and combine or supernode, the remaining nodes. Any other devices that are left connected to only one node after supernoding are then also removed. This new capability is off by default, but can be activated by adding `.options topology supernode=true` to your netlist.
bug 1602: VBIC model incorrectly handling TNOM parameter	Xyce was improperly converting the TNOM value specified by the user in Celsius to Kelvin, and the VBIC model was expecting the value in Celsius. This was fixed in release 5.1.2.
bugs 1774, 1775, and 1776: incorrect handling of initial guess during nested DC sweeps	These long-standing issues rarely caused failures in existing devices, but were the reason that certain steps in nested DC sweep over VBIC models were failing. All three have been fixed, and Xyce is now correctly resetting its initial guesses at apporpriate times during a nested DC sweep.
bug 1770: Add convergence enhancements to VBIC	Prior to release 5.1.2, the VBIC model attempted no junction-voltage limiting. This meant that running any realistic VBIC model generally required homotopy approaches to get convergence. In this release, VBIC transistors use the same sort of voltage limiting as the standard SPICE BJT to aid convergence. It is now possible to use this model in more realistic circuits without resorting to GMIN stepping.
bug 1626: BSIM4 `.IC` and `.NODESET` not working	Attempting to set initial conditions on a BSIM4 transistor with `.IC` or `.NODESET` was broken until Release 5.1.2. This has been fixed.
bug 1765: **Xyce** crashes when using semiconductor capacitor	The voltage-dependent capacitor feature introduced in version 5.1.1 of Xyce introduced a bug that led to crashes of Xyce if the semiconductor capacitor was used. This has been fixed in Release 5.1.2.

Table 2: Fixed Defects.

Known Defects and Workarounds

Defect	Description
Connectivity checking is broken for devices with more than 10 leads [SON Bug 37]	The diagnostic code used by the **Xyce** setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, "Internal: lead index not found" after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If you see the error message "Internal: lead index not found." and you have such a large mutual inductor, this bug is the source of the problem. *Workaround:* Disable connectivity checking by adding the line `.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0` to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.
`.DC` sweep output.	`.DC` sweep calculation does not automatically output sweep results. *Workaround:* Use `.PRINT` statement to output sweep variable results.
BJT Current Crowding	"Timestep too small" failures can result when IRB nonzero with level 2 and level 4 BJT *Workaround:* If such failure observed, disable current crowding effect by setting IRB to zero in all BJT models. Please feed back such circuits to the **Xyce** development team so that this bug can be characterized and eliminated.
Microsoft Windows installation restrictions	Users with insufficient privileges (i.e. `Limited Account`) are not permitted to install **Xyce** into folders on the System Drive (usually `C:`). *Workaround:* First, manually create the desired folder on the System Drive. It is then possible to install **Xyce** into this folder by following the standard Setup procedure.

Defect	Description
Incompatible proprietary file formats.	Netlists created with programs like Microsoft Word and Microsoft Wordpad will not run in **Xyce**. **Xyce** does not recognize proprietary file formats. *Workaround:* It is best not to use such programs to create netlists, unless netlists are saved as *.txt files. If you must use a Microsoft editor, it is better to use Microsoft Notepad. In general, the best solution is to use a Unix-style editor, such as Vi, Gvim, or Emacs.
One known instance of restart results not matching original run results.	There is one case for a customer's parallel run of a large digital circuit of BSIM3's where the restart output does not match the original results for the same time range. *Workaround:* The only choice for now is to check the restart results against the baseline results for some block if the run results have a very tight tolerance for success. It is suggested to overlap the original run time with the restart time allowing comparison.
Infinite-slope transitions in B-sources causes "time step too small" errors [bug 772]	The nonlinear dependent source ("B-source") allows the user to specify expressions that could have infinite-slope transitions, such as `Bcrtl OUTA 0 V={ IF( (V(IN) > 3.5), 5, 0 ) }` This can lead to "timestep too small" errors when **Xyce** reaches the transition point. Infinite-slope transitions in expressions dependent only on the `time` variable are a special case, because **Xyce** can detect that they are going to happen in the future and set a "breakpoint" to capture them. Infinite-slope transitions depending on other solution variables cannot be predicted in advance, and cause the time integrator to scale back the timestep repeatedly in an attempt to capture the feature until the timestep is too small to continue. *Workaround:* Do not use step-function or other infinite-slope transitions dependent on variables other than `time`. Smooth the transition so that it is more easily integrated through.

Defect	Description

Epetraext uses bad address in parallel, causing **Xyce** core dump [bug 1072]	If **Xyce** is run in parallel on a netlist that is so small that all devices are assigned to the same processor, **Xyce** can core dump when the processor with no work attempts to access invalid memory. *Workaround:* It is best not to try to run **Xyce** on very small problems in parallel, as this capability is intended for and optimzed for very large problems; small problems should be run in serial. If trying to run medium-sized problems in parallel and these core dumps are observed, try running with Zoltan partitioning and singleton removal turned off:
	
	`.OPTIONS LINSOL TR_partition=0`
	`+ TR_singleton_filter=0`

Table 3: Known Defects and Workarounds.

Incompatibilities With Other Circuit Simulators

Issue	Comment
AC Analysis not supported	**Xyce** does not currently support AC analysis.
.OP is not complete	A .OP netlist will run in **Xyce**, but will not produce the extra output normally associated with the .OP statement.
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the .TRAN line.
Mutual Inductor Model.	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
.PRINT line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work. Also, specifying V(*) or I(*) (to get all voltages or currents) will not work.
BSIM3 level.	In **Xyce** the BSIM3 level=9. Other simulators have different levels for the BSIM3.
BSIM SOI v3.2 level.	In **Xyce** the BSIM SOI (v3.2) level=10. Other simulators have different levels for the BSIM SOI.
Node names vs. device names.	Currently, circuit nodes and devices MUST have different names in **Xyce**. Some simulators can handle a device and a node with the same name, but **Xyce** cannot.
Interactive mode.	**Xyce** does not have an interactive mode.
ChileSPICE-specific "operating point voltage sources."	These are not currently supported within **Xyce**. *However...* **Xyce** does support "IC=<value>" statements for capacitors, inductors, and the two BSIM devices which will automatically set these voltage drops at the beginning of a transient simulation.
Syntax for .STEP is different.	The manner of specifying a model parameter to be swept is slightly different. Also, it is not possible to do a .STEP sweep over a global parameter. See the Users' and Reference Guides for details.

Table 4: Incompatibilities with other circuit simulators.

Important Changes to **Xyce** Usage Since the Release 5.1.

Table 5 lists some usage changes for **Xyce**.

Issue	Comment
New parameter added to rad-aware models.	In all versions of **Xyce** prior to Release 5.1.1, the rad-effects models had some terms in the photocurrent that inappropriately depended on the global `GMIN` setting. For very small devices, these terms were found to dominate the real effects. This dependence has now been replaced with a dependence on a device-specific parameter `TFGMIN` that defaults to zero. We have found that for most existing large-device examples, this change has negligible effect, while for small devices it eliminates the non-physical GMIN-dependent behavior. Should the user wish to produce results that are exactly compatible with prior releases, simply add a setting of `TFGMIN=1e-12` to each model card for a rad-aware device. The `TFGMIN` parameter should be considered deprecated, and may be removed along with the terms dependent on it in a future release.

Table 5: Changes to netlist specification since the last release.

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Trademarks

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Bug Reports	http://charleston.sandia.gov/bugzilla
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