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DOE High-Penetration Project Report

Distribution Modeling and Laboratory Verification of Power Conditioning

Project Report
DOE/EE0002060-1
March 2012

Submitted to

Department of Energy
Contract No. DE-EE0002062

Future Energy Electronics Center

Distribution Modeling and Laboratory Verification of Power Conditioning

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EXECUTIVE SUMMARY

This project investigated solar variability, power conversion and electric power grid response aspects of high penetration solar PV. These are the primary determining factors for acceptable penetration levels. Therefore, the study not only focused on the power system interactions, but also on the design of advanced power conditioners to explore more efficient design options and to look into advanced control impacts to the higher penetration PV deployment systems. Through extensive laboratory and field testing, the team gathered the essential information to better understand grid characteristics, PV systems configuration and power conditioning systems.

In this Phase 1 effort, four major tasks were planned and performed. The team followed the planned work closely to ensure that the stated goals were achieved. Major tasks and achievements are summarized as follows.

Task 1 – three subtasks were planned to test and demonstrate the commercial PV power conditioners including SB5000-US from SMA, SolarMagic™ from National Semiconductor, and Enphase Micro-inverter. The actual tests performed include all the above-mentioned power conditioners and two other types: the Exeltech AC module and the in-house developed micro-converter and H6-inverter. The remaining tasks include the energy production and cost effectiveness analysis.

Task 2 – three subtasks were planned to create PV resource models for different geographical regions, to create power conditioner models for different system configurations, and to incorporate the described models into EPRI OpenDSS for distribution system study. The actual work performed covers all the above-mentioned modeling and simulation. The remaining task is to simplify the PCS models and incorporate them into the OpenDSS simulation.

Task 3 – three subtasks were planned to test inverter-grid interactions, the power conditioning system under abnormal voltage conditions, and the protection function under utility transients and faults. The first two tasks have been performed with detailed results included in this report. The remaining protection function and stress tests, which may be destructive, were completed after other tasks were finished.

Task 4 – four subtasks were planned to test paralleled inverters for control and communication, test different communication methods, demonstrate communication and control between distributed PV systems, and evaluate mode transition between islanded and grid-tie conditions. The actual tasks performed include some of all the above, but the present focus is on monitoring and communication. The control function remains to be done. Additional work to better understand the power system impact and effectiveness with existing anti-islanding methods is considered to be a future high priority activity.

1. INTRODUCTION

The objective of this project is to verify and demonstrate existing and new high-penetration level photovoltaics in the distribution grid while addressing current technological issues. To achieve this objective, the project started with testing and demonstration of the commercial power conditioners using laboratory power supplies and small-scale photovoltaic (PV) panels. The improved power conditioner configuration and design can be developed based on the results of extensive testing. Improvements are focused on efficiency, cost effectiveness, power system interactions, and grid interconnection issues. Power system interactions include voltage sags, swells, harmonics, and flickers. The grid interconnection issues include anti-islanding techniques, dc injection, reactive power generation, and fault reactions.

Virginia Tech's approach to evaluate the steps needed for an advanced inverter was to review and test several commercially available inverters. The purpose of the testing was to understand the inverter operations, and to identify any weaknesses. Based on this knowledge, the Virginia Tech team then set about designing inverters that would avoid the potential weaknesses identified through testing. Laboratory testing and field demonstration of existing PV power conditioners is focused on three well-recognized, commercially available products that are manufactured by Enphase Energy, SMA America, and National Semiconductor (Texas Instruments). Virginia Tech also developed an advanced power conditioner that avoids the use of bulky electrolytic capacitors. Cost effectiveness of the PV system installation using the above-mentioned power conditioners were evaluated for high-penetration PV systems.

Utility grid interconnection issues associated with distributed generation such as voltage regulation, reverse power flow, unintentional islanding, false inverter trips, reactive power control, fault contribution, protection, unbalanced loads, communications, and anti-islanding operation were tested.

PV resource and power conditioning system (PCS) models were established through laboratory and field measurements. The models have been incorporated into the system level study for OpenDSS simulation and hardware-in-the-loop simulation, which can be used as the platform for the development of advanced control and communication methods that are implemented with an advanced digital signal processor.

The project team collaborated to study and address two complimentary objectives of the future deployment of high penetration PV. The first objective is to better understand, characterize and model the effects of high penetration and variable PV on the power system, focusing on the electric distribution system. The second objective is to research and develop a more effective PV power conditioner design and implementation that can avoid impacting the existing power system. The ultimate goal has been to come up with cost-effective technologies that will benefit and support the deployment of high penetration PV systems.

This report divides the technical contents into the following five chapters.

Chapter 2 describes the results of testing and demonstration with different PV system configurations as planned in Task 1. Each configuration requires specific power conditioners

including (1) centralized inverter with a string of series PV panels, (2) centralized inverter with DC-DC power optimizer for individual PV panels, and (3) microinverter for individual PV panels. Energy production of these systems and their respective commercial power conditioners is measured to show their effectiveness in terms of energy production and key design features. A newly developed high-efficiency electrolytic capacitor-less micro-converter/inverter technology is also described.

Chapter 3 describes the PV resource modeling for distribution system simulation. Modeling efforts include evaluation of the PV resources in different geographic regions and under varying cloud movement, and how to incorporate them into OpenDSS software. Simulation results of different high penetration PV levels are presented with a 10-MW example system.

Chapter 4 summarizes the power system interaction test results with comparison to the IEEE 1547 Standard. Test conditions include abnormal voltages such as over-voltage, under-voltage, sag and swell, abnormal frequencies such as over-frequency and under-frequency, harmonics, and reconnection following abnormal conditions.

Chapter 5 summarizes the grid interconnection test results related to the PCS design issues. Possible impact on power systems with burst mode operation under light-load conditions are studied extensively. Different islanding detection and anti-islanding techniques were tested and are discussed in detail. Monitoring and communication approaches and equipment are introduced to show how they can be deployed for distributed PV system study.

Chapter 6 summarizes the major efforts and describes findings of the entire project. This chapter discusses in detail the PCS design issue based on our solar house PV system installation experience and laboratory test results, modeling effort and associated simulation results, and the development of the advanced PCS without the use of electrolytic capacitors.

2. TESTING AND DEMONSTRATION OF COMMERCIAL PV POWER CONDITIONERS

2.1 PV System Configurations with Different PV Power Conditioners

Solar PV systems can be configured with different types of PCS connected to PV panels. In this project three configurations, shown in Figure 2.1, were compared at the same power level to demonstrate their efficiency, energy performance and power system compatibility. Figure 2.1(a) is the configuration with a string of PV panels tied to a centralized DC-AC inverter for grid connection. The voltage and power level of the DC-AC inverter needs to match that of the PV string. Because all series-connected PV modules are forced to have the same current, this type of system suffers from a significant reduction in power or energy output during shaded or clouded conditions. The second system shown in Figure 2.1(b) adds a DC-DC converter to allow each panel to track the maximum power point (MPP) to avoid unnecessary energy loss due to the current limit of the shaded panel. This type of DC-DC converter is also called a "power optimizer." The third system configuration shown in Figure 2.1(c) has individual panels matched with a microinverter or AC module for grid connection. Each microinverter can track MPP individually, thus the output power is always optimized. The only drawback is the cost because each microinverter requires its own power circuit and control system.

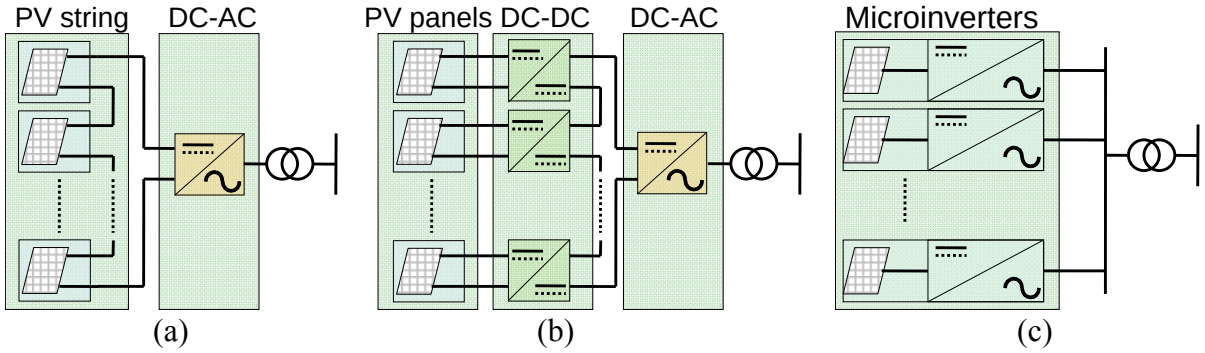


Figure 2.1. Different PV power conditioner configurations: (a) string PVs with a centralized DC-AC inverter, (b) string of PV panels with DC-DC power optimizers and a centralized DC-AC inverter, (c) individual PV panel and microinverter.

Commercially available products were acquired for evaluation of power and energy output performance. The SMA string inverter Model SB5000US was selected as the centralized inverter, the National Semiconductor SolarMagic™ Model SM3320 was selected as the DC-DC power optimizer, and the Enphase microinverter Model M190-72-240 was selected as the microinverter for extensive testing and demonstration.

The performance of the SolarMagic™ DC-DC converter was first assessed with a simple shading test. In this test, twelve PV panels are connected in series with a total capacity of 1.92-kW. The first test condition connects the entire PV string with the SMA inverter and puts two panels under shade for 5 seconds. The test result shown in Figure 2.2(a) indicates that the power drops from 1300 to 60 W, or a 95% reduction. The second test condition has individual PV panels connected through a SolarMagic™ to form a power optimized string, and the whole string

is then connected to the SMA inverter as the centralized string inverter that was used in the first test. The test result shown in Figure 2.2(b) indicates that the power drops from 1450 to 1200 W, or a 17% reduction. The percent reduction corresponds to the percent of shaded panels (2 out of 12) very well.

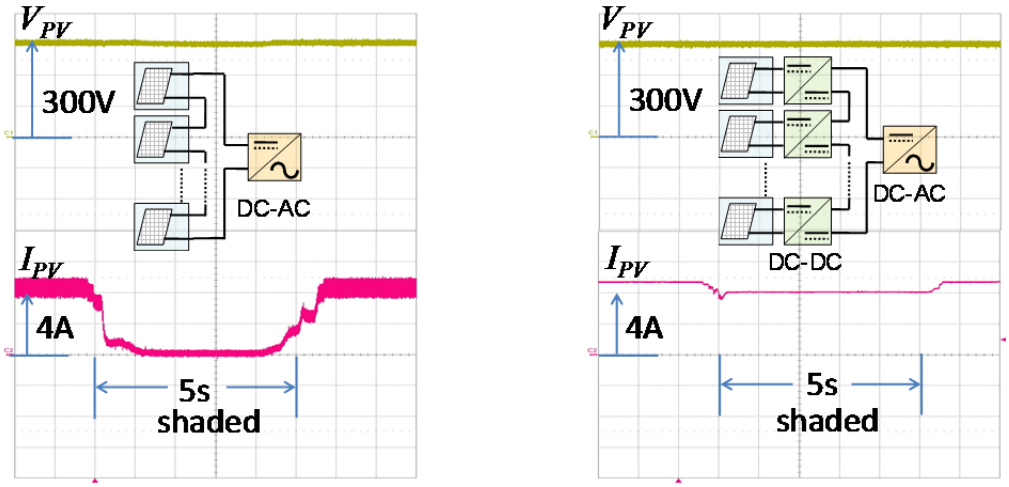


Figure 2.2. PV power outputs under shaded conditions: (a) without DC-DC power optimizer, inverter output power drops from 1300W to 60W, and (b) with DC-DC power optimizer, inverter output power drops from 1450W to 1200W.

Note that the addition of DC-DC in the circuit apparently increases the power conversion loss under shaded conditions. If the panels are not shaded, the added power DC-DC may reduce the overall system efficiency because of the power conversion loss by the DC-DC converter. In the following study, the panels were mounted on the Virginia Tech (VT) solar house that is located in a wide open space, and the use of a DC-DC power optimizer actually yields less energy output than the system without the power optimizer.

The VT solar house shown in Figure 2.3 has 78 PV panels divided into three groups. Each panel is rated 75 W with 17 V at MPP. Figure 2.4 shows the complete solar house PCS configuration with three groups: (1) a string of PVs connected with an SMA inverter, (2) individual PV panel groups connected with corresponding SolarMagic^{TM} DC-DC converters and then series connecting their outputs to an SMA inverter, and (3) individual PV panel groups connected with corresponding Enphase microinverters. Each group consists of 26 panels mounted in the same orientation and connected to one type of commercial PCS. To match the voltage requirement of the SolarMagic^{TM} DC-DC and Enphase microinverter, every two panels are connected in series. Therefore, only 13 DC-DC converters and 13 microinverters are needed. All three system outputs are connected to a common AC bus, which is the output of a standalone bidirectional DC-AC inverter. The complete installation including three PCS groups and the bidirectional DC-AC inverter can also be considered as a 100% penetration case. The DC side is a 48-V battery bank, which serves as the energy storage when it is charged by solar energy. Under the DC-AC discharging mode, the bidirectional inverter serves as the voltage stabilizer and the voltage reference for the PV inverters.

Figure 2.3. Photograph of VT solar house for power conditioner energy production study.

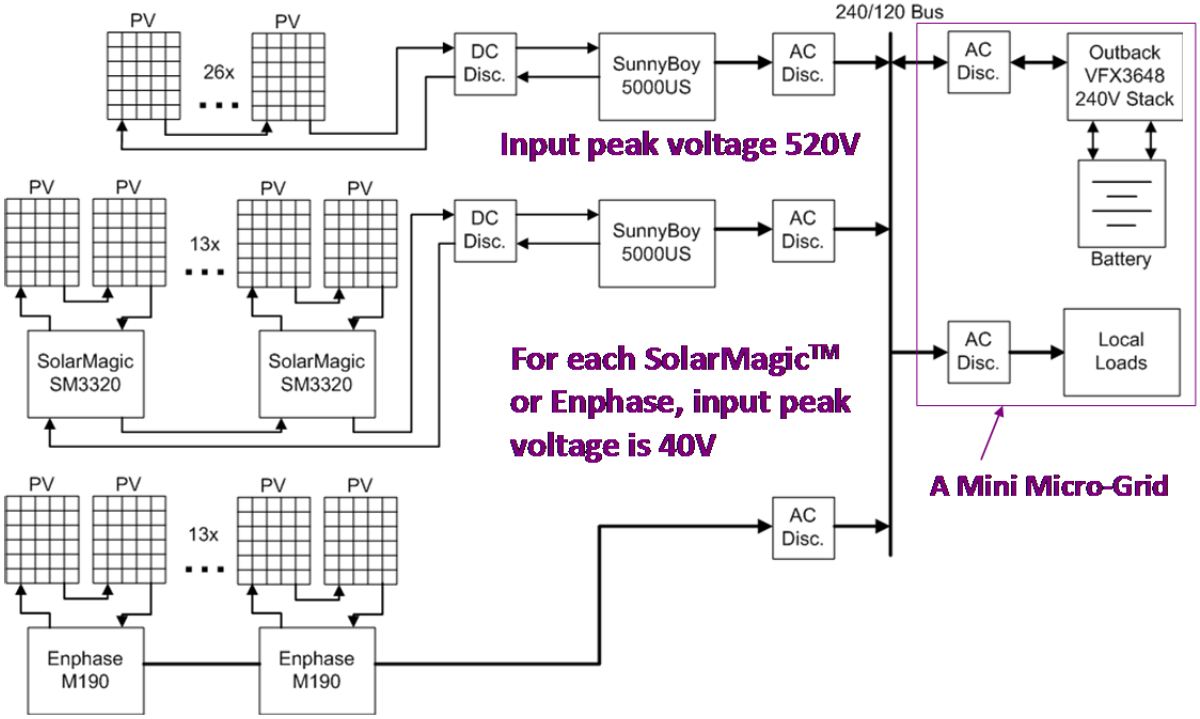


Figure 2.4. Solar house PCS configuration for three groups of PV panels: (1) SMA centralized inverter, (2) SolarMagic™ converters cascading with SMA inverter, and (3) Enphase microinverter.

2.2 Energy Production with Different PV System Configurations

A. Without Manual Shading

The first part of the study monitored the VT solar house power and energy outputs of the three PCS groups over a long period. Sample daily energy production profiles are shown in Figure 2.5. The day stamps are shown on top of the figure. Energy productions in kilo-watt-hours (kWh) are marked in the middle of the daily power output. Three commercial power conditioner groups clearly show different energy production outputs. From the product datasheet, the SMA and Enphase inverters have a similar weighted efficiency as defined by the California Energy Commission (CEC), and their daily energy production outputs are also very similar. The major difference between their outputs is during morning startup. The SMA inverter often has a long waiting time before it finally kicks in, possibly to avoid frequent relay operation. The same situation applies to the case with SolarMagic™ because it relies on the SMA inverter to produce the AC output. The inferior energy production output of the SolarMagic™ case can also be attributed to the additional power conversion loss of the DC-DC converter. As mentioned before, this added SolarMagic™ power optimizer has a significant advantage only when there are frequent shading and cloudy conditions. Under mostly sunny conditions, the added power conversion loss effectively reduces the energy production output. The profiles on Feb. 11 indicate a very significant morning startup delay for SolarMagic™, which is a discrepancy between the two manufacturer's products. In other words, the SolarMagic™ group may perform much better with a matched centralized inverter. The energy output profiles on Feb. 11 also indicate that the Enphase microinverter produces less energy than that of the SMA centralized inverter. The difference is clearly shown during the peak hour where the Enphase inverter trips often due to external load transients. Such sensitivity to the load transient is one area that needs design improvement.

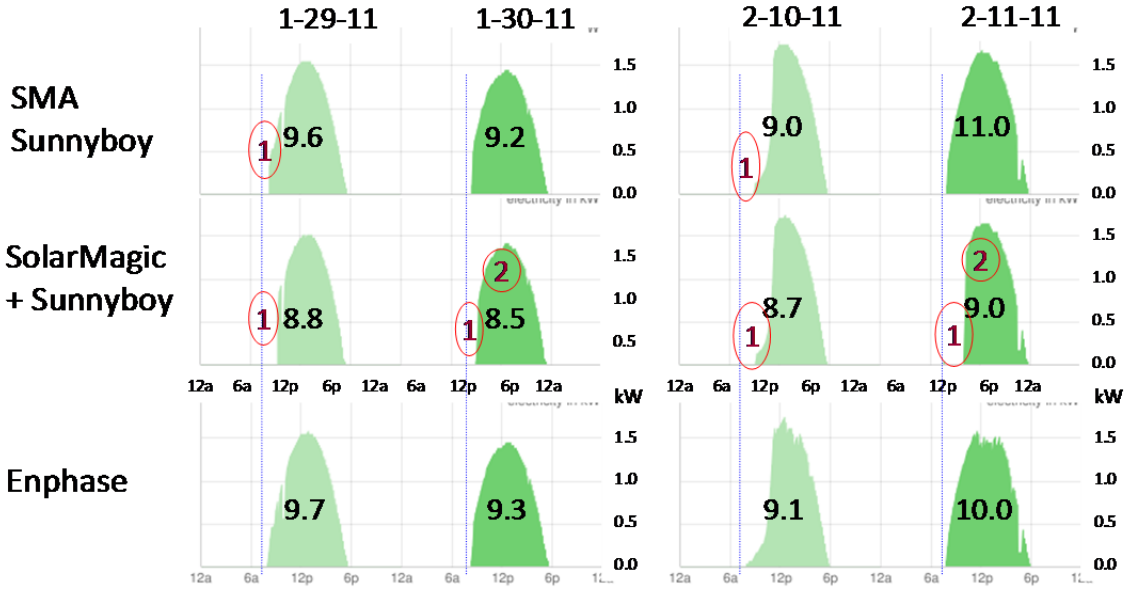


Figure 2.5. Energy production of three different PV PCS configurations.

Figure 2.6 shows the close up of power and energy productions for Jan. 30. The detailed curves indicate that the SolarMagic™ group has at least half an hour morning startup delay, which

results in noticeably lower energy output. Even without zoom-in details, the Feb. 11 case in Figure 2.5 shows a much worse startup delay and energy production loss for the SolarMagic™ group. Therefore, by comparing the energy production outputs, it is not possible to assume poor performance of the DC-DC converter serving as power optimizer. The matching design between the DC-DC converter and centralized inverter is crucial and requires attention during the design stage.

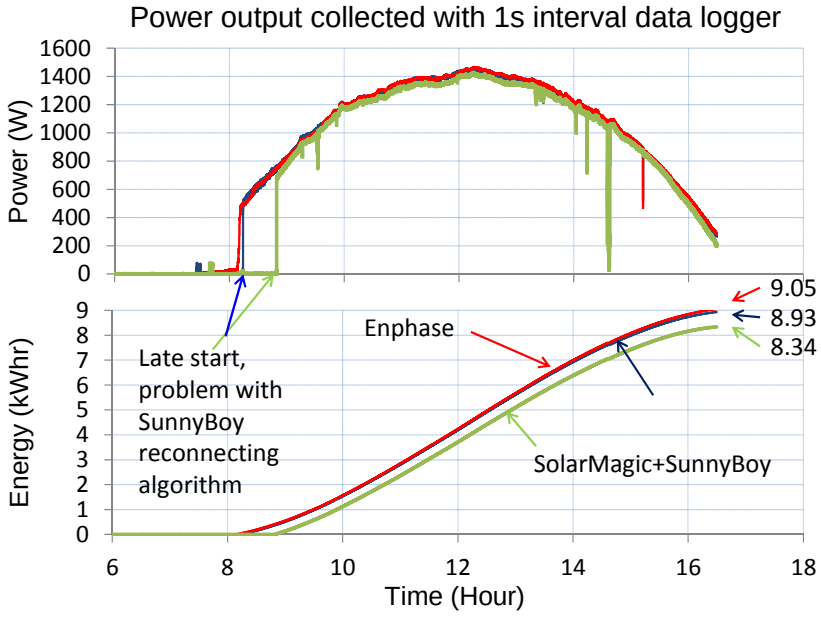


Figure 2.6. Typical power and energy production within one day.

Figure 2.7 shows the irradiance and power outputs of the three groups under frequent cloudiness. The clouds apparently decrease the PV output significantly. However, the output power can exceed the installed PV rating after the sun comes back. For the 1.95-kW installation, the figure indicates an output greater than 2-kW produced by all three groups at two time stamps, and the irradiance frequently exceeds 1000 W/m^2.

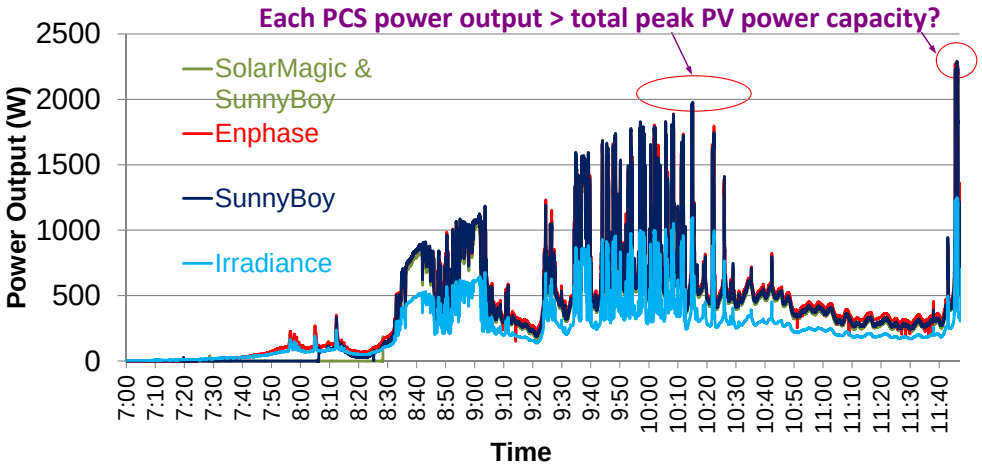


Figure 2.7. Frequent cloudiness may result in higher irradiance and power output.

Figure 2.8 shows the zoom-in second time stamp within a two-minute interval. It can be seen that the irradiance clearly exceeds the 1000-W/m^2 mark during cloud movement. This can be attributed to cloud reflection that enhances the irradiance level. The corresponding power outputs of all three PCS groups also shoot over 2 kW. This power overshoot can easily trip the PCS if the PCS capacity is less than the PV capacity, which is normally suggested by most PCS manufacturers.

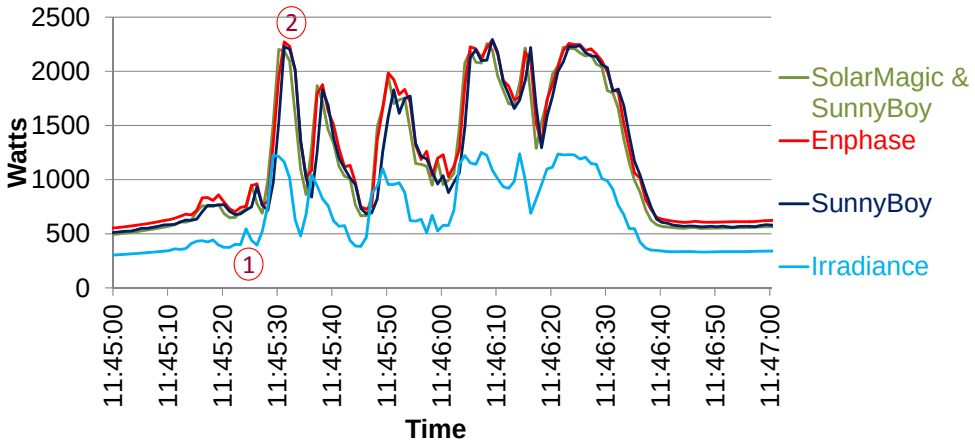


Figure 2.8. PCS outputs frequently exceed the PV installed capacity with cloud reflection.

The result of this study clearly indicates that the recommended practice by PCS manufacturers needs a second opinion. As part of this project is to design cost effective power conditioners, our recommendation is not to raise the PCS power rating over the PV installed capacity but to modify the PCS design specifications with two peak power ratings. One rating should be based on the thermal limit, and the other rating should be based on the continuous power limit. The converter should not trip at the continuous power limit if the thermal limit of key electronic components or the heat sink stays within the tolerable range. Such a change requires a small design modification but should not incur any cost penalty on the PCS.

Over the entire month of February 2011, the daily and cumulative energy production outputs of three PCS groups are shown in Figure 2.9. Overall, the Enphase microinverter produces the highest energy followed by the SMA centralized inverter, and then the distributed SolarMagic^{TM} DC-DC with centralized inverter. Similar results in April 2011 are shown in Figure 2.10. The microinverter may produce less energy sporadically due to load transient sensitivity, but in general it produces more energy because of the early morning startup, and because it is less prone to shading and cloudy conditions.

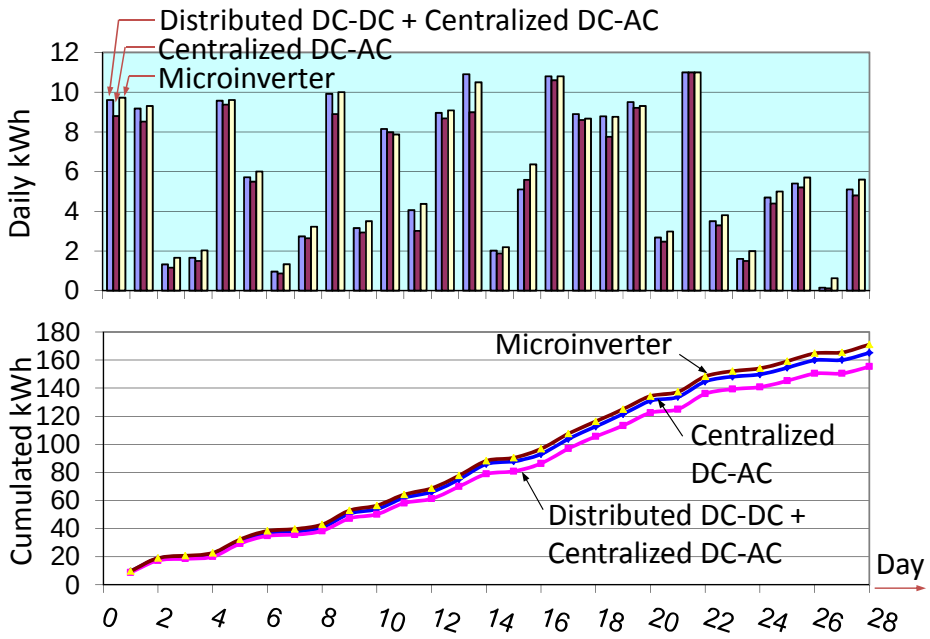


Figure 2.9. Comparison of three PCS groups' energy production outputs in February 2011.

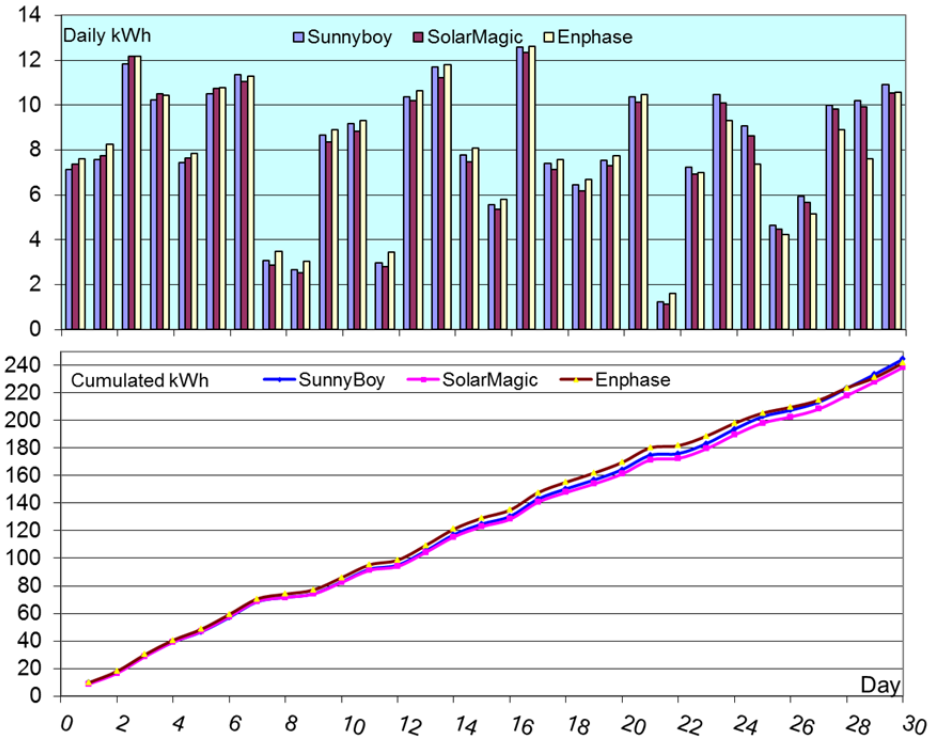


Figure 2.10. Comparison of three PCS groups' energy production outputs in April 2011.

B. With Manual Shading

In order to verify that partial shading or cloudiness can affect the energy production of the series-connected PV string with centralized inverter much more than the cases with the microinverter or distributed DC-DC converter serving as power optimizer, we used a semi-transparent sheet to cover 3 out of 26 panels for all three groups in June 2011. The photograph of the first group covered with a semi-transparent sheet is shown in Figure 2.11.

Figure 2.11. Photograph showing manually created partial shading for the three PCS groups.

Figure 2.12 compares the three PCS groups' energy production outputs in June 2011. The results indicate that the string PV with centralized inverter produces the least amount of energy daily as well as monthly. The use of SolarMagic™ DC-DC converter as the power optimizer actually shows some benefits for energy production. Its overall output is still less than that of the microinverter due to the mismatch of its centralized inverter and power conversion loss, but the energy gain under partial shading conditions provides possible justification for its usage.

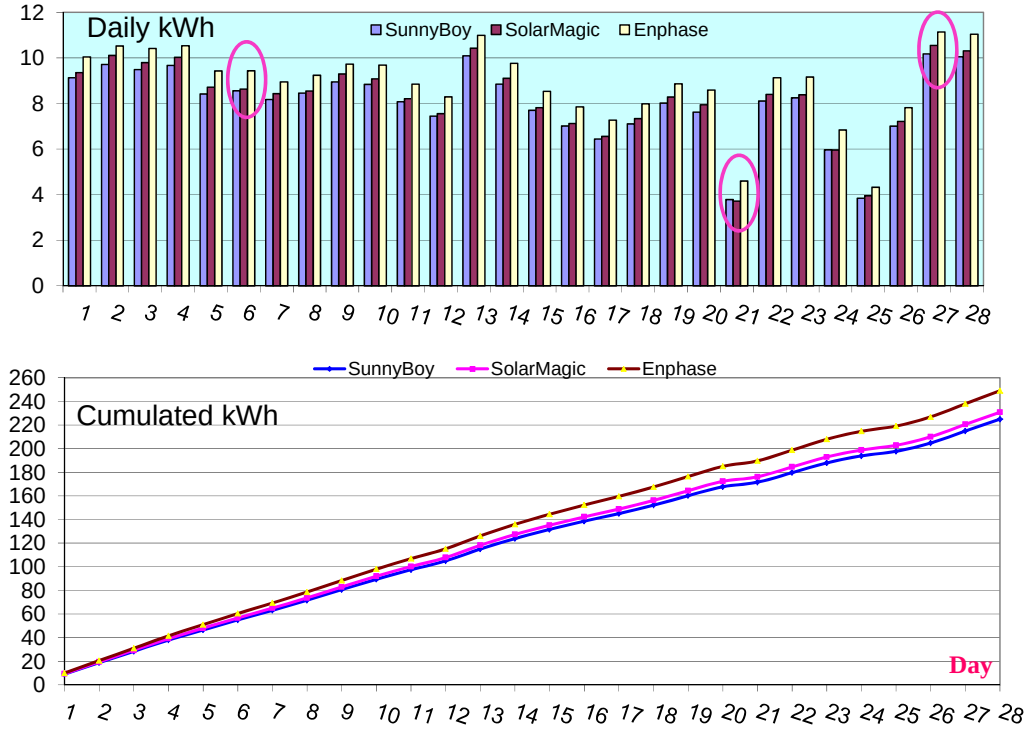


Figure 2.12. Comparison of three PCS groups' energy production outputs in June 2011.

2.3 SMA Inverter Characterization

A 5-kW centralized DC-AC inverter, SMA Model SB5000US, has been tested extensively. The inverter requires a minimum of 250 V DC input to start working. Its output has a low-frequency transformer that can be tapped at 208, 240, or 277 V. Figure 2.13 shows the schematic circuit diagram and key components of the SMA inverter, which consist of four insulated-gate-bipolar-transistors (IGBTs) as the main switching device. During basic operations, the top two switches S_1 and S_3 operate at the 60-Hz fundamental frequency and bottom switches S_2 and S_4 operate at 16-kHz pulse-width-modulation (PWM) frequency. This type of operation requires S_1 and S_3 to be synchronized with the line frequency, so it is not possible to produce reactive power. The DC input is paralleled with a large capacitor bank to absorb the double line frequency ripple. The output of the PWM stage is a low-frequency transformer containing a significant leakage inductance to smooth the output waveform.

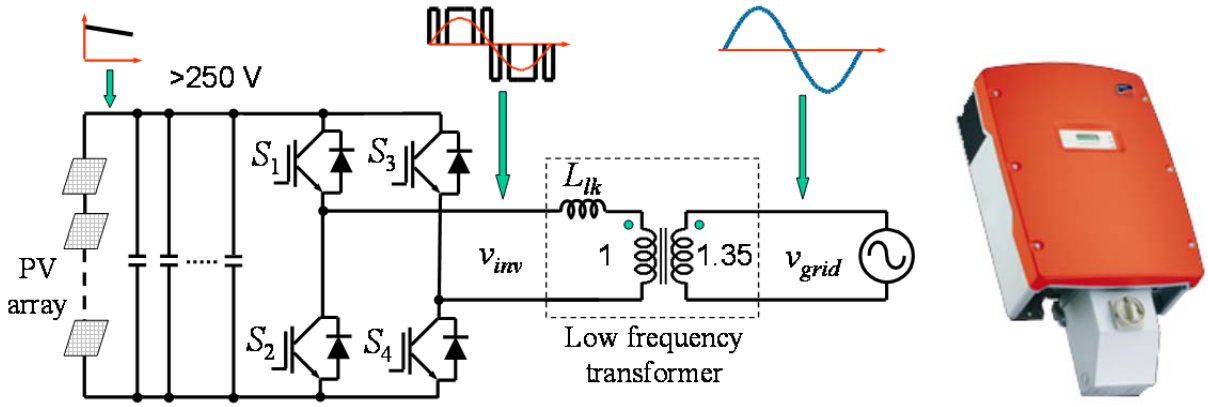


Figure 2.13. SMA SB5000US inverter power circuit diagram and photograph.

Figure 2.14 is the plot of a spectrum analyzer showing the harmonic spectrum of the output current. The most significant harmonic frequency occurs at 16.1 kHz, which confirms that the nominal switching frequency is 16 kHz.

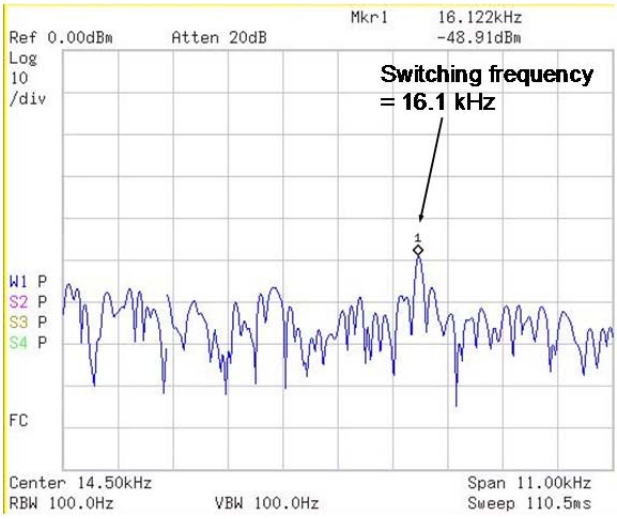


Figure 2.14. Spectrum analyzer plot showing SMA inverter switching frequency at 16.1 kHz.

The inverter efficiency as a function of input voltage and output power is plotted in Figure 2.15. Lower input voltages tend to have higher efficiency because the output transformer leakage inductance L_{lk} and current ripple are lower and thus the circulating energy is lower. The measured peak efficiency of 96% at 250-V input is 0.8% less than its brochure stated 96.8%, and the measured CEC efficiency over the measured input voltage range is 94.7%, which is also 0.8% less than its brochure stated 95.5%.

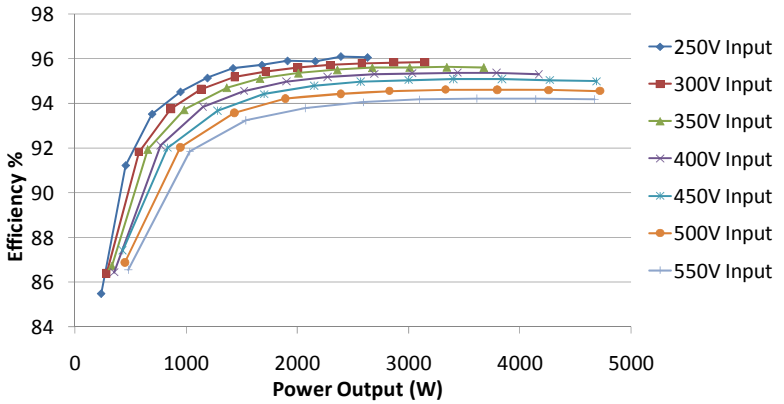


Figure 2.15. SMA inverter efficiency as a function of input voltage and output power.

The main problem with the SMA inverter is the waveform quality, especially at light-load conditions. Figure 2.16 shows the measured output voltage and current waveforms at 5% load conditions. The square-type voltage V_{PWM} is the voltage measured at the middle point between switches S_1 and S_2, which also indicates the device voltage stress. The transformer and grid currents, $I_{transformer}$ and I_{grid}, are highly distorted even with a clean sinusoidal grid voltage, V_{grid}. The main reasons for such a severe waveform distortion are low output inductance and insufficient control loop gain at the line frequency. A large current ripple of the $I_{transformer}$ indicates that the core loss is substantial, which eventually results in poor light-load efficiencies, as reflected in Figure 2.15.

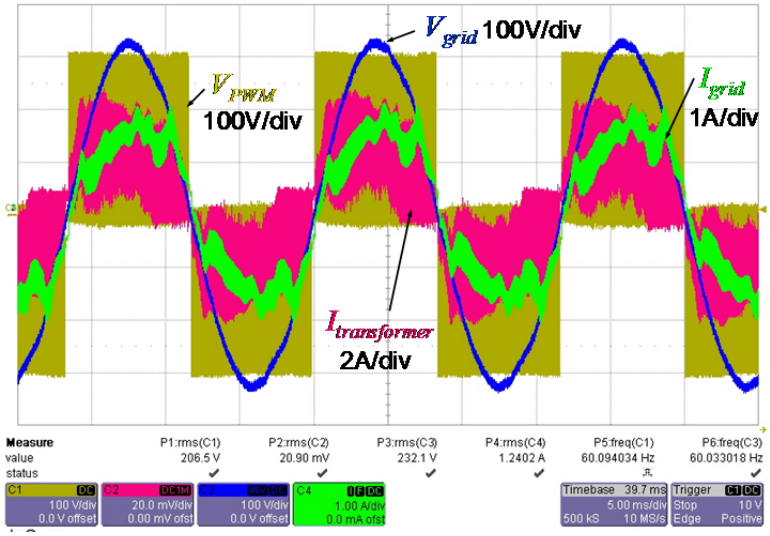


Figure 2.16. SMA inverter output voltage and current waveforms.

The inverter output current total harmonic distortion (THD) as a function of input voltage and output power is plotted in Figure 2.17. The input voltage does not affect THD much, but the output power level has a strong impact on the THD level. At 20% load, the THD is clearly higher than 20%. At full load, the THD barely passes the 5% threshold that is required by the IEEE-1547 standard.

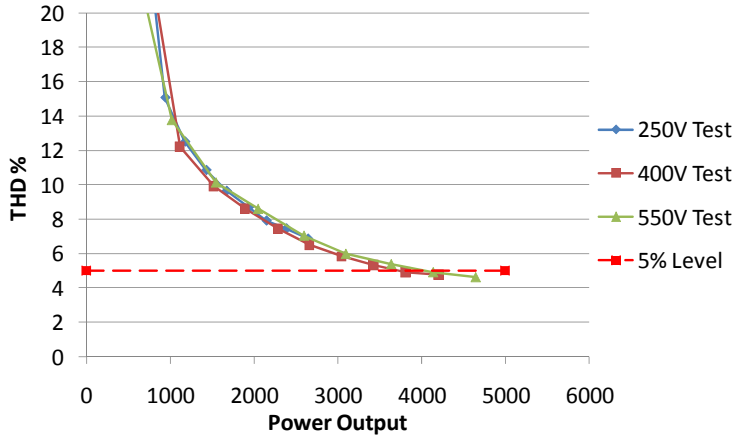


Figure 2.17. SMA inverter output current THD as a function of input voltage and output power.

The main reason for poor light load THD can be attributed to two factors: (1) low transformer leakage inductance causing the inverter output current operating in discontinuous conducting mode (DCM) and (2) poor control loop compensation at the line frequency. The control loop normally requires an admittance compensation to prevent interaction with the grid voltage feeding back to the inverter and a large gain at the line frequency with implementation of proportional-resonant (PR) control or the use of a synchronous rotating reference frame transformation controller design approach. From the severe zero-crossing distortion on the grid and transformer currents, I_{grid} and $I_{transformer}$, shown in Figure 2.18, it is clear that the inverter does not implement advanced control loop compensation.

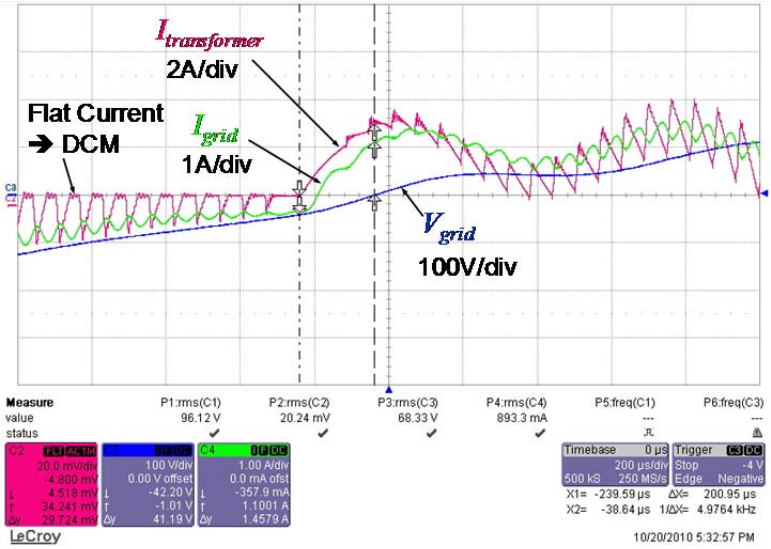


Figure 2.18. Transformer current freewheels to zero periodically, indicating DCM operation during light load operation.

The transformer current shown in Figure 2.18 also indicates that the inverter runs in DCM mode at light loads as can be seen from its flat portion where the inductor current stays at zero when the switches are flowing freewheeling current. The operating mode is defined as discontinuous conducting mode because the inductor or transformer leakage inductance current runs into zero in freewheeling mode and back to conduction when switches are active. The measured leakage inductance is 1.2 mH. With 16-kHz switching, it can easily go into DCM operation and result in severe harmonic distortion. At higher currents, the transformer current may be in continuous conducting mode (CCM) or in the boundary mode between DCM and CCM. Figure 2.19 shows a higher current condition where $I_{transformer}$ runs into the boundary mode. The grid current is smoothed out by a filter capacitor connected at the transformer output.

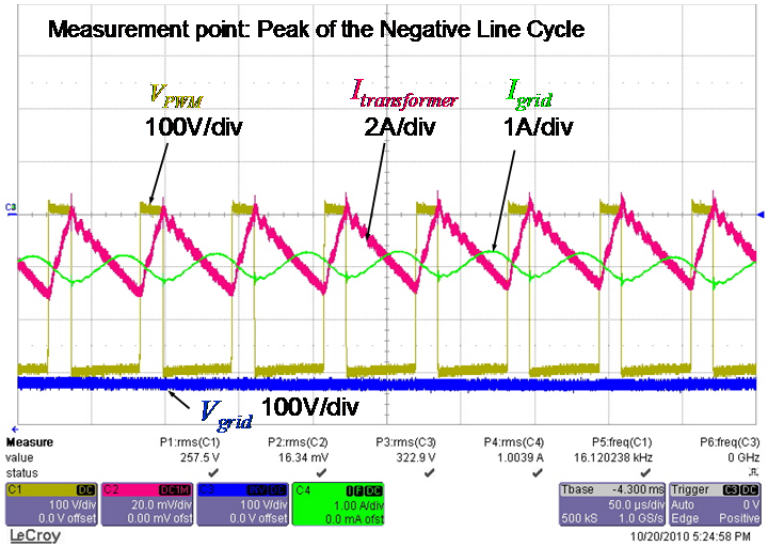


Figure 2.19. Transformer current runs in boundary mode between DCM and CCM.

The waveform distortion can also be attributed to the phase-locked-loop (PLL) error that occurs at zero-crossing. Figure 2.20 shows a severe current spike at zero crossing where the inverter is not switching, which is likely due to PLL error. The function of PLL is to detect zero crossing of the grid voltage and to synchronize the PWM switching. In this figure, the PWM stops functioning before V_{grid} reaches zero, thus resulting in a large current caused by the slope of the grid voltage.

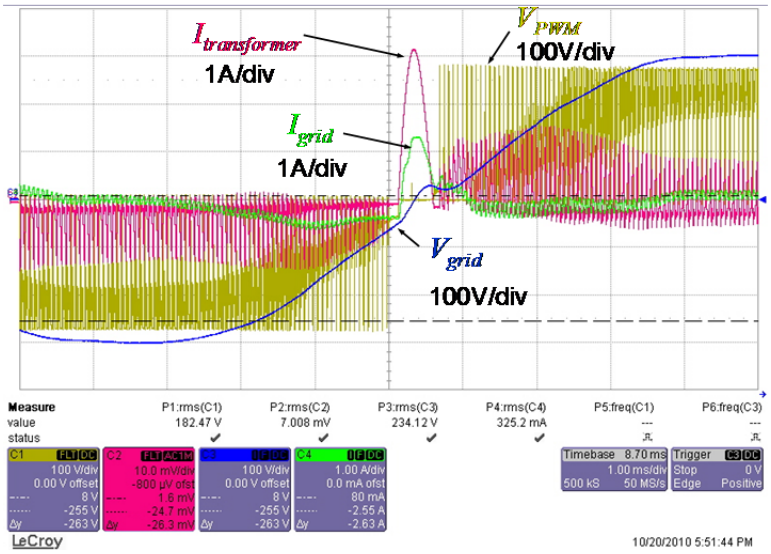


Figure 2.20. Phase-locked-loop error at zero crossing.

2.4 SolarMagic™ Micro-converter Characterization

SolarMagic™ is attractive based on its website that claims ultrahigh efficiency. If the follow-on inverter is also very efficient, then the overall system efficiency should be high and the system should be cost-effective. The basic idea of using SolarMagic™ for PV applications is to regulate the PV output at a proper voltage level under the fluctuating PV input conditions. Figure 2.21 shows the suggested system configuration for the use of SolarMagic™ in a grid-tie PCS. A series connected SolarMagic™ stack provides a high voltage output that supplies the DC-AC inverter for grid connection.

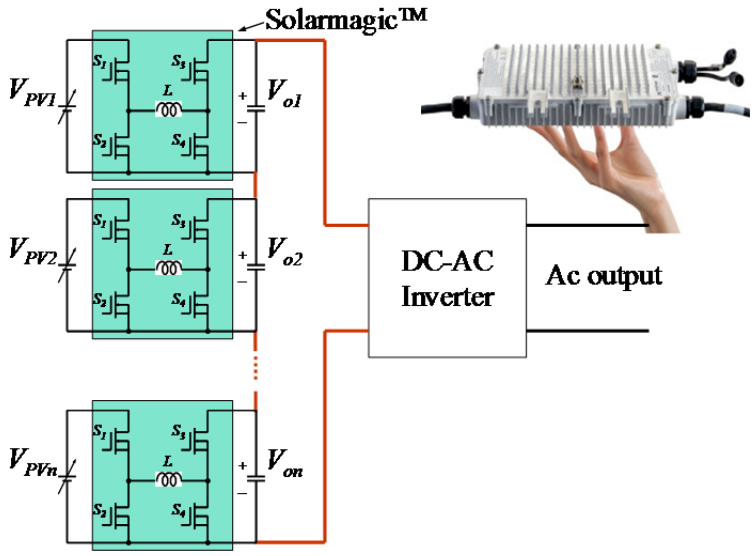


Figure 2.21. SolarMagic™ micro-converter for PV applications.

The power circuit of the SolarMagic™, shown in Figure 2.22(a), is a buck-cascaded-with-boost DC-DC converter. When the input voltage is high, switch S_3 is always turned on, S_2 and S_4 are always turned off, and S_1 is operating in pulse-width modulation (PWM) to reduce the output voltage to a proper level while producing the maximum power output. When the input voltage is low, switch S_1 is always on, S_2 and S_3 are always off, and S_4 is operating in PWM to increase the output voltage to a proper level while producing the maximum power output. If the voltage level is very close, the efficiency can be very high because the circulation current is minimal. Figure 2.22(b) shows the measured efficiencies as a function of boost ratio for the early version SM1230-4A1 and for the new version SM 3230-1A1. The peak efficiency is 98.7%, at which point the voltage conversion ratio is near unity. The early version has a relatively flat efficiency with respect to the boost ratio.

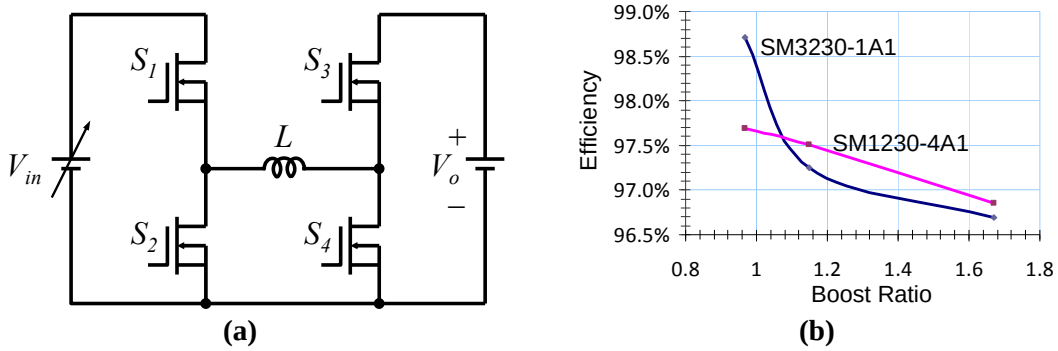


Figure 2.22. (a) Power circuit of SolarMagic™ and (b) measured efficiency as a function of boost ratio.

The main issue with SolarMagic™ is the startup operation, which does not go into boost mode automatically. This will limit the power production in the morning. Another potential issue is the use of a second-stage inverter, which may also run with its own MPPT control that tends to conflict with the SolarMagic™ operation and potentially results in stability problems.

2.5 Enphase Micro-inverter Characterization

The main power circuit and photograph of Enphase micro-inverter is shown in Figure 2.23. The circuit is considered a single-stage power conversion design because only the DC-DC converter is performing PWM. The PWM has a special pattern, which contains a fixed-frequency but variable duty cycle high-frequency AC signal that is half-wave symmetrical with respect to the line frequency. The DC-DC converter contains two active-clamped flyback converters interleaving each other to reduce the high-frequency noise back to the source. Switches S_1 and S_2 are the main switches performing the PWM function, and S_{x1} and S_{x2} are the auxiliary switches serving the active clamping purpose. The output of the flyback converter is high-voltage AC and is rectified to obtain half-wave symmetry sinusoidal PWM voltage, which is then unfolded to sinusoidal AC output with four thyristor switches, Q_1, Q_2, Q_3, and Q_4. Switch pair Q_1 and Q_4 turn on during positive half line cycles, and Q_2 and Q_3 turn on during negative line cycles.

Note that the input capacitor bank contains five electrolytic capacitors that are necessary to reduce the double line frequency ripple that is reflected back from the line. The ripple voltage and current at the input tends to reduce the MPPT efficiency. For such a single-stage power

conversion design, the ripple content can only be decoupled with a large capacitor bank at the input. Life expectancy of these electrolytic capacitors is questionable, and is the weakest point of this design.

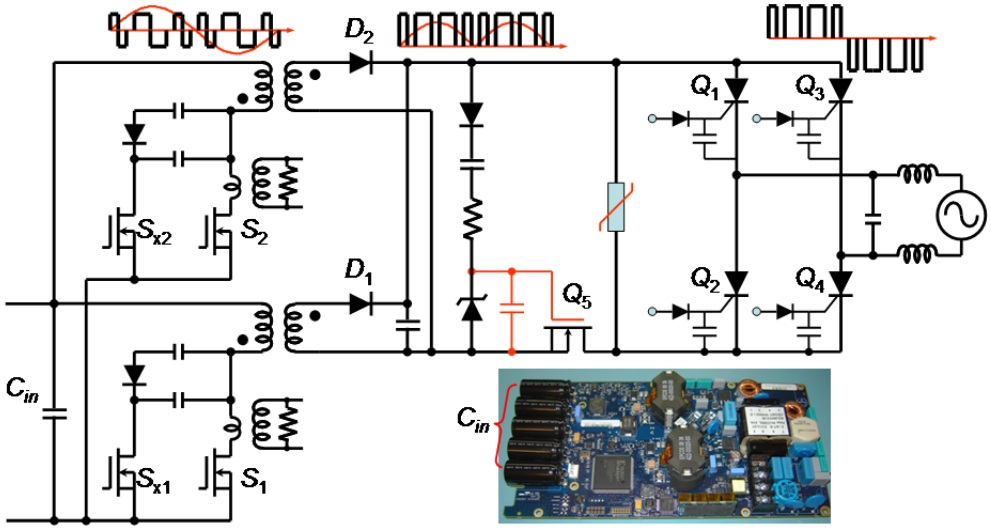


Figure 2.23. Enphase microinverter power circuit and photograph.

Another concern with this design is the use of expensive components. The flyback converter output diodes D_1 and D_2 are silicon carbide Schottky diodes, which are significantly more expensive than their silicon counterpart. The main reason for using such an expensive part is to avoid diode reverse recovery loss. Switch Q_5, serving as the commutating device for the thyristor bridge, is also an expensive super junction power MOSFET. Its conduction voltage drop is low, but its cost is much higher than a regular power MOSFET.

The waveform quality in steady state is acceptable. As shown in Figure 2.24, the output voltage and current are clean sinusoidal with only a small glitch current occurring at the zero crossing. The power level tested here is 175 W, and the output is continuous. The output current waveform will become bursting when the output power level is reduced. This burst mode operation will be described in a later section of this report.

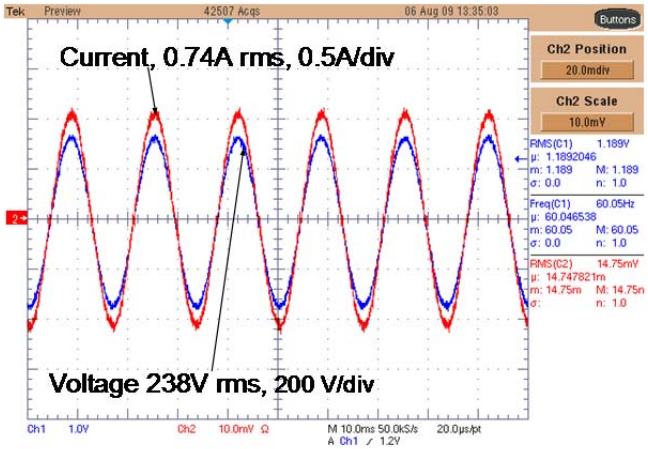


Figure 2.24. Enphase micro-inverter output voltage and current under steady-state conditions.

The Enphase micro-inverter is reasonably efficient at its power level. Figure 2.25(a) shows the measured efficiency as a function of output power. The measured CEC efficiency is 94%, which is 1% lower than the brochure stated 95%. However, its hot spot device temperature, shown in Figure 2.25(b), is reasonably low, and should not cause over-temperature failure. The hottest spot measured is 53.4°C, which is well below the silicon temperature limit.

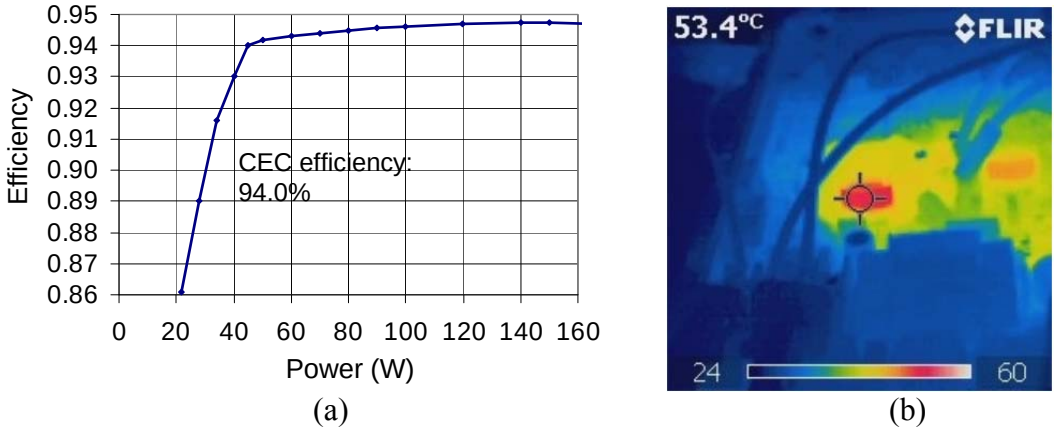


Figure 2.25. (a) Enphase micro-inverter efficiency and (b) hot spot temperature.

Figure 2.26 shows the output current THD as a function of output power. The THD cannot be measured below 20% power because it runs into burst mode. The continuous operating mode, however, indicates a significantly lower THD as compared to that of the SMA inverter.

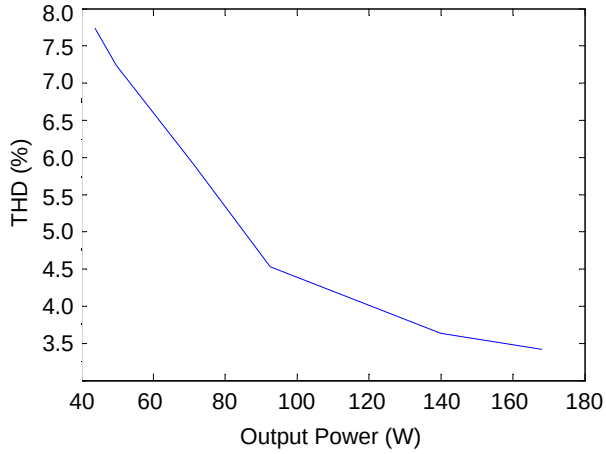


Figure 2.26. Enphase inverter output current THD as a function of output power.

2.6 Virginia Tech Micro-Converter and H6-Inverter Characterization

The Virginia Tech in-house developed micro-converter, shown in Figure 2.27(a), is a high boost ratio DC-DC converter that converts low-voltage PV output, V_{pv}, to high voltage DC, V_{dc}, which can be used to supply a DC-AC inverter. The proposed H6 inverter, shown in Figure 2.27(b), is similar to the European version SMA H5™ inverter except that we use six switches to equalize the device current sharing while avoiding the ground loop current for a non-isolated PV power

conditioning system. The entire system contains no electrolytic capacitors. The control has the DC-DC converter operating in Maximum Power Point Tracking (MPPT) mode because it has the information about PV voltage and current and the DC-AC inverter regulating the DC bus voltage. Test results indicate that the DC-DC converter in this case can operate in a high control loop bandwidth so the DC bus voltage is well regulated, which results in effective suppression of the DC link low frequency ripple current, thus avoiding the use of bulky electrolytic capacitors. Figure 2.28 shows the photograph of the complete Virginia Tech micro-converter and H6-inverter.

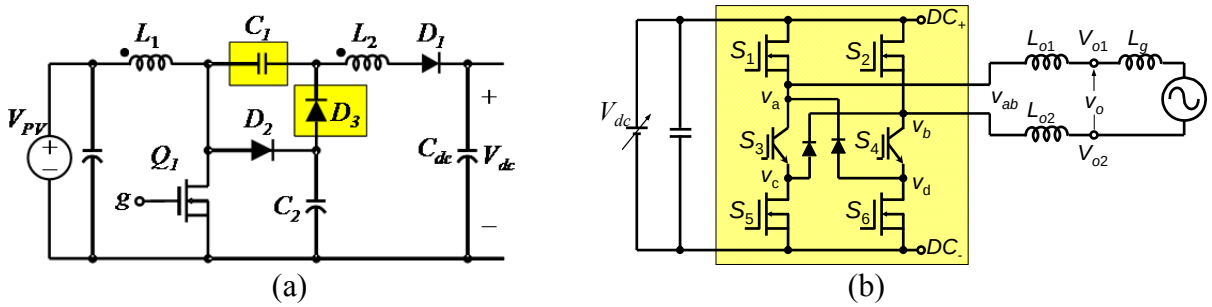


Figure 2.27. (a) Virginia Tech micro-converter and (b) H6-inverter power circuit diagram.

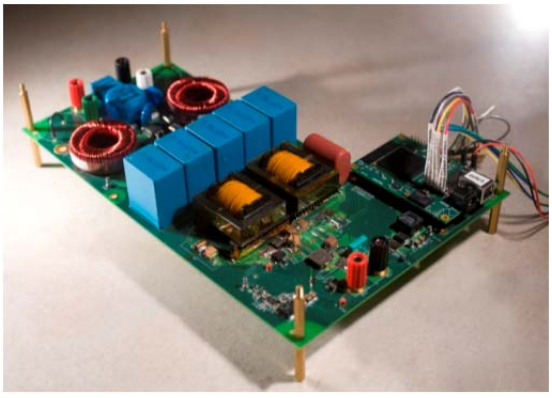
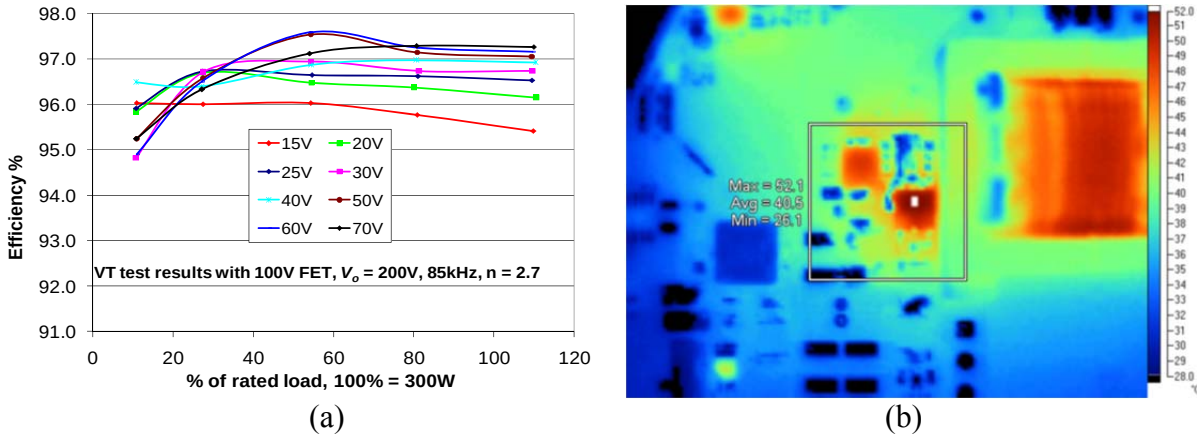


Figure 2.28. Photograph of the complete Virginia Tech micro-converter and H6-inverter.

Note that unlike the SolarMagic™ that relies on many units in series to operate with the follow-on stage inverter, the VT microconverter can operate independently as a standalone high boost ratio DC-DC converter. The inverter can be any commercial DC-AC inverter. The laboratory test was focused on the DC-DC converter only. Figure 2.29(a) shows the converter efficiency over a wide input voltage range. Under high input voltage conditions, the peak efficiency is 97.5%, and the CEC efficiency is 96.4%. The design can be optimized for a narrower input voltage range, and the efficiency can be further improved. Figure 2.29(b) shows the hottest spot temperature at 52.1°, which demonstrates the high efficiency operation of the unit.

Based on the hot spots of the thermal image, the main losses are found in the following three power components: (1) the main switch Q_1, (2) the clamping diode D_2, and (3) the coupled inductors L_1 and L_2. With continuing improvement of semiconductor device performance, especially with gallium nitride (GaN) transistors becoming available, the switching speed can be increased to reduce the magnetic component loss and size while reducing the switching losses.

The next generation VT microconverter based on GaN devices should see significant efficiency improvement and size reduction.

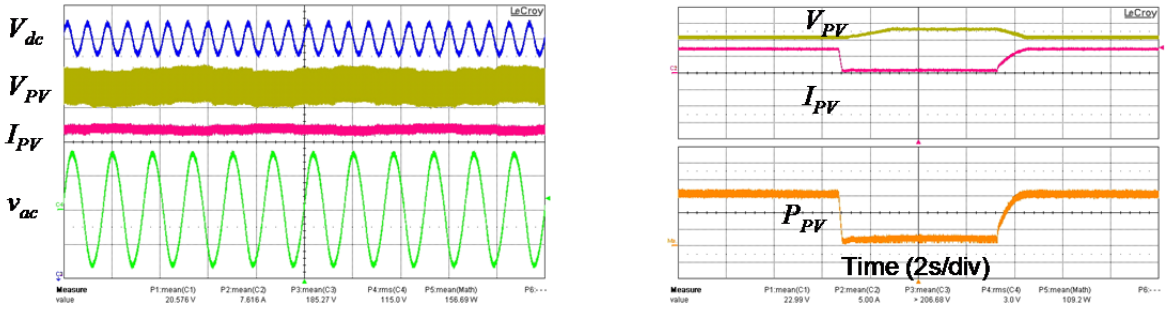


(a) (b)

Figure 2.29. Virginia Tech micro-converter efficiency and hot-spot temperature.

With the micro-converter and H6-inverter connected together, the entire system has been tested with PV panels to verify the control loop stability and response of MPPT. Figure 2.30 shows the steady state voltage and current waveforms. It can be seen that the DC bus voltage V_{dc} contains low-frequency ripple, but the inverter output voltage is a clean sinusoidal, and the input PV current is a flat DC, which should allow for stable MPPT operation.

A high bandwidth (1 kHz) control loop has been designed in the MPPT loop to maximize the power production during cloud movement and return to MPPT after the shading. Figure 2.30(b) shows the response of the MPPT control under transient shaded conditions. If the MPPT control responds too slowly, it will result in significant energy loss when the sunlight comes back due to sluggish MPPT operation. The Virginia Tech version can return to MPPT within less than 1 second after sunlight returns.



(a) **(b)**

Figure 2.30. (a) Virginia Tech micro-converter and H6-inverter voltage and current waveforms and (b) MPPT performance under shaded conditions.

3. MODELING OF PV RESOURCE FOR DISTRIBUTION SYSTEM STUDY

3.1. PV Resource Modeling

The objective of this task is to develop a modeling procedure based upon both theory and experimental measurements that can be used in conjunction with a circuit simulator such as EPRI's OpenDSS to study and predict with one-second time resolution the power quality impact of point-by-point distributed PV generation on power distribution feeders that are subjected to significant cloud movement.

A. Test Setup

The first step was to collect data on PV panel power injections with one-second resolution. This was completed at three locations – EPRI Knoxville, Southern Company Birmingham, and U.T. Austin. This report shows data from the U.T. Austin station, which became operational in October 2010. Two other identical stations are at EPRI Knoxville, and Southern Company, Birmingham.

At each station, actual maximum DC power output (P_{MAX}) of the panel pair is obtained twice every 5-seconds by sweeping the I-V curve and finding the maximum IV product. This was performed twice during each 5-second interval – once during a short circuit test, and again during a carefully-controlled curve sweeping action where the sweep speed is reduced during the peak portion of the power curve. In addition, Licor solar radiation readings were taken at several points during each 5-second interval to aid with interpolation. The goal was to have two P_{MAX} measurements during each interval, then use cubic spline interpolation to produce high confidence pseudo-measurements of P_{MAX} with integer 1-second spacing.

Except for the data logger, all test equipment was designed specifically for this project and the one-year EPRI effort that led up to this project. In summary, a DC-DC converter interfaced between the test panel and a fixed resistor load. The DC-DC converter acted as an impedance matcher, reflecting the fixed resistor load so that it became a variable resistance attached to the test panel. By controlling the speed at which the variable resistance is adjusted, very accurate yet fast I-V curve sweeps can be made with high resolution in the peak power region. A block diagram is shown in Figure 3.1.

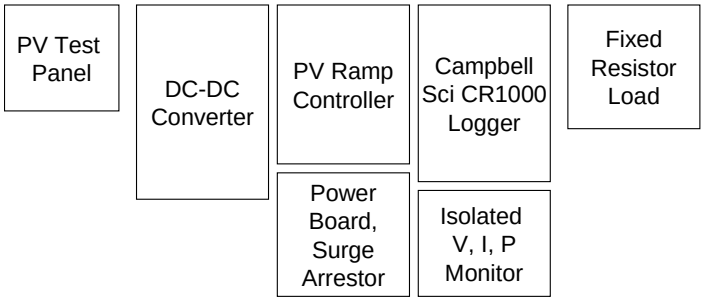


Figure 3.1. Block diagram of test equipment.

Simultaneous solar radiation measurements permit accurate interpolation via Excel spreadsheet offline processing to achieve 1-second spaced max PV panel output points. Test instruments include a Campbell Sci CR1000 data logger with Garmin time stamping, Licor GH, Licor plane-of-array, and Kipp&Z GH. Two 12-V class 65-W panels are connected in series. Figure 3.2 shows the front view and side view of the installation setup. Figure 3.3 shows a photograph of the installation in EPRI-Knoxville.

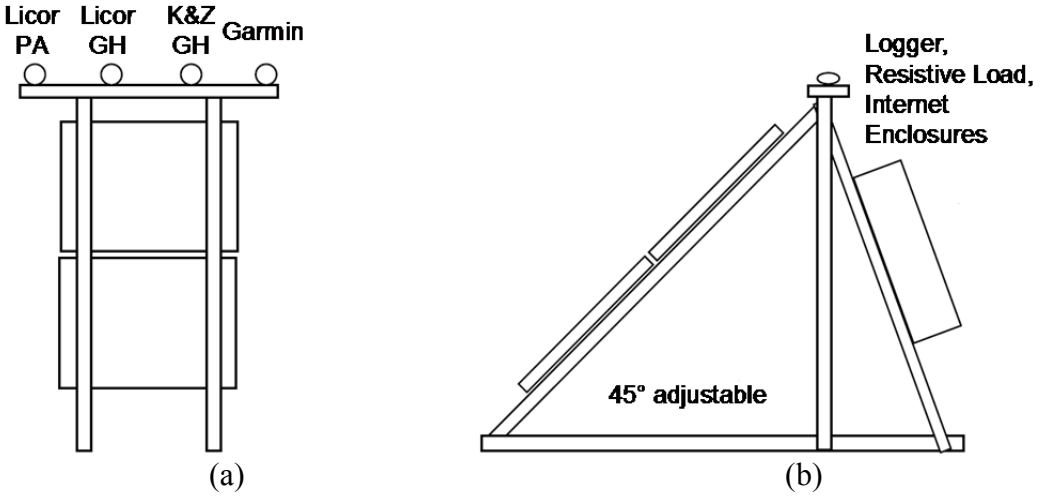


Figure 3.2. Installation of test equipment: (a) front view, (b) side view.

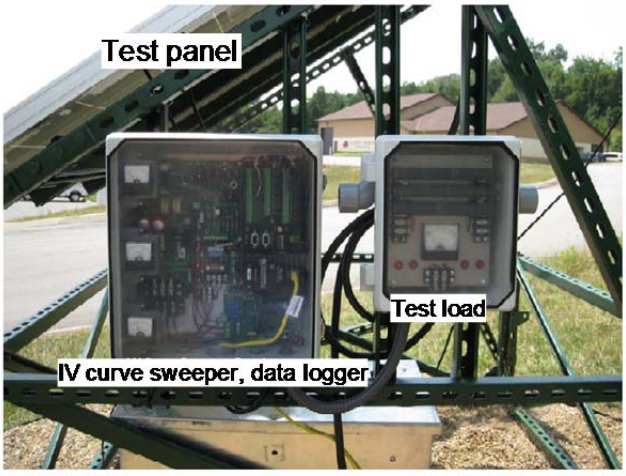


Figure 3.3. Photograph showing installation in Knoxville.

B. Cloud Movement Model

As shown in Figure 3.4, the proposed cloud shadow movement study pattern was designed as a repeating pattern. The circles represent moving shadows due to clouds. When there is no shadow, panel clear sky P_{max} is used for the given time of day and panel orientation. When inside a 50-second diameter, or A, $P_{max}/3$ is used. When inside a 5-second circular transition ring, or $C - A$, the power is assumed to be linearly varied between P_{max} and $P_{max}/3$.

Dimensions of A and C can be determined as follows.

For cloud shadow speed = 5 m/s, A = 250 meters, C = 300 meters
For cloud shadow speed = 7 m/s, A = 350 meters, C = 420 meters

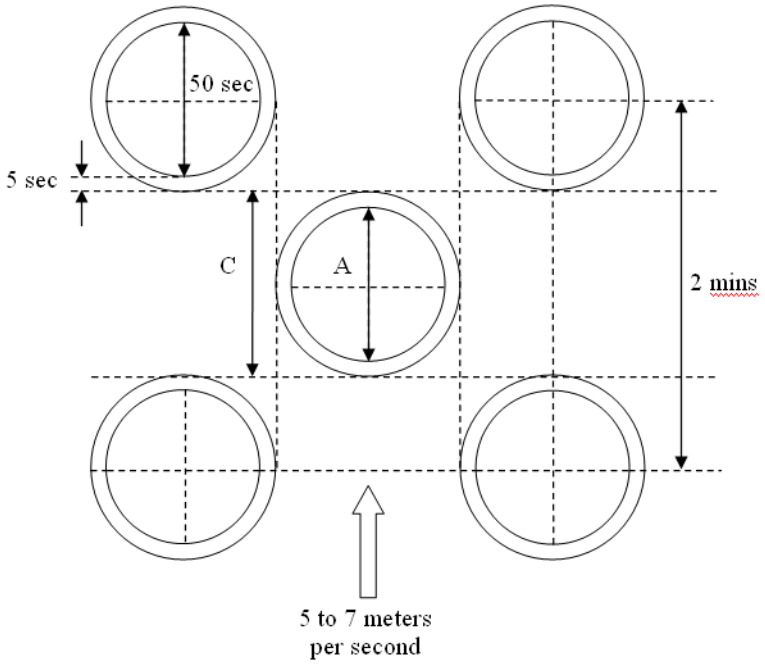


Figure 3.4. The proposed cloud shadow movement study pattern.

C. Computation of the Shading Ratio

Figure 3.5 presents the building block of the repeating cloud shadow pattern. First, consider the case *without* transition shading rings, $A = C$. The total area of all four squares is $4C^2$. With no transition shading rings, the net shading ratio SR (fraction of area with full shade) is

$$SR = \frac{2\left(\pi C^2/4\right)}{4C^2} = \frac{\pi}{8} = 0.393 \qquad (1)$$

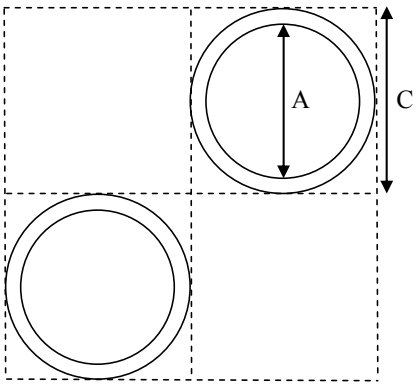


Figure 3.5. Building block of the repeating cloud shadow pattern.

Assuming uniform spatial distribution of panels and 1/3 power production in shade, the reduction in PV power compared to full sun is

PV_R = (1 – *SR*) (for panels in full sun) + *SR*/3 (for shaded panels)

PV_R = (1 – 2·*SR*/3) = 0.738 times full sun output. (2)

Now, consider the case *with* transition shading rings. The area of the two fully-shaded circles is $2\cdot\pi A^2/4 = \pi A^2/2$. The circular transition rings have full shading at their inner boundary, and no shading at their outer boundary. Assuming linear variation in shading, the equivalent shading area for each transition ring is

$$\int_{r=\frac{A}{2}}^{\frac{C}{2}}\left[2\pi r\bullet\frac{\left(\frac{C}{2}-r\right)}{\left(\frac{C}{2}-\frac{A}{2}\right)}\right]dr=\frac{4\pi}{(C-A)}\bullet\int_{r=\frac{A}{2}}^{\frac{C}{2}}r\left(\frac{C}{2}-r\right)dr=\frac{4\pi}{(C-A)}\bullet\left(\frac{C}{4}r^2-\frac{1}{3}r^3\right)_{r=\frac{A}{2}}^{\frac{C}{2}}$$

$$=\frac{4\pi}{(C-A)}\bullet\left(\frac{C^3}{16}-\frac{C^3}{24}-\frac{CA^2}{16}+\frac{A^3}{24}\right)=\frac{4\pi}{(C-A)}\bullet\left(\frac{C^3}{48}-\frac{CA^2}{16}+\frac{A^3}{24}\right)$$

$$=\frac{4\pi\left(C^3-3CA^2+2A^3\right)}{48(C-A)}=\frac{\pi\left(C^3-3CA^2+2A^3\right)}{12(C-A)}.$$

Thus, the net shading ratio for the repeated pattern, consisting of two shaded circles and two transition rings is

$$SR=\frac{\frac{\pi A^2}{2}+2\bullet\frac{\pi\left(C^3-3CA^2+2A^3\right)}{12(C-A)}}{4C^2} \tag{3}$$

$$=\frac{\pi A^2}{8C^2}+\frac{\pi\left(C^3-3CA^2+2A^3\right)}{24(C-A)C^2}=\frac{\pi A^2}{8C^2}+\frac{\pi\left(C^3-3C^3\frac{A^2}{C^2}+2C^3\frac{A^3}{C^3}\right)}{24C^3-24C^3\frac{A}{C}}$$

$$=\frac{\pi A^2}{8C^2}+\frac{\pi\left(1-3\frac{A^2}{C^2}+2\frac{A^3}{C^3}\right)}{24\left(1-\frac{A}{C}\right)}=\frac{\pi}{8}\left(\frac{A}{C}\right)^2-\frac{\pi}{24}\left(\frac{2\left(\frac{A}{C}\right)^3-3\left(\frac{A}{C}\right)^2+1}{\frac{A}{C}-1}\right).$$

Synthetic division of the second term, and combining, yields

$$SR = \frac{\pi}{8}\left(\frac{A}{C}\right)^2 - \frac{\pi}{24}\left(2\left(\frac{A}{C}\right)^2 - \frac{A}{C} - 1\right) = \frac{\pi}{24}\left(\left(\frac{A}{C}\right)^2 + \frac{A}{C} + 1\right). \quad (4)$$

For our case, we have $A/C = 50/60$, which yields a net shading ratio of

$$SR = \frac{\pi}{24}\left(\left(\frac{5}{6}\right)^2 + \frac{5}{6} + 1\right) = \frac{\pi}{24}(0.6944 + 0.8333 + 1) = 0.331.$$

Assuming that shade reduces panel output from P_{max} to $P_{max}/3$, the overall reduction in power in a building block area with uniformly distributed PV panels becomes

$PV_R = (1 - 2 \cdot SR/3) = 0.779$ times full sun output.

D. Same Repeating Pattern, with Smaller Clouds

Consider the case where cloud shadow diameter C is less than repetitive square side length D, as shown in Figure 3.6.

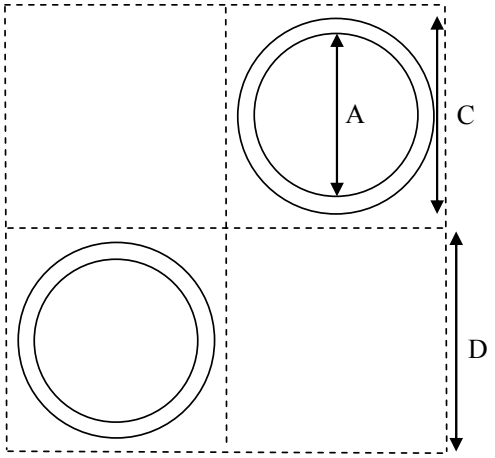


Figure 3.6. Case with cloud shadow diameter *C* is less than repetitive square side length *D*.

The denominators of (1) and (3) represent the area of the entire four-square repeating pattern. Replacing numerator C with D is the only change needed. Thus, to handle the smaller cloud shadow problem, the only modification needed is to multiply the previous SR expressions by $(C/D)^2$, where $C \le D$.

E. Incorporation Model into DSS

The procedure described here for adding the cloud shadow model is based on the idea that DSS input bus data text files with assigned PV capacity are modified externally using a separate computer program at each time step. A one-second time step is recommended, with a simulation period long enough for the cloud shadow pattern to advance through, or totally cover, the study area. Tap changing under load transformers and capacitor banks should remain fixed during the simulation period. Figure 3.7 shows the example cloud movement over a substation with a total load about 20 to 40 MW.

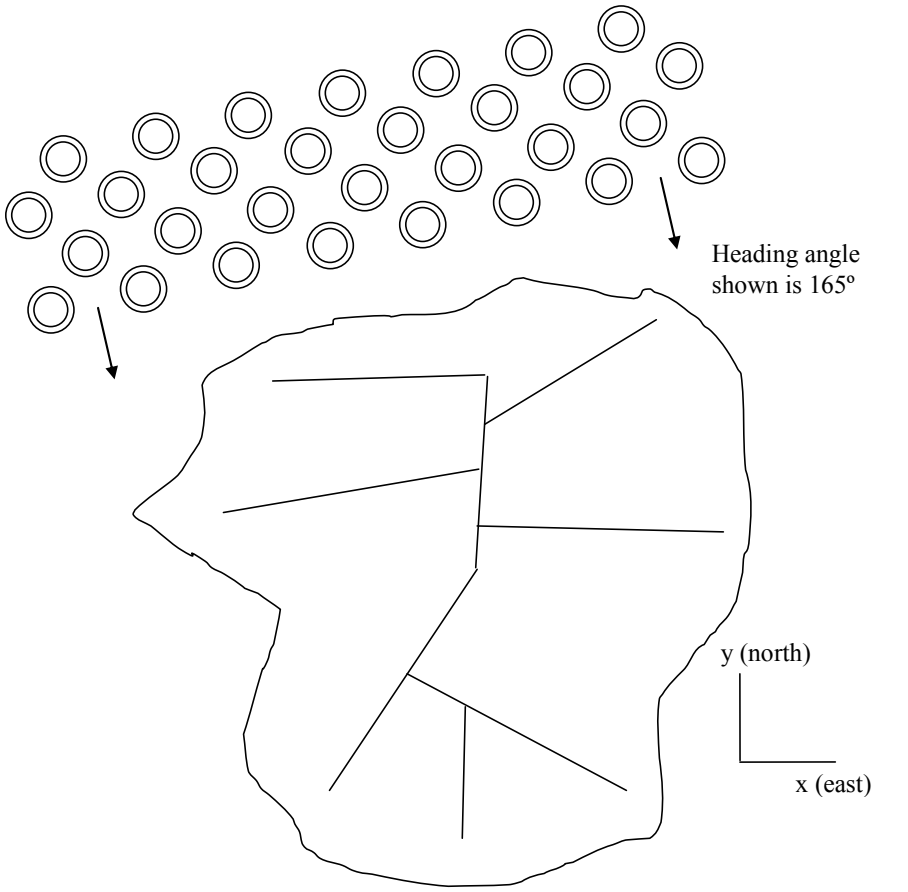


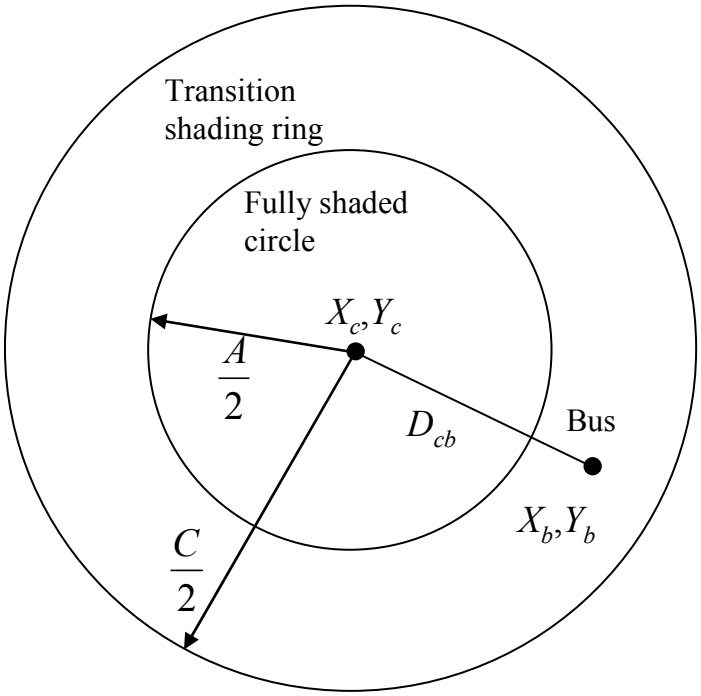
Figure 3.7. Example cloud movement over a substation with a total load about 20 to 40 MW

The programming logic, which is mostly geometry, follows:

1. Individual bus locations are at X_b, Y_b.
2. Establish a matrix of the cloud shadow centers X_c, Y_c at $t = 0$.
3. To facilitate searching, sort the cloud shadow centers by X_c (primary sort), then Y_c (secondary sort).
4. One bus at a time, search the cloud shadow centers for one that has $|X_c - X_b| < (C/2)$ and $|Y_c - Y_b| < (C/2)$. For any bus, there will be either one candidate or none, so stop searching when you find one.
5. If there is a candidate, compute center-to-bus distance $D_{cb} = \sqrt{(X_c - X_b)^2 + (Y_c - Y_b)^2}$.
6. PV generation at the bus is
   - If $D_{cb} < \frac{A}{2}$, $PV_{gen} = \frac{PV_{\max}}{3}$ (i.e., inside the fully-shaded circle)
   - If $D_{cb} \geq \frac{C}{2}$, $PV_{gen} = PV_{\max}$ (i.e., outside the transition shading ring)

- Otherwise, $PV_{gen} = \frac{PV_{\max}}{3}\left[1 + \frac{2D_{cb} - A}{C - A}\right]$ (i.e., inside the transition shading ring)

where PV_{max} is the user-assigned PV generation at the bus for a given clear sky condition and panel orientation. Figure 3.8 illustrate the calculation within the transition shading ring.



$$D_{cb} = \sqrt{(X_c - X_b)^2 + (Y_c - Y_b)^2}$$

$$PV_{gen} = \frac{PV_{\max}}{3}\left[1 + 2\frac{D_{cb} - \frac{A}{2}}{\frac{C}{2} - \frac{A}{2}}\right]$$

$$= \frac{PV_{\max}}{3}\left[1 + \frac{2D_{cb} - A}{C - A}\right]$$

Figure 3.8. Illustration of PV_{gen} calculation within the transition shading ring.

7. Solve DSS.
8. At each Δt = 1-second time step, advance the cloud shadow centers in the chosen heading φ direction at rate R = 5 to 7 meters per second. Heading φ = 0º is due north, heading φ = 90º is due east, etc. Thus, for each time step, $\Delta X_c = R \cdot \Delta t \cdot \sin(\varphi)$, $\Delta Y_c = R \cdot \Delta t \cdot \cos(\varphi)$.
9. Return to Step 4.

3.2. OpenDSS Simulation

The Open Distribution System Simulator (*OpenDSS*, or simply, *DSS*) is a comprehensive electrical system simulation tool for electric utility distribution systems. OpenDSS technically refers to the open-source implementation[1] of the DSS.

The program is developed for the Microsoft® Windows operating system. It supports nearly all frequency domain (sinusoidal steady-state) analyses commonly performed on electric utility

[1] In 2008 EPRI announced that its Distribution System Simulator (DSS) program was now available as the OpenDSS open source software project on the SOURCEFORGE.NET® website. This step was taken to cooperate with various Smart Grid and grid modernization efforts that also provide open source software.

power distribution systems. In addition, it supports many new types of analyses that are designed to meet future needs related to grid modernization efforts.

The OpenDSS tool has been used for more than a decade in support of various research and consulting projects requiring distribution system analysis. Many of the features found in the program were originally intended to support the analysis of distributed generation interconnected to utility distribution systems. Other features support analysis of such things as energy efficiency in power delivery and harmonic current flow. The OpenDSS is designed to be indefinitely expandable so that it can be easily modified to meet future needs.

The OpenDSS program has been used for:

- Distribution Planning and Analysis
- General Multi-phase AC Circuit Analysis
- Analysis of Distributed Generation interconnections
- Annual Load and Generation Simulations
- Wind Plant Simulations
- Distribution Efficiency Improvement
- Analysis of Unusual Transformer Configurations
- Annual Power Flow Simulations
- Harmonics and Interharmonics analysis
- Neutral-to-earth Voltage Simulations
- Development of IEEE Test feeder cases
- Monte Carlo Studies
- And more ….

The program has several built-in solution modes, including:

- Power Flow at a Snapshot in Time
- Daily Power Flow
- Yearly Power Flow
- Harmonics
- Dynamics
- Fault study
- And others …

A. OpenDSS Architecture

Shown in Figure 3.9, the OpenDSS is provided as both a stand-alone program and a solution engine implemented as an in-process COM server DLL. The stand-alone version provides a basic user interface for the solution engine to assist users in developing scripts and viewing solutions.

Many users find that the scripting interface available with this version is sufficient for nearly all their work.

Through the COM interface, users are able to define circuit models, execute the functions of the program, and implement algorithms that interact with the simulator. This makes it a good platform for developing and testing new algorithms for such things as distribution automation controls. For example, users can drive the OpenDSS with the Mathworks MATLAB® program. This provides powerful external analytical capabilities as well as excellent graphics for displaying results. Programming languages such as Python and Visual Basic are also popular choices.

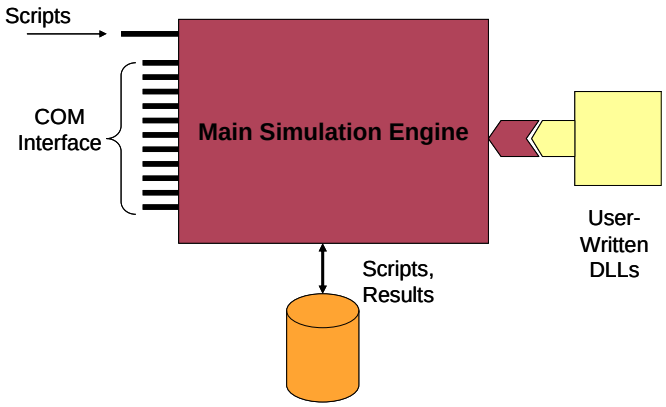


Figure 3.9. OpenDSS structure.

Objects within the OpenDSS are broken down into various elements as shown in Figure 3.10. For this project, the PV PCS is currently being implemented as a Control for a Generator PC Element (Power Conversion Element). If deemed necessary, further development may encompass a new PCElement for PV as well.

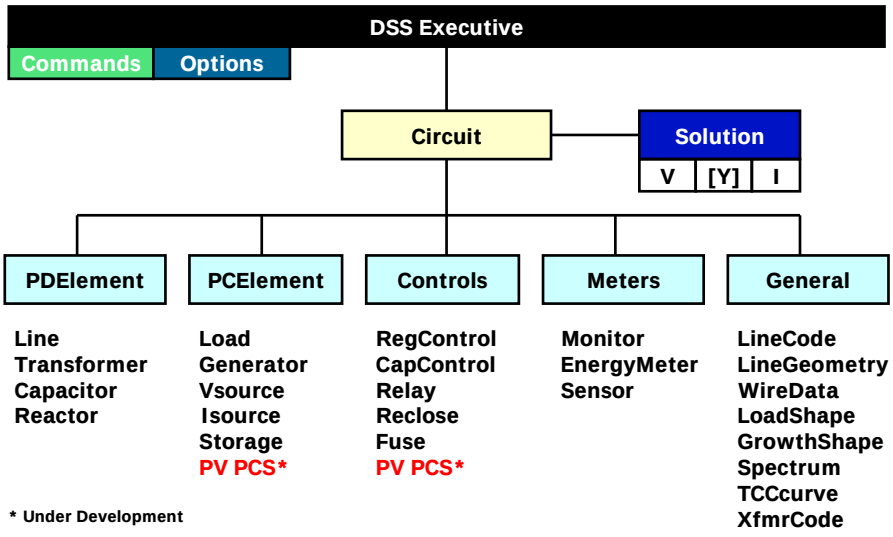


Figure 3.10. DSS objective structure.

B. Prototype PCS Control Implementation

As mentioned previously, the PV PCS has initially been implemented as a Control for the existing Generator Power Conversion Element (PC Element). The Generator PC Element simply acts as the generic "host" for providing PV output to the grid. This Generator element is generic in the sense that it can be used to mimic any type of generation (wind, PV, energy storage, etc). The Control placed on the generator is what actually determines how the Generator responds/interacts with the grid. This is further illustrated in Figure 3.11.

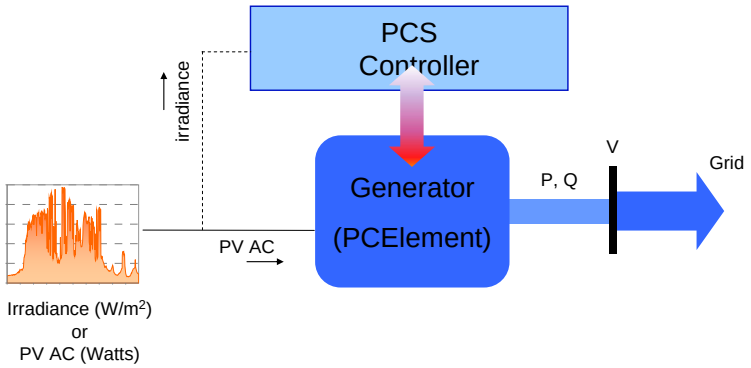


Figure 3.11. PV PCS implementation in OpenDSS

The initial framework for this PCS Controller has been implemented within OpenDSS. This framework will allow EPRI to further include additional characteristics necessary to accurately represent PV and the PCS for distribution studies. Some of the important characteristics that will be considered in this model will include:

- Inverter efficiency, including typical inverter manufacturer efficiencies as a function of DC power (irradiance). This is shown as the hashed line in Figure 3.11.
- Cut-in and cut-out due to DC voltage
- Cut-in and cut-out at various system voltages (IEEE 1547 compliance, etc.)
- Inverter power factor as a function of AC output power (PF(P))
- Advanced PCS control capability such as volt-var control

To date, the PCS framework implemented within the OpenDSS has been updated to include the advanced volt-var control. This control is capable of simulating volt-var control under steady-state conditions, as well as simulation of "dynamic" power flows in which the distribution system is simulated over time. The solar variation for this case is PV output (AC) over time, with the controller modifying the var output based upon a user-defined volt-var curve as shown in Figure 3.12.

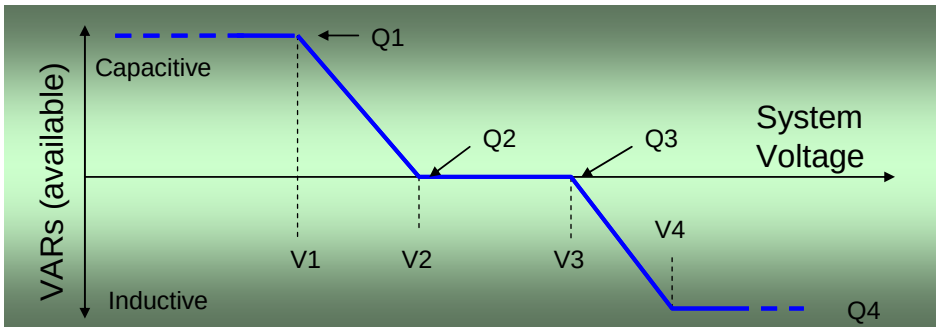


Figure 3.12. Advanced inverter volt-var control

C. Simulation Results with High Penetration PV

The following discussion and series of figures illustrate several cases of simulation results with high penetration PV added into the model for the actual feeder. Using OpenDSS, the PV PCS controller can be defined and implemented anywhere within the circuits. Therefore, any number of PV generators can be added to the circuit along with the associated PV PCS Control. Steady-state simulations analyzing any distribution system modeled within the OpenDSS can be considered. An example circuit one-line diagram is shown in Figure 3.13. The corresponding feeder voltages simulated in OpenDSS are shown in Figure 3.14 where the lowest bus voltage is about 0.95 pu, and the overall voltage control is relatively ineffective. Note that v(1), v(2), and v(3) represent the three phase voltages on the circuit.

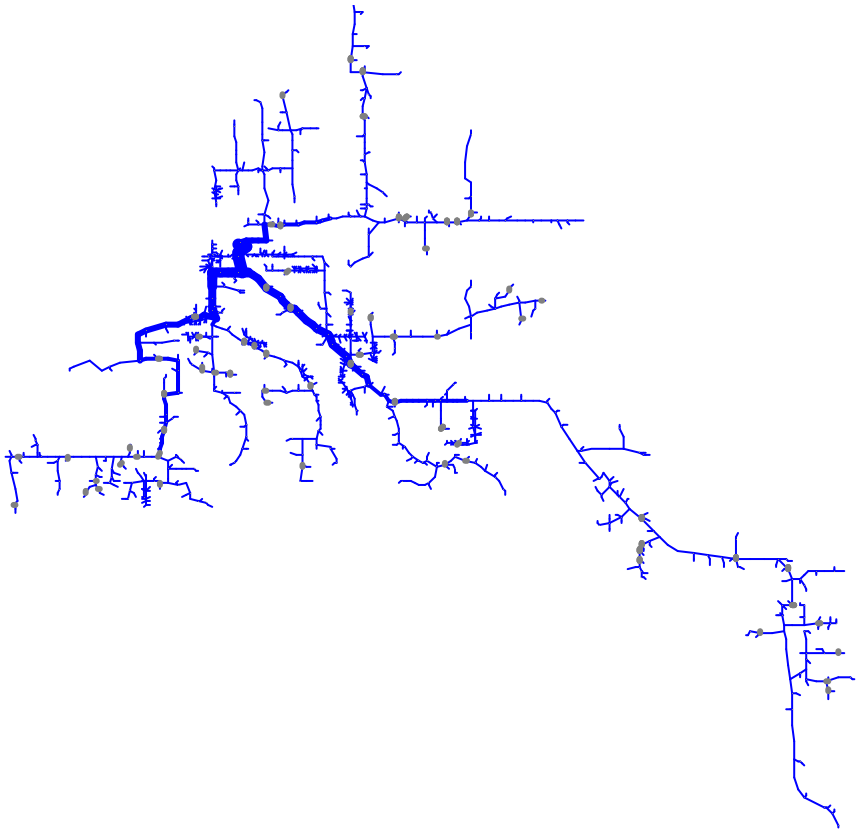


Figure 3.13. Base distribution circuit model with no PV.

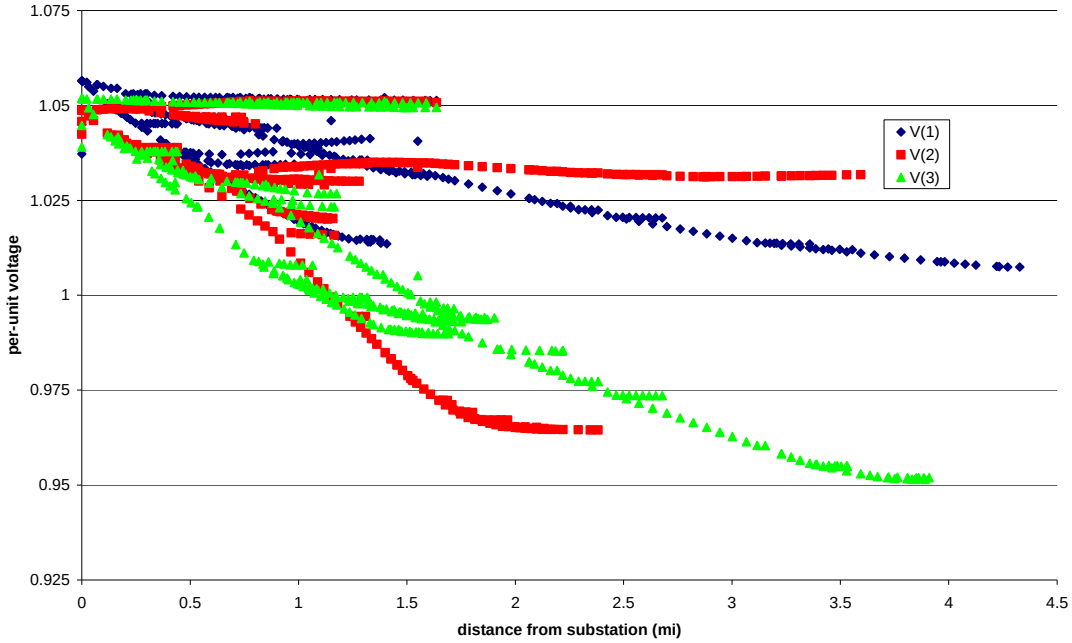


Figure 3.14. Simulated primary bus voltage profile of the base case with no PV.

Figure 3.15 shows this same circuit, however with 2.5 MW of small roof-top solar PV distributed throughout the feeder. For this case, the advanced volt-var control was simulated along with each PV system to assess distribution voltage impacts due to operation at varying PV penetration levels. Figure 3.16 illustrates a block diagram of the entire volt-var control system used with each PV system. The resulting primary bus voltage profile is shown in Figure 3.17. As compared to the no-PV case, the 0.95-pu bus voltage is now improved to 0.98-pu. The additional PV, along with the volt-var control, assists in "flattening" the voltage profile along the circuit.

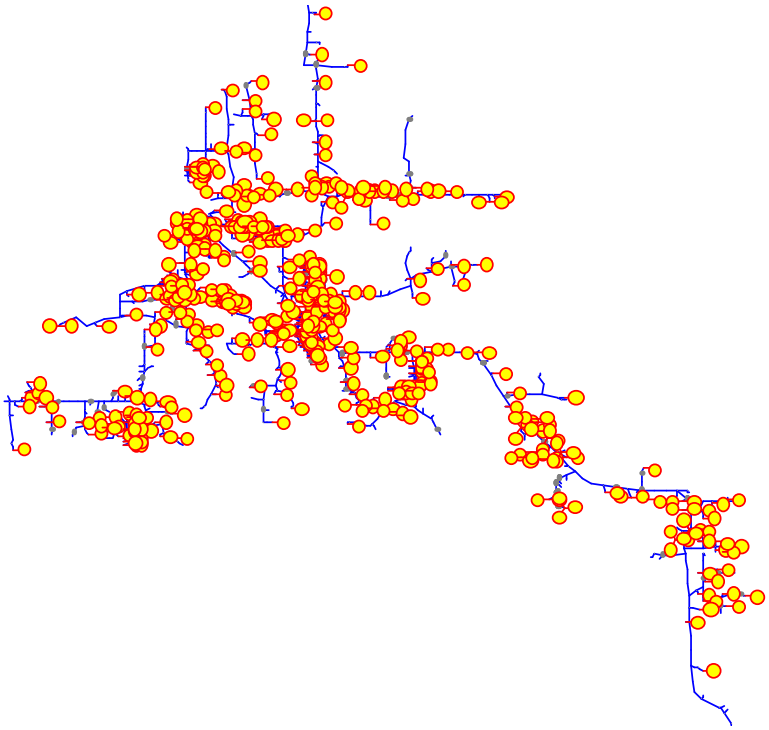


Figure 3.15. Base distribution circuit model with 2.5 MW of small roof-top solar PV modeled throughout the feeder (yellow circles indicate PV)

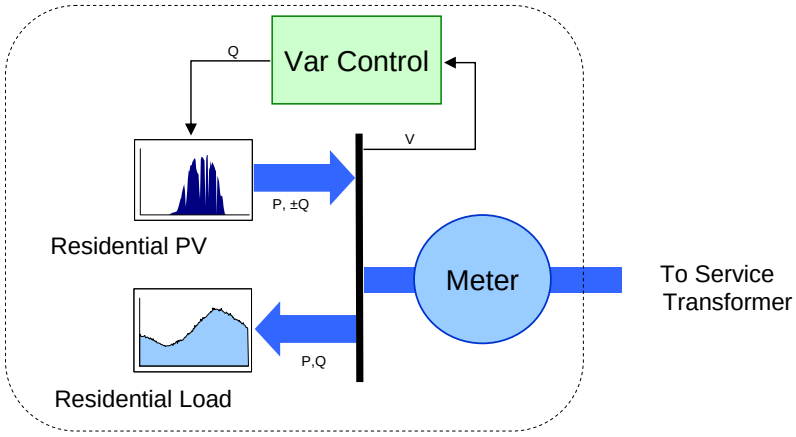


Figure 3.16. Volt-var control with inclusion of PV installation.

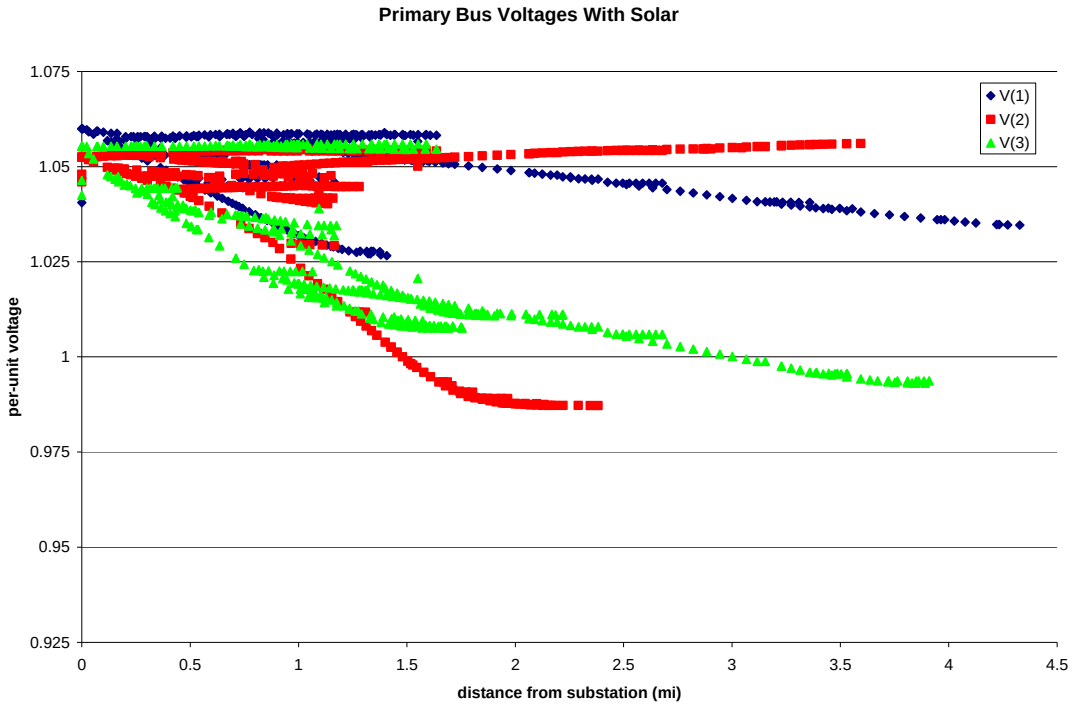


Figure 3.17. Simulated feeder voltage results with 2.5 MW of small roof-top solar PV modeled throughout the feeder.

D. Time-Series Simulated Case Study of a 10-MW System Modeled with 40% PV Penetration Level

Figure 3.18 shows a 12-kV, 10-MW feeder example. The system consists of 1800 customer loads with 17 miles on 3-phase primary and 115 miles on single-phase primary distribution lines. Assuming a 40% of peak load penetration of PV with respect to peak load, PV customers are randomly selected throughout the entire feeder. A time-series simulation is then performed on the feeder, considering three separate scenarios:

- Basecase - no PV
- 40% PV, no-volt/var control
- 40%PV, each PV system with autonomous volt/var control

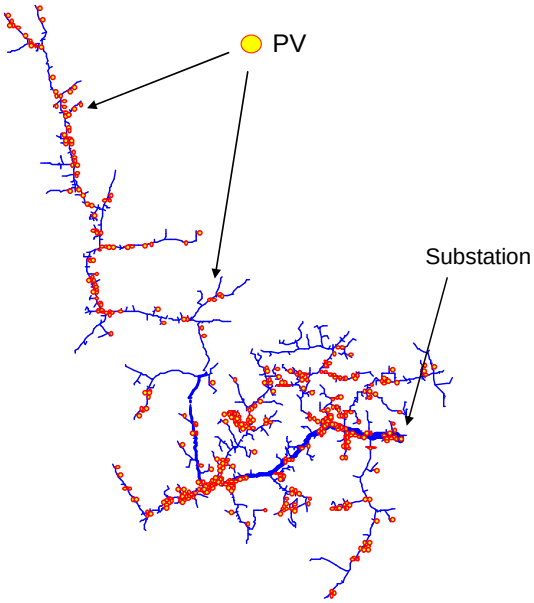


Figure 3.18. Example 10-MW system with 40% of peak load PV penetration.

Figure 3.19 shows the profile of a typical single customer load and PV source with peak load at 7.5 kW and peak PV power production at 4 kW.

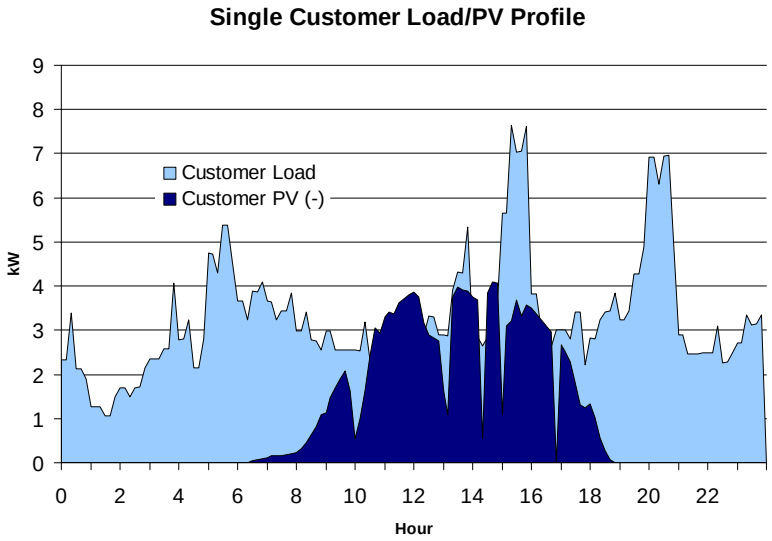


Figure 3.19. Single customer load and PV source profile.

Figure 3.20 shows simulated primary voltage profiles with and without PV penetration and with and without volt-var control. The "green" curve is the baseline without PV penetration. Under heavily loaded conditions, the voltage dips below 0.92pu. With 40% PV penetration, the voltage level, shown in the "blue" curve, increases but fluctuates with the cloud movement. By adding volt-var control, the voltage level, shown in the "red" curve, stabilizes with a much narrower band. The minimum voltage level stays above 0.95pu, and the maximum voltage does not exceed 1pu.

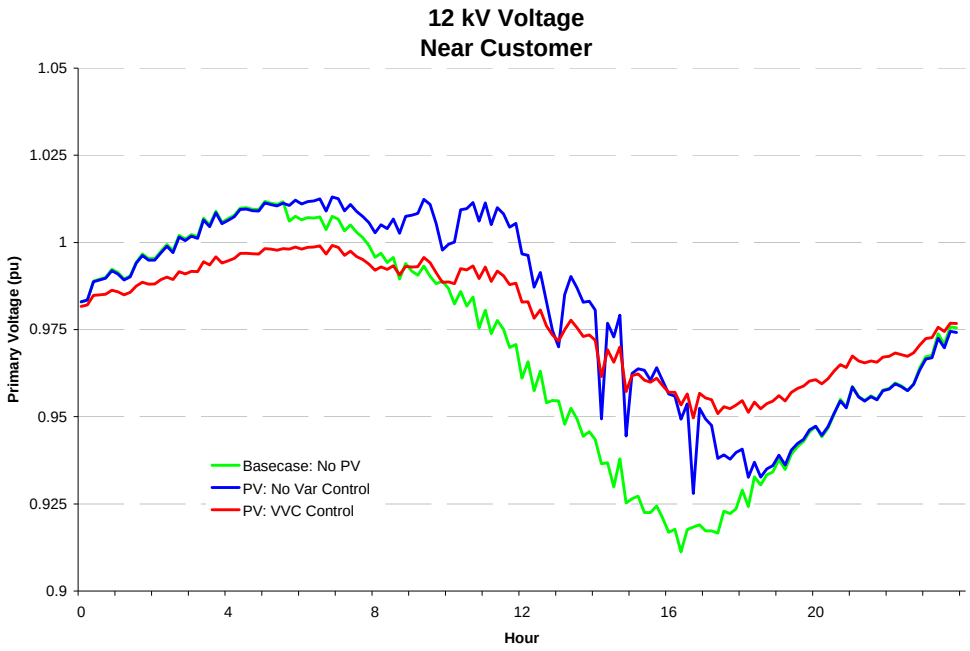


Figure 3.20. Voltage profile with and without PV penetration and var control.

Figure 3.21 shows the real power and reactive power injection that helps stabilize the voltage level. The injected reactive power depends on the voltage level. If the voltage level is within the "deadband," there is no need to inject reactive power.

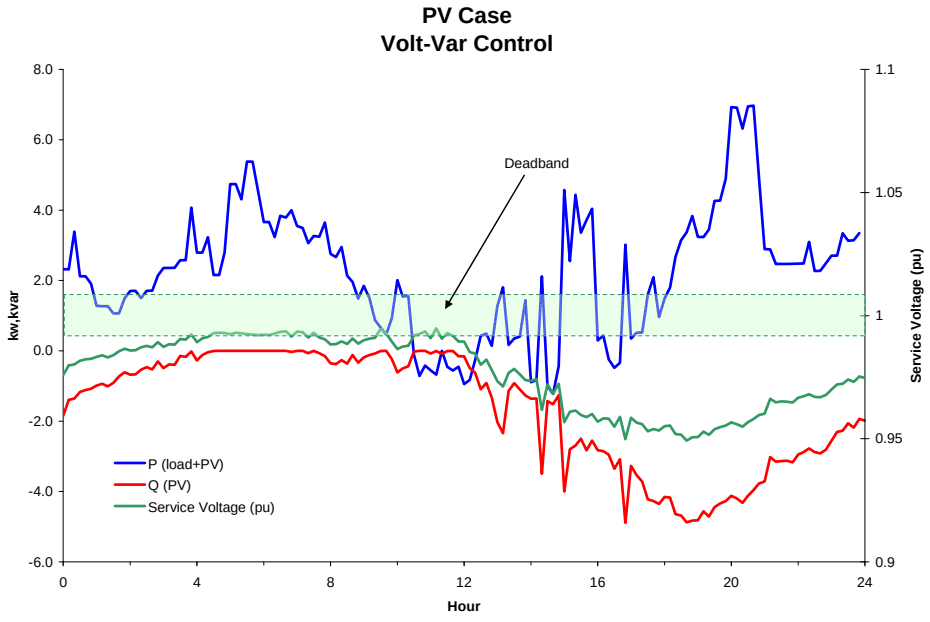


Figure 3.21. Voltage profile with var control.

4. TESTING POWER SYSTEM INTERACTION WITH PV PCS

The grid interface tests for PV power conditioners highlight not only the grid interconnection capabilities of the system, but also its response to various power quality related events and conditions that may occur in the distribution feeder. IEEE 1547 provides a set of guidelines and requirements for devices connected to the grid and supplying power to a load. Important grid handshaking requirements related to the PV inverters were tested under this task. The objectives of these tests were:

1. To characterize the performance of the inverter and verify that it meets the manufacturer's specifications.
2. To uncover any application issues that will be valuable to the end user.
3. To determine the device's ability to disconnect from the grid based on events specified in IEEE 1547.
4. To determine if there are any power quality related concerns, such as excessive inrush, harmonics, or dc injection.

4.1 Test Setup

Test setups to evaluate the grid integration of the SB5000US inverter from SMA have been developed in EPRI's Knoxville laboratory. The setup is capable of testing an inverter in a 208V, 240V, and 480V configuration. For all the testing performed, the 240V residential setting was used. A block diagram level schematic of the test setup is shown in Figure 4.1.

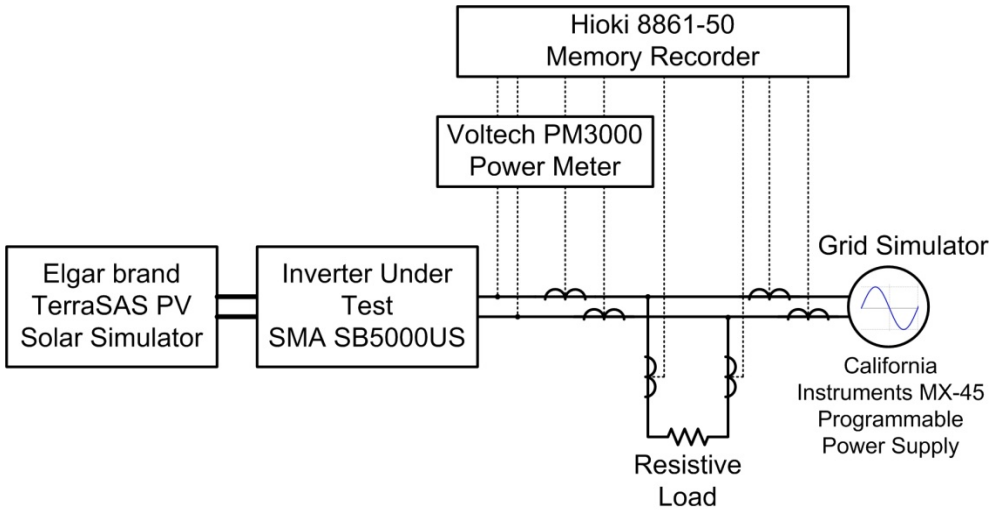


Figure 4.1. Block diagram of test setup

This test setup employed a California Instruments MX-45 programmable power supply as the grid simulator supplying 240-V, 60-Hz AC output. For all tests except harmonics, the MX-45 was in the circuit. For the harmonics testing, the test setup was powered by an external 50 kVA 480/240 V residential transformer. The EPRI Sag Generator was placed in series with the MX-45, performing no duties until sag and swell tests were performed. While in bypass mode, the Sag Generator did not have any impact on the circuit, it merely passed the voltage through. The PV inverter received its DC voltage from a PV simulator. The load for the test was a simple

resistive load of 10 kW. Even though the inverter was rated for 5 kW, because of the inclusion of MX-45, the load was increased to prevent the inverter from back-feeding the source. Data was recorded for input voltage and current, PV output voltage and current, and load voltage and current.

As shown in Figure 4.2, EPRI installed an Elgar brand TerraSAS PV Solar Simulator in the PV test area of its Knoxville laboratory. This rack-mounted system provides an easily programmable means of simulating the response of a PV array and can generate multiple user-defined IV curves so that inverters and charge controllers can be tested under repeatable conditions. Moreover, the system can be programmed for any PV module, and simulated modules can be grouped in series/parallel combinations to form a desired PV array simulation that, for example, characterizes the MPPT algorithm with a power source.

The simulator's key specifications include:

- Two PV simulated channels (expandable to four);
- Ethernet-based remote control;
- DC open circuit voltage, V_{oc} of up to 600 V DC per channel;
- DC short circuit current, I_{sc} of up to17 A per channel;
- 5 kW maximum output power at fill factor of 1.0 (10 kW total); and
- -40°C to 90°C temperature simulation range.

Figure 4.2. The TerraSAS PV solar simulator in EPRI's Knoxville lab.

Figure 4.3 is a photograph of the actual test setup employed in laboratory for the inverter grid interface tests. Figure 4.4 shows the EPRI sag generator which was used for the sag and swell tests. EPRI designed and developed portable three phase voltage sag generators for on-site power

quality tests. This unit allows a quick assessment of the ride-through characteristics of connected loads by controlling the magnitude and duration of voltage sags. It operates at any nominal voltage between 100 and 480 V and can carry current up to 200 A. Its built-in data acquisition system instantly displays voltages, currents, and other user-connected signals after every sag event. Using this custom-engineered test equipment, EPRI has tested hundreds of manufacturing processes, semiconductor tools, machine tools, and devices since 1994.

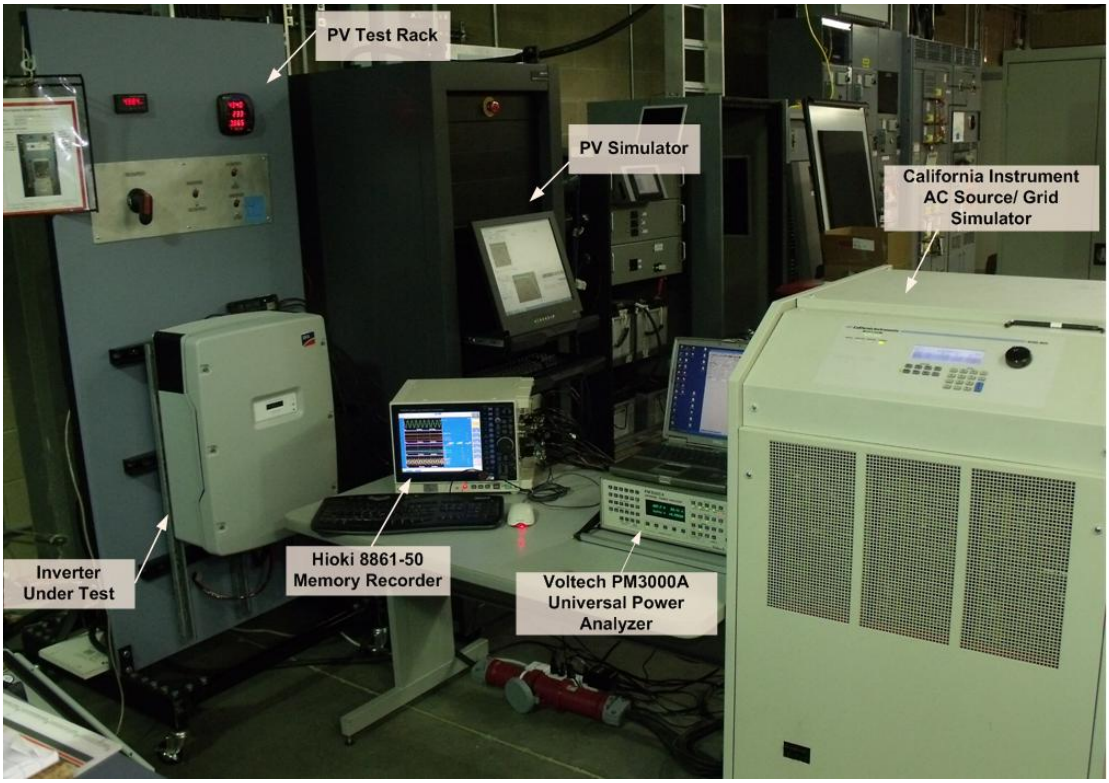


Figure 4.3. **Actual test setup in the PV test area of EPRI's Knoxville laboratory.**

Figure 4.4. EPRI's sag generator.

4.2 Response to Abnormal Voltage Conditions

The first group of tests was used to determine how the PV inverter reacted to abnormal voltage conditions. IEEE 1547 describes how grid interconnected distributed resources (DR) should monitor and react to abnormal conditions. Table 4-1 lists the voltage levels and clearing times required for interconnected devices.

Table 4.1. Response requirements to abnormal voltages

Voltage Range (% of Nominal Voltage)	Clearing Time for DG ≤ 30kW
V < 50%	0.16s
50% ≤ V < 88%	2.00s
110% < V < 120%	1.00s
V ≥ 120%	0.16s

IEEE 1547.1 is the standard used to test the unit for compliance to the IEEE 1547 standard. For the purpose of these tests, the test methodology outlined in IEEE 1547.1 was followed for tests relating to interconnection.

A. Over-Voltage Test

The first test performed evaluated the response of the PV inverter to over-voltage conditions. The objective of this test is to determine if the inverter can sense an over-voltage condition and clear within the specified time. The inverter has two over-voltage set points. The first is at 110%

of nominal voltage (264 V) and the second is at 120% of nominal voltage (288 V). The test method involved ramping the voltage higher at a set ramp rate, based on the accuracy of the inverter. The manufacturer's stated accuracy being ±2% of nominal grid voltage (4.8 V) and ±0.1% of nominal trip time gives a ramp rate of 1.29 V/s. Once the ramp rate had been determined, the MX-45 was programmed according to the test protocol. The test was repeated five times and Table 4-2 lists the test results of five over-voltage conditions.

Table 4.2. Over-voltage test results

Over voltage test	Trip voltage (V)
1	262.49
2	262.28
3	262.08
4	262.66
5	261.67
Average over-voltage trip limit	262.24

Based on the manufacturer's stated accuracy of 4.8 V, the unit should have tripped between 259.2 and 268.8 V. As shown by the test results, the unit's average trip voltage was 262.24 V which is within the stated accuracy of the PV inverter. Figure 4.5 shows both the instantaneous and RMS line input voltage, and the inverter output current during the over-voltage ramp test. During the over-voltage ramp conditions, the inverter output current went to zero once the voltage had ramped to the trip point. As tested, the inverter was found to be in compliance with IEEE 1547.

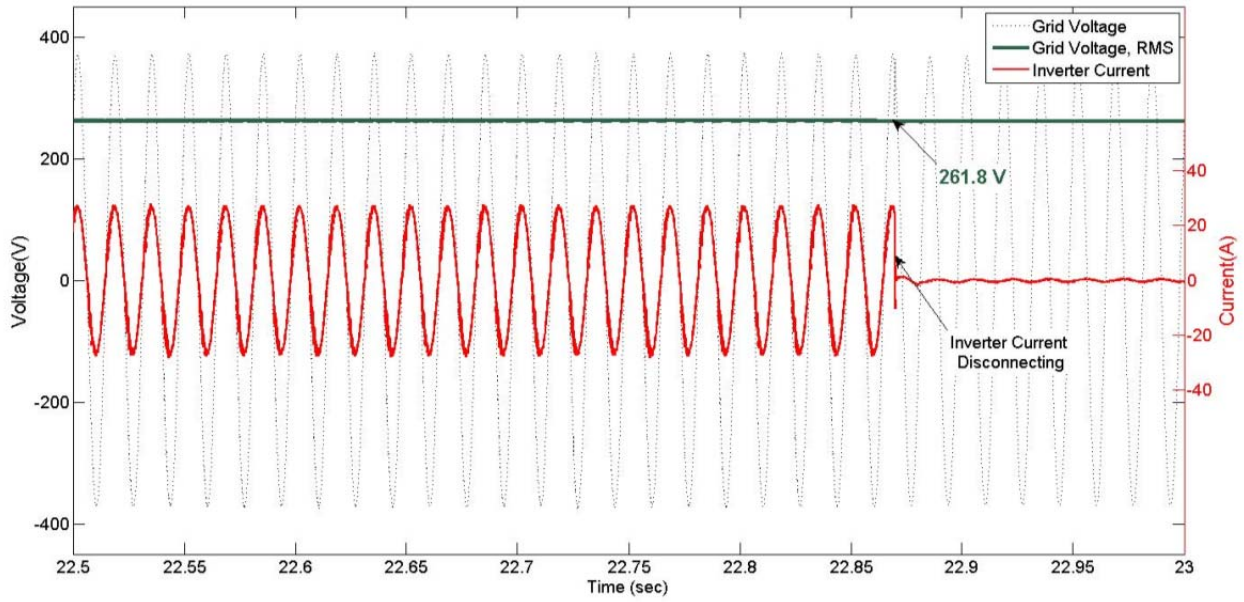


Figure 4.5. Grid voltage and inverter current during over-voltage magnitude test.

B. Under-Voltage Test

The second test performed evaluated the response of the PV inverter to under-voltage conditions. The purpose of this test was to determine if the inverter can sense an under-voltage condition, and clear within the specified time. The inverter has two under-voltage set points. The first is at 88% of nominal voltage (211 V) and the second is at 50% of nominal voltage (120 V). The same test methodology was followed to test the under-voltage trip magnitude as was used during the over-voltage testing. The test involved ramping the voltage lower, at a set ramp rate, based on the accuracy of the inverter. The manufacturer's stated accuracy being ±2% of nominal grid voltage (4.8 V) and ±0.1% of nominal trip time allows a ramp rate of 0.599 V/s. The difference in ramp rates is based on the trip time and sensitivity of the two test points. For 110% of nominal, the unit has to clear in one second. For 88% of nominal, the unit has two seconds to clear. Once the ramp rate had been determined, the MX-45 was programmed according to the test protocol. The test was repeated five times. Table 4-3 contains the results of these under-voltage tests.

Table 4.3. Under-voltage test results

Under-voltage test	Trip voltage
1	211.07
2	210.89
3	211.41
4	211.35
5	211.14
Average under-voltage trip limit	211.17

Based on the manufacturer's stated accuracy of 4.8 V, the unit should have tripped between 206.4 V and 216 V. As shown by the test results, the unit's average trip voltage was 211.17 V, within the stated accuracy of the PV inverter. Figure 4.6 shows both the instantaneous and RMS line input voltage and the inverter output current during the under-voltage ramp test. As shown in the figure, during the under-voltage ramp condition, the inverter output current went to zero once the voltage had ramped down to the trip point. As tested, it was found to be in compliance with IEEE 1547.

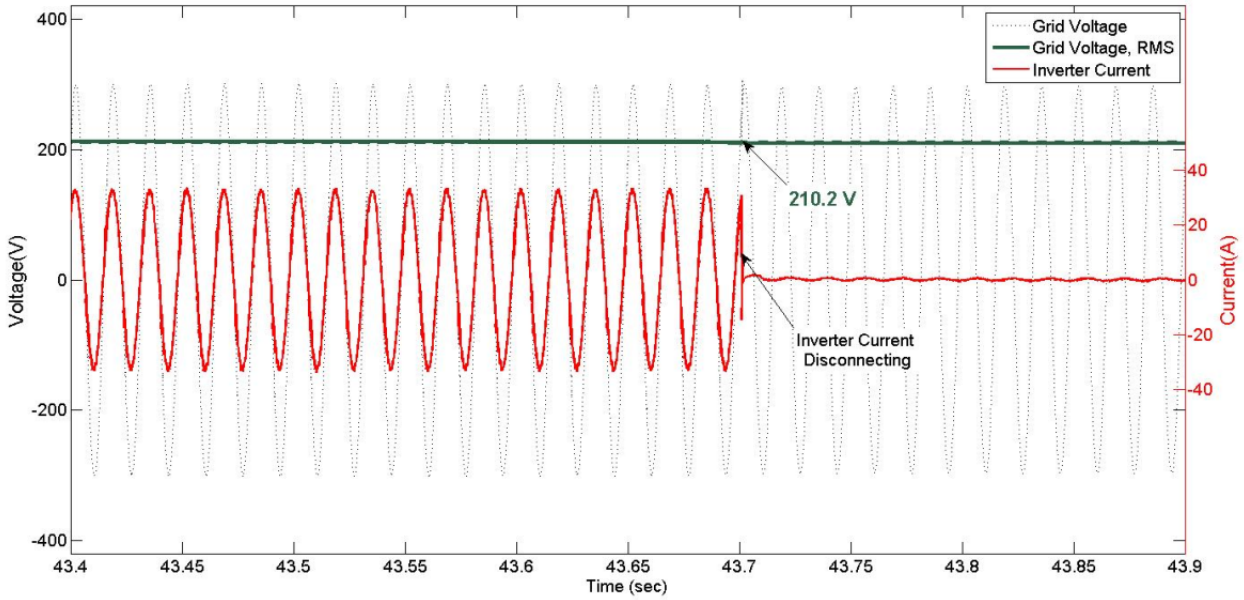


Figure 4.6. Grid voltage and inverter current during under-voltage trip conditions.

C. Over-Voltage Trip Time

The third test evaluated the trip time response of the inverter due to over-voltage. The purpose of the test was to determine the time that the inverter under test takes to disconnect from grid in response to an instant voltage transition to a point above the trip settings.

The over-voltage trip time may be tested at both the higher and lower trip points since the transition is instantaneous and not a ramp function. The PV inverter has a timer accuracy of ±0.1% of nominal trip time. For the over-voltage set points, those times are a maximum of 0.1602 seconds for 120% of nominal voltage, and 1.001 seconds at the 110% test point. The test was performed according to the test procedure outlined in IEEE 1547.1. The MX-45 was able to raise the voltage from the holding point to beyond the trip point within a cycle. Once the voltage transitioned, the time was measured from that point until the point at which the inverter current went to zero, indicating that it had disconnected from the grid. After the tests were performed, the data was analyzed to determine if the unit was able to clear during its required time. Tables 4-4 and 4-5 show the over-voltage trip test results at 110% and 120% over-voltage conditions.

Table 4.4. 110% trip point test results

110% Voltage Test	Trip time (s)
1	0.696
2	0.730
3	0.527
4	0.713
5	0.666
Average under-voltage trip limit	0.666

Table 4.5. 120% trip point test results

120% Voltage Test#	Trip time(s)
1	0.061
2	0.042
3	0.038
4	0.053
5	0.051
Average under-voltage trip limit	0.049

For the 110% trip time test, the unit was required to disconnect from the grid within 1.001 seconds. According to the average test results, the unit disconnected in 0.666 seconds. For the 120% trip time test, the unit is required to disconnect from the grid within 0.1602 seconds, and it did so within 0.049 seconds. Based on the test results, the unit performed as required by the IEEE 1547 standard. Figure 4.7 shows the grid voltage and inverter current for 110% over-voltage clearing time test.

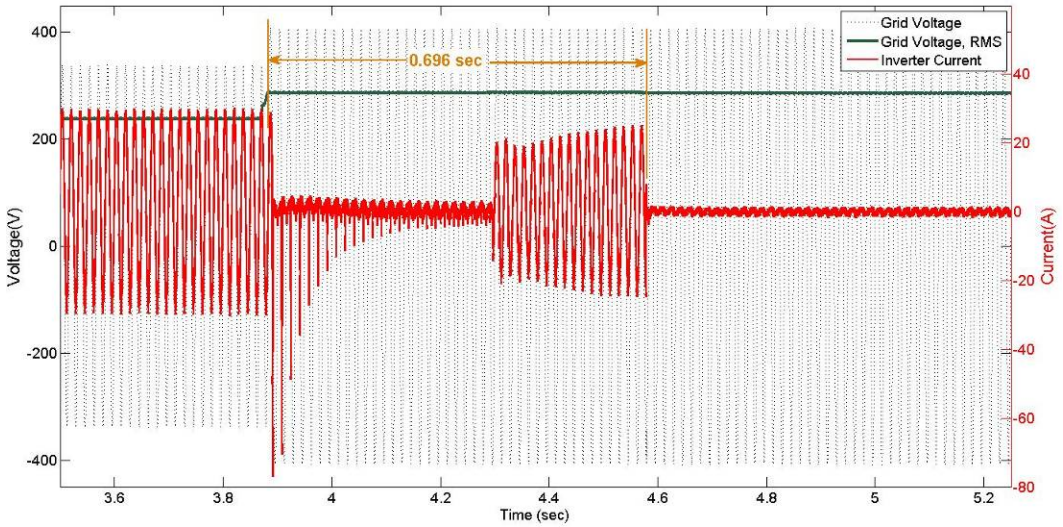


Figure 4.7. Grid voltage and inverter current for 110% over-voltage trip time test.

D. Under-Voltage Trip Time

The fourth test evaluated the trip time response of the inverter due to under-voltage. The purpose of the test was to transition the voltage instantly to a point below the trip settings and calculate the time it takes to disconnect from the grid. By measuring the time difference, the accuracy of the time trip setting could be measured.

The under-voltage trip time was tested at both the higher and lower trip points since the transition is instantaneous, and not a ramp function. The PV inverter has a timer accuracy of ±0.1% of nominal trip time. For the under-voltage set points, those times are a maximum of 0.1602 seconds for the 50% of nominal point, and 2.002 seconds at the 88% test point. The test was performed according the test procedure outlined in IEEE 1547.1. The MX-45 was able to lower the voltage from the holding point to beyond the trip point within a cycle. Once the voltage transitioned, the time was measured from that point until the point at which the inverter current went to zero, indicating that it had disconnected from the grid. After the tests were performed, the data was analyzed to determine if the unit was able to clear during its required time. Tables 4-6 and 4-7 show the trip time test results with 88% and 50% under-voltage conditions, respectively.

Table 4.6. 88% under-voltage trip point test results

88% voltage test	Trip time (s)
1	1.79
2	1.77
3	1.77
4	1.78
5	1.77
Average under-voltage trip limit	1.78

Table 4.7. 50% under-voltage trip point test results

50% voltage test	Trip time (s)
1	0.179
2	0.176
3	0.168
4	0.128
5	0.131
Average under-voltage trip limit	0.156

For the 88% trip time test, the unit was required to disconnect from the grid within 2.002 seconds. According to the average test results, the unit disconnected in 1.78 seconds. For the 50% trip time test, the unit is required to disconnect from the grid within 0.1602 seconds, and it did so within 0.156 seconds. Based on the test results, the unit performed as required by the IEEE 1547 standard. Figure 4.8 shows the grid voltage and inverter current for 88% over-voltage clearing time test.

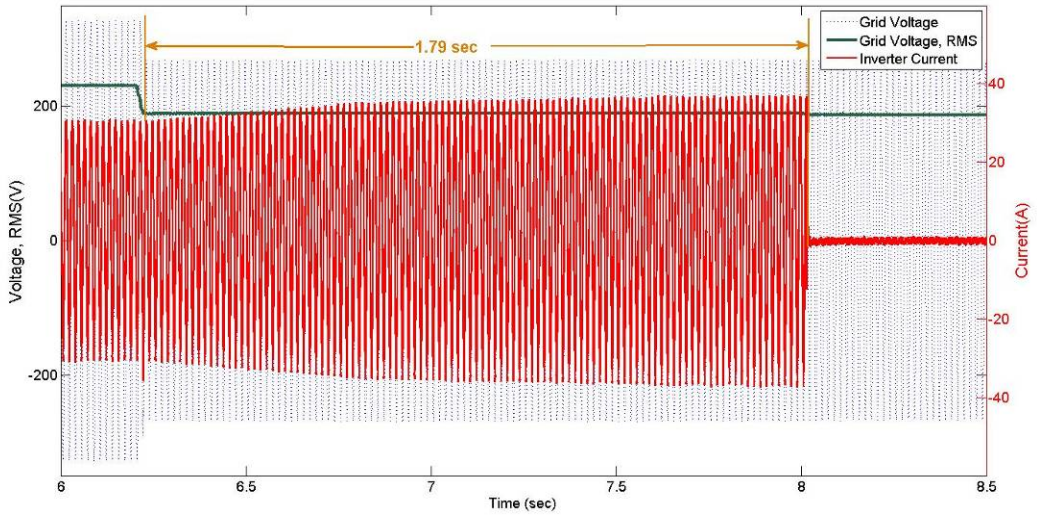


Figure 4.8. Grid voltage and inverter current for 88% under-voltage trip time test.

4.3 Response to Abnormal Frequency Conditions

The second group of tests determined how the PV inverter reacts to abnormal frequency conditions. IEEE 1547 describes how grid-interconnected distributed resources (DR) should monitor and react to abnormal conditions. An abnormal frequency condition is any condition in which the grid frequency falls outside of a certain range. During these conditions, any DR that is connected to the grid must sense the disturbance and disconnect from the grid until conditions return to normal. Table 4-8 shows the frequency ranges and clearing times required for interconnected devices. The PV inverter, being an interconnected device which supplies power, falls in this category.

Table 4.8. Response requirements to abnormal frequency condition

Frequency range (Hz)	Clearing time
Frequency > 60.5	0.16s
Frequency < 59.3	0.16s

As opposed to the voltage variations, there is only a single upper and lower set point and clearing time. The trip times are relatively fast, requiring clear times in milliseconds as opposed to seconds.

A. Over-Frequency Test

The first frequency test performed evaluated the response of the PV inverter to over-frequency conditions. The purpose of this test was to determine if the inverter can sense an over-frequency condition and clear within the specified time. The inverter has one over-frequency set point at 60.5Hz, with an accuracy of ±0.1% of nominal frequency (0.06 Hz). The test method involves ramping the frequency higher, at a set ramp rate, based on the accuracy of the inverter. The manufacturer's stated accuracy being ±0.1% of nominal grid frequency (0.06 Hz) and ±0.1% of nominal trip time allows a ramp rate of 0.094 Hz/s. The MX-45 was programmed with the required ramp rate and the frequency was raised accordingly. The test was repeated five times and the results are shown in Table 4-9.

Table 4.9. Over-frequency test results

Over-frequency test	Trip frequency
1	60.46
2	60.39
3	60.39
4	60.39
5	60.42
Average over-frequency trip limit	60.41

The IEEE 1547 standard indicates that it must clear at 60.5 Hz. The accuracy of the inverter allows a 0.06 Hz window in which the unit will clear. The average of the five tests indicates that the unit was below the trip point and in compliance with IEEE 1547. Figure 4.9 shows the frequency of grid voltage and inverter current during one of the over-frequency magnitude tests. As shown in Figure 4.9 the inverter was able to disconnect during the over-frequency test. The frequency of the cycle was measured over one cycle once the inverter had tripped offline.

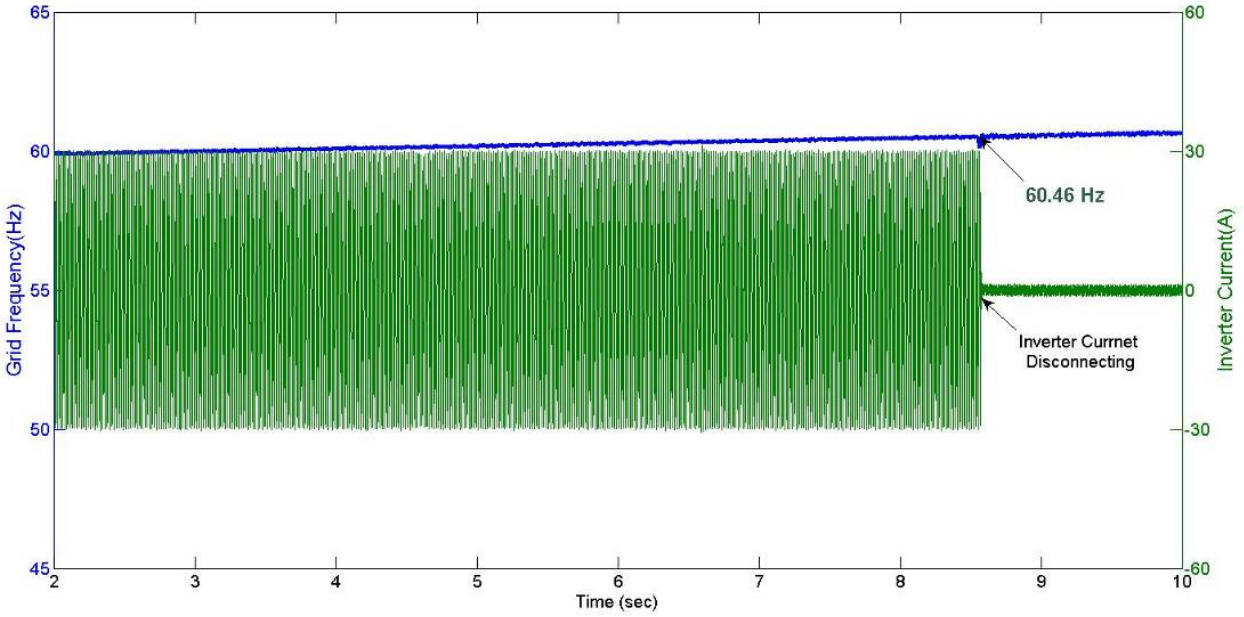


Figure 4.9. Grid voltage and inverter current during over-frequency test.

B. Under-Frequency Test

The second frequency test performed evaluated the response of the PV inverter to under-frequency conditions. The purpose of this test was to determine if the inverter may sense an under-frequency condition and clear within the specified time. The inverter has one under-frequency set point at 59.3.5Hz, with an accuracy of ±0.1% of nominal frequency (0.06 Hz). The test method involves ramping the frequency lower, at a set ramp rate, based on the accuracy of the inverter. The manufacturer's stated accuracy, being ±0.1% of nominal grid frequency (0.06Hz) and ±0.1% of nominal trip time, allows a ramp rate of 0.094Hz/s. The MX-45 was programmed with the required ramp rate and the frequency was lowered accordingly. The test was repeated five times and the results are shown in Table 4-10.

Table 4.10. Under-frequency magnitude test results

Under-frequency test	Trip frequency
1	59.31
2	59.45
3	59.31
4	59.42
5	59.35
Average under-frequency trip limit	59.37

The IEEE 1547 standard indicates that it must clear at 59.3 Hz. The accuracy of the inverter allows a 0.06 Hz window in which the unit must clear. The average of the five tests indicates that the unit was below the trip point and in compliance with IEEE 1547. Figure 4.10 shows the grid voltage and inverter current during one of the under-frequency tests. As shown, the inverter

current was able to disconnect during the under-frequency test. The frequency of the cycle was measured during the time it tripped.

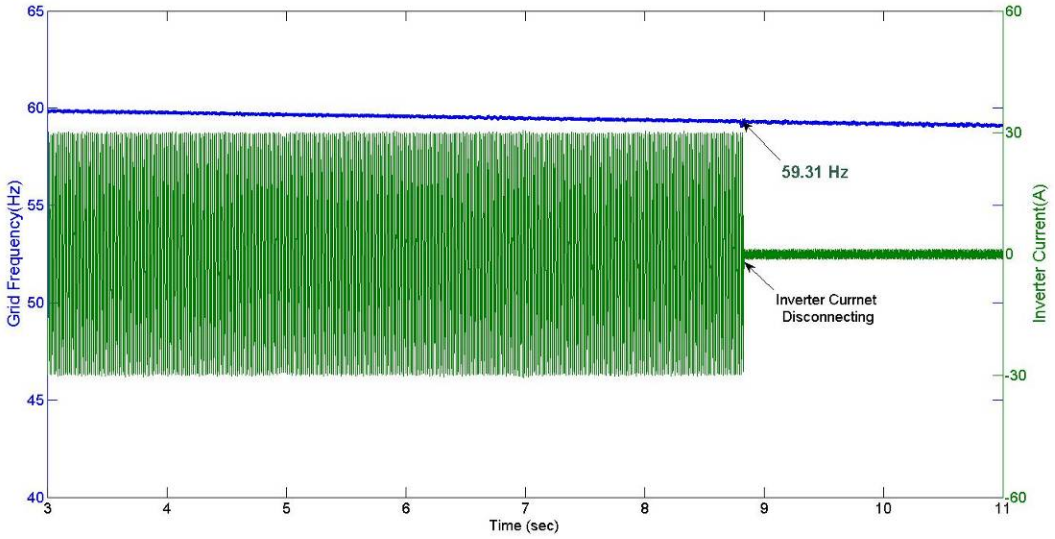


Figure 4.10. Grid voltage and inverter current during under-frequency test.

C. Over-Frequency Trip Time

The third frequency test evaluated the trip time response of the inverter. The purpose of the test was to transition the frequency instantly to a point beyond the trip settings and calculate the time it takes to disconnect from the grid. By measuring the time difference, the accuracy of the time trip setting could be measured. The PV inverter has a timer accuracy of ±0.1% of nominal trip time. For the over-frequency set points, that time is a maximum of 0.1602 seconds.

The test was performed according the test procedure outlined in IEEE 1547.1. The MX 45 was able to raise the frequency from the holding point to beyond the trip point within a cycle. Once the frequency transitioned, the time was measured from that point until the point at which the inverter current went to zero, indicating that it had disconnected from the grid. Table 4-11 shows the over-frequency trip point test results.

Table 4.11. Over-frequency (60.5Hz) trip point time test results

Over-frequency trip time test	Trip Time (s)
1	0.1099
2	0.10982
3	0.10989
4	0.10991
5	0.10979
Average over-frequency trip limit	0.109862

The unit is required to disconnect from the grid within 0.16 seconds. According to the average test results, the unit disconnected in 0.109 seconds. Based on the test results, the unit performed as required by the IEEE 1547 standard. Figure 4.11 presents the grid voltage frequency and inverter current for one of the five over frequency trip time tests.

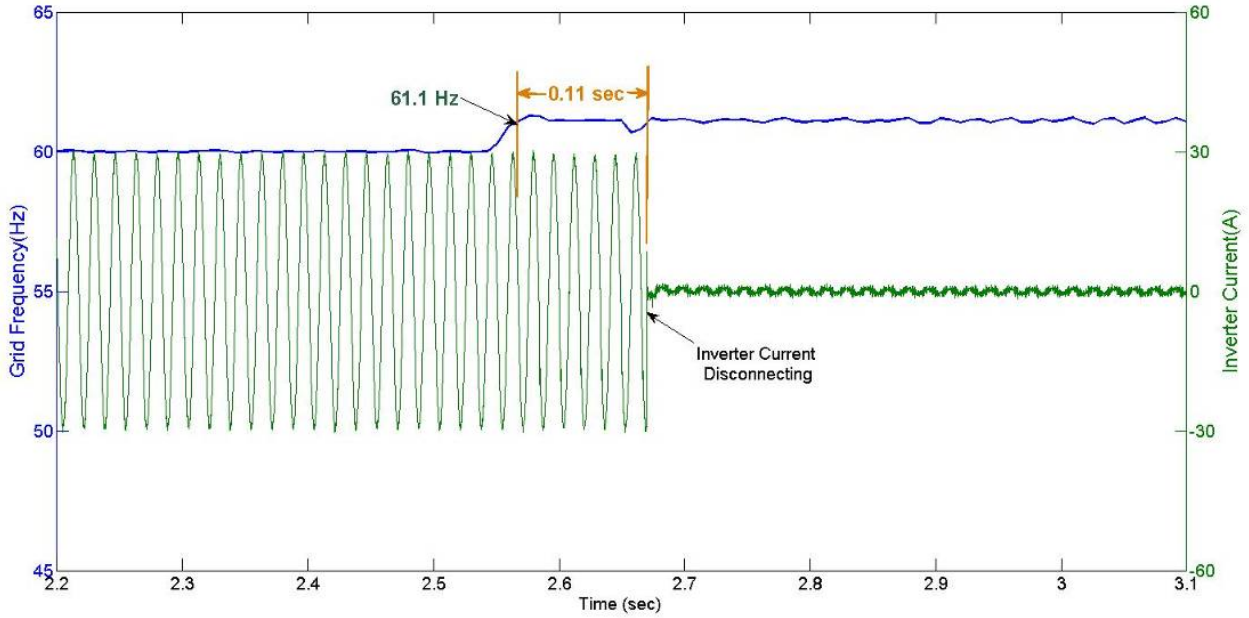


Figure 4.11. Grid voltage frequency and inverter current for over frequency trip time test.

D. Under-Frequency Trip Time

The fourth frequency test evaluated the lower trip time response of the inverter. The purpose of the test is to transition the frequency instantly to a point below the trip settings and calculate the time it takes to disconnect from the grid. By measuring the time difference, the accuracy of the time trip setting can be measured. The PV inverter has a timer accuracy of ±0.1% of nominal trip time. For the under-frequency set points, those times are a maximum of 0.1602 seconds. The test was performed according the test procedure outline in IEEE 1547.1. The MX-45 was able to lower the frequency from the holding point to beyond the trip point within a cycle. Once the frequency transitioned, the time was measured from that point until the point at which the inverter current went to zero, indicating it had disconnected from the grid. After the tests were performed, the data was analyzed to determine if the unit was able to clear during its required time. Table 4-12 shows the time results from these tests. The unit was required to disconnect from the grid within 0.16 seconds.

Table 4.12. Under-frequency (59.3 Hz) trip time test results

Under-frequency test	Trip time (s)
1	0.12066
2	0.11406
3	0.13066
4	0.11392
5	0.13073
Average under-frequency trip time limit	0.122006

According to the average test results, the unit disconnected in 0.122 seconds. Based on the test results, the unit performed as required by the IEEE 1547 standard. Figure 4.12 presents the grid voltage frequency and inverter current for one of the five under frequency trip time tests.

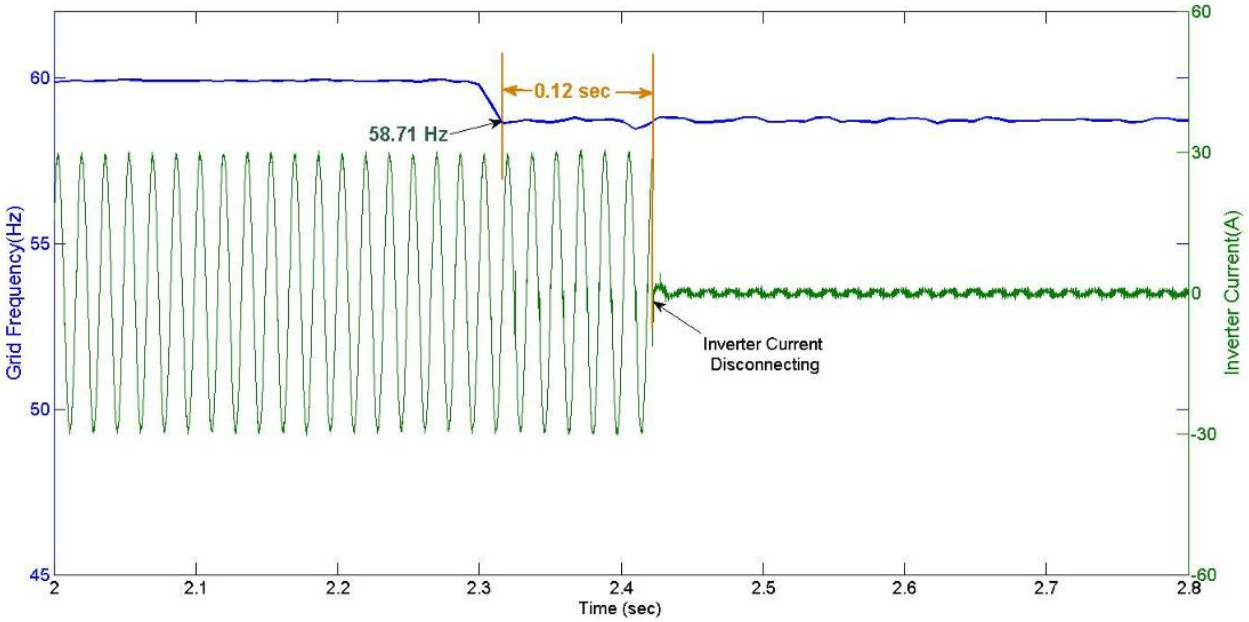


Figure 4.12. Grid voltage frequency and inverter current for under-frequency trip time test.

E. Sag Immunity

A voltage sag is defined as a decrease in RMS voltage magnitude lasting from 0.5 to 30 cycles. Voltage sags are usually caused by a fault in the utility transmission or distribution system. Such power-line faults can be caused by animals on lines, a car striking a utility pole, or lightning strikes to power lines. Although proper maintenance, grounding, and arresters can minimize the number of faults, faults can never be eliminated completely.

While the voltage magnitude and timer test were used to test for the IEEE 1547 standard, voltage sag testing was performed as well to determine a voltage sag ride-through curve and to determine how the inverter reacts in potential sag situations that occur in residential settings. For testing purposes, a voltage sag generator was placed in series with the source and the load. Phase-to-phase sags affecting both legs of the 240-V source were injected into the system. Voltage sags were injected on the line in varying lengths from 1 cycle to 130 cycles. The results were recorded and are shown in Table 4-13.

Sag test results revealed that the unit performed as expected, indicating a further confirmation of the ability of the unit to detect voltage variations and disconnect from the grid. The results were graphed to develop a ride-through curve. This curve displays a region of both online and offline performance. Figure 4.13 shows the resulting voltage ride-through curve generated using the sag test responses of the specific inverter unit under test.

As shown in both the graph and the table, the inverter had a predictable ride-through curve based on the expected results from IEEE 1547 requirements. The areas shaded in green indicate the durations and magnitudes of sags that the unit encountered during testing while continuing to operate. The areas in red are those areas that the inverter tripped and disconnected from the grid, based on their duration and magnitude. As soon as the unit reached below 50% of nominal

voltage, it tripped within the required disconnect time of 10 cycles, as specified by IEEE 1547. However, down to 50% of the nominal voltage, or 120 V line voltage, the unit remained connected to the grid at around 90 cycles.

Table 4.13. Phase to phase voltage sag results

% Nominal Voltage	Sag Duration in # of Cycles	Inverter Response
90	110	**Tripped**
90	105	
85	105	**Tripped**
85	100	
80	100	
75	100	**Tripped**
75	95	
70	95	
65	95	
60	95	
55	95	
50	95	**Tripped**
45	9	**Tripped**
45	8	
40	8	**Tripped**
40	5	
35	5	**Tripped**
35	3	**Tripped**
35	1	
0	1	

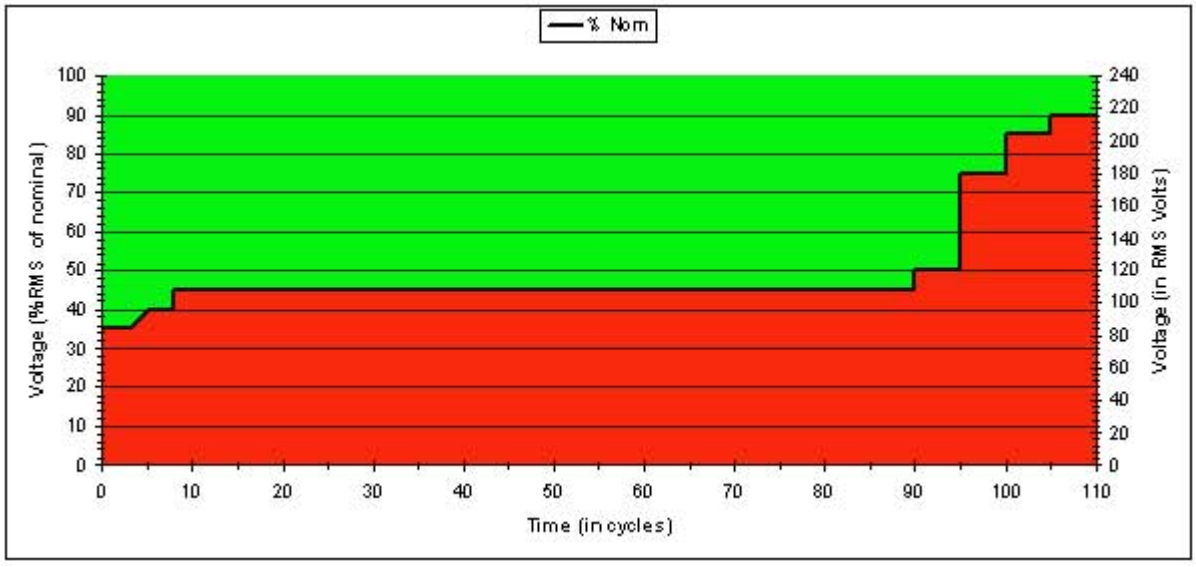


Figure 4.13. Low voltage ride-through curve for the inverter under test.

F. Swell Immunity

A voltage swell is a momentary rise in the line voltage. While not as common as voltage sags, they do occur in real world scenarios. The inverter has protection in place for over-voltage conditions from 110% to 120% of nominal. Testing occurred from 1 to 60 cycles, from 105% of nominal to 125% (the sag generator's limit). The results of the testing are shown in Table 4-14.

Table 4.14. Swell testing results

% Nominal Voltage	Swell Duration in # of Cycles	Inverter Response
105	60	**Tripped**
105	55	
110	55	
115	55	
120	55	**Tripped**
120	50	
125	50	**Tripped**
125	45	

As shown, the inverter failed to clear from the grid at the upper end of the trip settings. The trip setting for the inverter is 120% of nominal at 10 cycles. The inverter failed to turn off during a 45-cycle 125% of nominal swell.

G. Reconnect Following Abnormal Conditions

During all the tests performed in which the inverter disconnected, the unit would reconnect to the grid. Typically a time interval between five and six minutes is necessary to confirm that the grid is stable. This delay is based on IEEE 1547, Section 4.2.6 which specifies a fixed delay of five minutes to allow restoration of the grid within tolerance voltage and frequency. After the inverter has made this determination, it re-synchronizes with the grid and begins operating again. Figure 4.14 shows a reconnection after a trip due to abnormal voltage conditions.

The graph in Figure 4.14 shows the inverter current disconnecting from the grid during an event. Based on the time measurements, it took 5 minutes and 30 seconds to reconnect to the grid. If during an event, the voltage or frequency was to remain outside of normal operating conditions, the unit would not attempt to reconnect until five minutes after the restoration of nominal conditions. Based on testing, the unit complied with the required delay stated in IEEE 1547.

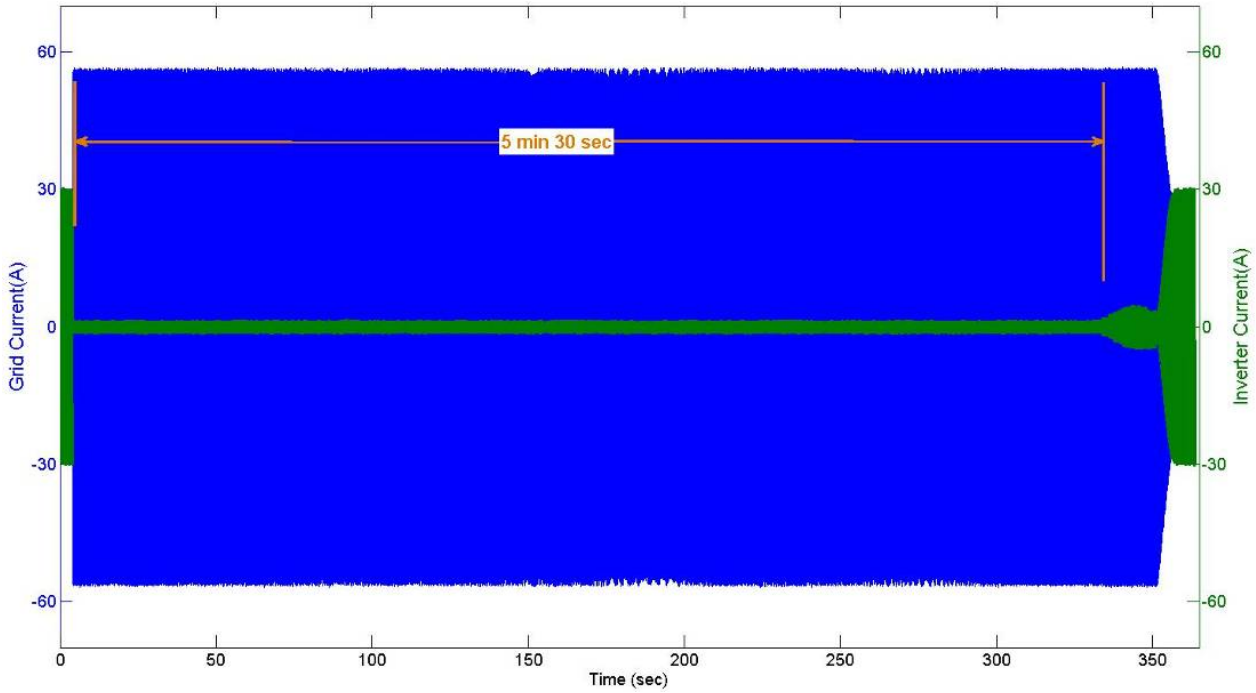


Figure 4.14. Reconnect after abnormal voltage condition

H. Determination of Inrush During Reconnect

During reconnection to the grid, there is the potential for inrush current to be present. This test is not specified by IEEE 1547; however, being a power quality concern it was tested. High inrush current has the potential to trip breakers, cause voltage sags, and blow fuses depending on the magnitude of the current. The unit was tripped offline, and waveform data was recorded during the reconnection. Figure 4.15 shows the current of the inverter and the grid during a reconnection.

Based on the recorded waveform, after the inverter re-connects to the grid, it takes approximately 8 to 10 seconds for the inverter to output at full power. The inverter has no discernible inrush during re-connection, and instead performs a slow ramp. The grid current can be seen reducing as the inverter current increases in this snapshot. Based on these observations, no level of inrush current is apparent that could be harmful to the unit or its operating environment.

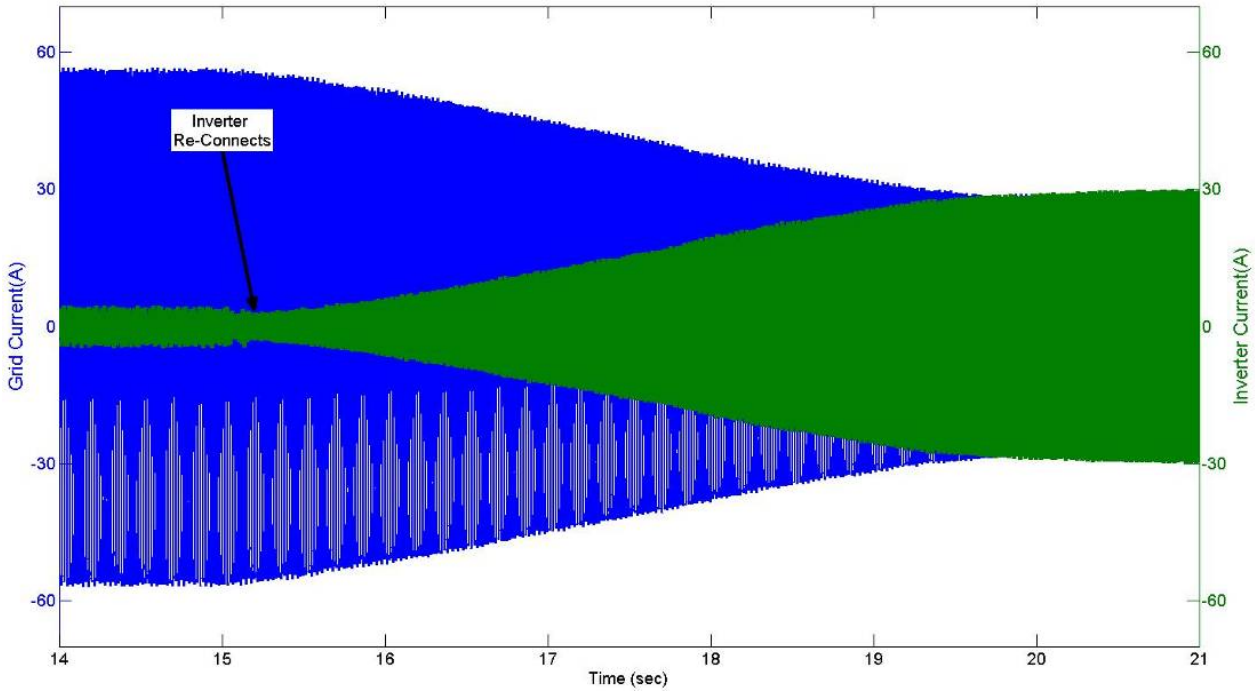


Figure 4.15. Inverter re-connecting to grid.

I. Harmonic Content

This test looks at the harmonic content present when the inverter is operating. For this test, the MX 45 was removed from the circuit and the test setup was wired to a 240-V panel similar to one that would be found in a residential setting. This was performed to accurately identify the inverters response in this type of setup. The upstream transformer is rated at 50 kVA.

The first part of the test involved the inverter being offline, with just the resistive load bank connected to the grid. The voltage and current connections were placed between the inverter and the disconnect breaker on the panel, to represent what an upstream meter would read. The load was set to 10 kW, and harmonic data was recorded for 10 minutes for a background harmonic profile. Figure 4.16 shows the 2^{nd} through 9^{th} harmonic content of the load with no inverter connected to the circuit. During this test, the average current over the test period was recorded at 38 amps, and the current THD was 4.4%.

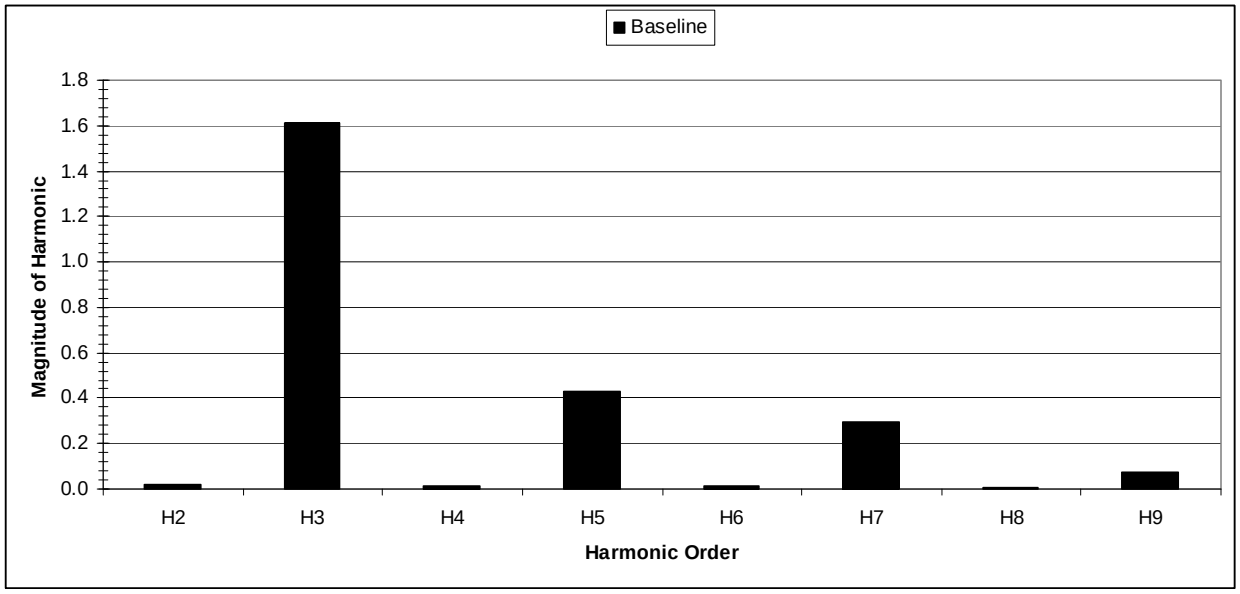


Figure 4.16. Harmonic content with no inverter online.

The second part of the test involved bringing the inverter online, and recording 10 minutes of data with the inverter supplying power. The load was kept at 10 kW, to ensure the inverter did not back feed the grid. Figure 4.17 contains the data recorded during this test.

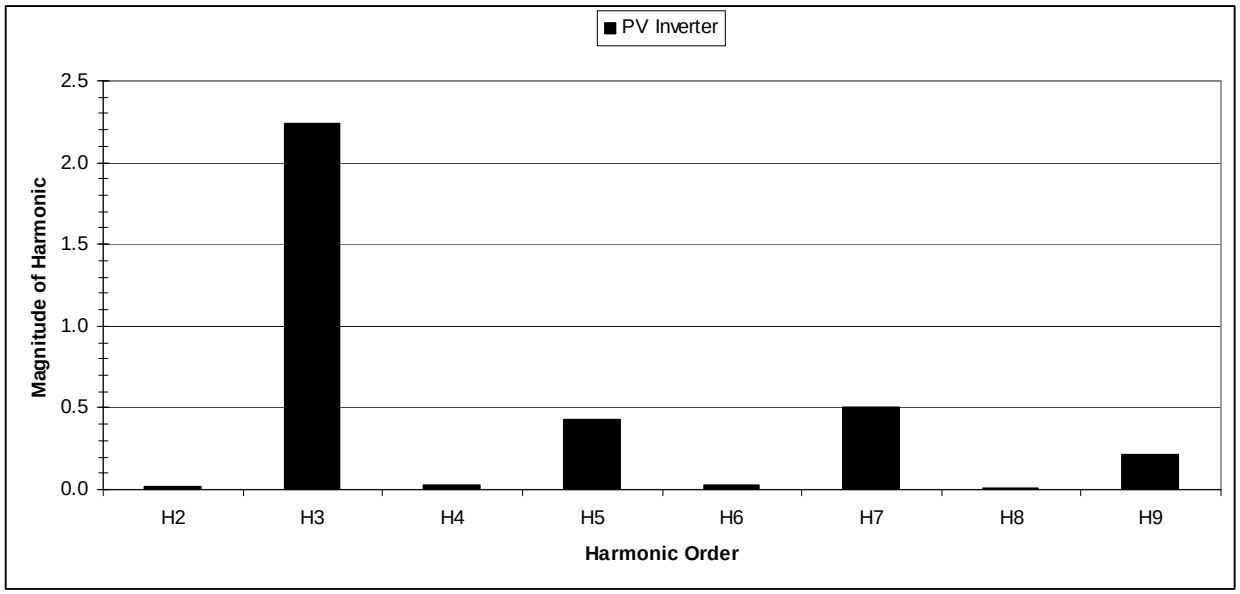


Figure 4.17. Harmonic content with the inverter online.

As shown above, the harmonics rose slightly with the inverter online as opposed to being disconnected from the grid. During the test, the current was measured to be 18 A, indicating that the inverter was supplying the remaining 20 A that was measured in the previous test. Table 4-15 shows the difference between the power measurements both with and without the inverter.

Table 4.15. Power measurements with and without PV inverter

	Voltage	Current	Power	PF	THD_i
No inverter	236.45	38.37	9.07	1.00	4.44%
With inverter	238.27	18.32	4.33	1.00	13.3%

With the inverter online, the current at the panel was reduced by 20 A, and the power was reduced by a little less than 5 kW. However, Figure 4.18 shows the combined harmonic plots. Based on the data taken, there is not a large increase in harmonics once the inverter is connected to the circuit.

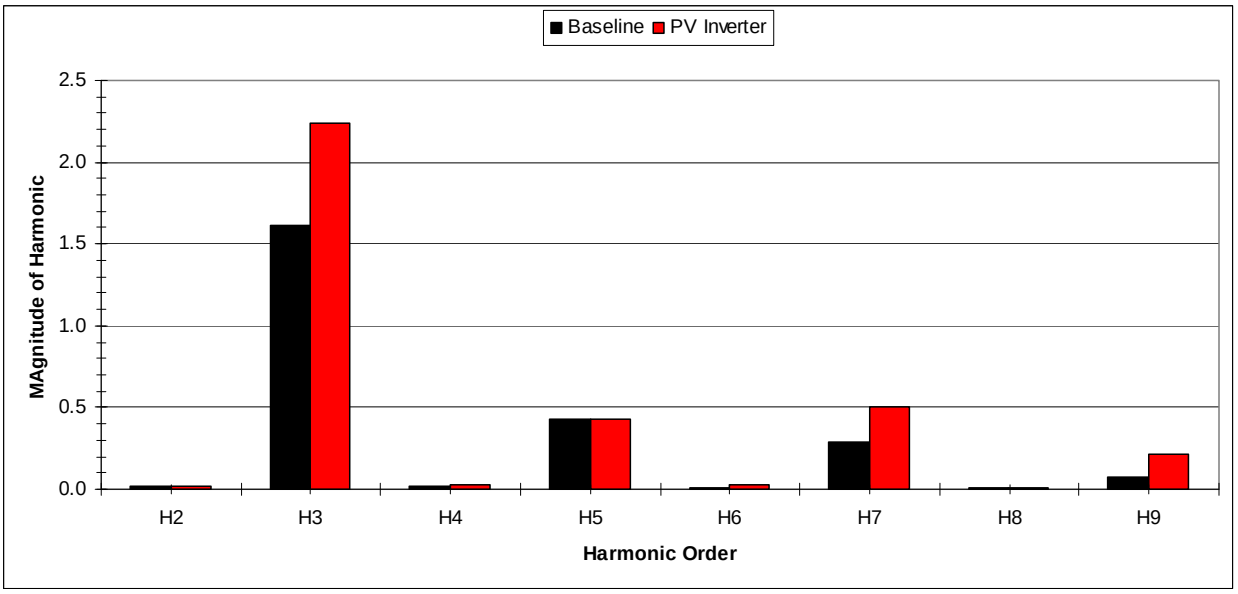


Figure 4.18. Harmonics with and without inverter

5. LABORATORY TESTING OF GRID-INTERCONNECTION

5.1 Enphase Burst-Mode Testing

The Enphase inverter uses burst-mode control technique at low power (30% and below) to avoid low efficiency, which helps the inverter reach high CEC efficiency. The inverter measures input current and voltage and then calculates the power to decide if it should operate in burst mode or not. If the power level is lower than the threshold, the inverter will operate in burst mode. As per our test results, the Enphase inverter will be in burst-mode operation when the input power is less than 22% of the rated power. During burst-mode operation, the inverter stores energy over one or more grid cycles and bursts the stored energy to the grid in one cycle. Figure 5.1 shows the experimental setup for the Enphase inverter testing. A transformer is connected between the inverter output and the utility grid to match the voltage levels. The inverter output voltage and current are marked as V_o and I_o.

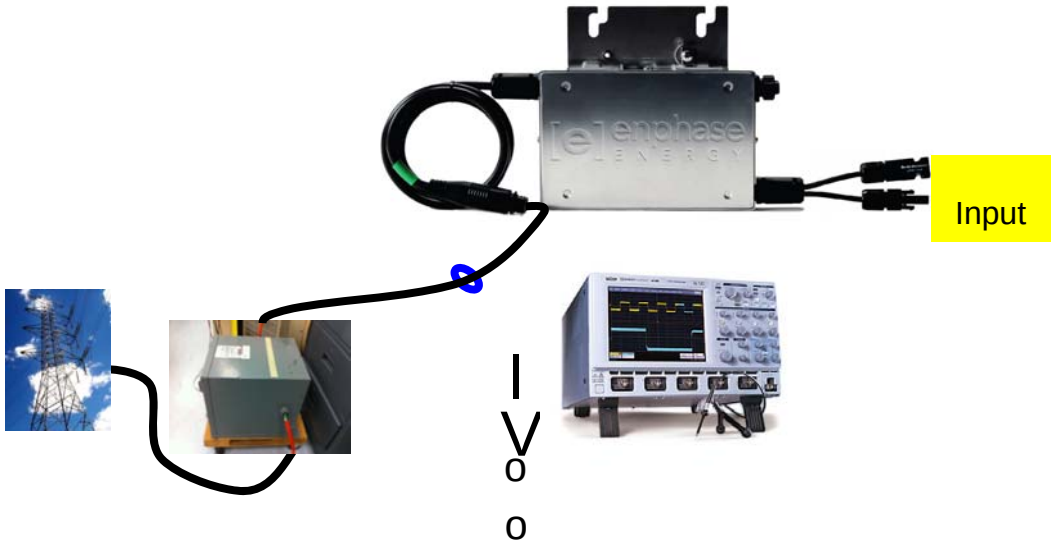


Figure 5.1. Experimental setup for Enphase inverter testing.

Figure 5.2 shows the measured voltage and current waveform under burst mode operation. The voltage, shown in the yellow curve, is fixed at 240 V, and the current, shown in the blue curve, varies from 4.4% to 22% of the rated power. When the power is at 22% and 11% levels, the inverter sends real power to the grid in every other cycle and draws reactive power in the alternate cycle. The reason for the inverter to draw reactive power is because the inverter output has a filter capacitor that draws a leading current. When the power level drops to 10%, the power burst appears in every three cycles, i.e. sending one-cycle real power and drawing two-cycle reactive power. When the power level drops to 7.5%, 5.3%, and 4.4%, the power burst appears in every four, five, and six cycles, respectively.

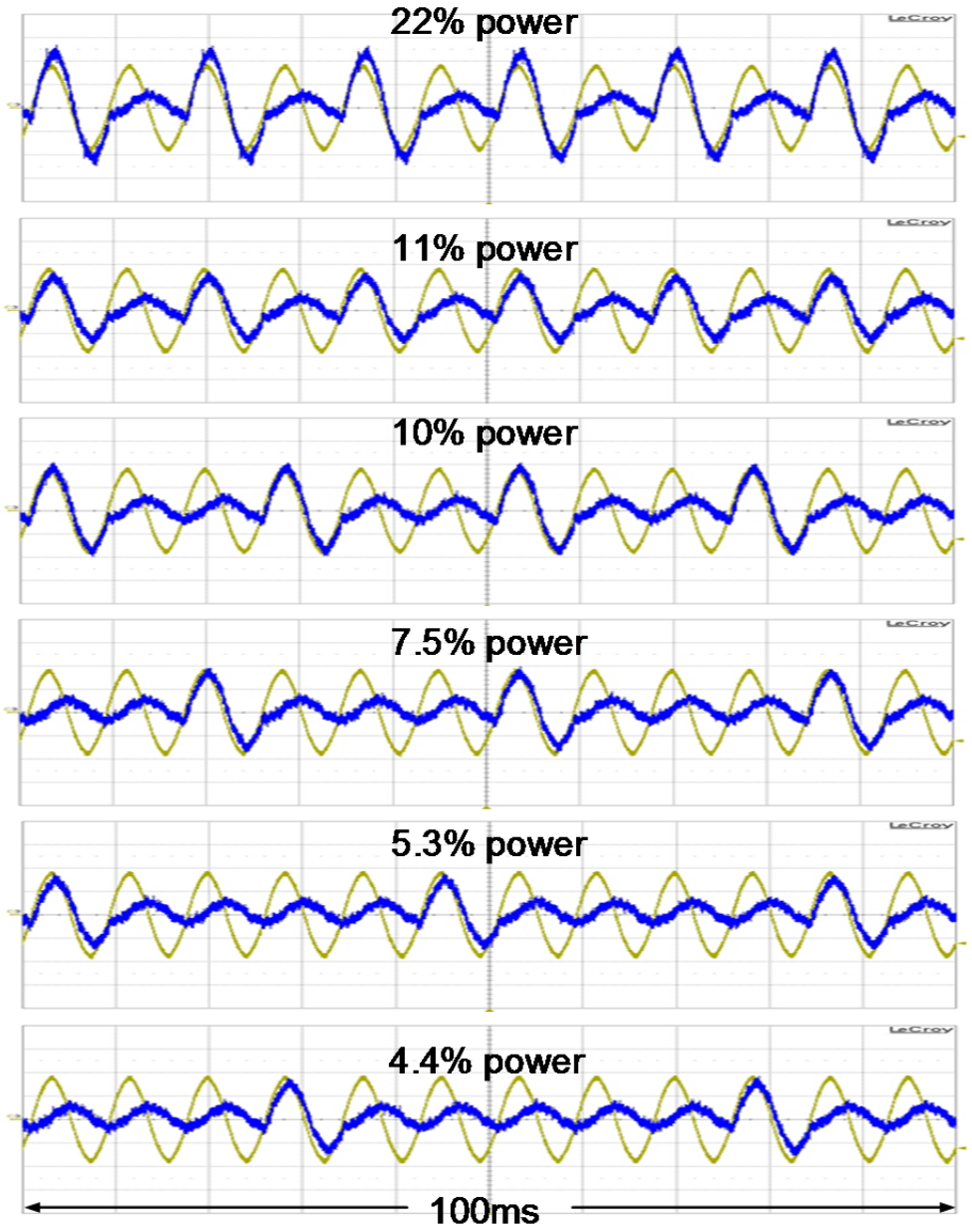


Figure 5.2. Bust mode operation test results for input power levels ranging from 4.4% to 22% of rated power (blue is AC current, and yellow is AC voltage).

The question for this type of burst mode operation is how it will impact the power system under high penetration PV conditions. Figure 5.3 shows the hardware test setup with six inverters. The test setup contains a 28-mH inductor between the inverter and grid, and a 1.75-Ω resistor bank as the inverter load to represent the scaled system parameters.

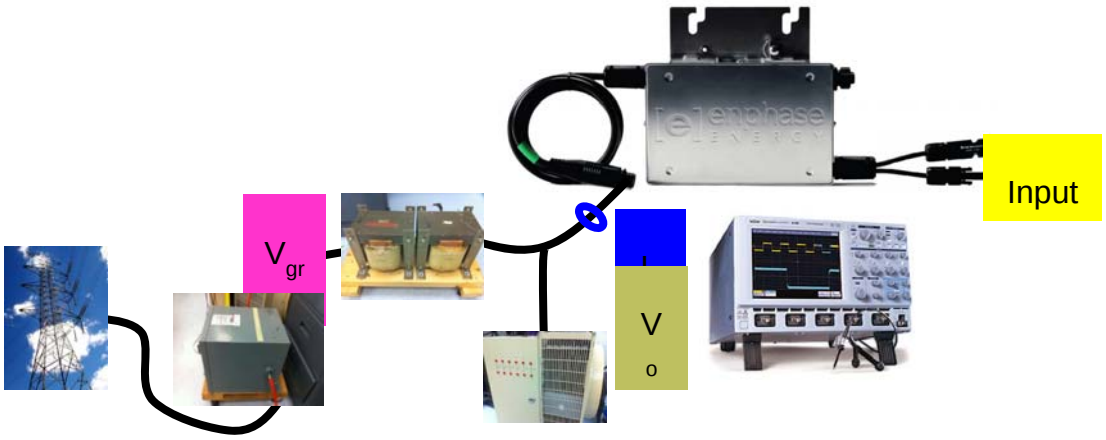


Figure 5.3. Experimental setup for 6-inverter system testing.

Figure 5.4 shows experimental results for the six-inverter system with the scaled system parameters for different load conditions. In this figure, the blue curve represents output current, i_o, the yellow curve represents output voltage v_o, and the pink curve is grid voltage, v_{grid}. Under no-load conditions, the inverter output current shows severe resonance. With 1% load, the resonance is slightly damped by the added load resistance. However, the damping effect is not noticeable because the load resistance is high. By increasing the load to 10% and 50%, the damping effect becomes obvious. Two major findings are identified from these experimental results.

1. Voltage flicker can be expected at high penetration levels. Figure 5.4 shows voltage distortion and potential flicker case under light-load conditions.
2. Current oscillation can be expected under high penetration and light-load conditions.

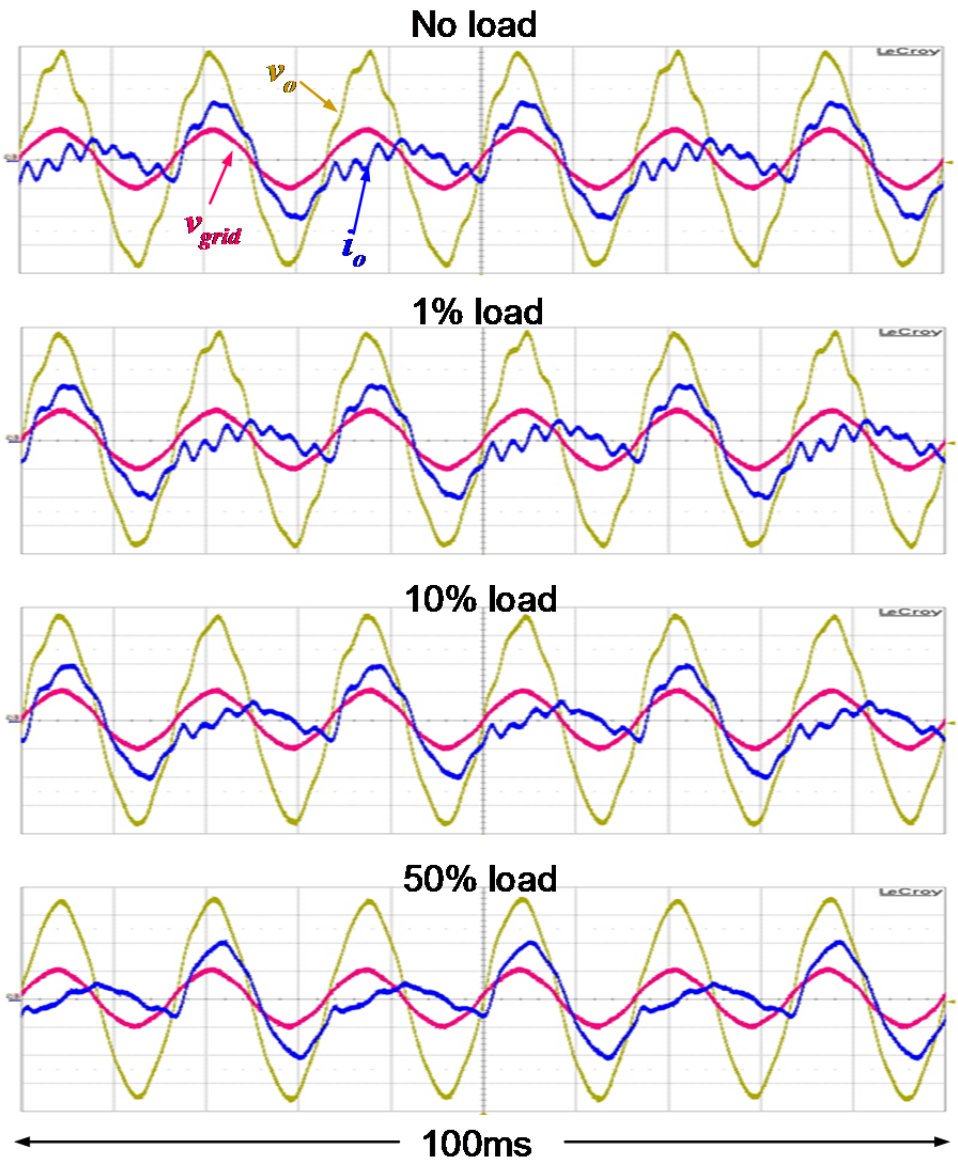


Figure 5.4. Experimental results of the 6-inverter system without load (blue is output current, yellow is inverter output voltage, and pink is grid voltage)

5.2 Anti-islanding Testing

An island may occur for many reasons such as a disconnection for servicing, human error, an act of nature, or one of the circuit breakers in the power system tripping as shown in Figure 5.5 with distributed generation (DG). Under the island condition, the DR is required to disconnect within 2 seconds according to IEEE 1547. There are many reasons for this requirement: the EPS may reconnect and the DR could be out of phase causing a large voltage spike, a line worker could get hurt, and the utility is liable for power lines even when DRs use them to transmit power.

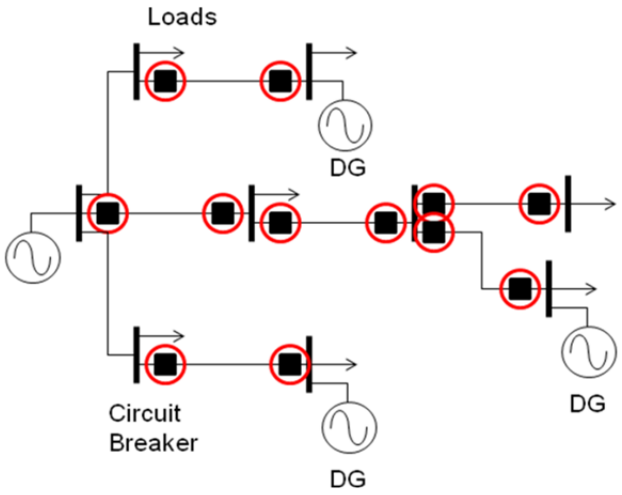


Figure 5.5. Example power system with circuit breakers and DGs.

There are many methods described in the literature to detect an island. Example methods include change in frequency, change in voltage, change in impedance, harmonic injection, reactive power injection, phase shift, frequency jump, voltage shift, power line carrier (PLC) communication, and supervisory control and data acquisition (SCADA). These can be categorized into (1) passive, (2) active, (3) hybrid, and (4) communication methods. The passive methods detect a change in the output when the grid is no longer connected. The active methods inject a disturbance that can be detected when the grid is no longer present. The hybrid method is a combination of both. The communication method such as PLC or SCADA uses communication between the system and the PCS to detect the loss of the grid. Each method has its strengths and weaknesses. The following is a brief list of different islanding detection methods:

- Passive
  - Change of frequency scheme
  - Change of voltage scheme
  - Change of impedance
- Active
  - Harmonic injection
  - Phase shift
  - Frequency jump
  - Voltage shift
- Communications
  - Power Line Carrier Communications
  - Supervisory Control and Data Acquisition

The passive method is relatively straightforward. It uses the abnormal voltage and frequency conditions defined in IEEE 1547 as the method for islanding detection. Figure 5.6 shows the voltage and frequency in normal operating range and the clearing time under abnormal cases including under- and over-voltage and under- and over-frequency conditions.

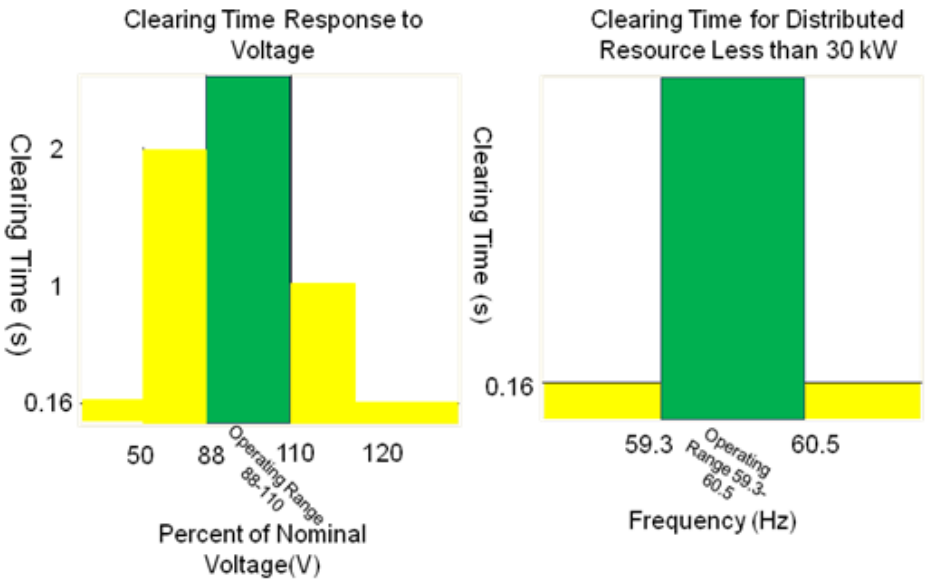


Figure 5.6. IEEE 1547 voltage and frequency in normal operating range and clearing time under abnormal cases.

A. Test Setup and Experimental Results

It is possible that the islanding is undetectable, or the system is in the non-detection zone (NDZ). Under these conditions, the load within the island matches the power generated, which means the current from the EPS goes to zero. Figure 5.7 shows a PV interconnection system that may go into NDZ when $I_{PV} = I_{load}$ or $I_{grid} = 0$. In this case the inverter may not trip which may result in a safety concern.

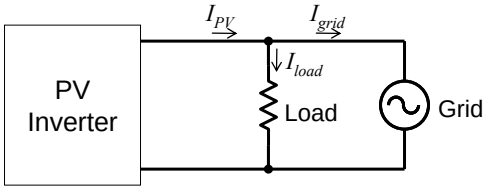


Figure 5.7. Diagram of non-detection zone condition with PV interconnection.

Figure 5.8 shows the voltage and current waveforms in the non-detection zone. The initial grid current is at noise level as compared to the inverter current. When the grid is disconnected, the inverter does not detect the situation and remains operational. This implies the failure of islanding detection, which is generally the case with the passive detection method.

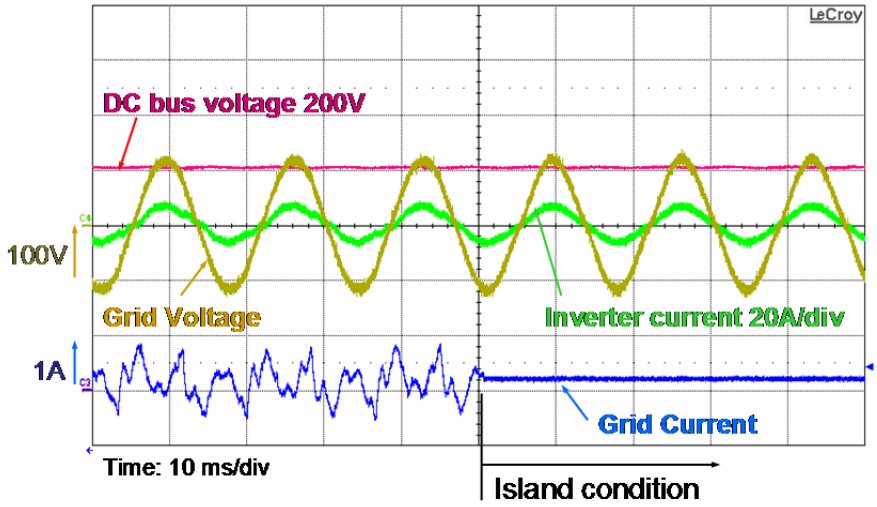


Figure 5.8. Voltage and current waveforms in non-detection zone.

B. Phase-Locked Loop and Anti-islanding Test Results

Figure 5.9 shows possible active approaches for islanding detection through modification of the phase-locked-loop (PLL). A standard PLL method has the 60-Hz line frequency going through integration, shown in Figure 5.9(a). The resulting phase information is used for synchronization. Any phase error will be filtered and eventually drops to zero through the loop filter.

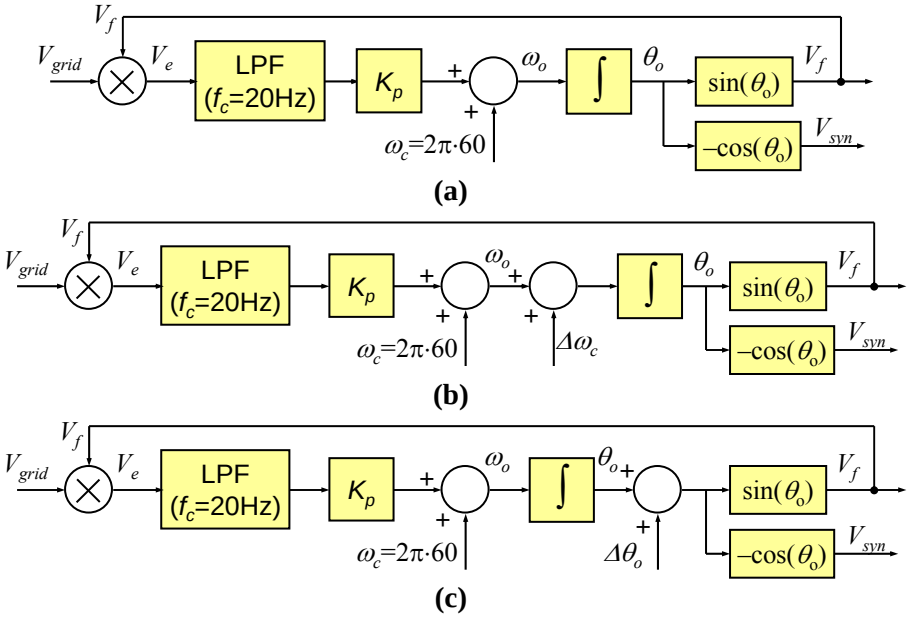


Figure 5.9. Islanding detection with modification of phase-locked-loop: (a) standard PLL, (b) PLL with frequency shift, and (c) PLL with phase shift (Enphase approach).

In Figure 5.9(b), the PLL is modified with a frequency shift that occurs periodically. Figure 5.10 shows the test results with a 67-Hz frequency shift for islanding detection. Initially the grid is connected with a standard 60-Hz frequency. If the grid is normal, the frequency shift will return

to 60Hz after a few cycles. When an island occurs, the 67-Hz island condition will be detected, and the inverter will trip.

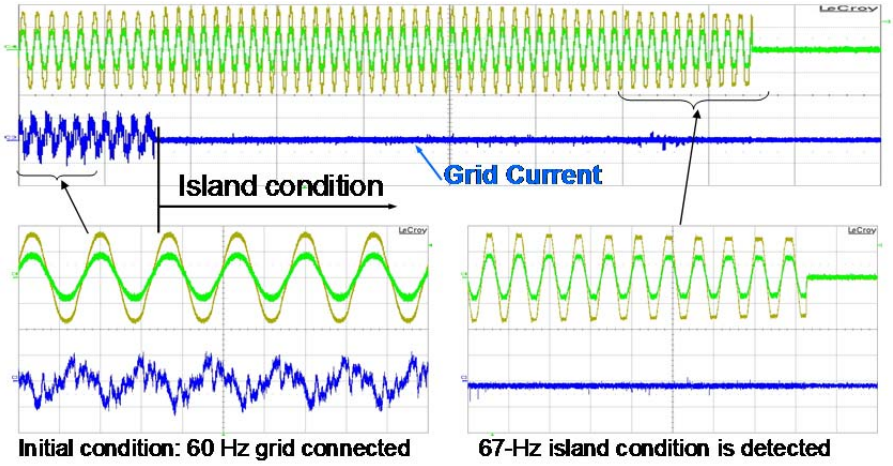


Figure 5.10. Test results of anti-islanding with frequency shift.

In Figure 5.9(c), the PLL is modified with a phase shift that occurs periodically. This method has been used in Enphase inverters. Figure 5.11 shows the test results with the Enphase inverter, which trips immediately after an island is detected. The Enphase design case has a 50-μs phase shift every 0.5 seconds.

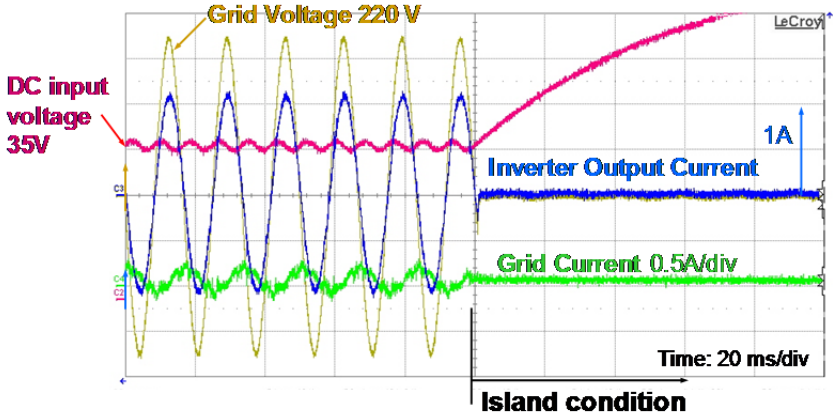


Figure 5.11. Test results of anti-islanding with phase shift using Enphase inverter.

Figure 5.12 shows the block diagram for the anti-islanding test with two Enphase inverters in parallel. Since the Enphase inverter requires 240-V to run the test, a transformer with a turns ratio of 1.2 is inserted between the Enphase inverter output and the 208-V grid. A magnetic contactor MC1 is used to create the island condition. A load bank is connected at the inverter output to create the non-detection zone condition.

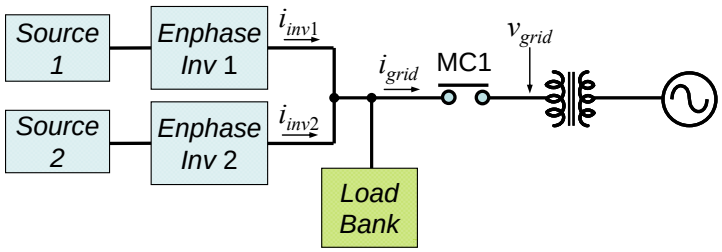


Figure 5.12. Two paralleled Enphase inverters under anti-islanding test.

Figure 5.13 shows the tested voltage and current waveforms of the two paralleled Enphase inverters before and after island creation. Similar to the single inverter case, the two inverters trip at the second zero crossing. This kind of tripping indicates that the Enphase inverters are not responding to the non-detection-zone island condition, but to the line transients.

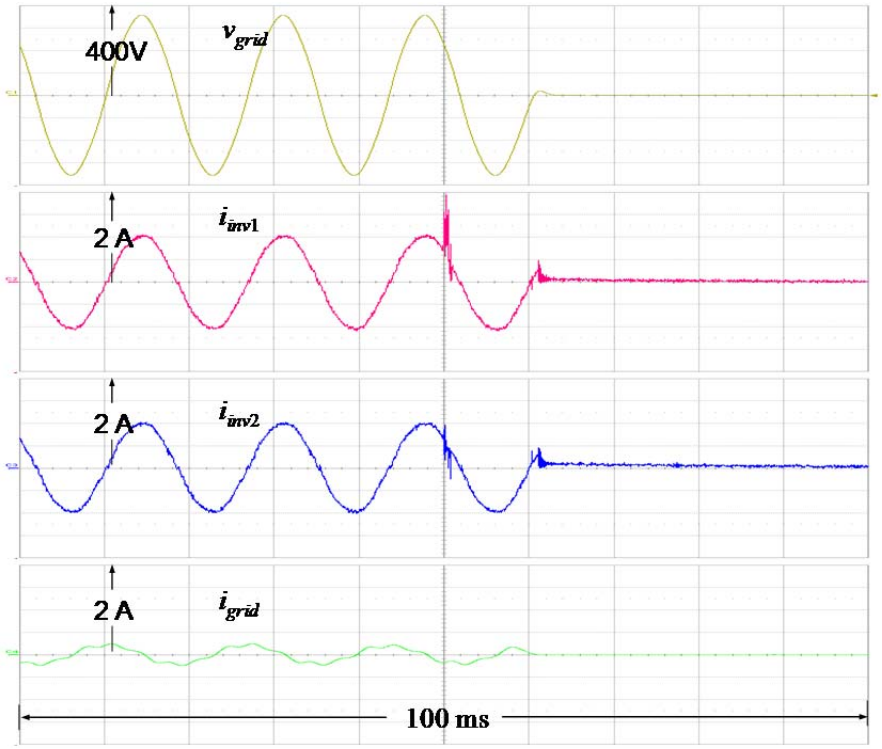


Figure 5.13. Voltage and current waveforms of two paralleled Enphase inverters under anti-islanding test.

To desensitize the Enphase inverter response, we paralleled one Enphase inverter with one VT inverter, as shown in Figure 5.14. In this test, the grid comes from a 120-V line instead of a 240-V line. The output of Enphase inverter is reduced to 120V through a step down transformer. The transformer also helps isolate the switch transient.

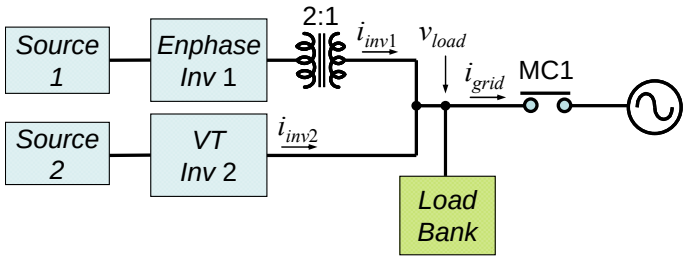


Figure 5.14. Anti-islanding test diagram with one Enphase inverter and one VT inverter in parallel.

Similar to previous tests, before the island formed, the grid current was adjusted to almost zero. Turning off MC1 did not create a noticeable transient at the Enphase output, and the VT inverter supported the voltage for a while until the Enphase anti-islanding detected the abnormal synchronization. Figure 5.15 indicates that the Enphase inverter output current, i_{inv1}, trips at about 0.67s, and then the VT inverter output current, i_{inv2}, trips at about 0.76s. This test clearly indicates that two or more inverters in parallel can affect each other's anti-islanding operation. If the Enphase inverter implements the PLL phase shifting every 0.5s, its tripping at 0.67s is apparently affected by the VT inverter, which is less sensitive to the line transient and stays on the line to keep a sufficiently high voltage that delays the Enphase trip time. This paralleled inverter case study indicates that many possible scenarios can happen with multiple inverters in parallel. Further studies are needed to examine other potential issues.

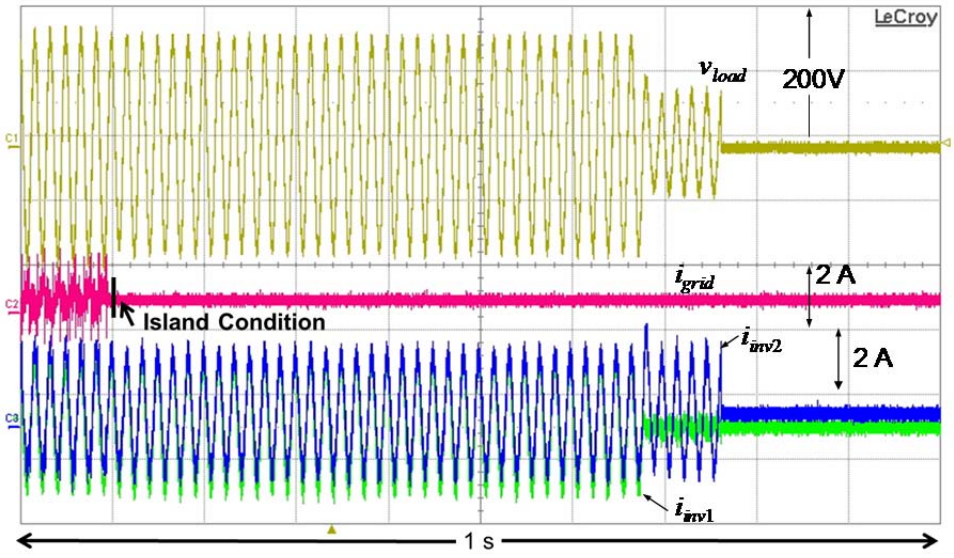


Figure 5.15. Anti-islanding test results with one Enphase inverter and one VT inverter in parallel.

C. On-Site Monitoring and Communication

EPRI's PV system output and sunlight conditions are monitored at 1 to 5 second intervals. The datasets are generated to help define the expected PV output and serve as the PV resource

models. The results and findings from site analyses will be aggregated for broader understanding of high penetration PV impacts on the system.

Figure 5.16 shows photographs of monitoring equipment including (a) data logger, (b) current transducer (CT) and metering unit, and (c) irradiance and temperature sensing unit. The data logger is synchronized with the internet time using onboard memory for temporary storage. The outbound transfers are firewall savvy. For the power meter, high accuracy transducers are used for measuring voltage, current, frequency, real power, reactive power, and cumulative energy. The environmental conditions are also monitored with irradiance and temperature sensors that detect the panel surface light and temperature.

(a) **(b)** **(c)**

Figure 5.16. On-site monitoring equipment: (a) data logger, (b) CT and power metering unit, and (c) irradiance and temperature sensing unit.

Figure 5.17 shows the outdoor enclosure package that contains all the sensing equipment and instrumentation. The unit will be installed throughout different regions.

Figure 5.17. Outdoor enclosure with the sensing equipment instrumentation package.

Figure 5.18 shows example monitoring results at Birmingham, AL on May 14, 2010. The power production was recorded throughout one entire day. The peak power is about 1 kW. It is interesting to see that a power dip occurred during the early afternoon under clouded conditions.

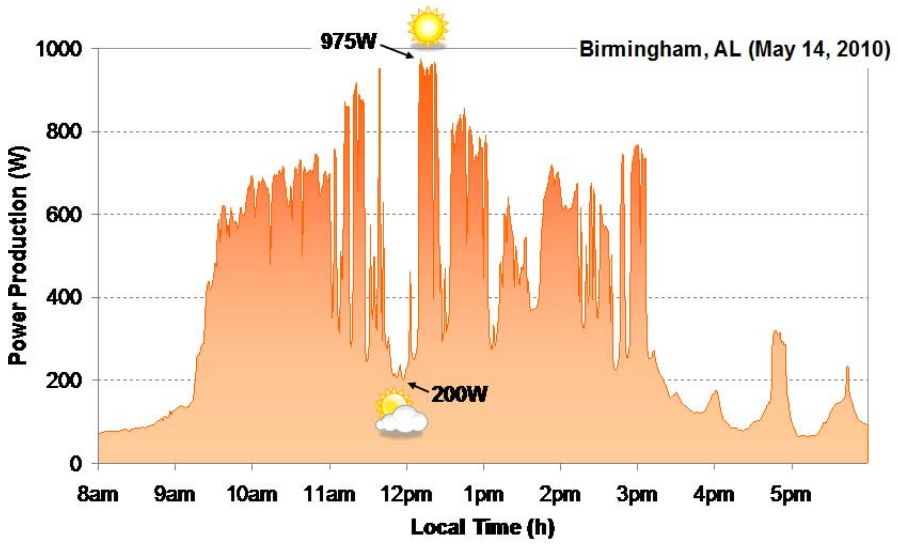


Figure 5.18. Example of monitoring results at Birmingham, AL on May 14, 2010.

Figure 5.19 shows the complete PV monitoring system with the instrumentation package. The system assumes a vendor will sell a panel along with a matched inverter that sends the AC output to the grid. The example here shows a 200-W panel and a matched micro-inverter. The EPRI monitoring system is equipped with a data acquisition system that sends information to the host utility through an ethernet or using wireless communication.

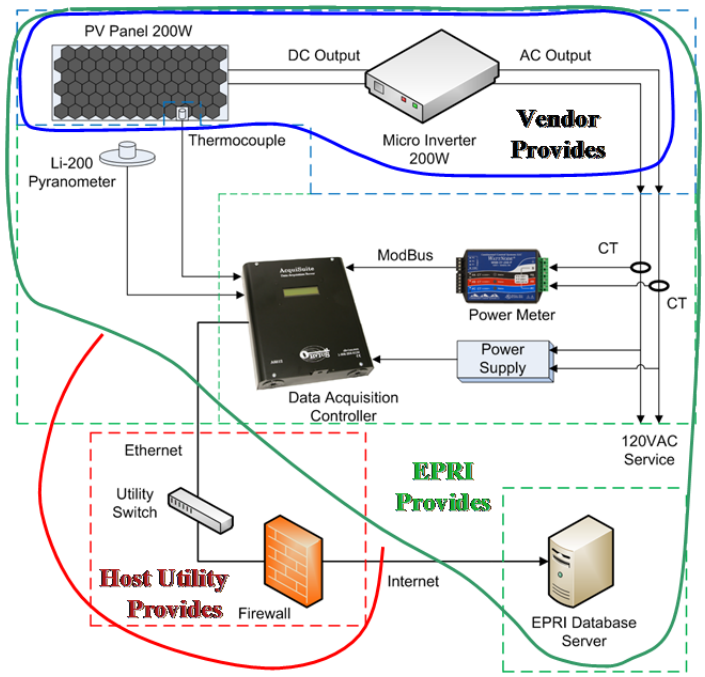


Figure 5.19. PV monitoring system with instrumentation package.

Figure 5.20 shows the distributed PV (DPV) site selection concept. The preferred site will have utility facilities with a cluster of 4 to 8 sites either along a distribution feeder or spaced to emulate a typical feeder PV deployment. Shading from nearby objects needs to be avoided every

day for at least 8 hours (±4 hours from solar noon) for the entire year. The internet connection can be either wired or wireless but must always be on.

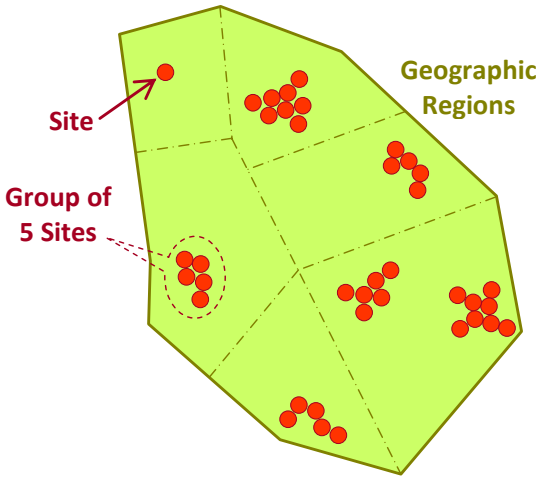


Figure 5.20. DPV site selection guidelines.

Figure 5.21 shows the selected DPV sites along a sample distribution feeder. This example system voltage level is 12.5 kV, and the total power is 20 MVA. The feeder supplies 1700 customers with 64% load consumed by residential houses.

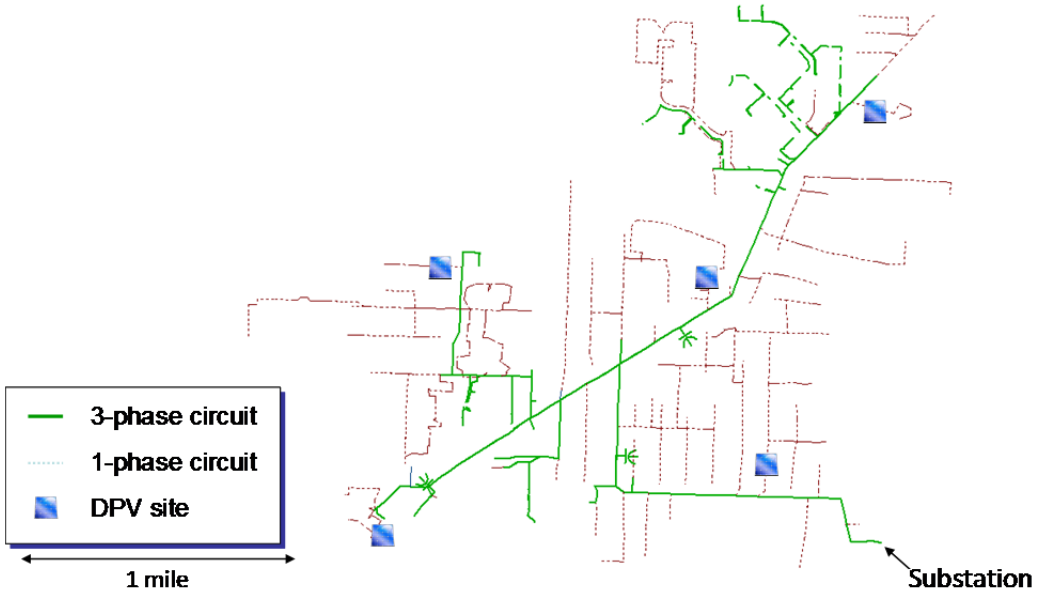


Figure 5.21. Selected DPV sites in a sample distributed feeder.

The outcomes of the study through this monitoring system are summarized as follows:

- Understanding operational and cost impacts of PV
- Providing a better estimate of a specific feeder's capacity for adding PV

- Enabling comparison of compatibilities and limitations for unique feeders and distributed PV cases
- Allowing a test drive of various inverter voltage control options on actual feeders
- Delivering lessons learned, broad conclusions and knowledge

5.3 Potential Component Failure Analysis

Electronic components tend to fail at higher temperature operating conditions. The following equation describes the life expectancy at the operating temperature L_T as a function of the operating temperature T_{op} and its life expectancy L_o at the reference temperature T_o. For capacitors, the ratio between the operating voltage and the rated voltage, α_V, also affects the life expectancy.

$$L_T = L_o \cdot \alpha_V \cdot 2^{\frac{T_o - T_{op}}{10}}$$

In order to improve the efficiency, the commercial PCS products studied in this report, including SunnyBoy and Enpahse inverters, all adopt the single-stage power conversion technique with only one PWM stage. The single-stage power conversion does not have an energy buffer stage, so the double line frequency (120 Hz) ripple will propagate back to the PV source. In order to ensure effective MPP tracking, these single-stage inverters require a large capacitor bank to filter the double line frequency ripple. The capacitance needed in this case must involve electrolytic capacitors due to size and cost considerations. The problem with the electrolytic capacitor is its relatively low life expectancy. Figure 5.22 compares the life expectancy between film and electrolytic capacitors. The life expectancy of the film capacitor is at least one order of magnitude higher than that of the electrolytic capacitor. Therefore, the use of electrolytic capacitors in these single-stage inverters needs further investigation.

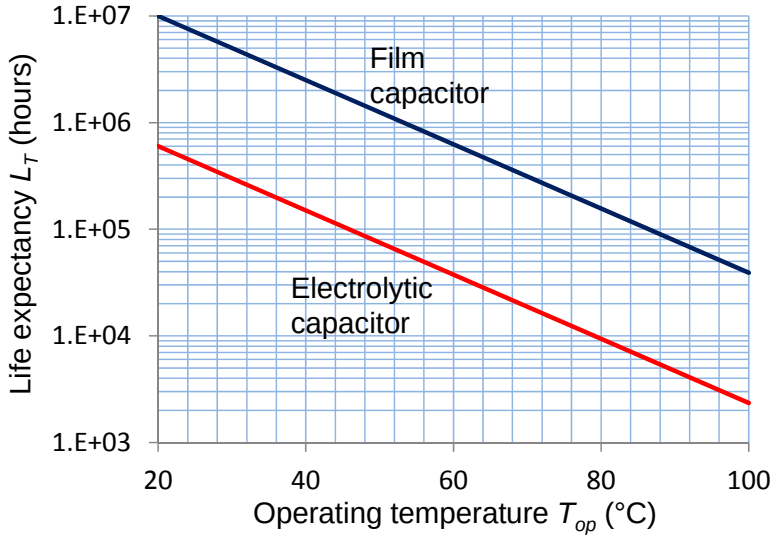


Figure 5.22. Comparison of life expectancy between film and electrolytic capacitors.

For other electronic component failure in time (FIT) and mean time between failure (MTBF), Table 5.1 lists typical component failure rates based on the US Department of Defense handbook, MIL-HB-217F [18]. The table clearly indicates that the electrolytic capacitor has lowest MTBF or highest failure rate. The silicon IGBT module is the second weakest link.

Table 5.1. Typical component failure rates based on MIL-HB-217F

Description	Type	Failure in time (FIT) in 10^9 hours	Mean time between failure (MTBF) in years
Resistors	Carbon	10	11415
	Wire-wound	25	4566
	Film	50	2283
Capacitors	Electrolytic	1500	76
	Tantalum	1000	114
	Paper	500	228
	Ceramic	250	456
	Plastic film	20	5707
Diodes	Silicon	50	2283
Transistors	Discrete silicon	80	1426
IGBT modules	Silicon	1450	78
Power module	Silicon carbide	100	1141
Power inductor	Copper winding	50	2283
Transformer	Copper winding	299	570
Connections	Soldered	19	11415
Connector	Per pin	50	2283

A. SunnyBoy 5-kW Inverter

Figure 5.23 shows the simplified circuit diagram of the 5-kW SunnyBoy inverter. The power stage is a simple full-bridge inverter consisting of four insulated-gate-bipolar-junction-transistors (IGBTs). The IGBT gates are controlled by a sinusoidal PWM to obtain sinusoidal output current, i_{ac}. Because the inverter allows input voltage to be as low as 250 V, which is far less than the peak line voltage of 340 V, the inverter output stage requires a transformer to boost the voltage. Based on our measurements, the turns ratio between primary and secondary is approximately 1:1.35. A magnetic contactor, MC1, is placed in between the transformer secondary and the grid. The input of the inverter has ten parallel branches of capacitor bank. Each branch contains two electrolytic capacitors in series.

Key passive component specifications are list as follows.

1. Capacitors: HU series (Hitachi), each rated 400 V, 770 μF, ESR = 130 mΩ, 2.54 A ripple rating at 105°C.
2. Transformer: Primary magnetizing inductance, L_{m1} = 0.154 H, primary leakage inductance, L_{k1} = 1.154 mH, turns ratio = 1:1.35.

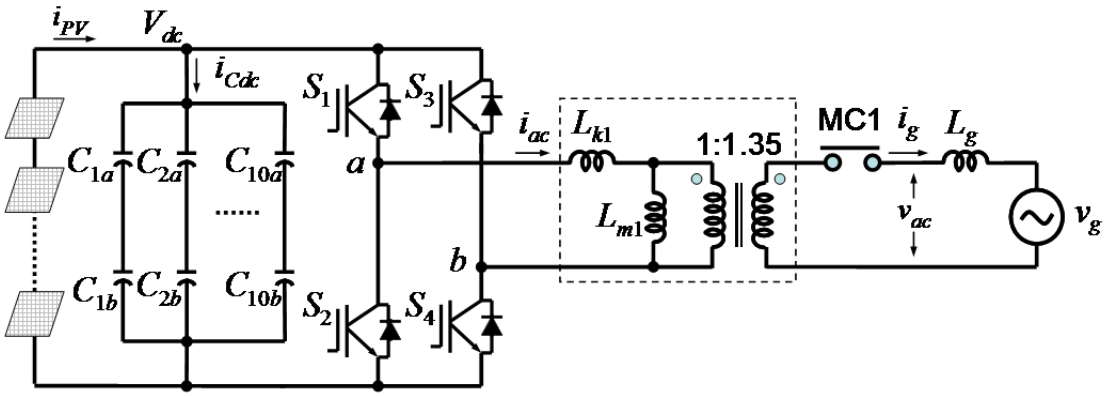


Figure 5.23. Simplified circuit diagram of the SunnyBoy 5-kW string inverter.

The electrolytic capacitor has the greatest risk for potential failure. Figure 5.24 shows a photograph of the upper section of the SunnyBoy 5000US 5-kW inverter. A large capacitor bank of 20 capacitors can be clearly identified. These capacitors are designed to handle the double line frequency current. The magnitude of the capacitor current depends on the DC bus voltage, V_{dc}, the wiring length and size, the modulation method, and the output power level. In order to determine the capacitor current, some operating conditions need to be assumed.

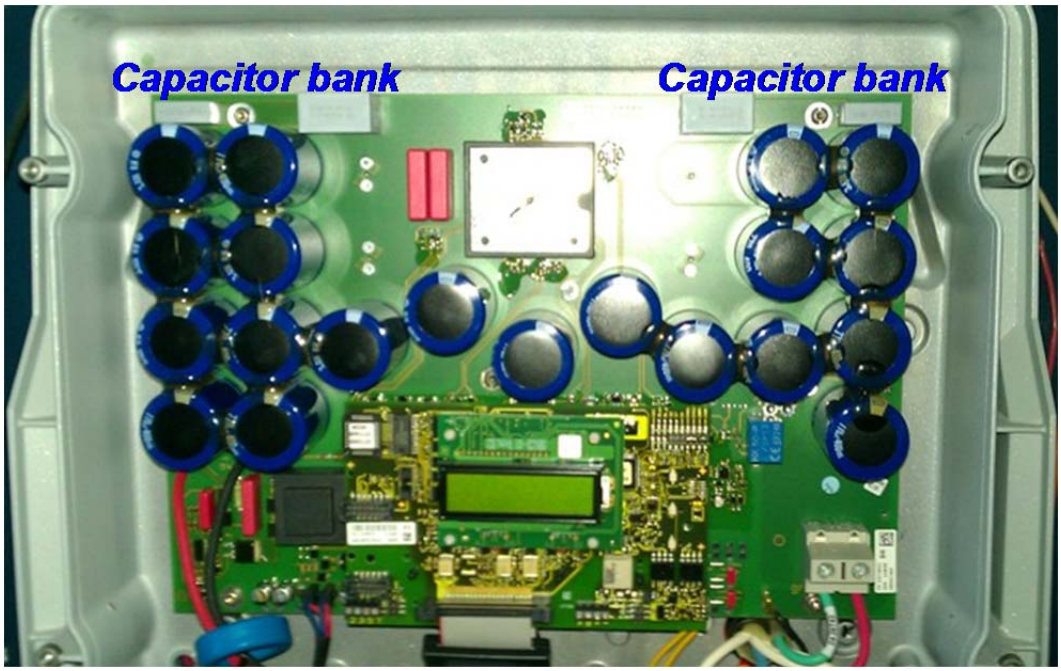


Figure 5.24. Photograph of the upper section of SunnyBoy 5000US 5-kW inverter.

Figure 5.25 shows simulated voltage and current waveforms of key components under 5-kW operating conditions. The grid voltage, v_g, is 240 Vrms, and the current send to the grid, i_g, is 20.9 Arms. The primary side transformer current is 28.2 Arms. The PV voltage and current, V_{dc} and I_{PV}, show noticeable ripples even with a large filter capacitor bank. With an average PV output voltage of 284.8 V, the entire DC bus capacitor bank draws a 17.6-Arms ripple current.

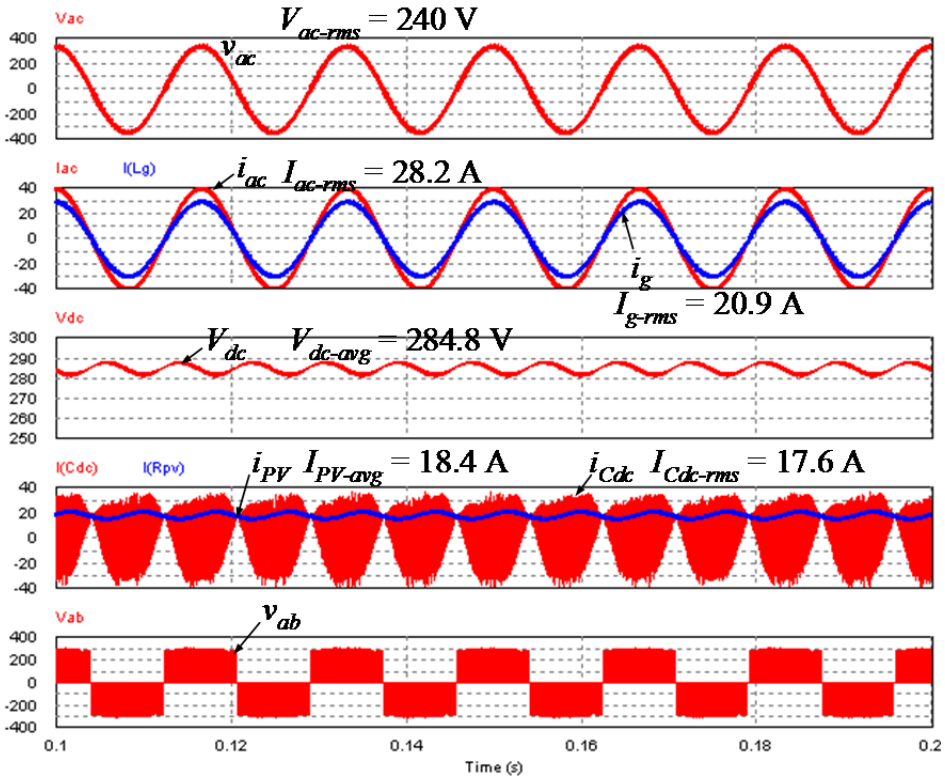


Figure 5.25. Simulated voltage and current waveforms of key components under 5-kW operating conditions.

Based on the HU-series capacitor datasheet, the simulated capacitor ripple current represents 69% of the 105°C rated ripple current, 25.4 A. Figure 5.26 shows the ripple current ratio and life expectancy of the HU capacitor under different ambient temperature conditions. If the inverter is installed inside a building with room temperature as the ambient, the capacitor should have a life expectancy of 250,000 hours. If the inverter is installed outside with a case temperature of 85°C, then the life expectancy drops to 50,000 hours.

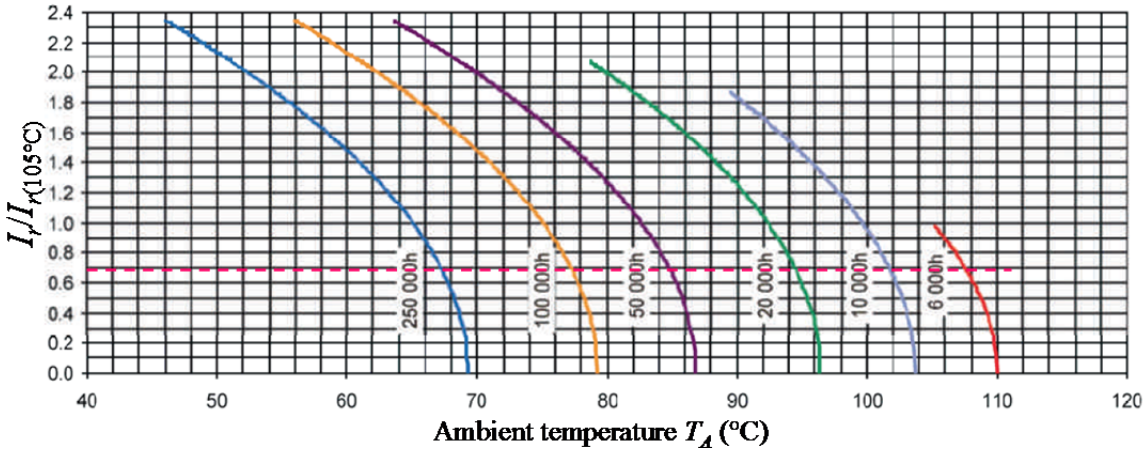


Figure 5.26. Ripple current ratio and life expectancy of the HU capacitor under different ambient temperature conditions.

The second component that needs to be considered for life expectancy impacts is the magnetic contactor, MC1. Depending on the electric contact material and operating current, a typical contactor has an expected 10% failure rate for every 100,000 operations. As discussed in Chapter 2, the SunnyBoy inverter has a special design to limit the number of MC1 operations per day. Its basic idea is to delay the morning startup operation until the input bus voltage is high enough, or the solar irradiance is stabilized. This way the energy production is reduced, but the contactor life is not damaged by frequent on and off.

The IGBT module normally causes the majority of failures in most power electronics equipment. In this 5-kW inverter, the IGBT module is mounted on a bulk heat sink and cooled by a large blower fan to ensure reliable operation of the inverter. Therefore the component that causes concern is the blower that cools the bulky heat sink. Figure 5-23 shows the photograph of the blower fan section of the SunnyBoy 5000US 5-kW inverter. Detailed specifications of this blower fan are not known, but a typical AC blower fan has a life expectancy of 50,000 hours.

Figure 5.27. Photograph showing the blower fan section of the SunnyBoy 5000US 5-kW inverter.

Taking all the above components' life expectancy information into account, the 50,000-hour operating life is a reasonable estimate for the SunnyBoy 5000US 5-kW inverter. Assuming the worst case of an average of 10 hours operation per day for 365 days a year, the inverter should have a minimum life of 13.7 years if it is not subject to severe lightning strike or natural disaster. For normal operations with an average of 8 hours a day and 300 days a year for the fan to blow, the life expectancy is around 20 years. The number depends largely on the weather conditions and geographical location and should be quoted very carefully.

B. Enphase 190-W Micro-inverter

Figure 5.24 shows the simplified circuit diagram of the Enphase 190-W micro-inverter prototype. The actual circuit has two-phase interleaved power circuits to eliminate the high frequency ripple. The power stage design adopts an active clamped flyback converter with power MOSFET M_1 as the main switch, and M_c as the clamping switch. Both switches are operating under soft-switching conditions, so the switching loss is negligible. The produced PWM waveform is high-frequency AC but with a low-frequency component embedded. The rectified low-frequency signal is unfolded through a thyristor bridge circuit, Q_1-Q_4. The commutation of the Thyristors relies on a series connected power MOSFET M_x, which naturally turns off when the line voltage is below the preset zener diode voltage across the gate and source pins of M_x. The input of the inverter has five parallel electrolytic capacitors. Each one is rated 63 V, 1.8 mF, LXZ type electrolytic capacitor.

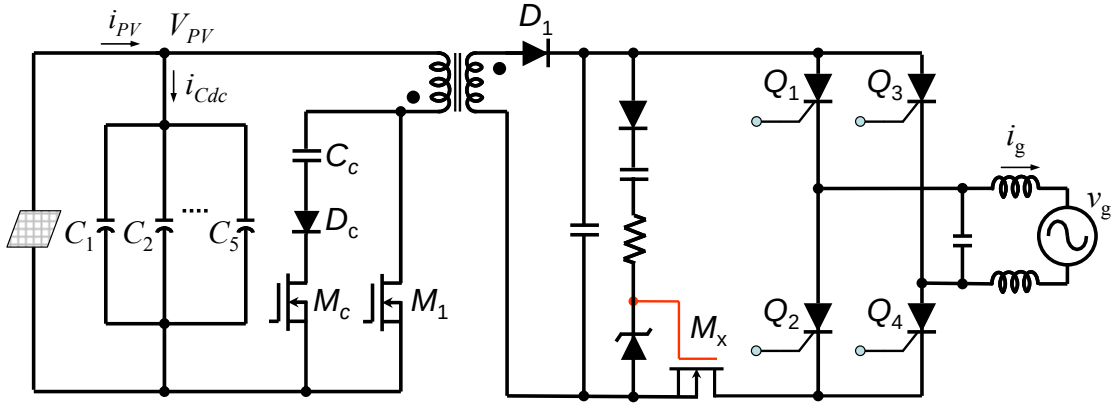


Figure 5.28. Simplified schematic circuit diagram of the Enphase micro-inverter prototype.

Figure 5-25 shows the photograph of the Enphase 190-W micro-inverter prototype. The five capacitors are shown on the left-hand side of the circuit board. It should be noted that the actual product is totally sealed and is smaller in size. The life expectancy estimate for the prototype inverter may not reflect that of the actual product, but it should provide a ballpark of the initial estimate for possible projection under different operating conditions and environments.

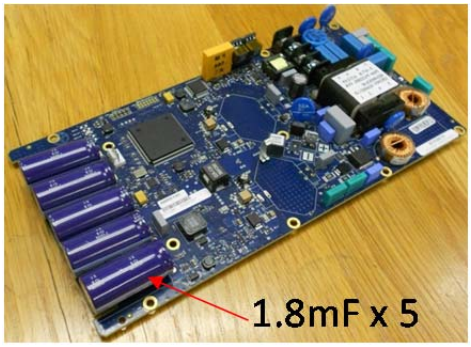


Figure 5.29. Photograph of the Enphase 190-W micro-inverter prototype.

To understand the capacitor current issue, a single-stage micro-converter was simulated. Figure 5.26 shows simulated voltage and current waveforms of key components under 240-W operating conditions. The grid voltage, v_g, is 240 Vrms, and the current sent to the grid, i_g, is 1 Arms. The

primary side transformer current is 28.2 Arms. The PV voltage and current, V_{dc} and I_{PV}, again show noticeable ripples even with a large filter capacitor bank. With an average PV output voltage of 37.0 V, the entire DC bus capacitor bank draws a 9.3-Arms ripple current.

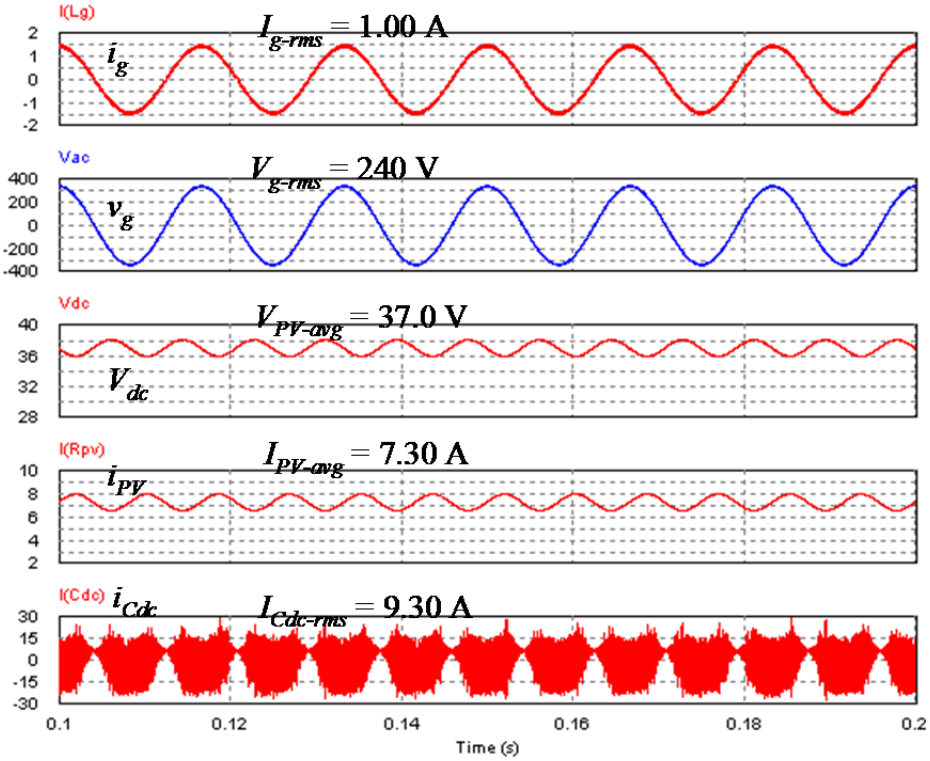


Figure 5.30. Simulated voltage and current waveforms for a single-stage micro-converter.

The simulated ripple current needs to be scaled down for 190-W operating conditions. Given the LXZ capacitor 120-Hz ripple current rating of 3.21A, the ratio of the capacitor current and its rating is 0.76. The projected life expectancy can be found in Figure 5-27. If the capacitor operating temperature is 105°C, the life expectancy is 6,000 hours. If the temperature is 85°C, the life expectancy becomes 24,000 hours. Since the commercial product of the entire micro-inverter is potted, the temperature should evenly disperse, and the average operating temperature throughout the day may be lower. Using an average operation of 8 hours per day and 300 days per year, the projected life expectancies for three temperature conditions are calculated as follows:

1. At 85°C, L85 = 24,000 hours ➔10 years
2. At 65°C, L65 = 90,000 hours ➔ 37.5 years
3. At 45°C, L45 = 360,000 hours ➔ 150 years

Note that the above projection does not consider potential electrolyte dry-out and degradation. However, even if the capacitor degradation happens, the inverter may not immediately fail, but the MPPT efficiency will reduce.

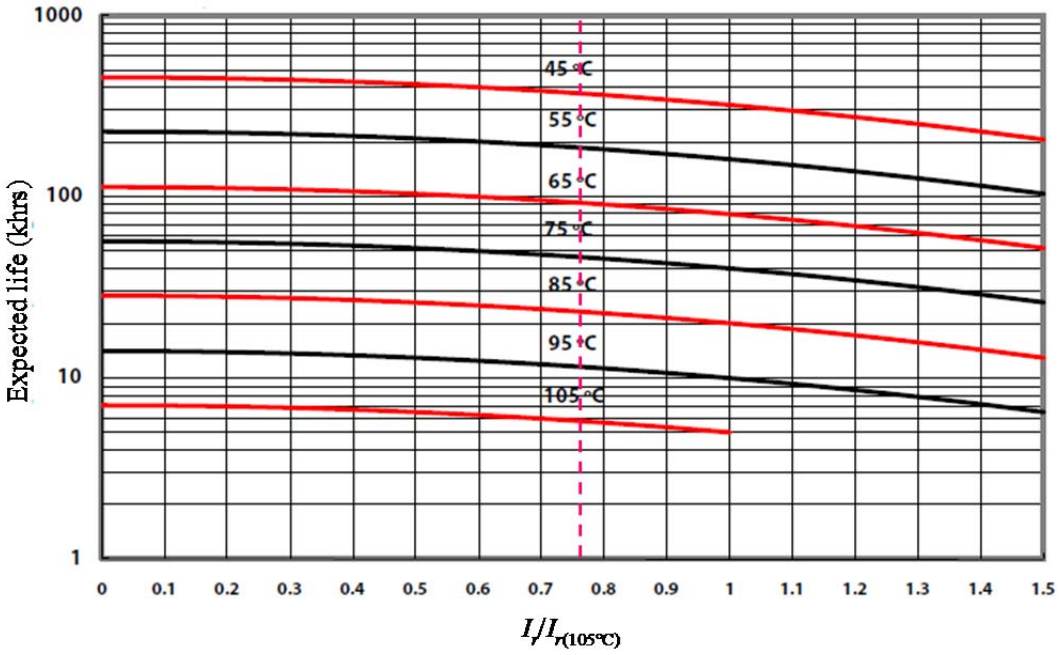


Figure 5.31. Small can electrolytic capacitor life expectancy as a function of temperature and ripple current.

The Enphase micro-inverter does not have mechanical moving parts such as a relay or cooling fan, so the next part most likely to fail is the main power MOSFET, M_1, which can be seen from the hot spot temperature photograph shown in Figure 2.25(b). The temperature rise under full load conditions was about 30°C, which is relatively low and safe for a semiconductor switch. The typical failure temperature for a silicon power MOSFET is 150°C, and the continuous operating temperature is normally limited to 125°C to allow for dynamic temperature fluctuation. With 30°C temperature rise under un-potted case conditions, the MOSFET should operate comfortably. According to Table 5.1, the MTBF of a discrete transistor is 1426 years. Similar to SunnyBoy inverter case, the actual operating temperature depends largely on the weather conditions and geographical location, and the life expectancy number should be quoted very carefully.

6. SUMMARY

This project investigated solar variability, power conversion and electric power grid response aspects of high penetration solar PV. These are the primary determining factors for acceptable penetration levels. Therefore, the study not only focused on the power system interactions, but also on the design of advanced power conditioners to enable higher penetration of PV power systems. The team consists of expertise in power electronics design, PV resource modeling, power system simulation, and power quality testing. Through extensive laboratory and field testing, the team gathered essential information needed to better understand grid characteristics, PV systems configuration, and power conditioning systems. Key findings and efforts are summarized as follows.

6.1 Key Findings

A. PCS Design Findings

1. Efficiency

Both the tested SMA inverter and Enphase micro-inverter show about 1% less than the manufacturers' listed CEC efficiency. High input voltage with the SMA inverter tends to have low efficiency due to high inductor current ripple and high switching loss. The SolarMagic™ microconverter SM3320-1A1 has a peak efficiency of 99.5% when the input and output voltages are at about the same level and the only loss is the diode voltage drop. Under fixed voltage testing with 24-V input and 40-V output, the peak efficiency becomes 98.7%. When combining SolarMagic™ converters as the power optimizer front stage and the SMA inverter as the centralized inverter, the energy production is always less than the case with the SMA inverter. However, under partially shaded conditions, the combination of SolarMagic™ converters and the SMA inverter can produce more energy.

The Enphase inverter operates in "burst" mode under light-load conditions to increase the CEC weight efficiency. If the power level is less than 22%, the inverter stops sending real power to the grid while drawing reactive power due to the output filter capacitor every one or few cycles depending on the power level. This approach can maximize the energy production at light load and increase the power conversion efficiency. The only concern is that under the condition with multiple inverters in parallel, the light-load pulsating operation tends to cause high frequency current oscillation and voltage distortion. This waveform distortion issue requires further testing verification for high penetration conditions.

2. Startup

The SMA SB5000US inverter requires a sufficient voltage level to start. There is a relay controlling on and off for the unit's operation. Under dusk conditions, the relay tends to click on and off too frequently due to its sensitivity to the voltage level. Our observation was that it could switch more than 50 times in one afternoon. This type of frequent mechanical operation is likely to be the weak link in terms of reliability.

The startup with the SolarMagic™ converters and SMA inverter is always later than the other cases. Although the voltage range of SolarMagic™ is wide (15 to 40 V) with its buck-cascaded-with-boost type power stage, it does not start until the load power reaches a threshold level of 5 W. This implies that the boost function does not kick in during startup. It will, however, work with the second-stage inverter during normal operation. Therefore, to configure a system with a DC-DC converter as the first stage running under maximum power point tracking and the second-stage inverter running as dc bus voltage regulator, it is very important to coordinate both units' control systems to avoid a late start and thus maximize energy production.

3. Harmonics

The Enphase inverter current output is relatively clean and its harmonic is not an issue. The SMA inverter in this study, however, presents severe harmonic contents and current ripples because it relies on a small output transformer leakage inductance interfacing with the utility grid. Due to (1) insufficient inductance, (2) inaccurate phase-locked loop, and (3) relatively low switching frequency at 16 kHz, the current ripple is excessively high, and the waveform is highly distorted, especially at light-load conditions. The phase of the inverter control loop reference voltage normally lags the utility voltage, and the control loop requires some compensation.

From the test results, it appears that the unit's control loop design does not apply proper gain at the fundamental frequency, and the output current contains a relatively high level of harmonics. The unit we tested showed some over-compensation at light load, and the zero-crossing point tends to have a current spike or current bump, which results in high harmonic contents. Its full-load current THD can barely pass the IEEE 1547 specified 5%, but the light-load THD is as high as 20% at the 10% load.

4. Anti-islanding

The IEEE 1547 standard requires that inverter disconnect from the line within 2 seconds of when an island forms. Both SMA and Enphase inverters shift the phase of the output current every second to detect the islanding condition. Under high penetration levels, the impact of such phase shift to the grid needs to be further investigated. Virginia Tech has studied and tested alternate anti-islanding methods including passive detection, frequency shift, harmonic injection, and communication between the power conditioner and grid. Phase-lock-loop simulations and experiments have been done to verify synchronization with the grid at step frequency changes.

When multiple inverters are in parallel, their anti-islanding mechanism may affect each other. If one of the inverters does not react to island operation, the other one may stay on the line without noticing or prolong its reaction time to the island condition. There are many possible scenarios, and they require further studies.

5. PCS Sizing

Most PCS manufacturers recommend that the PV panel capacity be larger than the PCS power rating. Some recommend a ratio of up to 140%. This recommendation is good from an economic standpoint, but it requires a new set of PCS datasheets or small modifications to the PCS design to avoid loss of energy production during cloud movement that tends to enhance the irradiance level via light reflection. Our recommendation is to have the ratio higher than 100% based on the installation area's sunlight conditions, but to change the manufacturer's datasheet that adds an over-load trip or current-limit power level based on the thermal condition of the PCS. This should help maximize the energy harness during cloud reflection.

6. Abnormal Voltage Test Results

For the 240-V system, the "over-" and "under-voltage" trip magnitudes derived from the tests are 262 and 211 V, respectively. In our test, the SMA inverter met the specifications. However, the Enphase inverter tripped right at 211 V immediately after a load transient was applied but reconnected back after three cycles. This indicates that the Enphase inverter is more sensitive to under-voltage conditions.

For the "voltage sag" test, we performed voltage sag tests for 90% to 0% nominal voltage conditions with different sag durations. Based on the inverter response, a low voltage ride-through curve was developed, and the results revealed that trip levels met the standard requirement.

For the "voltage swell" test, the inverter tripped at the 50^{th} cycle but did not turn offline during the 45^{th} cycle voltage swell at the 125% voltage level. However, the inverter did not fail under such a severe short-term over-voltage condition.

For the "clearing time" under 110 and 120% of nominal voltage conditions, the SMA inverter clearing times are 0.67 and 0.049 seconds, respectively, which are within the standard limits. For 88% and 50% nominal voltage conditions, clearing times (1.78 seconds and 0.156 seconds) are also within the standard limits.

For the "reconnection time" after abnormal conditions, the standards require the unit be reconnected after 5 minutes. In average, the tested SMA inverter took 5.42 minutes to reconnect to the grid once the abnormal condition was cleared. Similar results were found for the Enphase inverter. Both inverters satisfied the reconnection time requirement.

7. Abnormal Frequency

For the "abnormal frequency" trip, the average over- and under- frequency trip limits calculated from the test results are 60.41and 59.37 Hz, respectively. Based on the test results, the clearing times of SMA for both under- and over-frequency conditions (0.1099 and 0.122 second respectively) are within the standard limits.

B. Modeling and Simulation

1. PV Resource Model

For the resource models, UT utilized 1-5 second single point PV data (Knoxville, Birmingham, or UT) and hourly cloud speed and direction information data in order to develop a model for any number of other PV installations located on the same distribution system. Each PV model would basically consist of the same single point data, but would be time-shifted appropriately to account for cloud movement and PV geographic diversity. Cubic spline curve fitting has been applied for the PV resource model.

2. Modeling and Simulation with OpenDSS

The PCS framework has been added to the OpenDSS. Prototype implementation has been tested using MATLAB® as the primary method for modeling the controls. The advanced PCS control previously implemented in MATLAB® has been added as a new control within PCS Framework in OpenDSS.

Simulations were initially performed without incorporating the PCS control for actual distribution circuits under high penetration cases. The reactive power control of PCS was then added in the same distribution systems at varying PV penetration levels. The results verified that the reactive power control along with the high penetration level helped stabilize the system and flatten the voltage fluctuation. The OpenDSS is proven to have the necessary functionality to model and analyze the impact of high penetration PV on the distribution system. The results of test cases indicate that OpenDSS can be used to model any number of PV systems on any distribution circuit, with the flexibility of modeling each PV with its own power production profile. Potential interaction with the grid can be simulated over time.

6.2 Suggestions for Future Work

1. Development of electrolytic capacitor-less micro-converter and -inverter

Micro-converters and -inverters mounted under PV panels are constantly operating under high-temperature conditions, which tend to reduce the life of the electrolytic capacitor and consequently the efficiency of the PCS. Most microinverter technologies today rely on electrolytic capacitors to smooth the double line frequency ripples, and their life span has been a major question in the industry. The ultimate solution is to develop new, advanced high-efficiency micro-converter-inverter systems that can operate without bulky electrolytic capacitors. This should allow PCS life span equal to or better than the PV panel itself and ease the concerns of the industry.

2. Field demonstration with different PCS architectures

The study results indicated that micro-inverter-based PV systems produce the most energy out of the three PCS configurations. The cost of the microinverter, however, is higher than that of a centralized inverter because it requires an individual MPPT and microprocessor

controller. The series-connected micro-converter-based system in this study did not perform well in energy production due to mismatched design. The parallel-connected micro-inverter-based system can eliminate the mismatch issue. The individual micro-converter can be highly integrated and incorporated in the junction box to eliminate the additional cost of interconnection; therefore, it has the potential to become a cost-effective solution. Field testing and demonstration is necessary to prove the concept.

3. Simulation verification of large-scale high penetration PV systems

With incorporation of PCS control in the OpenDSS, the simulation results of a distribution feeder with different penetration levels in this report indicate that the voltage can be regulated with reactive power control. Such simulation results need to be verified through the study of large-scale systems. Once the model is verified, more studies can be performed with different penetration levels for both active and reactive power controls for system frequency and voltage regulation.

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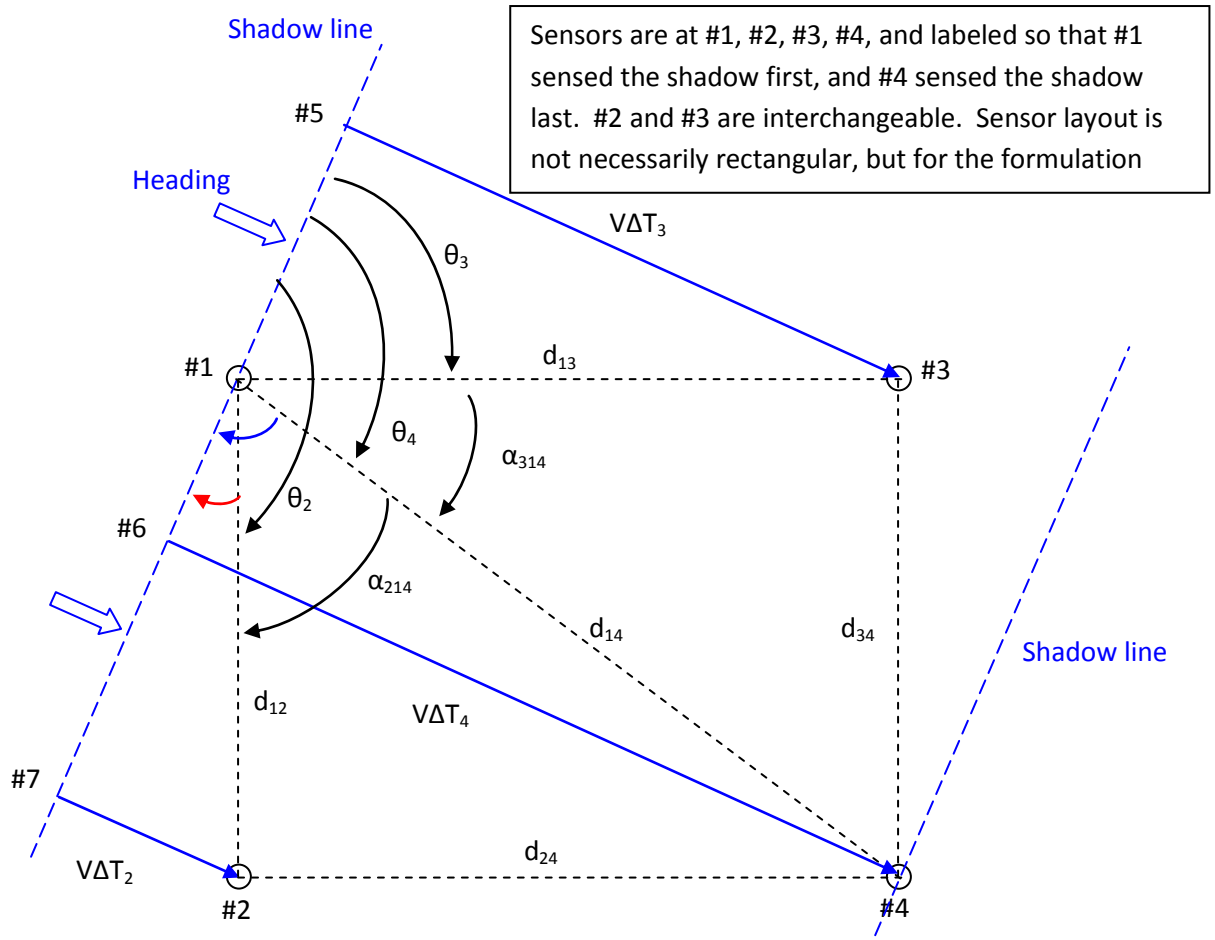
8. GLOSSARY

AC – Alternate current
CCM – Continuous conducting mode
CEC – California Energy Commission
DC – Direct current
DC-DC – Direct current to direct current converter
DC-AC – Direct current to alternate current inverter
DCM – Discontinuous conducting mode
DOE – Department of Energy
DPV – Distributed PV
DSS – Distribution System Simulator
EPRI – Electric Power Research Institute
FEEC – Future Energy Electronics Center
IEEE – Institute of Electrical and Electronics Engineering
IGBT – Insulated gate bipolar transistor
kVA – Kilo-Volt-Ampere
MOSFET – Metal oxide semiconductor field effect transistor
MPP – Maximum power point
MPPT – Maximum power point tracking
MVA – Mega-Volt-Ampere
NDZ – None detection zone
OpenDSS – Open Distribution System Simulator
PCS – Power conditioning system
PLC – Power line carrier communication
PLL – Phase lock loop
PWM – Pulse width modulation
PR – Proportional Resonant
PV – Photovoltaic
RLC – Resistor-inductor-capacitor
SCADA – Supervisory control and data acquisition
UT-Austin – University of Texas, Austin
THD – Total harmonic distortion
VA – Volt-Ampere
VT – Virginia Tech

APPENDIX A: CLOUD SHADOW MOVEMENT CALCULATIONS

A.1 Determining the Heading and Velocity of a Cloud Shadows Using Four Licor Global Horizontal Solar Radiation Sensors

Problem Statement: Given a moving shadow line sweeping over four sensors with velocity V, determine velocity V and the heading angle. ΔT represents the time relative to the shadow passing #1. This document gives a quick look at the procedure and a first-day example (January 4, 2012).



- From triangle 5-1-3, $\sin\theta_3 = \frac{V\Delta T_3}{d_{13}}$.

- From triangle 6-1-4, $\sin(180° - \theta_4) = \frac{V\Delta T_4}{d_{14}}$, so $\sin(180° - \theta_3 - \alpha_{314}) = \frac{V\Delta T_4}{d_{14}}$. (see unmarked blue arrow).
- From triangle 7-1-2, $\sin(180° - \theta_2) = \frac{V\Delta T_2}{d_{12}}$, so $\sin(180° - \theta_3 - \alpha_{314} - \alpha_{214}) = \frac{V\Delta T_2}{d_{12}}$ (see unmarked red arrow).

Thus we have three equations, and two unknowns (θ_3 and V). The problem is overdetermined and can be solved by minimizing least squared error. Begin the process by rewriting the equations as

- $\sin\theta_3 = \frac{V\Delta T_3}{d_{13}}$, yields $V = \frac{d_{13}\sin\theta_3}{\Delta T_3}$
- $\sin(180° - \theta_3 - \alpha_{314}) = \frac{V\Delta T_4}{d_{14}}$, yields $V = \frac{d_{14}\sin(180° - \theta_3 - \alpha_{314})}{\Delta T_4}$
- $\sin(180° - \theta_3 - \alpha_{314} - \alpha_{214}) = \frac{V\Delta T_2}{d_{12}}$, yields $V = \frac{d_{12}\sin(180° - \theta_3 - \alpha_{314} - \alpha_{214})}{\Delta T_2}$

Adding the three equations and rewriting yields

$$3V = \frac{d_{13}\sin\theta_3}{\Delta T_3} + \frac{d_{14}\sin(180° - \theta_3 - \alpha_{314})}{\Delta T_4} + \frac{d_{12}\sin(180° - \theta_3 - \alpha_{314} - \alpha_{214})}{\Delta T_2},$$

$$3 = \frac{d_{13}\sin\theta_3}{V\Delta T_3} + \frac{d_{14}\sin(180° - \theta_3 - \alpha_{314})}{V\Delta T_4} + \frac{d_{12}\sin(180° - \theta_3 - \alpha_{314} - \alpha_{214})}{V\Delta T_2}$$

$$\frac{d_{13}\sin\theta_3}{V\Delta T_3} + \frac{d_{14}\sin(180° - \theta_3 - \alpha_{314})}{V\Delta T_4} + \frac{d_{12}\sin(180° - \theta_3 - \alpha_{314} - \alpha_{214})}{V\Delta T_2} - 3 = 0 \qquad (1)$$

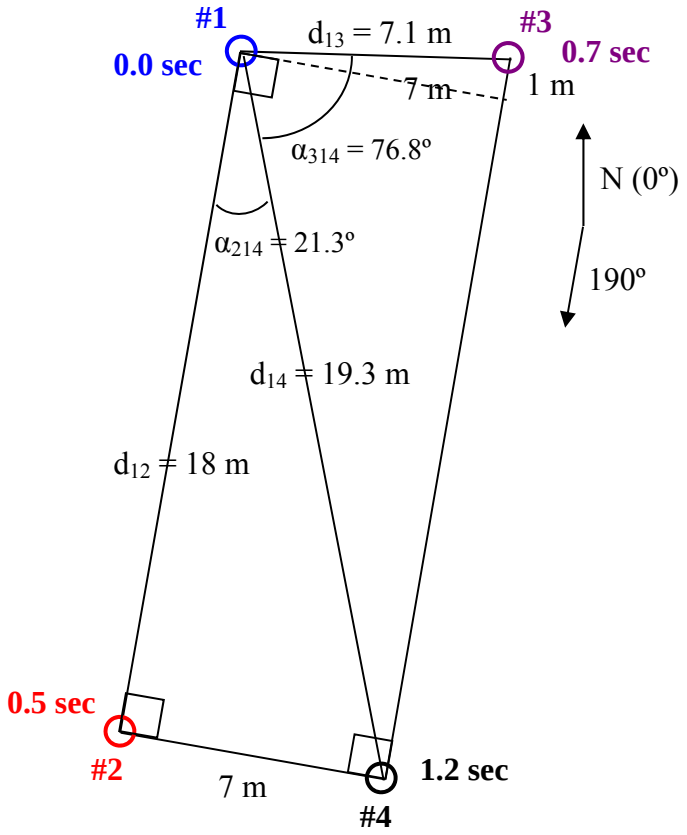
Equation (1) can solved, with V and θ_3 as unknowns, using the Excel Solver. The suggested error function to minimize is

$$\left[\frac{d_{13}\sin\theta_3}{V\Delta T_3} - 1\right]^2 + \left[\frac{d_{14}\sin(180° - \theta_3 - \alpha_{314})}{V\Delta T_4} - 1\right]^2 + \left[\frac{d_{12}\sin(180° - \theta_3 - \alpha_{314} - \alpha_{214})}{V\Delta T_2} - 1\right]^2$$

A.2 Example:

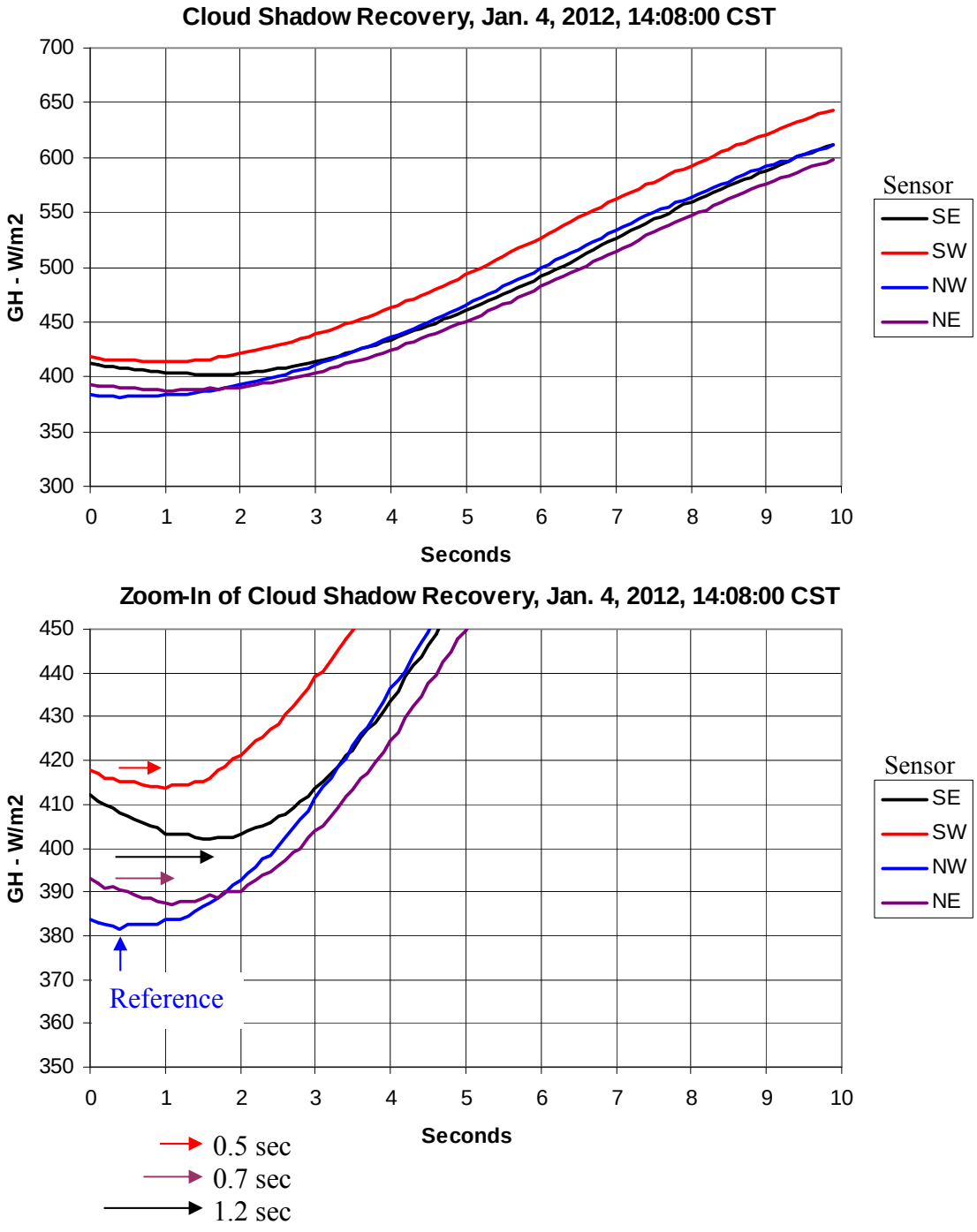
The sensor polygon is shown in the diagram below. For now, the dimensions are approximate (stepped off) values. These will be refined later. To avoid shadows and fit the roof space, the

polygon is somewhat narrow and not perfectly square. The significance of the "stepped off" errors has not yet been determined. The building alignment is 10º off a true N-S line. For the example given, the ΔT's are 0.5, 0.7, and 1.2 seconds.



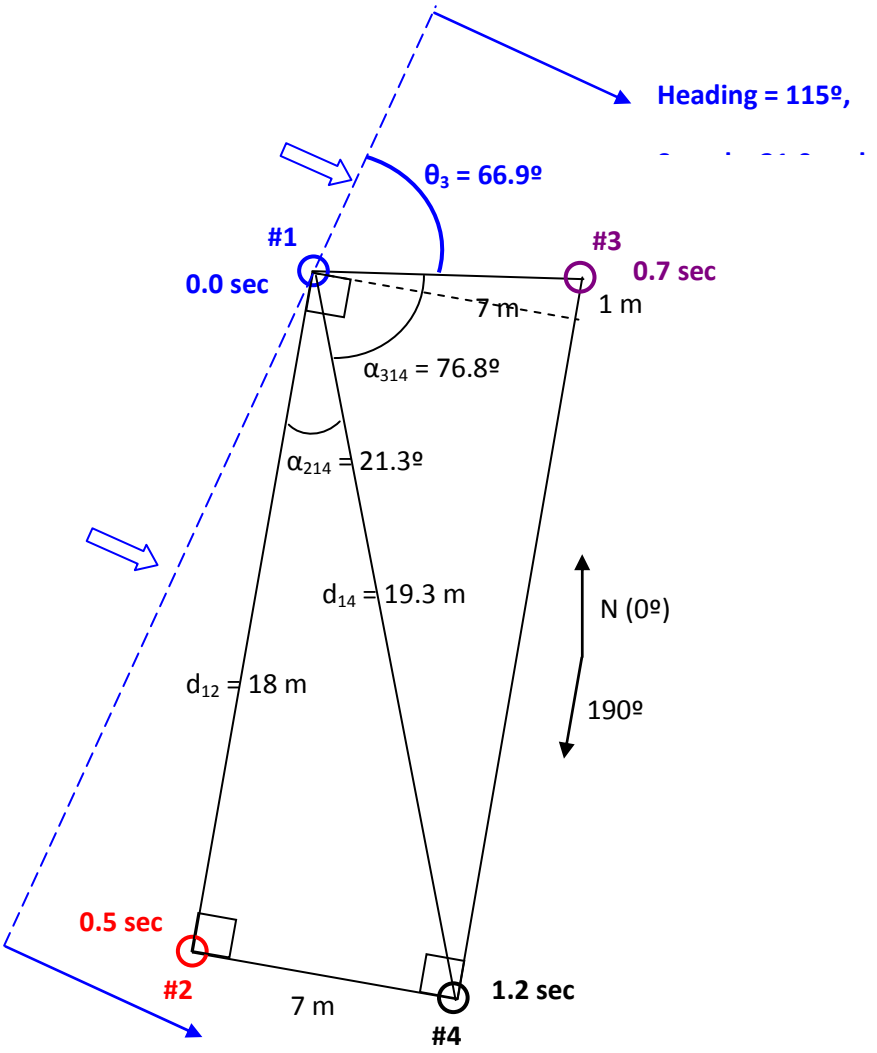
Standing Near the Center of the Sensor Polygon, January 4, 2012.
High, Thin Clouds are Moving From Left to Right in the Photo
(photo courtesy of Lucy Stolzenburg, Texas Solar Energy Society)

The recorded event is shown below. Eventually, a better procedure for estimating the ΔT's will be used. For now, the time shift is approximated only by estimating the time shifts in the minimum points. The magnitude differences are due to the fact that the Licors have not yet been properly calibrated.



The solution for this example is

- $\theta_3 = 66.9^o$,
- V = 9.40 meters/sec (corresponds to 21.0 miles per hour)
- From the figure, working in relation to line 1-2 which is oriented at 190º, the heading angle is 190º - 21.3º - 76.8º - 66.9º + 90º = 115º



The errors for the three terms are shown below:

$$\left[\frac{d_{13}\sin\theta_3}{V\Delta T_3}-1\right]^2+\left[\frac{d_{14}\sin(180^\circ-\theta_3-\alpha_{314})}{V\Delta T_4}-1\right]^2+\left[\frac{d_{12}\sin(180^\circ-\theta_3-\alpha_{314}-\alpha_{214})}{V\Delta T_2}-1\right]^2$$

$$[\,0.008\,]^2 \quad + \quad [\,0.006\,]^2 \quad + \quad [\,0.014\,]^2$$