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Matthew G. Blain, Grant Biedermann, Francisco M. Benito, James E. Stevens

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

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Matthew G. Blain, Grant Biedermann, Francisco M. Benito
Photonic Microsystems Technology

James Stevens
MESA Fab Engineering

Sandia National Laboratories
P.O. Box 5800
Albuquerque, New Mexico 87185-MS1082

Abstract

A design concept, device layout, and monolithic microfabrication processing sequence have been developed for a dual-metal layer atom chip for next-generation positional control of ultracold ensembles of trapped atoms. Atom chips are intriguing systems for precision metrology and quantum information that use ultracold atoms on microfabricated chips. Using magnetic fields generated by current carrying wires, atoms are confined via the Zeeman effect and controllably positioned near optical resonators. Current state-of-the-art atom chips are single-layer or hybrid-integrated multilayer devices with limited flexibility and repeatability. An attractive feature of multi-level metallization is the ability to construct more complicated conductor patterns and thereby realize the complex magnetic potentials necessary for the more precise spatial and temporal control of atoms that is required. Here, we have designed a true, monolithically integrated, planarized, multi-metal-layer atom chip for demonstrating crossed-wire conductor patterns that trap and controllably transport atoms across the chip surface to targets of interest.

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NOMENCLATURE

SNL	Sandia National Laboratories
LDRD	Laboratory Directed Research and Development
MESA	Microsystems Engineering Science Applications
MOT	Magneto Optical Trap
QED	quantum electro dynamics
IMD	Inter Metal-level Dielectric
CMP	Chemical Mechanical Planarization

ADVANCED ATOM CHIPS WITH TWO METAL LAYERS

A design concept, device layout, and monolithic microfabrication processing sequence have been conceived for a planarized, multi-metal-layer atom chip with high thermal conductivity dielectric separation of the conductor wires for advanced position control of an ultracold ensemble of trapped atoms. Atom chips are an intriguing system for precision metrology and quantum information devices. These devices combine ultracold atoms—well known for pristine quantum control—with the precision of microfabrication techniques. Using the magnetic fields generated by current carrying wires microfabricated upon the substrate, atoms can be confined via the Zeeman Effect. This allows magnetic guides for matter wave interferometers and atom conveyors for controllably positioning atoms near microfabricated structures and optical resonators. An attractive prospect for atom chips is the possibility of constructing more complex potentials using complicated conductor patterns (realized by monolithic microfabrication techniques and multi-level metallization), and the precise spatial and temporal control of the resulting magnetic potentials. Current state-of-the-art atom chips, however, are single-layer or hybrid-integrated multilayer devices with limited flexibility and repeatability. Here, we have designed a true, monolithically integrated, planarized, two metal-layer atom chip capable of carrying high current densities for demonstrating crossed-wire conductor patterns that trap and controllably transport atoms across the chip surface to targets of interest.

In previous efforts, crossed wire conductor patterns have been achieved by either patterning wires on both sides of a substrate with a large spacing between conductors and limited alignment precision or screen printing with metallic and dielectric pastes resulting in conductors with severe surface roughness. In the former, the exaggerated spacing demands large currents to generate sufficient trapping fields while the limited alignment precision deteriorates the accuracy of the field control. For example, transporting atoms across the chip surface requires energizing many conductor wires in a precisely timed sequence. In both efforts, inaccurate knowledge of conductor geometry (including rough wire edges) has lead to heating of the ultracold ensemble due to unpredictable shifts in the trapping potential which imparts energy to the atoms. In our approach, the two layers are two orders of magnitude closer than in reference [1] and the conductor edge roughness, fabrication precision, and heat transfer capability is greatly improved compared to reference [2].

A two layer atom chip for cross wire patterns is an untried device holding great potential for enhanced control of ultracold atom ensembles. It is worth noting that another singular effort [3] has approached this goal with wire bridges formed atop polyimide spacers. That work is quite relevant and accomplishes much of what is conceived here; however, several features render it much less than ideal, viz. non-uniform and poor thermal dissipation from the upper-level, sub-micron conductors that result in highly variable current limits, as well as intrinsically rough conductor wire edges due to lift-off metal technology.

The objective of the atom chip is to transfer atoms collected in the magneto-optical-trap (MOT) to a purely magnetic trap and subsequently shuttle the atoms across the surface to an optical cavity. Hybrid or monolithic integration of micro-optical cavities with an atom chip is desirable and may be accomplished, in principal, by fabricating optical cavities in Si (silicon) substrates. Relevant prior work describing the fabrication and performance of micro-optical cavities in Si

may be found in reference [4]. An approach similar to that in reference [2] for “long distance” transport of atoms was adopted in which two metal conductor layers are used, the top layer creating a magnetic waveguide and the bottom layer creating a “conveyor belt” for precise control and movement of atoms along the waveguide. Guided by Biot-Savart numerical simulation results from reference [5], the appropriate wire patterns for generating the magnetic trapping potentials for atom loading and shuttling were determined. The calculated positions for the upper-level and lower-level conductor wires from [5] are shown in Figures 1 and 2. These calculations were used to define the layout of the photomasks (shown in Figure 3) and will be used in the (future) fabrication of the two-level-metal atom chip. Figure 4 shows photomask detail of the three-way splitting in the upper conductor wave-guide for transporting atoms to the micro-optical cavities and Figure 5 shows detail of the locations of the cavities.

Next, we defined a process integration sequence for micro-fabrication of this atom chip microfabrication in Sandia’s MESA facility. The process integration sequence extends a single level conductor fabrication technology that was successful in an earlier effort. That effort demonstrated a single metal-level atom chip with a smooth dielectric top layer plus dielectric mirror stack for trap loading of Rb (rubidium) atoms.

Using photolithographically defined and plasma etched aluminum conductors, much smoother wire edges result compared to the typical wire edges formed from lift-off or electroplated metal (Figure 6). The conductors are buried in a planarized dielectric to form each layer and this may be repeated more than twice, in principal, to form a many layer device. In this work, a chemical mechanical polish (smoothing) step *between* the metal layers is added to the process sequence to maintain device planarity throughout the process. Interlayer electrical vias made of W (tungsten) are used to connect the two layers, thereby accommodating the high currents in conductors having a crossed-wire configuration. As in our prior device, the top surface of the final dielectric layer that covers the upper conductor layer is then polished and a mirror coating of gold, copper, or a dielectric mirror stack, is deposited. Thus, employing lithographically-based, solid-state, and in particular silicon device fabrication techniques, a true monolithically integrated, multi-layer atom chip device may be realized. An added advantage of this approach is the possibility of either hybrid or monolithic integration of micro-optical cavities for quantum information experiments. A schematic cross-section of the atom chip film stack design is shown in Figure 7.

The materials used for fabrication of the current carrying current wires in two metal levels also must provide sufficient heat dissipation from both levels of wiring to the silicon substrate. Comparison of alternative dielectric spacer materials for improved heat dissipation shows AlN (aluminum nitride) with a thermal conductivity of 140-180 W/m·K to be a two order-of-magnitude improvement over SiO₂ (silicon dioxide) which has a thermal conductivity of 1 W/m·K. As sputter deposition of AlN is an established capability in Sandia’s MESA facility, a process integration sequence has been defined that will utilize AlN as both the inter-metal-level (IMD) dielectric and the electrical insulator between the bottom metal conductor level and the underlying silicon substrate, replacing SiO₂ in both places. A dielectric layer of sputtered aluminum nitride (AlN) is deposited on top of the silicon followed by a layer of sputtered metal (Al-1/2%Cu) after which the patterned and etched metal lines are covered by another layer of insulating aluminum nitride and the gaps filled with SiO₂. Vias are etched through the oxide and the AlN layer to form contacts to the AlCu metal lines and then filled with tungsten. An

oxide “etchback” process partially exposes tungsten plugs so that a top layer of AlCu may be deposited and patterned to form the upper level wires and wire-bonding pads at the edge of the chip.

In summary, this very small LDRD project has resulted in a design concept, device layout, and monolithic microfabrication processing sequence definition for microfabricating a planarized, multi-metal-layer atom chip with high thermal conductivity dielectric separation of the conductor wires for advanced position control of an ultracold ensemble of trapped atoms. Future work should entail fabricating the atom chip using Sandia’s MESA microfabrication facility and experimentally demonstrating its atom trapping and transporting capabilities. The four key advancements in the atom chip design concept developed in this work are:

1. multi-level, etched Al current conductors wires resulting in ultra-smooth conductor wire edges
2. tungsten (W) via technology for wire crossings and inter-level electrical connection
3. planarized dielectric layers between metal layers and for placement of a top mirror surface (mirror MOT) in extremely close proximity (a few micrometers) to the conductor wires
4. use of aluminum nitride (AlN) inter-metal dielectric in place of silicon dioxide (SiO_2) for increased thermal dissipation from the conductors to the chip substrate (Si)

The benefit of a multi-level atom chip is the establishment of a hardware technology platform on which advance sensing and quantum information processing capabilities may be realized using the quantum states of clouds of cold atoms. Demonstrating a two-layer device for controlled atom transport to microfabricated structures such as micro-optical cavities may ultimately be useful for building a scalable device for quantum networking using ultracold atoms in cavities, a topic of immediate interest for many investment areas concerned with secure information transfer.

FIGURES

Figure 1: Figure 1.5 from Reference [5] showing the calculated position of the upper metallization layer which moves a cold atom cloud from the collection region (i.e. the MOT Center) to a micro optical cavity for cavity QED (quantum electrodynamics) experiments.

Figure 2: Figure 1.9 from Reference [5] showing the calculated position of the lower metallization layer which provides confinement of the atoms in the x direction by canceling out magnetic bias field in the positive x direction.

Figure 3: Shows the two-level-metal atom chip layout using data from Reference [5].

Figure 4: Detail of two-level-metal atom chip layout showing three-way splitting in upper metal wave-guide for transporting atoms to the micro-optical cavities.

Figure 5: Location of micro-optical cavity mirrors (green circles - 30 total) for cavity QED experiments.

Figure 6: Atom chip conductor wire edge roughness. Left: Electroplated Au wires. Middle: Au wires formed by metal lift-off. Right: Photolithographically patterned and plasma etched Al wires.

Figure 7: Planarized, two-level metal atom chip, using AIN (aluminum nitride) for thermally conductive, electrically insulating inter-level-metal dielectric (IMD) and W (tungsten) electrical vias for wire cross-overs.

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