Thermal Analysis of a DZero H-Disk Wedge

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1.0 Introduction

Each H-Disk ring assembly is comprised of 24 wedge assemblies. Figures 1-1 and 1-2 show the wedge mechanical layout. Each wedge consists of sets of two single-sided silicon detectors (referred to as inner and outer detectors, corresponding to their radial positioning) as provided by Moscow State University. Since these detectors are single sided, two mated inner/outer sets are arranged back-to-back such that they effectively become a double-sided detector with a 15° angle between the strips on either side.

Six SVX II chips are mounted near the outboard edge of each outer detector since this location provides access to bond pads spanning the entire detector surface. Since the detector and chip bond pads are on significantly different pitches (approximately 80 vs. 48 microns), a pitch adapter is used to transition this jump, thus simplifying wirebonding. With the accompanying electronics required to support detector operation placed adjacent to the chips, the mounting ring, which also acts as a means of cooling for the wedge, is by necessity located some distance from the chips, which are the primary heat source.

The purpose of this report is to document the results of a thermal performance study of a wedge assembly. The methods, assumptions, and results for this investigation are discussed below.

2.0 Methodology

2.1 Description of the Model

A two-dimensional finite difference model has been developed to investigate the thermal performance of a wedge assembly. This modeling is similar in technique to that developed for other silicon detector designs by Paul Ratzmann (e.g., see [1] and [2]). Essentially, thermal resistances are calculated along a material layer and between different material layers, and, with the imposition of boundary conditions and a driving heat load, the total resistance network can be solved for temperatures and heat flows. The EES code [7] is used for this study.

There are eight layers included in the model, as listed below. Note that the term "cooled" and "exposed" refers to the side of the detector that is cooled and that which is not, respectively.

Exposed side SVX II chip
Exposed side readout structure Be substrate
Exposed side Si detector set
Exposed side center Be layer
Cooled side center Be layer
Cooled side Si detector set
Cooled side readout structure Be substrate
Cooled side SVX II chip

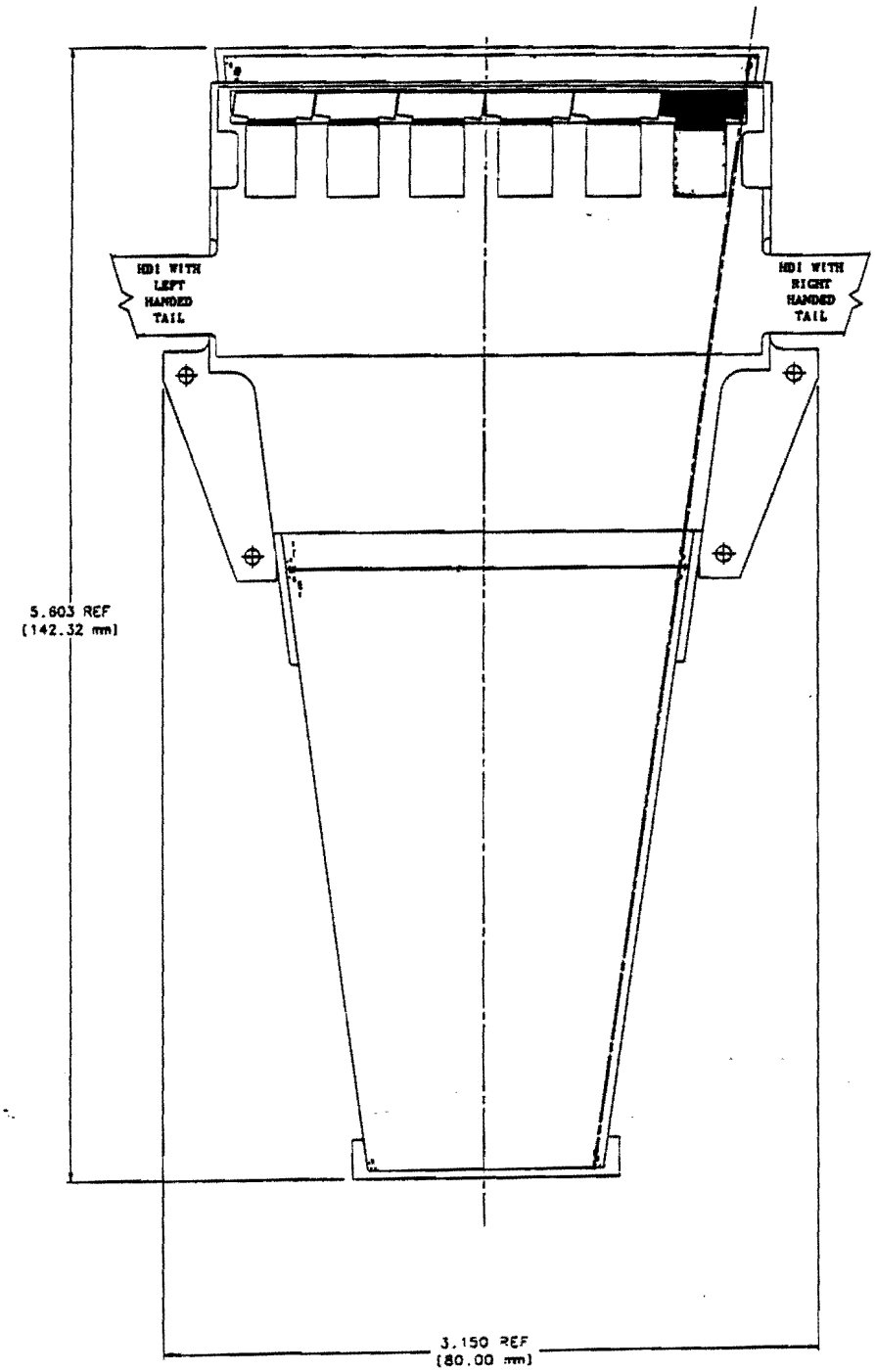

Figure 1-1
H-Disk Wedge Layout

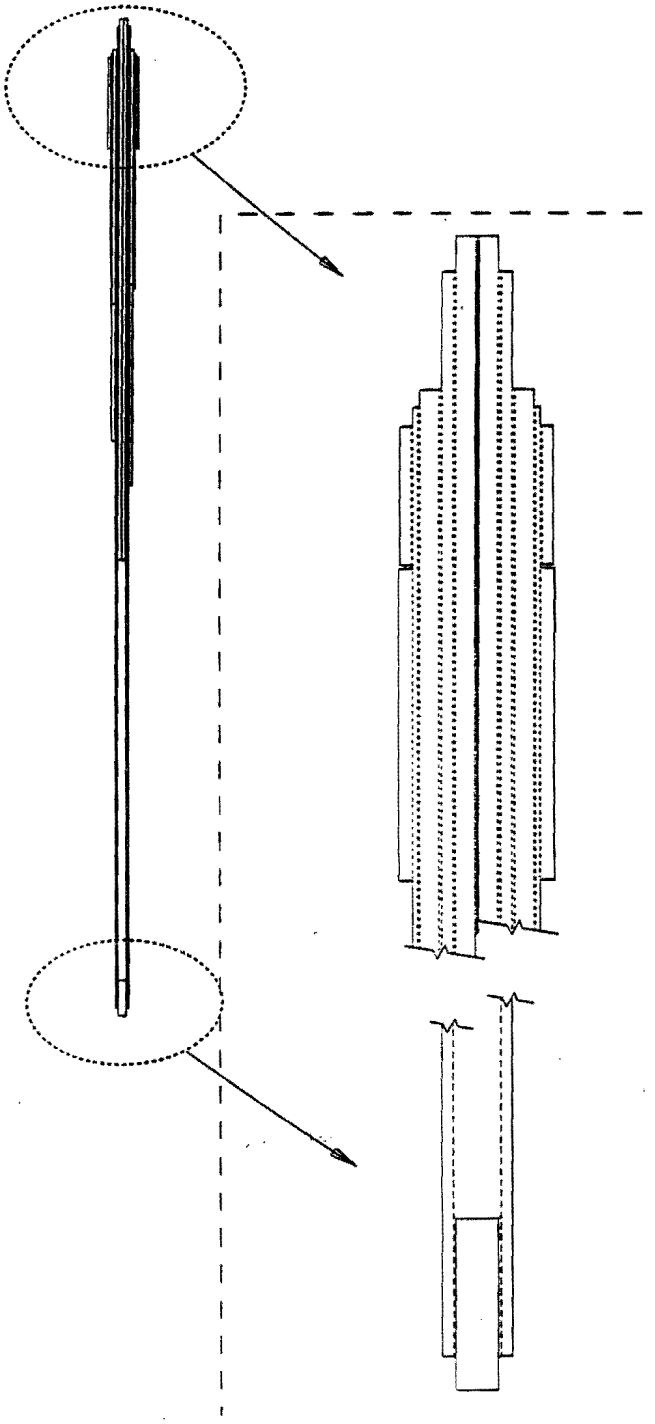

Figure 1-2
H-Disk Wedge Side View

The other axis is oriented along the centerline of the wedge, with X=0 defined as the outer edge of the readout structure substrate and X = Xmax at the inner edge of the inner silicon detector. The small amount of the detector that extends outboard of the readout structure substrate is ignored, as is the spacer located at the inner edge. Several regions are defined for computational purposes based on the physical extent of the layers and the boundary conditions. Since the detector is wedge-shaped, the reduction in width along the wedge length is accounted for in the model (except for the cooled side Be substrate, which is assumed to conduct over its full width due to its configuration in relationship to both the wedge and the cooling channel).

Several cases are analyzed to evaluate the sensitivity to the following parameters:

- SVX II chip power dissipation
- Beryllium substrate thickness
- Epoxy thickness
- Cooling ring surface temperature
- Ambient temperature

2.2 Input Assumptions

The following information represents the assumptions used for the Reference Case. Deviations from some of these assumptions are investigated to gauge parameter sensitivity.

a. SVX II chip heat load = 0.64 Watts per chip [3].

b. No heat generation internal to the silicon, resulting from radiation damage to the detectors, has been included in this study.

c. Each of the four beryllium layers are 20 mils thick. The silicon detectors and pitch adapter are 300 μm thick while the SVX II chip is 500 μm thick.

d. Thermal conductivities for beryllium and silicon are assumed to be 215 and 149 W/m-K, respectively [4,1].

e. An HDI thickness of 5 mils is used [5]. A thermal conductivity of 0.24 W/m-K is assumed.

f. The following interface gaps are modeled [6].

	t = 1 mil	k = 0.85 W/m-K
SVX II chip to HDI (Tracon)		
Pitch adapter to HDI (Ablestik)	2	1.0
HDI to Be (Ablestik)	2	1.0
Readout substrate to Si (Ablestik	2	1.0
as an insulator plus Hexcel)	1	0.2
Si to center Be (Hexcel)	3	0.2
Center Be to Center Be (Hexcel)	3	0.2
Thermal grease on mount interface	2	0.7

g. The ambient environment is assumed to be 20°C and is dry enough to preclude condensation. A heat transfer free convection coefficient of 5 W/m^2-K is used.

h. The surface temperature of the cooling channel is assumed to be uniformly at -5°C. The determination of the temperature difference between the bulk coolant temperature and the mounting surface temperature is outside of the scope of this report. For the purposes of this analysis, it is simply assumed that the effect of cooling ring wall conductivity and coolant channel convection resistances and the difference between the local and inlet coolant temperatures are designed such that the above surface temperature can be achieved.

3.0 Results

For the Reference Case, the temperatures in the two silicon and two readout structure substrate layers are shown in Figure 3-1. The two inner detectors (X > ~60 mm) are at approximately the same temperature. With no heat generation in this region, the temperatures are set by conduction to the rest of the detector and convection with the ambient environment. At the inner-to-outer detector gap a significant temperature jump occurs, especially for the silicon on the exposed wedge side. Heat flow in this region must be transferred from the inner detectors through the glue gap to the center Be layers (not shown) or through the large resistance across the Si-to-Si gap simulating the wirebonds.

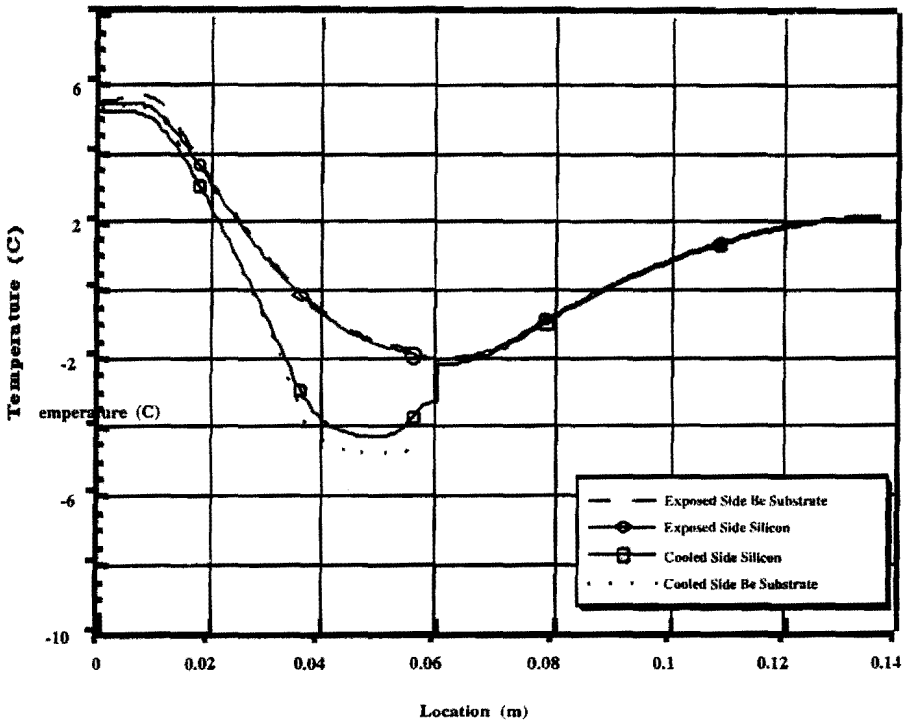

Figure 3-1
Silicon and Readout Structure Substrate Temperatures, Reference Case Results

The area of the cooling channel (X = approximately 36 to 56 mm) has the highest thermal gradient through the thickness of the wedge, with the cooled side substrate and silicon relatively close to the cooling channel temperature and the exposed side layers significantly warmer due to the intermediate layers of Be and adhesive.

In the region between the chips and the cooling channel (X = approximately 14 to 36 mm), no heat generation is modeled, and the difference in slopes shows how the heat is migrating from the exposed side of the wedge to the cooled side. In the region beneath the SVX II chips (X = approximately 5 to 14 mm), the substrates and silicon are at their warmest.

The temperatures in the two Be layers between the silicon layers is not shown in this figure, but temperatures there are generally bounded by the silicon layers between which they are sandwiched except in the area near the chips, in which the layers nearer the chips are warmer, and in the area inboard of the inner-to-outer silicon wafer gap, where the center Be layers cool the warmer silicon "fins".

Since the detector is symmetrically constructed, "bimetallic strip" effects due to differential thermal expansion coefficients between layers is minimized. Even for a symmetric configuration, a temperature gradient in a cross-section can induce some amount of bowing. For the gradients shown in Figure 3-1, these deflections would be expected to be small (less than 10 microns).

Figure 3-2 shows the results for the case with Reduced SVX II Chip Power and demonstrates the same general trends as the Reference Case. As expected, the wedge runs cooler, with the maximum silicon temperature 2.1°C lower in the chip region. Since the inner detector temperature behavior is dominated by convection with the surroundings rather than chip power, it is only slightly impacted by the chip power.

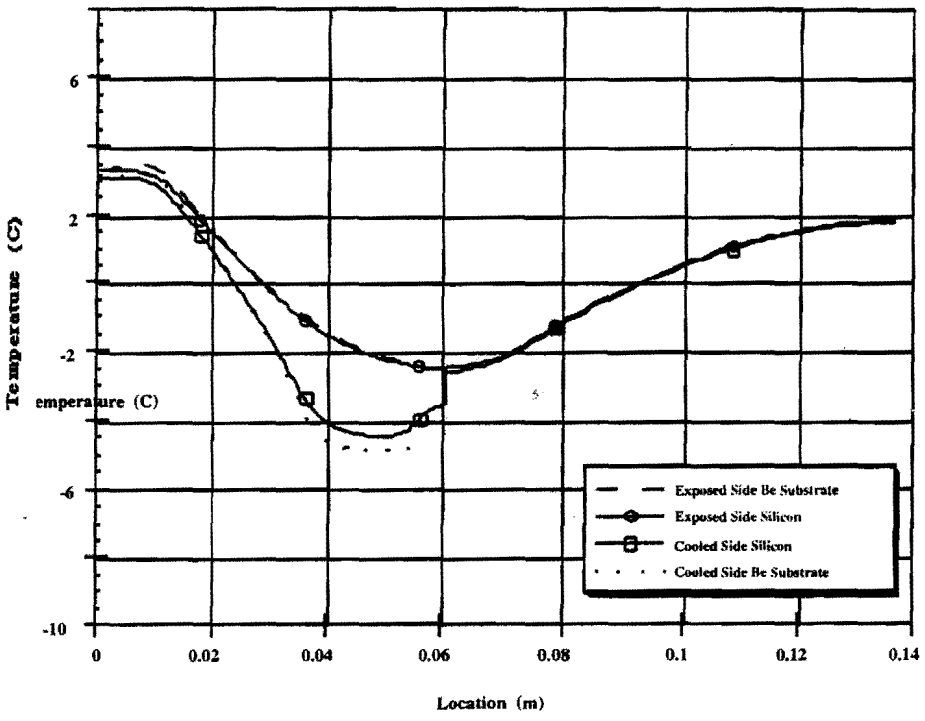

Figure 3-2
Silicon and Readout Structure Substrate Temperatures, Reduced SVX II Chip Power from 0.64 W/chip to 0.50 W/chip

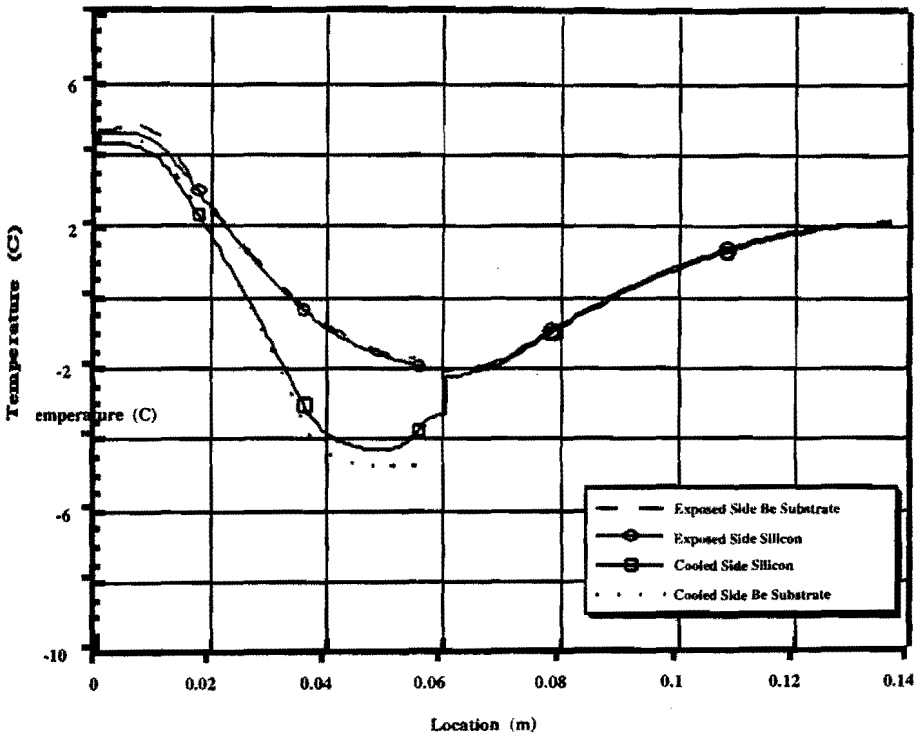

Figure 3-3
Silicon and Readout Structure Substrate Temperatures,
Increased Readout Structure Substrate Thickness from 20 to 25 mils

Figure 3-3 shows the results for the case with Increased Readout Structure Substrate Thickness and demonstrates the same general trends as the Reference Case. As expected, the wedge runs slightly cooler, with the maximum silicon temperature 0.8°C lower in the chip region. The temperature of the inner detectors is nearly unchanged from the Reference Case results.

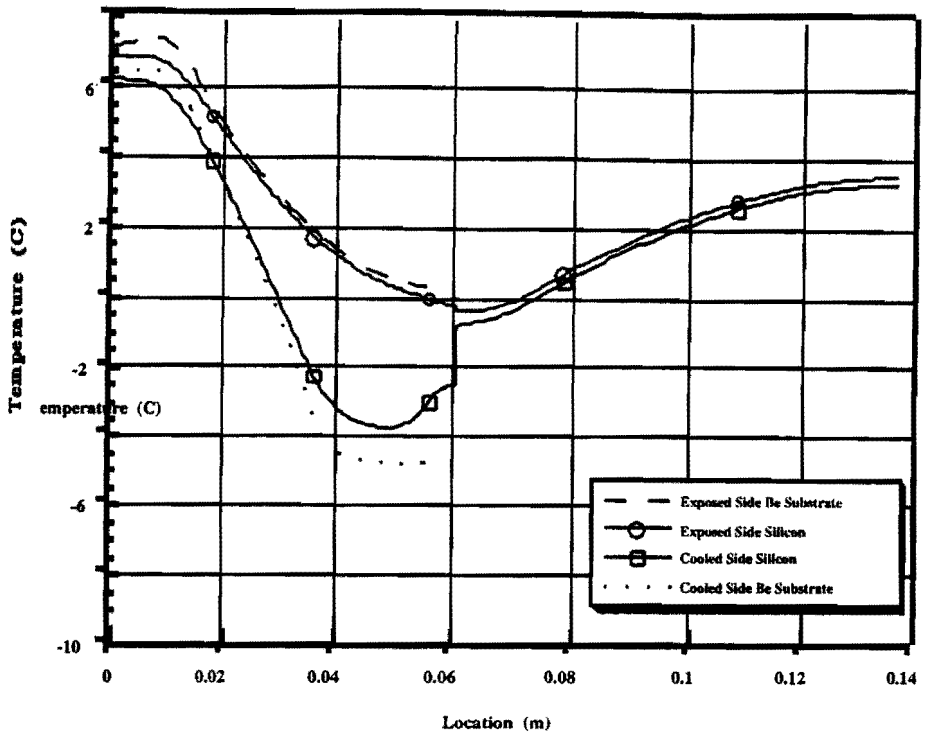

Figure 3-4
Silicon and Readout Structure Substrate Temperatures, Increased Si-to-Be Adhesive Thicknesses from 3 to 5 mils

Figure 3-4 shows the results for the case with Increased Si-to-Be Adhesive Thickness and demonstrates the same general trends as the Reference Case. The temperature difference between the exposed side and cooled side layers is more pronounced for this case due to the added thermal resistance between layers. The wedge therefore runs significantly warmer, with the maximum silicon temperatures about 1.5°C hotter in the chip region and 1.3°C higher at the innermost edge of the inner detectors.

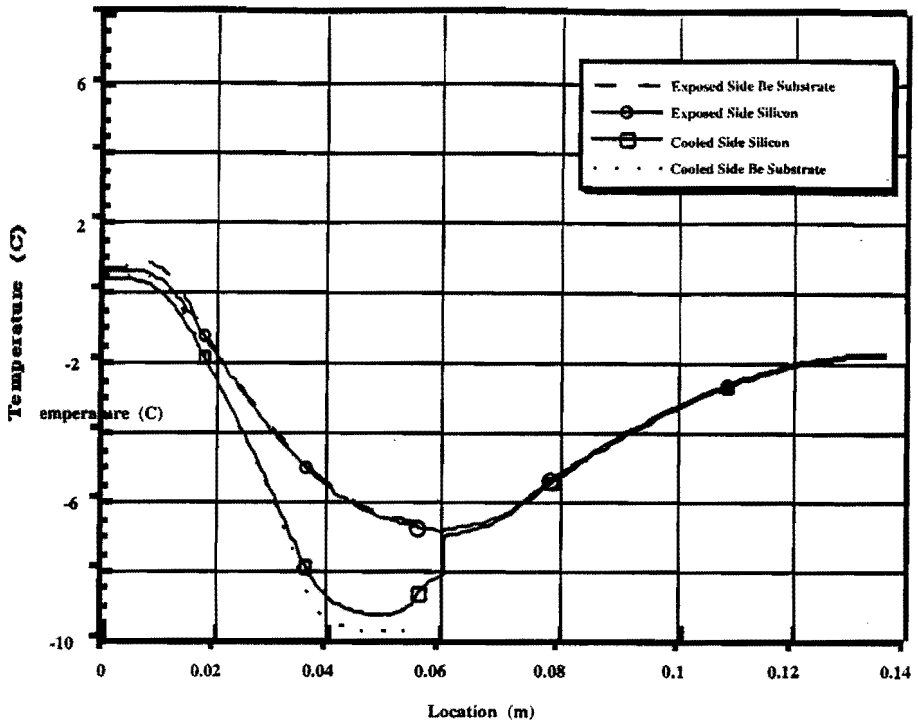

Figure 3-5
Silicon and Readout Structure Substrate Temperatures, Decreased Cooling Channel Surface Temperature from -5 to -10 °C

Figure 3-5 shows the results for the case with Decreased Cooling Channel Surface Temperature and demonstrates the same general trends as the Reference Case. As expected, the wedge runs considerably cooler, with the maximum silicon temperature 4.8°C lower in the chip region (nearly a 1°C change for each degree change in the cooling channel) and 3.9°C cooler at the innermost edge of the inner detectors.

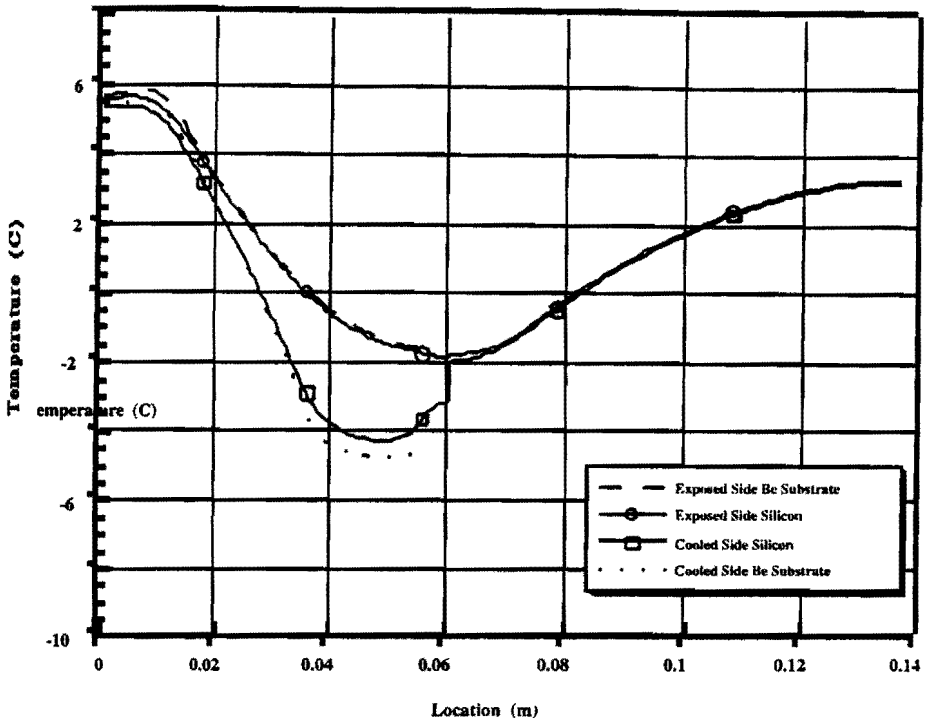

Figure 3-6
Silicon and Readout Structure Substrate Temperatures, Increased Ambient Temperature from 20 to 25 °C

Figure 3-6 shows the results for the case with Increased Ambient Temperature and demonstrates the same general trends as the Reference Case. In the chip region, the silicon temperature increases only 0.2°C, as the temperature here is dominated by the chip heat load rather than by convective loading. For the inner detector, which is more sensitive to the ambient conditions, the temperature at the innermost radial edge increases by 1.1°C.

4.0 Summary / Conclusions

Figures 3-1 through 3-6 show the sensitivity trends of the H-Disk detector wedge design to several parametric variables. A summary of these effects is shown in Table 4-1 below. For each case, the table shows the maximum Si detector temperature (found in the region beneath which the SVX II chips are mounted), the maximum temperature in the inner detector wedges (found at the innermost radius), and a factor that indicates how much of the heat load removed by the cooling channel is attributable to the chip power dissipation. As this last factor indicates, convective loads comprise an additional heat load above that contributed by the chips. The cooling design should therefore give some consideration to this additional heat load.

Table 4-1
Summary of Thermal Analysis Sensitivities

Case Description	Maximum Si Temperature (°C) Beneath Chip Region	Maximum Si Temperature (°C) in Inner Detector Region	Total Cooling Channel Heat Removal / Chip Heat Load
Reference Case	5.4	2.2	1.16
Reduced Chip Power (0.64 to 0.50 Watts/chip)	ΔT = -2.1 from Ref. Case	ΔT = -0.3 from Ref. Case	1.21
Increased Substrate Thickness (20 to 25 mils)	ΔT = -0.8 from Ref. Case	ΔT = -0.1 from Ref. Case	1.17
Increased Si-to-Be Adhesive Thickness (3 to 5 mils)	ΔT = +1.5 from Ref. Case	ΔT = +1.3 from Ref. Case	1.15
Decreased Cooling Channel Surface Temp. (-5 to -10°C)	ΔT = -4.8 from Ref. Case	ΔT = -3.9 from Ref. Case	1.20
Increased Ambient Temp. (20 to 25°C)	ΔT = +0.2 from Ref. Case	ΔT = +1.1 from Ref. Case	1.20

5.0 References

1. Ratzmann, Paul, "Thermal Analysis of the D0 3 Chip Single Sided Ladder," D0EN 3823.112-EN-447, 6/18/96.

2. Ratzmann, Paul, "Heat Transfer and Thermal Bowing Calculations of the D0 F-Disk," D0EN 3823.112-EN-456, 8/26/96.

3. Email Message, "Re: NWA Test," from Bill Cooper to Bruce Squires, 2/15/97.

4. Ratzmann, Paul, "L0 Ladder Thermal Measurements and Radiation Damage Update for the SVX II," Technical Note dated 5/5/97.

5. Conversation with Mike Matulik, 11/21/97.

6. Gillespie, G., Jostlein, H., and Ratzmann, P., "Thermal Conductivity Measurements of a Variety of Epoxies and Greases used for CDF/D0 Silicon Detector Ladder Construction, Revision 1," Technical Note dated 1/23/96.

7. Engineering Equation Solver (EES) version 4.401, by F-Chart Software, Middleton, Wisconsin.