Engineering Note

CALORIMETER PREAMPLIFIER HYBRID CIRCUIT TEST JIG

ENGINEERING NOTE

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Project: Calorimeter Preamplifier Hybrid Circuit Test Jig.
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Subject: Theory Of Operation

Introduction:

The purpose of the Calorimeter Preamplifier Hybrid Circuit is to do the initial amplification of the Calorimeter signals. The test jig consists of the following main blocks:

- 1- Main power supply, which converts 120V AC to the regulated +15V, -15V, and +5V DC values.
- 2- LED display board
- 3- Zero insertion force board (ZIF) which includes:
 - a_ ZIF socket.
 - b_ U1 and S1 DIP switches, which are accessible to the vendor. They are used to select the desired detector capacitor which is applied to the input of the related preamp specie.
- 4- Electronic board which includes:
 - a_ Two NOR gates which are configured as a latch to eliminate the switch (Push-to-Test button) bounce.
 - b_ +10V, -10V, -10V ref, -5.2V, +12V, +8V, and -6V voltage regulators.
 - c_ +15V, -15V, and +5V voltage window comparators.
 - d_ +12V, +8V, and -6V current window comparators.
 - e_ Digital logic
 - f_ Test pulse and trigger pulse.
 - g_ Current source.
 - h_ U26 DIP switch, which is accessible to the vendor. It is used to select the desired resistor value at the emitter of the current source. The selected resistor value depends on the device under test (DUT) category. There are three categories:
 - 1- DUT with 5 pF feedback capacitor includes preamplifier species: A, B, C, and D.
 - 2- DUT with 10 pF feedback capacitor includes preamplifier species: E, F, G, Ha, Hb, Hc, Hd, He, Hf, and Hg.
 - 3- DUT with 22 pF feedback capacitor includes only one specie: I.

NOTE: THE FIRST TWO CATEGORIES ARE TESTED BY ONE TEST JIG AND THE THIRD CATEGORY BY ANOTHER TEST JIG CALLED I. THEREFOR THE ADVICE TO THE VENDOR

IS TO ACCESS THE U26, U1, AND S1 DIP SWITCHES WHEN TESTING THE FIRST TWO CATEGORIES AND NOT TO ACCESS THESE DIP SWITCHES WHEN TESTING THE THIRD CATEGORY.

The following diagram shows the test jig block diagram and its connection to the external equipment:

Note:

TP1, TP2, and TP3 are the outputs of the DUT for each of the first, second, and final stage respectively. TP4, TP5, and TP6 are the outputs for current measurements of each power rail, including +12V, -6V, and +8V respectively.

TL is the terminal load used to terminate DUT output.

L/R is the Local/Remote switch to switch the test jig to the desired mode of operation.

Theory of operation:

There are two ways in which the testing may be initiated, remotely or locally. If the remote operation is desired, an external TTL level signal must be provided to the test jig with the remote/local switch on the side of the test jig switched to remote. A logic high will initiate the test. A logic low will terminate the test. In the event that an external signal is connected to the test jig while local operation occurs, the local control takes precedence over remote control.

Once a DUT has been locked in the ZIF socket and the DIP switches are selected, the Push-to-Test button may be depressed. Momentarily depressing the button will initiate a test with a minimum 400 ms duration. At the same time a PBCLOCK and PBLATCH pulses will be initiated and the power rails +12V, +8V, and -6V will be ramped to full voltage. The time at which the power rails reach the full voltage is about 13 ms and it is synchronized with bypass capacitors placed on COMP input of U20 and U22 and on the output of U23 voltage regulators (see schematic #2). The voltage rails are supplied to a

$\pm 10\%$ window comparator (see schematics 3, 4, & 5). A red LED indicates the rail is below or above 10% of the design value. A green LED indicates the rail is within acceptable limits. For DUT with a 5 pF and 10 pF feed back capacitor, the +12V and +8V rails are current-regulated to 19mA and 22 mA respectively and the -6V rail is short-circuit protected within the regulator. For DUT with a 22 pF feed back capacitor the current regulation is the same as above except that the +8V rail is current regulated to 43 mA. The power rails are supplied to the DUT via a 10 Ω resistor. The voltage drop across this resistor is sensed by a differential amplifier AD620 and amplified by a gain of 10 (see schematics 6, 7, & 8). An external BNC connection is provided from this point to allow for current measurements by the vendor. The current value for each rail is calculated by measuring the voltage value at this point and divided by (10*10 Ω). The next stage inverts and amplifies the voltage signal by a factor of 5 for +12V and -6V rails and by a factor of 1 for +8V rail. For DUT with 22 pF feed back capacitor the amplification factors are same as above except that the amplification factor for +8V rail is a gain of 2. An offset null potentiometer is provided between the AD620 and the inverting stage which eliminates device offset current errors. The inverted and amplified voltage is presented to two window comparators. One of them compares the inverted and amplified voltage to the low threshold point and the other one compares the inverted and amplified voltage to the high threshold point. If the inverted and amplified voltage is within the low and high threshold points, both the low and the high current LEDs illuminate green indicating the current is within acceptable limits. If the inverted and amplified voltage is below the low threshold point or above the high threshold point, the low current LED or the high current LED illuminates red, respectively, indicating the current is outside acceptable limits.

The following tables show:

- 1- The current ranges in respect to the designed target current.
- 2- The window current ranges that the window comparators are capable of handling.

For DUT With 5 pF Or 10 pF Feedback Capacitors

Current Window Comparator		+8V	+12V	-6V
Target Current		20.45 mA	9.25 mA	10.4 mA
Current Range		$\pm 34.47 \%$	$\pm 10.27 \%$	$\pm 10.58 \%$
Window Current Range	Low	9 mA	6 mA	7 mA
	High	33 mA	11 mA	12 mA

For DUT With 22 pF Feedback Capacitor

Current Window Comparator		+8V	+12V	-6V
Target Current		18.2 mA	9.18 mA	10.2 mA
Current Range		$\pm 10 \%$	$\pm 10 \%$	$\pm 10.58 \%$
Window Current Range	Low	8 mA	6 mA	7 mA
	High	24 mA	11 mA	13 mA

When the PBCLOCK pulse is initiated an 18 ms delay pulse is generated by U12:A (see schematic #9). This 18 ms delay pulse is used to delay the test pulse to the DUT, and the current rails data to the LED board. This delay is needed for two purposes:

- 1- To make sure that the power rails +12V, +8V. and -6V are ramped to the full voltage. So, that the DUT is stabilized on these full voltage rails before getting the test pulse.
- 2- To make sure that the current rails are stabilized. So, that the LED board will get the correct data.

As it is mentioned earlier, the power rails need about 13 ms to ramp up to the full voltage, but an addition of 5 ms is added to it to make it 18 ms which is the time needed for the DUT currents to stabilize.

When the PBCLOCK pulse is initiated a 268 ms delay in the trigger pulse is generated. 18 ms by U12:A and 250 ms by U40:A (see schematic #12). This delay in the trigger pulse is needed to make sure that DUT output base line is stable.

To synchronize the trigger pulse with the rising edge of the DUT output, two AND gates are used to AND the output of the Crystal oscillator U24 with DFF output U42:A:5 and with DFF output U42:B:9 (see schematic #12).

If the DUT passes the supply current test (the summation signal is satisfied in schematic #9), then a 1 ms test pulse period is generated by U25:A (see schematic #12). U27 is used to convert the generated test pulse from TTL level To MECL level. This MECL level is presented to the current source circuit to generate an amount of current (I_e) to charge the DUT. The amount of current produced depends on the DUT categories. The amount of current produced is controlled by the test pulse width (T_w) generated by U25:A and by the resistor value (R_e) at the emitter of Q5 and Q6. The following table shows the I_e values and the corresponded T_w , and R_e values.

DUT Categories	I_e	T_w	R_e
5 pF Feedback Cap.	75 μ A	200 ns	44.89 K Ω
10 pF Feedback Cap.	175 μ A	200 ns	22.95 K Ω
22 pF Feedback Cap.	1320 μ A	50 ns	2.515 K Ω

Title		-6 Volt Current Monitor	
Size		Colorimeter Test Jig	
C	Number	3823-121-EC-330241	Rev
Date		10-11-96	Drawn by Linda Bagby
Filename		FINALJ.SCH	Sheet 2 of 13

Title		Digital
Calorimeter Test Jig					
Size	Number			Rev	
C	3823-121-EC-330241			-	
Date	10-11-96			Drawn by Linda Bagby	
Filename	FINAL1.SCH			Sheet	4 of 13

Title		POWER DISTRIBUTION	
Calorimeter Test Jig			
Size	Number	Rev	
C	3823-121-EC-330241	-	
Date	10-11-95	Drawn by	Linda Bagby
Filename	FINALJ.SCH	Sheet	7 of 13

Title		+8 DISPLAY	
Calorimeter Test Jig			
Size	Number	Rev	
C	3823-121-EC-330241	-	
Date	10-11-96	Drawn by	Uda Bagby
Filename	FINAL SCH	Sheet	8 of 13

Title		+12 DISPLAY	
Calorimeter Test Jig			
Size	Number	Rev	
C	3823-121-EC-330241	-	
Date	10-11-96	Drawn by	Linda Bagby
Filename	FINALJ.SCH	Sheet	10 of 13

- +12HLEDF
- +12HLEDR
- +12LLEDF
- +12LLEDR
- +8HLEDF
- +8HLEDR
- +8LLEDF
- +8LLEDR
- 6HLEDF
- 6HLEDR
- 6LLEDF
- 6LLEDR
- SUMLEDF
- SUMLEDR
- +12RAILF
- +12RAILR
- +8RAILF
- +8RAILR
- 6RAILF
- 6RAILR
- +15VLED
- 15VLED
- +5VLED
- +5V
- GNDA

HDR26M
J1

TO LED DISPLAY BOARD

Title		Digital to LED Display Connector	
Calorimeter Test Jig			
Size	Number	Rev	
C	3823-121-EC-330241	-	
Date	10-11-96	Drawn by	Linda Bogby
Filename	FINALJ.SCH	Sheet	11 of 13

A=C1+C2
B=C1+C2+C5+C6
C=C12+C13
D=C7+C8+C14+C15

E=C1+C2
F=C5+C6
G=C7+C8
Ha=C3+C4
Hb=C12+C13
Hc=C14+C15
Hd=C3+C4+C5+C6
He=C5+C6+C12+C13
Hf=C1+C2+C5+C6+C12+C13
Hg=C7+C8+C14+C15

ICD ONLY
S1:1 OPEN
S1:2 OPEN
S1:3 OPEN

For all species, except, I
the J2 is replaced by
400" 30 ohm cable for
impedance matching.

Title	ZIF Interface
Calorimeter Test Jig			
Size	Number		Rev
C	3823-121-EC-330241		-
Date	10-29-96	Drawn by	Linda Bagby
Filename	F_ZIF2.SCH	Sheet	12 of 13

Title LED Display Calorimeter Test Jig
Size C	Number 3823-121-EC-330241		Rev -	
Date 10-10-96		Drawn by L. Bogby		
Filename F_DISP.SCH		Sheet 13	of 13	