A Novel Digitization Scheme with FPGA-based TDC for Beam Loss Monitors Operating at Cryogenic Temperature

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Abstract— Recycling integrators are common current-to-frequency converting circuits for measurements of low current such as that produced by Fermilab’s cryogenic ionization chambers. In typical digitization/readout schemes, a counter is utilized to accumulate the number of pulses generated by the recycling integrator to adequately digitize the total charge. In order to calculate current with reasonable resolution (e.g., 7-8 bits), hundreds of pulses must be accumulated which corresponds to a long sampling period, i.e., a very low sampling rate. In our new scheme, an FPGA-based Time-to-Digital Convertor (TDC) is utilized to measure the time intervals between the pulses output from the recycling integrator. Using this method, a sample point of the current can be made with good resolution (>10 bits) for each pulse. This effectively increases the sampling rates by hundreds of times for the same recycling integrator front-end electronics. This scheme provides a fast response to the beams lost and is potentially suitable for accelerator protection applications. Moreover, the method is also self-zero-suppressed, i.e., it produces more data when the beam loss is high while it produces significantly less data when the beam loss is low.

Index Terms— Cryogenic Loss Monitors, Dark Current, TDC, FPGA Firmware

I. INTRODUCTION

OSS monitors are typically one of the main diagnostic devices used in high beam power super-conducting RF accelerators for protecting the machines from beam induced damage and radiation damage; high gradient RF structures can produce field emission that results in so called “dark current”. The dark current related radiation that results can cause significant damage to accelerator components. Although the placements of loss monitors are critical, most facilities do not cover cold sections of the machine with loss monitors. To address these issues a Cryogenic Loss Monitor (CLM) ionization chamber capable of operation in the cold sections of a cryomodule has been developed and will be installed and tested at the Superconducting RF accelerator test facility currently under construction at Fermilab [1-3]. The monitor electronics have been optimized to be sensitive to DC losses and the signals from these devices will be used to study and quantify dark current losses in particular.

The ionization chamber current is usually measured with a recycling integrator current-to-frequency converter to achieve a required measurement capability for the low current and a wide dynamic range. The recycling integrator typically is digitized using a pulse counting scheme as shown in Fig. 1(a).

Fig.1. Typical recycling integrator pulse counting digitization scheme (a) the hardware, (b) digitizing values

In the pulse counting scheme, a counter is utilized to accumulate the number of pulses generated by the recycling integrator to digitize the total charge. In order to calculate current with reasonable resolution, a long period must be waited for each sample. For example, to achieve 7-bit resolution, the sampling period corresponds to 128 pulses when input current is at an upper limit. This scheme provides a total dosage of the radiation over long period but is not fast enough for accelerator beam protection.

An alternate approach is shown in Fig. 1(b); if the time interval (dt) between two pulses is measured using a time-to-digital converter (TDC) [4], then the average current is known given that a pulse represents a finite charge. As soon as the recycling integrator outputs the second pulse, a measurement point becomes available which is significantly faster than the traditional pulse counting scheme.

The oscilloscope traces of the background dark current
losses measured at the Fermilab A0-Photo-injector test accelerator as shown in Fig. 2. The advantages of a non-pulse counting scheme can be further explained with this data. The lower image shows the scope trace from a 40 µs pulse of the RF with no photo-electrons present in the machine. The upper trace is the measured dark current output from the CLM recycling integrator electronics and corresponds to about 400 nA (~200 mR).

When the CLM pulses are sent to a conventional counter, a total count (~ 9 pulses) is accumulated over the entire 40 µs RF gate range. This corresponds to a single sampling point with 3-4 bits resolution. However, with a TDC measuring time differences between leading edges of the pulses, 9 sampling points can be produced with > 10 bits resolution.

In this document, we will describe the implementation of such a TDC-based scheme in detail and present some bench top test results.

II. THE TDC-BASED DIGITIZATION SCHEME

In our new scheme shown in Fig. 3, the same recycling integrator output is sent to an FPGA in which a TDC is implemented. The TDC is based on a multi-sampling scheme in which the input transition is sampled with four different phases of the system clock. With a 250 MHz system clock and four-phase sampling, a 1-ns time measurement resolution can be achieved.

The actual FPGA we used is an Altera Cyclone III low-cost device (EP3C25F324C6N) located on an evaluation card. The recycling integrator is made by Bridgeport Instruments LLC. The electronics produces a 1.2 µs discharge pulse. The pulses are output in the form of a NIM logic level which is then converted into LVDS level. The LVDS signals are directly connected to the FPGA pin pairs that are assigned as differential inputs. The NIM to LVDS converter module and the module hosting the FPGA evaluation card are shown in Fig. 4.

When the input current is not too high, the recycling integrator pre-charges the capacitor with the fix width pulse in each cycle so that a known constant charge Q is stored in the capacitor. When the time difference dt between two leading edges of the output pulses is measured, the average current during the time interval is approximately: \( I = \frac{Q}{dt} \). When the input current is not too high and \( dt > 2 \mu s \), an 11-bit measurement resolution can be anticipated given that the time measurement resolution is 1 ns.

Unlike a counter, using a TDC to digitize the recycling integrator output produces a precise current measurement sample which is available for each output pulse. The TDC scheme simply digs out and utilizes useful information; the time differences between pulses that are not measured individually in the typical counter scheme.

This scheme provides a fast response to a rapid beam loss so that it is potentially suitable for the beam protection applications.

The TDC digitizes both leading edges and the widths of the recycling integrator pulses. The hit data are stored in a RAM on the evaluation card and then readout via a USB cable. An example of the data format is shown in Fig. 5.

Each long hexadecimal in the file represents a recorded
pulse. The file contains 8 columns for 8 channels. (Two columns are shown here.) Note that different columns may have different heights depending on number of pulses recorded in each channel. If there is no pulse recorded in a channel, the corresponding column remains empty.

Inside the FPGA, the time for the leading edge of the input pulse is first digitized with 40 bits, which are sufficient for a time range >1000 sec at 1 ns LSB resolution. Once the time for the trailing edge is digitized, the pulse width is calculated and 16 bits are kept which can represent a width up to 65 μs.

A hit is a 56-bit hexadecimal integer composed with the 40-bit leading edge time and the 16-bit pulse width. In actual operating condition, the pulse widths are usually 1-2 μs so 16 bits should be sufficient, while the time interval between two pulses can be very long and therefore, it is more convenient to represent the leading edge with an absolute time.

III. BENCH TOP TEST

The FPGA TDC described earlier samples input continuously and digitizes both leading edge and trailing edge transitions. When a leading edge of a pulse is detected, the time value is stored inside FPGA. After detecting the trailing edge, the time values of both the leading and falling edges are packed together and stored into a RAM on the board.

The data are readout via the USB port on the evaluation card to a PC and stored into a text files. Bench top test results are shown in Fig. 6.

In Fig. 6(a), the upper oscilloscope trace represents the input current with a scale of 100 nA/div and the lower trace is the output of the recycling integrator with a calibration of approximately 2 pC/pulse. If the pulses are accumulated in a counter, about 60 pulses are counted for the entire time frame indicating a total charge of 120 pC and the measurement resolution is approximately 6 bits. With the TDC, differences of time between pulses are measured that gives a current measurement sample per pulse as shown in Fig. 6(b). It can be seen that when the input current becomes large, it is detected almost immediately and corresponds with the time interval between two pulses being short.

IV. REDUCED ANALOG DESIGN CHALLENGES

With the TDC as the digitization device, challenges to the analog circuit design in the recycling integrator can be reduced. For example, when the input current is large, the discharge pulse in the integrator may become wider which causes more total charge to be stored in the capacitor.

The TDC can measure the transition times of both edges of the output pulse and the width of the pulse can be considered to be proportional to the total charge stored in each cycle. With tolerance of the pulse width, the dynamic range of the recycling integrator can be further extended.

V. SELF ZERO-SUPPRESSION

It is interesting to compare features of this combined recycling integrator and TDC scheme with the regular ADC scheme. In the regular ADC circuit, an amplifier circuit with sufficient gain and careful grounding is necessary to interface with the low current and noise sensitive signal source of the ionization chamber; whereas the recycling integrator is designed to interface directly with such low current sources. Regular ADCs provide data samples at a constant rate and fix resolution. This scheme, on the other hand, provides rapid response with relatively low measurement resolution when the input current is high, while it provides slower measurements for low current with higher resolution when the time interval between pulses is longer. This is a good fit for accelerator beam loss monitoring since both a rapid high beam loss protection and precise measurement of the dark current are needed.

Unlike a regular ADC device that produces the same amount of data no matter the magnitude of the input current, this scheme is self zero-suppressed, i.e., it produces more data when the beam loss (and therefore the input current) is high and produces significantly less data when there is no beam loss. This feature further simplifies design of the readout system and the data analysis software.

In our test hardware, a 1 MB memory is utilized to store recorded pulses from 8 channels. Each pulse, taking 16 Bytes, is stored as ASCII text for the convenience of post processing. Therefore, up to 8192 pulses can be stored for each test run.

This small amount of memory location would be filled very quickly in regular ADC system. With self zero-suppression in this scheme, test runs lasting hundreds of seconds have been achieved in our practical operations.
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REFERENCES


