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Effect of DC Voltage Pulses on Memristor Behavior

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Abstract

Current knowledge of memristor behavior is limited to a few physical models of which little comprehensive data collection has taken place. The purpose of this research is to collect data in search of exploitable memristor behavior by designing and implementing tests on a HP Labs Rev2 Memristor Test Board. The results are then graphed in their optimal format for conceptualizing behavioral patterns. This series of experiments has concluded the existence of an additional memristor state affecting the behavior of memristors when pulsed with positively polarized DC voltages. This effect has been observed across multiple memristors and data sets. The following pages outline the process that led to the hypothetical existence and eventual proof of this additional state of memristor behavior.

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Table of Contents

Table of Contents	5
Introduction.....	7
Materials and Methods.....	8
Test 1	8
Test 2.....	13
Test 3.....	15
Test 4.....	17
Summary	20

Chip mount with HP Labs 32x 32 crossbar chip inserted.

Components to control voltage pulse size and measure resulting current.

Figure 1: Picture of HP ReV2 Memristor Test Board

Introduction

Memristors - which have been theorized to be fourth fundamental circuit component alongside resistors, capacitors, and inductors – are devices whose resistive malleability is dependent upon the polarity and magnitude of an electric current passed through them. There are multiple different combinations of materials used to construction memristors. Those used for this research are comprised of three layers of material: tantalum oxide (a transition metal compound) pressed between two conductive plates - one pure tantalum and the other platinum. The oxygen atoms in the tantalum oxide cause the middle layer to be less conductive than the pure tantalum and platinum layers, thus giving the memristor its resistive property. When current is passed through the tantalum oxide, electron movement causes oxygen atoms to break off and move outwards in the material attaching to other Ta atoms. The vacancies left by displaced oxygen atoms in the path of the current increase the device's conductivity. Many aspects of this process are still unknown to the scientific community. One such aspect is the effect of previous resistive state on the change in resistance of the device when a controlled voltage is applied. It is widely hypothesized that the previous resistive state of a memristor and the size of the voltage pulse applied to the device are the only factors which determine the final resistive state. Other unknowns include: maximum voltage magnitude that will not destroy the devices functionality, range of resistive functionality and endurance/maximum number of voltage cycles of the device. HP Labs and Sandia National Laboratories have fabricated chips that contain thirty-two memristors in a crossbar orientation. These chips are capable of being mounted into a HP Labs board which can be programmed to isolate a specific memristor on the crossbar, pulse it with a given voltage polarity and magnitude and then measure its final resistance. The many unknowns involved with memristor study including inconsistencies in chip fabrication and the never before used test environment necessitate a progressive approach to experimental design. This report consists of the data and observations obtained from utilizing this new test environment to design and conduct various experiments into the effects of direct current voltage pulses on the resistive state of memristors.

Materials and Methods

The structure of the program utilized in conducting the following experiments was designed by Erik DeBenedictis and Fred Rothganger at Sandia National Laboratories. The basic functions of this program are as follows:

- 1) Isolate a single row and column in the 32 x 32 crossbar of memristors.
- 2) **Read** - apply a benign voltage, measure the current and determine the resistive state of a single device using the equation*

$$R = V/I$$

- 3) **Write** - apply a voltage to a single memristor of a given magnitude, polarity and duration.*

Two chips were used in the collection of the following data:

- 1) HP Labs 32x32 crossbar
- 2) Sandia National Laboratories 32x32 crossbar

Note: The first challenge in determining the effect of a constant write pulse on a given resistance is to be able to set a memristor to a given resistance. This was completed by writing a program which essentially “nudged” the resistor into place using .01 V increases or decreases to the write voltage until the resistance was within 20 Ohms of its target. This deviation was determined by calculating the standard deviation of 200 successive reads of the same memristor. This process was repeated for several different memristors. The device’s functional range of resistance, including internal resistance of the chip, is between 1500 Ohms and 20000 Ohms so a 20 Ohm deviation is reasonable. Though the process of nudging a memristor is time consuming it has proven to be effective without damaging the devices. **

** for the duration of this paper “read” and “write” will reference this context.*

*** for the duration of this paper “set function” will reference this context.*

Test 1

Objective: Compile a data set that can be used to visualize a single memristive device’s range of functionality.

Procedure: Set the memristor to a certain resistance utilizing the set function, write it with a given pulse magnitude and polarity and read and record the post-pulse resistance.

This experiment was first implemented on a narrow range of resistances and pulse sizes both of which increased as knowledge of the devices durability increased. The program was eventually automated to test all 32 memristors. The program first determined if the memristor was functional. Many memristors on the chip were either “frozen” in one resistance or broken – meaning that they had infinite resistance. If the memristor was determined to be functional then Test 1 would proceed on a voltage range of -6 V to +6 V – with a increment of .1V - and starting resistance of 2500 Ohms to 6000 Ohms – with an increment of 100 Ohms.

Test duration:

- Single memristor: 3 Hrs ~2500 data points
- Entire Crossbar (approx. 20 functional memristors): 60 Hrs ~50,000 data points

Results: Figures 2 & 3 were created using a single data set. Figures 4 & 5 were also created using a single data set. The “Post Pulse Resistance” graphs show pre-pulse or “set” resistance on the y-axis, the pulse height at which the memristor was written on the x-axis, and the post-pulse read resistance on the z-axis. The “Change in Resistance” graphs show the pre-pulse or “set” resistance on the y-axis, the pulse height at which the memristor was written on the x-axis and the change in resistance between pre-pulse resistance and post-pulse read resistance on the z-axis.

Figure 2: HP chip crossbar location (1,1)

Figure 3: HP chip crossbar location (1,1)

Figure 4: HP Chip crossbar location (8,8)

Figure 5: HP Chip crossbar location (8,8)

Figure 6: HP Chip crossbar location (4,4)

Figure 7: HP Chip crossbar location (4,4)

Discussion:

Figures 2 & 3: These graphs are indicative of a fully functional or healthy memristor. Of the 20 memristors tested on this chip 8 were considered to be in this category.

+2 V to -1.7V: This is a region of “no change” for all memristors tested.

-1.7V to -6V: In Figure 2 a smooth concave curvature can be seen beginning around -2 V and eventually flattening out asymptotically to some minimum value around -6 V. This correlates to the information in Figure 3 where a bowl shaped area can be seen beginning around -2 V. The smoothness of this curve indicates a consistency to the results of negatively polarized voltage pulses. However, the curve does not support the idea that pre-pulse resistance has an effect on post-pulse resistance since all negative voltage pulses of the same magnitude write to nearly identical resistances.

+2V to +6V: In this range memristors have an increasing post pulse resistance. There is a somewhat identifiable shape to this curve which has a saturation point similar to the negative pulse region. There is a lot of “noise” in this region which indicates inconsistency in post pulse resistances for positive voltage pulses of the same magnitude. Also, similar to the negative pulse region, post pulse resistance does not seem to be dependent on starting resistance.

Overall Shape: This is one of the few memristors whose minimum resistance can clearly be seen in the data. One interesting aspect of Figure 3 is that once a memristor has been set to its minimum resistance it does not increase in resistance when pulsed at a very high magnitude.

Figures 4 & 5: These graphs are indicative of a limited functionality memristor. Of the 20 memristors tested on this chip 12 were considered to be in this category.

- +2 to -1.7V: This is a region of “no change” for all memristors tested.
- 1.7V to -6V: In contrast to the smooth curve drop off seen in Figures 2 & 3, a cliff-like drop off is observed. The cliff region takes place over the voltage increment between -1.7V and -1.8V. After 1.8 V there is a smooth consistency to the post pulse resistance which is dependent upon the pre pulse resistance.
- +2V to +6V: In this range post pulse resistance is gradually increasing. There is considerably less noise than in Figures 2 & 3. Higher resistances are not as responsive to pulsing and are frequently skipped by the testing algorithm due to their inability to set within the 20 Ohm target range. Within the functional range of data, post pulse resistance is independent of pre pulse resistance.

Figures 6 & 7: These graphs were created by running the same test 3 times on a single memristor. The mean and standard deviation for the three sets of data were calculated and then processed in groups of 500 Ohms. This was done in order to see if the “noise” in the positive pulse region could be quantified in some way. The resulting graphs do show a more defined curvature in the positive pulse region with an asymptotic trail off at the peak implying a maximum resistance value for that memristor. Standard deviation peaks at + 5 V and then decreases possibly due to saturation of the device. The other jump in deviation at - 1.8 V can be attributed to the “cliff” effect in higher resistances.

Conclusions: It can be concluded from Test 1 that all functioning memristors have a similar pattern of response to varying sized voltage pulse. This pattern includes a uniform post pulse resistance independent of the starting resistance in response to negatively polarized voltage pulses. For positive voltage pulses the response is somewhat linear in that larger pulses tend to have a larger change in resistance. Although, due to the amount of noise seen in this region there is some indication that a hidden state is present. It is the goal of the following experiments to shed some light on this hidden state and find out what is causing such a large deviation in the change of resistance for positively polarized pulses of the same height.

Test 2

Objective: Collect data regarding the behavior of memristors dependent on previous write voltages and resistances.

Procedure: Set memristor 2500 Ohms, write it with a +3.5V pulse, read resistance, write again with a -2.5V pulse and read resistance. Set memristor to 5000 Ohms, write it with a -2.2V pulse, read resistance, write again with +4.5V pulse and read resistance. Set memristor to 2500 Ohms, write it with a +3.5V pulse, read resistance, write again with a +4.5V pulse and read resistance. Set memristor to 5000 Ohms, write it with a -2.2V

pulse, read resistance, write again with a -2.5V pulse and read resistance. Repeat 300 times.

Test Duration: 52 minutes.

Results: A random slice was taken from the beginning of the data set in order to help visualize the pulse size/post-pulse resistance relationship in a linear manner. The x-axis represents iterations of the pulse sequence. Post-pulse resistance is plotted on the y-axis. Pulse size is labeled at the point where that pulse took place with the resulting resistance change represented by the colored line following the pulse size label. “NaN” labels indicate when the memristor has been set to a given value (either 5000 Ohms or 2500 Ohms).

Figure 8: HP Chip crossbar location (4,4)

Pulse size/Position	Mean Post-Pulse R (Ohms)	Standard Deviation (Ohms)
-2.2V	2395	129.7
3.5V	3485	491.4
-2.5 following -2.2	2207	41.9
-2.5 following 3.5	2187	20.5
4.5V following -2.2	5737	978.8
4.5V following 3.5V	5747	1179

Figure 9: HP Chip crossbar location (4,4)

Discussion: Figure 8 helps to illuminate the process used to collect this data. However, due to the limited range of data it covers, one cannot determine behavioral patterns by solely examining this plot. Figure 9 represents the whole of the data collected during this experiment.

4.5V: It can be concluded from Figure 9 that due to the relative size of the standard deviation between positive pulses that follow negative pulses and positive pulses that follow positive pulses the difference between the two deviations does not appear to be significant. Also, post-pulse data reveals that on average positive pulses of the same size go to the same post-pulse resistance independent of pre-pulse resistance or previous voltage polarity.

-2.4V: Data for pulses of magnitude -2.5V is as expected from the results of Test 1. All negative pulses of the same magnitude accurately change to the same post-pulse resistance independent of pre-pulse resistance or previous pulse polarity.

Conclusion: Although somewhat inconclusive, due to the limited amount of data collected, this experiment encourages the idea that the change in resistance due to negatively polarized voltage pulses is independent of pre-pulse resistance and previous pulse magnitude and polarity. There is some data to indicate that positive voltage pulses behave in a similar manner, but with a much larger error factor. It is unknown if the memristor was being saturated (meaning pushed to its highest and lowest possible resistance settings) during this experiment which would result in a false observation of behaviors. Additionally, it has been proposed that the set function is affecting the state behavior of the device. Future tests should be designed to reduce the use of the set function.

Test 3

Objective: Determine effects of memristor program history by training memristor to jump between 4 different resistance settings and examining the resultant voltage pulse magnitude.

Procedure: Using 3 different target resistances (R2, R3 and R4) and one variable resistance (R1,k) write a program that adjusts the write pulse magnitude between each

resistance depending on how far off target the post-pulse read is. Once all four resistances are set within a 20 Ohm deviation exit the program and print the final voltage values used (V2 and V3 - V1 is inconsequential to the results because $R_{1,k}$ varies). Increment the variable resistance by 50 Ohms (starting at 2500 Ohms and ending at 3500 Ohms) and re-run test. $R_{1,k}$ is set using the standard set function.

Figure 10: Test 3 Diagram

Test Duration: Average - 12 minutes.

Results: Figures 11 & 12: This test ran several times without any indication of a distinct pattern. These graphs are indicative of the data gathered and do not imply linearity to the results.

Figure 11: HP chip crossbar location (18,18)

Figure 12: HP chip crossbar location (18,18)

Discussion: Though an attempt has been made to minimize the use and of the set function by separating it from the collected pulse data by two previous pulses there is still the possibility that it is causing an unknown effect on the data collected. It is also possible that inconsistencies in change in resistance due to positively polarized voltage pulses caused the test to exit the loop in odd places (i.e. if pulse happened to land on correct resistance too early in the loop then voltages would not have settled to optimum magnitude or if pulse took too long to land on correct resistance then other voltages would have wandered from their optimum magnitude).

Conclusion: Figures 11 & 12 show that there is no identifiable trend to the data gathered from this test. Although prior evidence pointed to a history effect due to previous resistance, this particular test design does not indicate similar results. It has been concluded, however, that, by using software programming, a memristor can be trained to move between a series of resistance settings by single voltage pulses with a reasonable degree of accuracy. Further investigation into the hidden state will require a data set that includes all possible sequences of write voltages and read resistances. It is essential that the set function not be included in order to eliminate any question of its effect on hidden state observations.

Test 4

Objective: Write a program to test every possible write history within the functional range of the memristor that does not utilize the set function. The format of the test and the data collected will have the potential for analyzing all history effects.

Procedure: Use the rand() function to randomly generate write pulses between -4.3V and +7V. A resistance range of 2000 Ohms to 10000 Ohms is maintained by a function that filters pulse magnitude to 0 V as pre-pulse resistances near the limits (See Figure 13.). Print resulting data in a two column matrix [pre-pulse resistance, pulse size].

Test Duration: 10 million data points in 22 hours.

Results: This procedure allows for the generation of many more data points in much less time than Test 1 by a factor of ~100. Also, it does not utilize the set resistance function, which may have an unknown effect on the data.

Figure 14 is from a smaller set of data collected from the Sandia National Laboratories chip crossbar location (4,4).

Figure 15 is of the large data set collected from the HP Chip crossbar location (4,4).

Figure 13: Possible voltage Range

Figure 14: SNL chip crossbar location (4,4)

Figure 15: HP chip crossbar location (4,4)

Discussion:

Figure 14: This data set was collected from a chip fabricated by Sandia National Laboratories. The negative pulse region is similar to what has been previously observed in Test 1. However, the positive pulse region shows 4 distinctive “layers” indicating a possible wear out of the memristor’s range of functionality. The SNL chip seems to have much less noise in the positive pulse region.

Figure 15: This graph is indicative of the kind of data yielded from this test. The original two column matrix was compiled into five columns: first pulse height, first resulting resistance, second pulse height, second resulting resistance and change in resistance. The new matrix was then narrowed down to *first resulting resistances* on a range of 3000 Ohms to 3500 Ohms pulsed with a *second pulse height* within the range of +3.0V to +3.3V. The resulting data is graphed by *first pulse height* versus the *change in resistance*. Figure 14 reveals that when the *first pulse height* is -1.7V or lower (purple box) change in resistance from the second pulse (+3.0V - +3.3V) is widely responsive, when the *first pulse height* was between -1.7V and +2.7V (green box) the *change in resistance* from the second pulse was less responsive, and finally when the *first pulse height* was above 3V (red box) there was nearly zero response to the *change in resistance* from the second pulse.

Conclusion:

Figure 14: Though the SNL chip shows a much more rapid wear out effect, similar behavior has been observed in the HP chip as well. Observation of the HP chip shows a 25% loss of responsiveness between the first and second groups of 5 million writes during a single test run. The cause of this wear out effect is yet to be determined, but most likely has to do with the physical aspects of the device. A permanent state of lower resistance means higher conductivity possibly resulting from the repeated heating of the Tantalum Oxide filament.

Figure 15: These results are a very promising step forward in the search for the cause of noise in positively polarized voltage pulses. The graph indicates that positive pulses that follow another positive pulse of significant size have less effect on the change in resistance than positive pulses that follow a negative pulse of significant size. This answers the question as to why the desired result from Test 3, which was designed to test the resistance history, was not achieved. Perhaps history of voltage is the significant factor instead. Further analysis of the data is necessary to determine the validity of this effect.

Summary

The purpose of these experiments was to find exploitable memristor behaviors with a focus on discovering if pre pulse resistance is the only variable necessary in determining the post pulse resistance of a write pulse of a certain polarity and magnitude. Test 1 revealed the basic structure of memristor response which seems to be consistent for all

functional memristors. The existence of noise in the positively polarized pulse region indicates the possible existence of a hidden state in memristor behavior. Tests 2 & 3 were designed to exploit the hidden state, but fell short of reliable data due to inconclusive results and the suspected interference of the set function. The relative failure of Tests 2 & 3 led to the development of Test 4, which relies on a randomizer function to generate voltage pulses and does not utilize the set function. The random pulse test is a breakthrough in memristor experimentation. It allows the user to quickly and accurately measure a device's range of functionality thus making Tests 2 & 3 obsolete. Test 4 is capable of collecting enough data points in reasonably short window that all imaginable sequences of pulses and resistances are represented without the use of the set function. The resulting data from this test has revealed the existence of a previously unknown state in memristor behavior that is dependent upon not only the most recent voltage pulse polarity and magnitude but also the history of previous voltage pulse's polarities and magnitudes. Further analysis of these trends is necessary to fully develop a model of the unknown state. Future experiments will compile data on all possible combinations of positive and negative pulse sequences and analyze them for trends in their post pulse resistance and change in resistance.

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