D0 ENGINEERING NOTE

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D0 SILICON UPGRADE

THERMAL ANALYSIS OF THE D0 DOUBLE SIDED
LADDERS

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A side view of the double sided ladder is shown in Figure 1. There are two types of double sided ladder; 6 chip and 9 chip. The 6 chip ladder has three SVX II chips mounted directly opposite the cooling channel and 3 chips mounted at the ladder end. The 9 chip ladder has 4 SVX II chips directly opposite the cooling channel and 5 chips at the ladder end. The power density is highest in the 6 chip ladder. All plots and calculations in this Engineering Note pertain to the 6 chip ladder with the understanding that the 9 chip temperature profile is somewhat improved over the 6 chip due to the reduced power density in the row of chips opposite the cooling channel.

441 The two dimensional finite difference technique used for these calculations is described in ~~DOEN, XXXX~~ and will not be described here. The assumed thermal conductivity of beryllium is 190 W/m-K, and that of silicon is 149 W/m-K. The SVX II power dissipation is assumed 0.400 W. There is no cable or hybrid component power dissipation in this set of simulations. The epoxy in the glue joints consists of 2 mils thickness of thermally conductive epoxy with 0.8 W/m-K conductivity and 1 mil thickness of 0.22 W/m-K unfilled epoxy. The assumed gas temperature outboard of the bulkhead is 15°C with a convection coefficient of 5 W/m²-K. The cooling channel temperature is 0°C.

The intention of this series of simulations is to determine the optimum thickness to achieve an acceptable silicon temperature during operation of the ladder. Once the operating temperature profile is known, the temperatures within the beryllium substrates are used as input for an ANSYS* calculation of the bow of the ladder during operation.

A series of calculations have been performed over the last several months in order to consider the effect of thickness, chip power, gas temperature, etc.. on the temperature profile. Only the final plots are shown here in runs 660, 661, and 662. In these three plots the conditions are identical except for the beryllium substrate thickness which is 0.3/0.3, 0.4/0.4, and 0.5/0.3 bottom/top beryllium thicknesses, which are in dimensions of mm.

* ANSYS calculations performed by Ang Lee of the FNAL Analysis group.

Fig 1

3-FRONT

Figure 2

Figure 3

Figure 4

The temperature profile which results from substrate thicknesses of 0.3 mm each (figure 2) has a maximum silicon temperature of 13.5°C. The maximum temperature allowable, although not completely specified for these conditions, was determined to be nearer to 10°C. The ladder end can be cooled accordingly by increasing the substrate thickness. There is also a limit to the amount of mass which can be used to build the ladders. A total thickness of 0.8 mm beryllium was determined to be used for the cooling of the double sided ladders.

Assuming the ladders are to be constructed at 22°C, cooldown to the operating temperature will result in bowing in the ladder due to the variation in temperature between the upper and lower substrates. The amount of bowing has been calculated using ANSYS (see footnote above), for the conditions in Figures 3 and 4 (Figure 2, with upper and lower substrates of thickness 0.3 mm each, was not considered for thermal bow calculations).

The moduli for beryllium and silicon are 303.4 and 131 GPa, respectively. The expansion coefficients for beryllium and silicon are 11.4 and 2.6 ppm/°C, respectively.

Shown in Figure 5 is the result of the bowing calculations for Run 661, with 0.4 mm thick substrates on top and bottom. The maximum deflection occurs on the ladder end with a total displacement of 0.555E-5 m, or 5.55 microns (variable DMX on the ANSYS output file).

Run 662 uses 0.5 mm thick substrates in the bottom and 0.3 mm in the top. The maximum deflection occurs for at the ladder end. The absolute deflection in a different direction than for Run 661, which can be seen in the magnified deflection plot from ANSYS, and was 0.755E-5 m, or 7.55 microns. The theoretical difference in deflection between these two ladder designs is immeasurably small so was not considered a factor in determining the final substrate thickness in the double sided ladders.

ANSYS 5.1)
JUL 15 1996
11:47:56
PLOT NO. 2
DISPLACEMENT
STEP=1
SUB =1
TIME=1
RSYS=0
DMX =0.555E-05
SEPC=12.298

DSCA=291.876
ZV =1
DIST=0.017235
XF =0.016732
YF =0.818E-03
CENTROID HIDDEN

Figure 5 Run 661. DEFLECTION PLOT

ANSYS 5.1)
JUL 15 1996
14:10:40
PLOT NO. 2
DISPLACEMENT
STEP=1
SUB =1
TIME=1
RSYS=0
DMX =0.755E-05
SEPC=12.705

DSCA=214.519
ZV =1
DIST=0.017374
XF =0.016606
YF =-0.124E-03
CENTROID HIDDEN

Figure 6 Run 662, DEFLECTION PLOT

svx_D0, case No__ run 662, thermal deflection, Tr=22C