The Chicagoland Observatory Underground for Particle Physics Cosmic Ray Veto System

M. Crisler, J. Hall, E Ramberg and T. Kiper
Fermi National Accelerator Laboratory Batavia, Illinois*

***Abstract*–A photomultiplier (PMT) readout system has been designed for use by the cosmic ray veto systems of two warm liquid bubble chambers built at Fermilab by the Chicagoland Observatory Underground for Particle Physics (COUPP) collaboration. The systems are designed to minimize the infrastructure necessary for installation. Up to five PMTs can be daisy-chained on a single data link using standard Category 5 network cable. The cables is also serve distribute to low voltage power. High voltage is generated locally on each PMT base. Analog and digital signal processing is also performed locally. The PMT base and system controller design and performance measurements are presented.**

I. Introduction

The COUPP[1] dark-matter search collaboration has constructed two bubble chambers at Fermilab. These bubble chambers are surrounded with liquid filled tanks which form part of their cosmic ray veto systems. One bubble chamber with an active volume of 2 liters uses a tank filled with scintillator oil and the other with an active volume of 60 liters a water tank. Light generated by transiting cosmic rays is detected by an array of 19 five inch photomultiplier tubes (PMTs) mounted on the oil tank and 12 eight inch PMTs mounted on the water tank. Cameras running at 100 frames per second are used to detect bubble formation within the chambers and supply a trigger to the data acquisition system (DAQ) which in turn triggers the PMT systems. These systems must operate at a low threshold and, given the bubble formation and detection timing, store about 100 milliseconds of data. To achieve this in a mechanically simple, inexpensive and compact way, we are providing the analog and digital functions required along with a high voltage power supply all mounted directly on each PMT base.

The analog processing section includes a charge integrator for use by the ADC which has a range of 12 bits with a least count of 25 femto-Coulombs (fC) and a sampling rate of 40 Msps and an anode discriminator for use by the on-board TDC. The digital section includes a small FPGA which is used to implement a variety of control functions and a 1.6 ns per bin TDC, a 32 Mbyte RAM, a microcontroller and a serial data and control link. The high voltage supply is a low noise resonant mode Cockroft-Walton type whose interference level is a fraction of an ADC count. Up to five bases can be daisy-chained on one data link. The base consumes approximately 1.4 watts.

A controller module housed in a 2" high 19" rack mount box is used for timing, synchronization, control and readout of up to four data links. The controller delivers power to the bases over the links and has outputs for driving an LED flasher system. The data path from the controller to the DAQ is 100 Megabit Ethernet.

II. Motivation

A cosmic ray veto is commonly used in low background searches to aid the rejection of background events. Typically scintillator either solid or liquid is used. PMTs are the still the sensor of choice for these systems because of their large sensitive are. What is unusual in the case of COUPP is the time scale over which PMT signals must be stored pending a trigger decision from the cameras observing the active volume of the bubble chambers up to several 10s of milliseconds. A conventional PMT system assembled from standard components requires an in-time trigger to record the PMT signals. The long look-back requirement presents the opportunity to design a simple to use, minimal infrastructure system which would have general applicability to a variety of PMT based systems.

III. Architecture

The system consists of two parts: a controller and a base. The controller is the interface between the bases and Ethernet, supplies power, timing reference and triggers to the bases over standard category 5 cables.

The bases contain a supply to deliver the high voltage required by the PMT, an analog section for integrating the anode charge and discrimination the time of arrival of the signal, an ADC, a large data buffer, a microcontroller for control and status functions, an FPGA for the TDC and interfacing the various digital sections, and a synchronous data link for communication to the controller. Twenty-four volts from the cable is connected to a series of secondary power converters for generating several voltages required. A key advantage of providing all the functions on the base is the reduction of the cable plant. A typical PMT system would require an ADC cable, a TDC cable and a high voltage cable for each tube. With this system, 15 patch cables connecting 19 PMTs into strings and four cables connecting the strings to the controller are all that are needed for the two liter chamber.

A. *Cable Signal Assignment*

The cables are standard category 5e. The voltage levels are LVDM, with FM encoding running at 25Mhz. Four cables operating at 25Mhz exceed the bandwidth available with a 100Mbit Ethernet link. In practice the Ethernet link achieves

Manuscript received November 12, 2010.
Operated by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the United States Department of Energy.

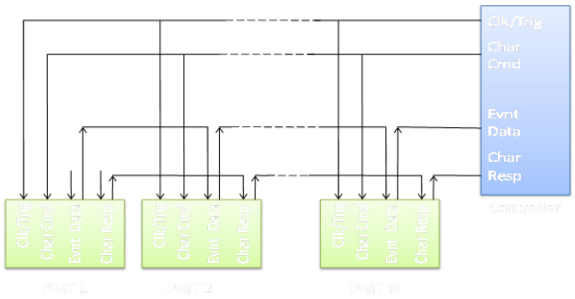

Fig. 1. Cable signal assignments.

about four Mbytes/sec transfer rate. Of the four pairs in the cables, two are bussed; two are daisy-chained. The bussed pairs are used for commands from the controller; the daisy chained pairs are the responses from the PMTs. With this scheme, there is no need for any drivers to change direction.

The use of FM makes it simple to phase lock the PMT system clocks to that of the controller. Since FM has constant activity on a pair, the first module in the chain can sense that it is at the end opposite the controller if it sees no activity on its input port. Addresses can be automatically assigned based on a PMTs position in the chain, so no address switches are needed. Once a geographic address is assigned, any logical address can be assigned afterwards. One bussed pair is used as the clock frequency reference and for synchronous messages such as triggers and timing initialization. One daisy chained pair is used for event data which is sent in binary format. The second bussed pair is used for control commands. Since control bandwidth is not large, ascii bytes are used to make the data readable with a terminal emulator. The second daisy-chained pair returns status information, also in ascii form.

B. *Controller*

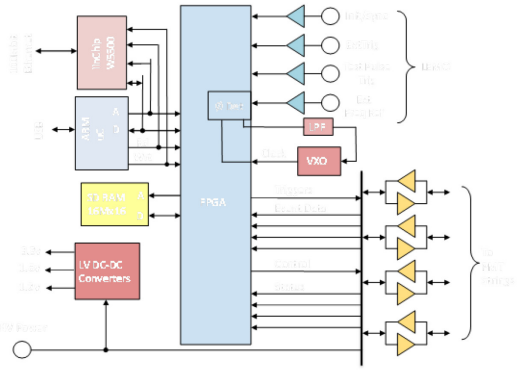

Fig. 2. Controller block diagram.

The controller is housed in a 2 inch high rack mount box. Mounted in the same box is a 50W 24 volt power supply, which is enough to power the controller and 20 PMTs. The links use standard power over Ethernet transformers for the power distribution. Included on the controller card are four channels of LED flasher outputs, which are AC coupled TTL pulsed outputs offset by a variable DC voltage. Small "postage stamp" cards at the far end of the flasher cables are fitted with a simple transistor switch which discharges a capacitor biased with this DC voltage across an LED. There is also a DDS frequency synthesizer chip configured as a numerically controlled divider within the VXO phase lock loop which allows the controller to phase lock to an arbitrary external reference frequency. Finally, there is an input compatible with a Fermilab built GPS receiver card which can be used as a reference for the VXO if absolute timing is desired.

The controller extracts event data from the PMTs upon receipt of an external trigger and builds a single block of data with a global header and presents this block to a Labview program running on the DAQ host. Status data is gathered periodically and pooled into single a block in the controller, simplifying the access to this information by the DAQ host.

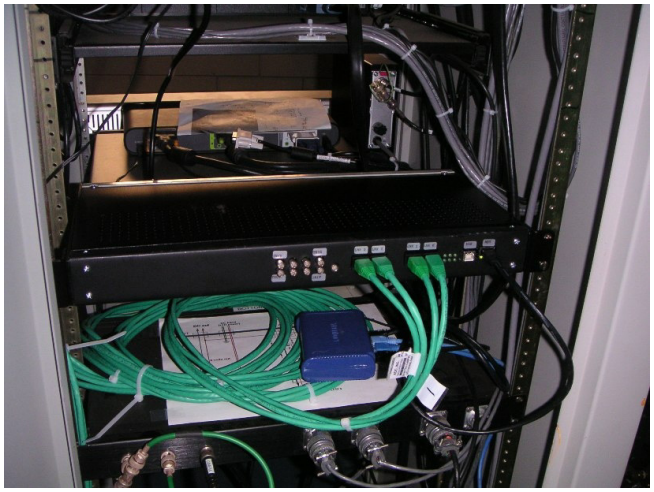

Fig. 3. Photograph of the controller installed for four liter test run at Fermilab. The green cables are the PMT links, the black is the Ethernet cable. The LEMO inputs are visible to the left of the PMT links.

C. *PMT Base*

Each base is equipped with a resonant Cockroft-Walton voltage multiplier, an anode charge integrator, a discriminator for timing information, a 40Msps 12 bit ADC with 25fC per count sensitivity, a DRAM buffer memory, a 1.6ns per bin TDC a, microcontroller for status and control, and serial links for communication. The buffering of the digital data allows for both pre and post trigger data readout.

Having the charge integrator right at the anode of the PMT affords a degree of insensitivity to interference from the high voltage supply[2]. Careful arrangement of the multiplier components is still necessary, but the bases have a fraction of an ADC count of HV power supply interference.

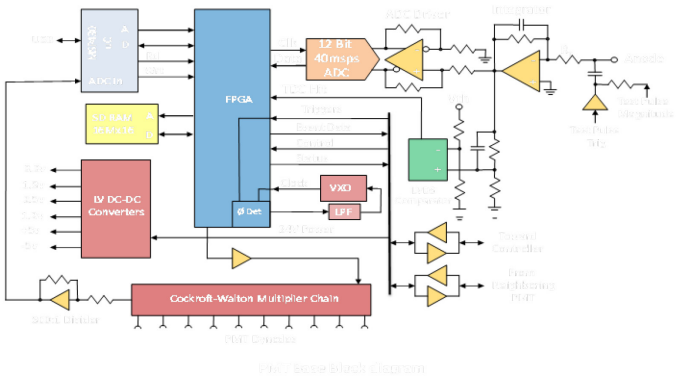

Fig. 4. Block Diagram of the PMT base

1) *Anode signal processing*

The since the PMTs are large (5 inch and 8 inch), the bases are positive high voltage, so the anode signal is AC coupled to the integrator input. Having the charge integrator adjacent to the anode means that there are no input impedance restrictions on the integrator as it is being driven by nearly an ideal current source. The negative input signal is inverted by the integrator. This positive integrator signal is differentiated and sent to a discriminator. By using the integrator output, a single supply comparator can be used, and a wide range of pulse widths, wider or narrower than the original PMT pulse that can be implemented by choosing the appropriate R-C network. A decay time constant (300ns) was chosen to allow the ADC to deliver multiple samples of the waveform and at the same time have a low probability of pile-up. In principle overlapping pulses can be resolved using the TDC information, but is not implemented here because the rates (KHz in the worst case) are so low.

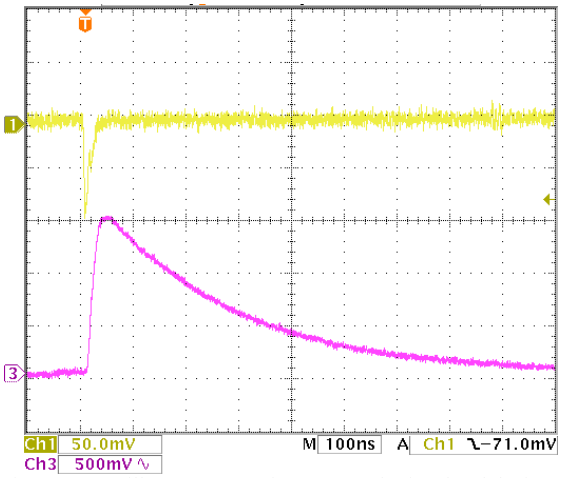

Fig. 5. An oscilloscope trace of a PMT anode signal and the integrator output.

A test pulse injector is included. A DAC channel on the microcontroller is used to set the magnitude and a pulse pattern memory is included in the FPGA logic. The pattern memory can be loaded with a list of times. When a counter clocked at 80MHz matches the time of a particular list entry, a test pulse is issued. The span if the counter is about 30 seconds and the table has 256 entries.

2) *Data formatting*

The discriminator output is fed to the FPGA which has a 1.6ns per bin TDC implemented in its logic. The minimum binning for this FPGA is 1.2ns, but 1.6ns conveniently subdivides one ADC sample interval by 16. TDC hits are used to zero-suppress the ADC data. For each hit, a programmable number of pre-hit and post-hit samples are written into the data buffer. Each event consists of a leading word count, the TDC time followed by the ADC data.

3) *Buffering Scheme*

In the COUPP case, the PMT system is externally triggered. The desired data is a list of hits that occurred from a specified interval before the trigger up to a specified interval after the trigger. To do this, three time counters are used. On receipt of a synchronous initialization message (INIT) one is set to negative pre-store value and the other to a (presumably) positive post-store value and the third, the counter used to from the upper order bits of the TDC word, is set to zero. Also in response to INIT, the event begin pointer is set to the beginning of the DRAM. During running, the value of the pre-store time counter is compared to the TDC data field of the oldest event in the buffer. When the counter equals the TDC value, the event read pointer is incremented to the next oldest event in the buffer and so on. This way the oldest relevant event is always ready to be read out. Upon receipt of a trigger events are copied from the DRAM to a single event buffer in the FPGA until the TDC value of a given event equals or exceeds that of the post-store counter. The reason for the second buffer is the desire to send data to the controller with a leading word count. This count isn't known until all the relevant hit data have been collected. When an event has been copied to the staging buffer, the on card microcontroller is interrupted, status information is appended and a total word count calculated. At this point the PMT microcontroller waits for a data request from the controller. When a readout request message with the correct address is received, the microcontroller starts a DMA controller implemented in the FPGA and data is transmitted over the link to the controller.

There is nothing in the hardware that precludes a self-triggered system, which might be desirable in other applications.

4) *High Voltage supply*

The resonant mode Cockroft-Walton topology offers advantages of high efficiency and low noise. The power consumption of the high voltage supply is less than 80mW. The operating frequency is around 400 kHz which allows the use of small magnetic components and filter section capacitors. The leakage inductance associated with separated transformer windings is not a problem for this topology, so it is straight forward to make a transformer that can isolate the

PMT voltage, a desirable feature for a positive base. By isolating the high voltage at the transformer, the match between an N stage multiplier chain output current capacity (1/N) and a N stage PMT dynode chain current consumption ($1/N^{\sim 4}$) is as it would be for a negative base. The control variable is frequency, in this case generated by a digitally controlled oscillator implemented in the FPGA. The supply is operated above resonance. Lowering the frequency increases the output voltage, raising the frequency lowers the voltage. One problem with this is that care must be taken not to go below resonance, which results in a positive feedback condition A resistive voltage divider provides the voltage feedback to an ADC input on the microcontroller. A PID servo controller updating at one kHz is implemented in the microcontroller. The frequency output of the FPGA is fed to a bridge driver which delivers a 11V pk-pk square wave voltage to the transformer primary circuit. A series inductor (L in figure 6) forms a resonant tank with the capacitance of the reversed biased diodes in the multiplier chain reflected back through the transformer[2].

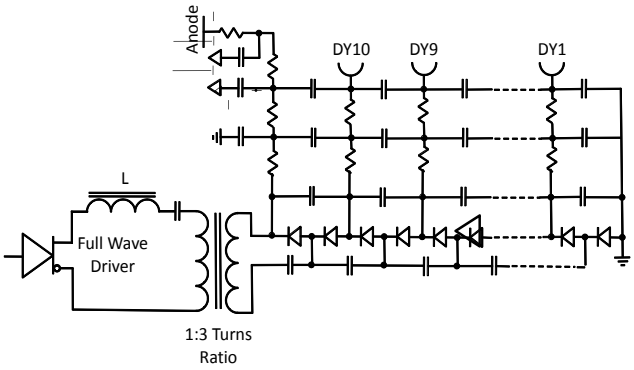

Fig. 6. The resonant Cockroft-Walton multiplier.

The Q of this resonance results in a quasi-sinusoidal primary current which in turn delivers a quasi-sinusoidal secondary voltage. The Q of the tank also gives a large voltage ratio across the transformer using a relatively small turns ratio. Typically the secondary voltage is 100V pk-pk with an 11V drive and a 1:3 turns ratio.

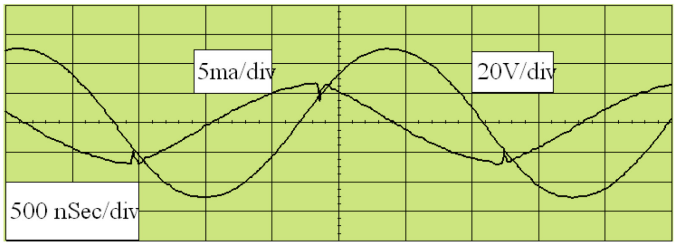

Fig. 7. Trace taken from a negative base of transformer primary current and secondary voltage which is very nearly sinusoidal. A positive base has the secondary voltage offset by the full multiplier chain voltage.

In spite of the smooth high voltage waveforms, care must be taken with the filtering and layout to keep power supply interference to a minimum. The reverse biased capacitance of all the diodes in the multiplier chain is effectively in parallel. As a result, there is a capacitive divider between the diodes and any dynode filter capacitors. The diodes have a reverse capacitance of order one pF and the filter capacitors are 10nF. Twenty-fours diodes in parallel in a divider with 10nF results in a ripple of about 300mV at the extreme ends of the chain where the capacitors are directly connect to ground. In the middle of the chain, the ripple is greater since the capacitance to ground is divided by the number of capacitors in series. This ripple must be filtered before connecting with the dynodes, so there are two stages of filtering per dynode. A particular feature of positive bases is that the anode must also be biased. This critical connection calls for a three stage filter. Unfortunately, the filter capacitors associated with the anode must withstand the full high voltage and are thus rather large. Since positive high voltage is usually associated with large tubes, this is not a problem. With the COUPP bases the ADC pedestal width is measured to be 1.3 bins RMS with the high voltage supply turned off and 1.7 bins RMS with the supply operating at nominal voltage, but with no PMT attached.

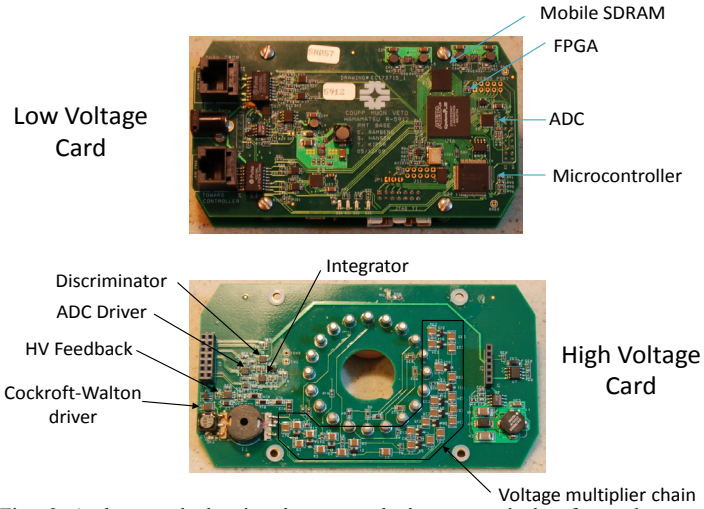

Fig. 8. A photograph showing the two cards that are stacked to form a base for an eight inch PMT.

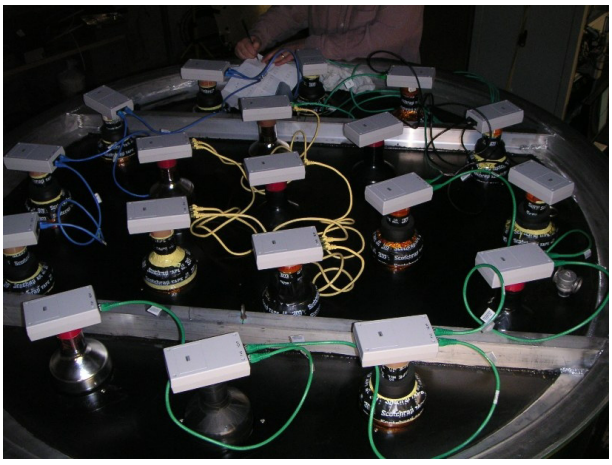

Fig. 9. A photograph of the top of the veto tank surrounding the four kg chamber at Fermilab. Nineteen five inch phototubes are read out over four cable chains. The green cables in the foreground can be seen daisy-chaining from base to base.

IV. Test Results

The tanks were set up on the surface and fitted with a scintillator telescopes. The measured efficiency of the vetos

was about 98%, the expected value given the geometry of the setup. Tests with the LED flasher indicate the TDCs are synchronized at the level of 100ns which is consistent with the internal reflection times of the tanks.

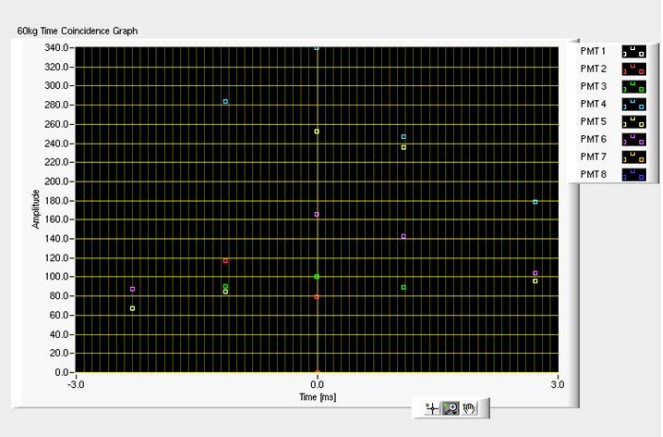

Fig. 10. A screen capture of the Labview display during the surface test of the 60 liter chamber showing a single scintillator trigger. The vertical axis is ADC counts, the horizontal time scale is milliseconds.

V. Operation

The 2 liter chamber was operated 150m below grade in the NuMi experimental at Fermilab hall for a few months. The veto system functioned properly with no failures. The chamber is as of this writing beginning a data collection run at the Sudbury Neutrino Observatory (SNO) in Ontario Canada. The site is sufficiently deep such that for a sensitive mass of 4kg, there is no need for a veto.

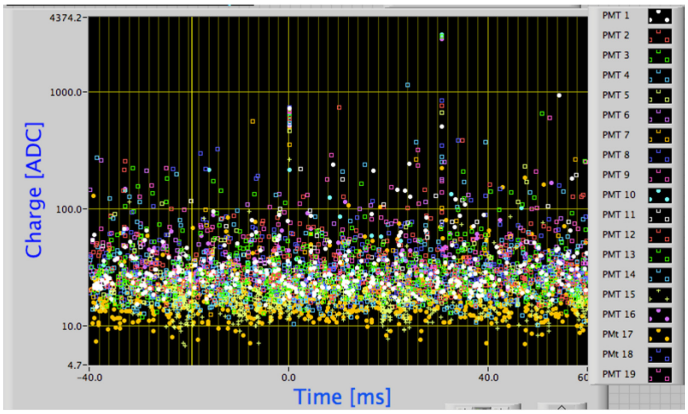

Fig. 11. A screen capture of the Labview display during the NuMi hall test of the two liter chamber. This shows all the camera triggers over a three day period. The peak visible at time zero is due to muons generated by the NuMi neutrino beam. The cluster of dots at time 31ms and 3000 ADC counts comes from the LED flasher system which is fired for each trigger to verify time synchronization.

The 60 liter chamber is now in a test run in the NuMi hall and its veto is functioning normally. The expectation is that it too will be moved to SNO, and since it is larger, will be fitted with its veto even at the deep site.

References

[1] Spin Dependent WIMP Limits from a Bubble Chamber. Science 319: 933-936, 2008.

[2] Henry W. Ott, *Noise Reduction Techniques in Electronics Systems,* 2nd ed., John Wiley & Sons 1988, pp. 79-95.

[3] C. Rivetta, G.W. Foster, S. Hansen, "HV Resonant Converter for Photomultipliers Tube Bases", Nuclear Science Symposium conference record, 1992, vol.1, pp. 438-440.