ELECTRIC POWER INFRASTRUCTURE RELIABILITY AND SECURITY (EPIRS)

RESEARCH AND DEVELOPMENT INITIATIVE

U.S. DEPARTMENT OF ENERGY AWARD NO.:
DE-FC26-07NT43221

FINAL SCIENTIFIC / TECHNICAL REPORT

JUNE 2010

(REV.1: 23 AUGUST 2010)

Florida State University
Center for Advanced Power Systems

DISCLAIMER

FORWARD

This is the final scientific/technical report for the Electric Power Infrastructure Reliability and Security (EPIRS) R&D Initiative sponsored by the U.S. Department of Energy, Office of Electricity Delivery and Energy Reliability, under award number DE-FC26-07NT43221. This report covers results from the FSU-led, multi-institution effort conducted over the period 10/1/2007 to 3/31/2010.

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EXECUTIVE SUMMARY

Introduction and Background

Power systems have become increasingly complex and face unprecedented challenges posed by population growth, climate change, national security issues, foreign energy dependence and an aging power infrastructure. Increased demand combined with increased economic and environmental constraints is forcing state, regional and national power grids to expand supply without the large safety and stability margins in generation and transmission capacity that have been the rule in the past. Deregulation, distributed generation, natural and man-made catastrophes and other causes serve to further challenge and complicate management of the electric power grid.

To meet the challenges of the 21st century while also maintaining system reliability, the electric power grid must effectively integrate new and advanced technologies both in the actual equipment for energy conversion, transfer and use, and in the command, control, and communication systems by which effective and efficient operation of the system is orchestrated – in essence, the "smart grid". This evolution calls for advances in development, integration, analysis, and deployment approaches that ultimately seek to take into account, every step of the way, the dynamic behavior of the system, capturing critical effects due to interdependencies and interaction. This approach is necessary to better mitigate the risk of blackouts and other disruptions and to improve the flexibility and capacity of the grid.

Building on prior Navy and Department of Energy investments in infrastructure and resources for electric power systems research, testing, modeling, and simulation at the Florida State University (FSU) Center for Advanced Power Systems (CAPS), this project has continued an initiative aimed at assuring reliable and secure grid operation through a more complete understanding and characterization of some of the key technologies that will be important in a modern electric system, while also fulfilling an education and outreach mission to provide future energy workforce talent and support the electric system stakeholder community.[1]

Building upon and extending portions of that research effort, this project has been focused in the following areas:

1. Building high-fidelity integrated power and controls hardware-in-the-loop research and development testbed capabilities (Figure 1).
2. Distributed Energy Resources Integration
   - Testing Requirements and Methods for Fault Current Limiters

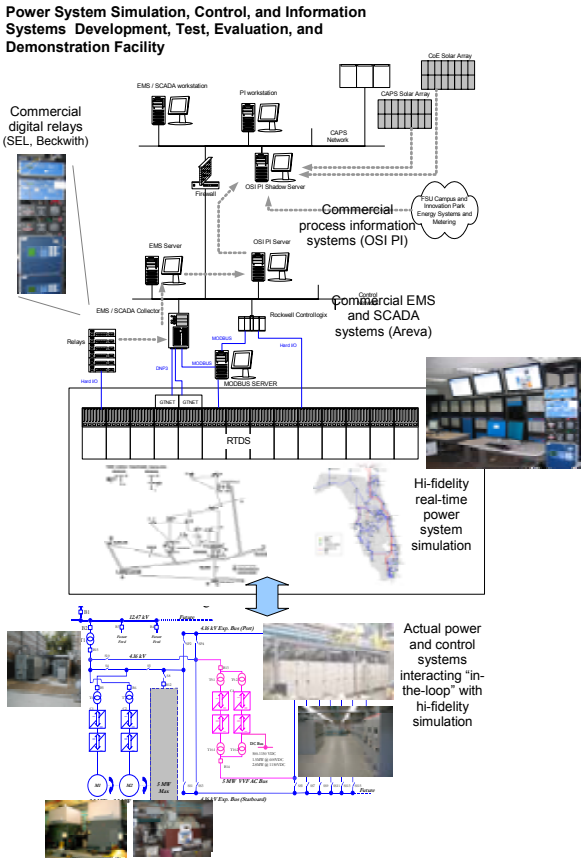

Figure 1. Integrated 5MW Testbed, HIL Simulation, Control and Information Systems Laboratory / Testbed at FSU CAPS

[1] This project is based in part on a previous effort under Department of Energy award No. DE-FC02-05CH11292.

- Contributions to the Development of IEEE 1547.7
- Analysis of a STATCOM Application for Wind Resource Integration
- Development of a Grid-Interactive Inverter with Energy Storage Elements
- Simulation-Assisted Advancement of Microgrid Understanding and Applications

3. Availability of High-Fidelity Dynamic Simulation Tools for Grid Disturbance Investigations
4. HTS Material Characterization
    - AC Loss Studies on High Temperature Superconductors
    - Local Identification of Current-Limiting Mechanisms in Coated Conductors
5. Cryogenic Dielectric Research
6. Workshops, education, and outreach

Results and Accomplishments

Highlights

This project resulted in valuable advances in simulation-assisted approaches to understanding grid-technology integration, grid-interactive converter development and control, understanding of AC losses and coated conductor properties in high-temperature superconductors, and dielectric material properties at cryogenic temperatures. In the process, important enhancements to laboratory simulation, testing, and characterization capabilities were completed.

The effort resulted in at least twelve (12) published papers or articles and a number of related presentations. During the project period, FSU CAPS has also been engaged with and contributing to the electric power stakeholder community through various national and international organizations, standards efforts, and working groups. Five (6) engineering students from the FAMU-FSU College of Engineering have been involved in the project, including five (5) graduate students and one (1) undergraduate student who subsequently graduated and was accepted into graduate school at in the FAMU-FSU College of Engineering, Electrical and Computer Engineering (ECE) Department.

Research Facility Capability Enhancements

The 14-rack Real Time Digital Simulator (RTDS®) system at CAPS has been upgraded to keep up with advances in simulation capabilities being released by RTDS® and to improve system performance. This includes faster back-plane transfer rates, more real-time electrical node capacity per rack, and more very low time step (<2 μS) gigahertz processor cards (GPC).

In addition, control and information system capabilities have been extended and expanded, particularly with commercial control and real-time information system platforms commonly used in the electric utility industry, including the Areva e-terra® EMS and SCADA systems and OSISoft's PI® real-time process information system. A software license agreement (SLA) with Areva was extended, and a new SLA with OSISoft was put in place.

Finally, lab capabilities in support of advancing the application of high temperature superconductors continue to be enhanced, building upon a foundation made possible with prior DOE funding. This includes continuing to improve the flexibility and accuracy of AC loss measurements for straight conductors and coils, and continuing to develop high-voltage dielectric testing capabilities for wide-ranging materials and over wide-ranging temperatures, down well into the cryogenic region.

Distributed Energy Resource Integration

A substantial part of the project effort has been in this area. CAPS simulation and testing facilities were utilized in research efforts to conduct controller hardware-in-the-loop (CHIL) simulation and testing for the controller for a distribution class static VAR compensator (dSVC) for use in the Distribution Circuit of the Future, the Avanti circuit at Southern California Edison (SCE). The dSVC was developed by American Superconductor (AMSC) who also cooperated in the simulation effort. CAPS also conducted testing of a new advanced Li-ion Iron Phosphate ($LiFePO_4$) battery based distributed energy storage system (DESS) developed by Greensmith Energy Management Systems and targeted for use in Progress Energy Florida's system as part of a collaborative project with the University of South Florida (USF).

CAPS also completed some analysis, started under prior DOE funding, on use of a STATCOM for volt/VAR control in wind farm applications.

A great deal of progress has been made in the development of a grid-interactive converter system with integrated energy storage elements to efficiently integrate small distributed power generation systems. The new converter and control concept developed includes a novel reactive power allocation strategy to improve rangeability, permits single-stage energy conversion to improve system efficiency, enhances system stability through improved control, has a lower cost due to tranformerless design, and features smooth and fast transition from grid-connected mode to stand-alone mode with minimal voltage fluctuation at the load.

In support of the broader stakeholder community and advancement of standards for distributed energy resource (DER) integration, CAPS personnel have been participating in and contributing to the IEEE-1547.7 working group to help develop the methodologies for conducting system impact studies to enable more effective and widespread DER integration.

Grid Reliability and Security

Inspired initially by a significant system disturbance that occurred in South Florida in Feb. 2008, CAPS has conceived and advanced an initiative with the Florida Reliability Coordinating Council (FRCC) and its member utilities to form a working relationship and framework from which to supplement event and system planning related simulation and analysis capabilities residing within the electric utilities and regional reliability entities with unique university-based resources and capabilities, including the advanced simulation and test facilities at CAPS. Through other funded projects, CAPS plans to continue the effort initialized under this project by further exploring and developing an appropriate and effective framework for aligning industry and university capabilities and needs.

In addition to the benefits in supporting system reliability and advancing effective technology integration and grid modernization, this closer cooperation is likely to contribute to better developing the energy workforce pipeline for new talent and improved continuing education for the existing energy workforce.

High Temperature Superconductivity (HTS)

Significant progress has been made on enhancing existing AC loss measurement techniques for coils and on carrying out a number of these measurements on coils constructed with 2G conductor. Capability has been established to make measurements on coils up to 14 cm in diameter and up to to 20 cm in length, with up to 150 A transport current.

In addition, an effort at the FSU Applied Superconductivity Center (ASC), associated with the nearby National High Magnetic Field Laboratory (NHMFL), has been focused on enhancing the current-carrying capacity of coated conductors, in particular, studying the current-limiting effects of grain boundaries. Electric fields and supercurrent paths were analyzed with the aid of a low temperature laser scanning microscope (LTLSM), magneto optical imaging (MOI) and a high-resolution scanning electon microscope (HRSEM). Measurements, images, and analysis are provided for YBCO coated conductors grown on RABiTS substrates.

Cryogenic Dielectric Research and Test Facility

Unique cryogenic dielectric testing facilities and procedures continue to be developed and improved. Electrical breakdown and tanδ (dielectric loss) measurements were completed with the specialized dielectric test laboratory and equipment, at both room temperature and liquid nitrogen temperature (77 K), for ThermaVolt, G10, Polymethyl Methacrylate (PMMA), and PMMA treated with the nano-material, Barium Titanate (BTA). Detailed test results are available and published or soon to be published.

Workshops, Conferences, and Outreach

CAPS has engaged in several workshop and outreach activities during the project period, including two open house events to engage the general public in electric power technology, research and education, a "townhall meeting" style event to engage state policymakers in energy and economics, and a workshop on smart grid, with strong participation and engagement from Florida utilities.

CAPS has also been participating in electric power stakeholder community organizations and initiatives including IEEE 1547, Cigre A3, the IEEE Task Force on Fault Current Limiters (FCL's), the Gridwise Alliance, the North American Synchrophasor Initiative (NASPI), and others. CAPS members are heaviliy involved in the IEEE 1547.7 working group on impact studies for distributed resources integration, and, the IEEE Task Force on FCL's was newly formed during this project effort, with a CAPS member as the lead.

Further Reading

In addition to the detail provided in this report, the reader is referred to publications arising from this work, as listed in the publications section at the end of this report.

RESEARCH FACILITY CAPABILITY ENHANCEMENTS

Real Time Digital Simulator

A 14-rack Real Time Digital Simulator (RTDS®) is an integral part of the CAPS high power hardware-in-the-loop (HIL) test facility (Figure 2). This system can perform high-fidelity electromagnetic transient program (EMTP) type simulations of complex electrical systems, including 3-phase systems, electrical machines and controls, and power electronics equipment, at time-steps down to 50 μS for an entire model and <2μS for portions of a model, with extensive input/output (I/O) capacity, enabling the insertion of real hardware interacting with the simulation.

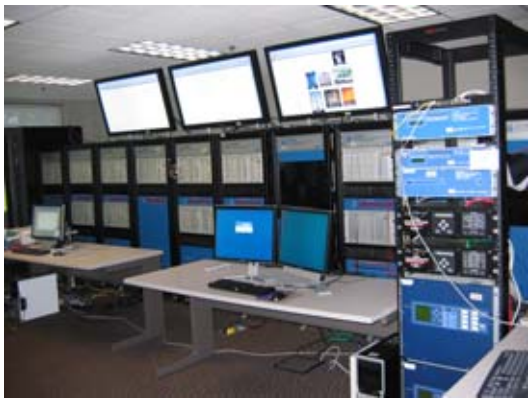

Figure 2. RTDS System at CAPS

This system is used extensively in the CAPS research program and supports some of the research conducted under this award. As part of this award, the system was upgraded with faster backplanes, expanded I/O capacity, and processor upgrades, including expanding the number of RISC-based Gigahertz Processor Cards (GPC) that allow the very small time step (<2μS) real-time simulation. Backplane upgrades increased the number of electrical nodes that can be simulated and externally accessed per rack from 54 to 66, and reduced bus transfer rates from 125 nS to 60 nS.

Information and Control Systems

To facilitate research, development, test and evaluation activities in the areas of power systems control, real-time information handling, and power systems analysis, CAPS had partnered with major suppliers of these systems, in particular Areva T&D and OSISoft, to integrate commercial control and real-time information systems into the CAPS test facility. When connected to the RTDS®, these systems function as though they are controlling or collecting data from a real physical power system, due to the real-time capability of the RTDS. These systems are also useful for education and training activities, and for collecting data from actual systems of interest in CAPS research programs.

Areva EMS and SCADA System

The software license agreement (SLA) was updated and renewed under this project for the Areva e-terra® electric power grid Energy Management System (EMS), Simulator, and Supervisory Control and Data Acquisition (SCADA) system in the CAPS simulator laboratory (Figure 3). Software components were installed or upgraded, and on-site training was conducted by Areva T&D. Per the SLA, the system is licensed for 341,800 points, 3000 transmission buses, 3000 simulator buses, and 90 generators.

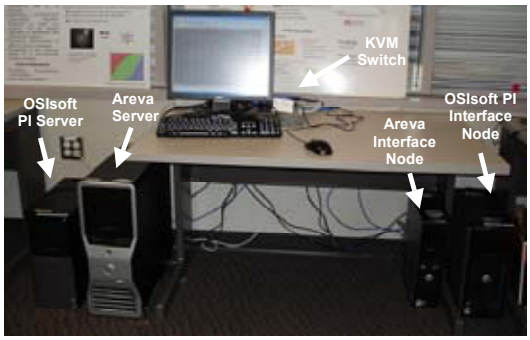

Figure 3. OSI PI and Areva e-terra EMS systems in the CAPS simulator lab.

OSI PI Real-time Information System

As part of this project, an SLA was executed and system installation and commissioning completed for an OSI PI® real-time process information system (Figure 3), licensed for 20,000 tags and 15 desk-top clients. The PI system is designed for the optimized collection, storage, and retrieval of large amounts of time-stamped data. PI is used by many commercial electric utilities. Properly handling large quantities of real time information becomes very important as the evolution of smart grid substantially increases the amount of data available from the power system, as well as the reliance upon this data for critical operating, control, maintenance, and

decision-support functions. Hundreds of software interfaces are available from OSISoft to bring data into PI. At CAPS, the following interfaces have been licensed and installed:

- MODBUS Ethernet (TCP)
- DNP 3.0
- Campbell Scientific Loggernet®
- C37.118 (synchrophasor / PMU communications)
- Areva e-terra® Habitat
- OPC
- HTML
- Universal File and Stream Loader (UFL)

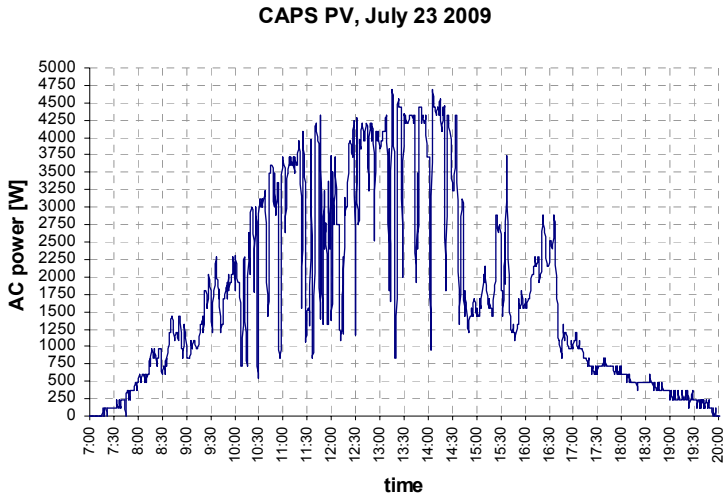

Figure 4. Summertime AC output from 6 kW system

PI interface and configuration work was completed to collect data from two (2) 6kW solar photovoltaic (PV) systems, one located on the CAPS facility and the other at the nearby FAMU-FSU College of Engineering. These systems provide one-minute data to the CAPS PI system via the Campbell Scientific Loggernet® interface. An example of the data collected is shown in Figure 4, illustrating solar PV AC power output variation on a July summer day. This will support future research in grid integration of intermittent renewable resources.

Control and Information Network

A process control and information network has been implemented in the CAPS simulator laboratory. The control network is separated from the CAPS business network for security through physical network topology and router configuration. The Areva SCADA interface and OSI PI interface nodes are connected to the control network and the CAPS business network using dual network interface cards (NICs). Also connected to the control network is a Schweitzer Engineering Laboratories (SEL) 2032 protection relay communication module, a Rockwell ControlLogix® PLC, and several RTDS interfaces, including RTDS GTNET interface modules supporting DNP 3.0 or IEC61850, and, Rabbit microcontrollers and RTDS digital I/O configured to provide MODBUS TCP communications support. The general network architecture related to the control and information and real-time simulation testbed is illustrated in Figure 5.

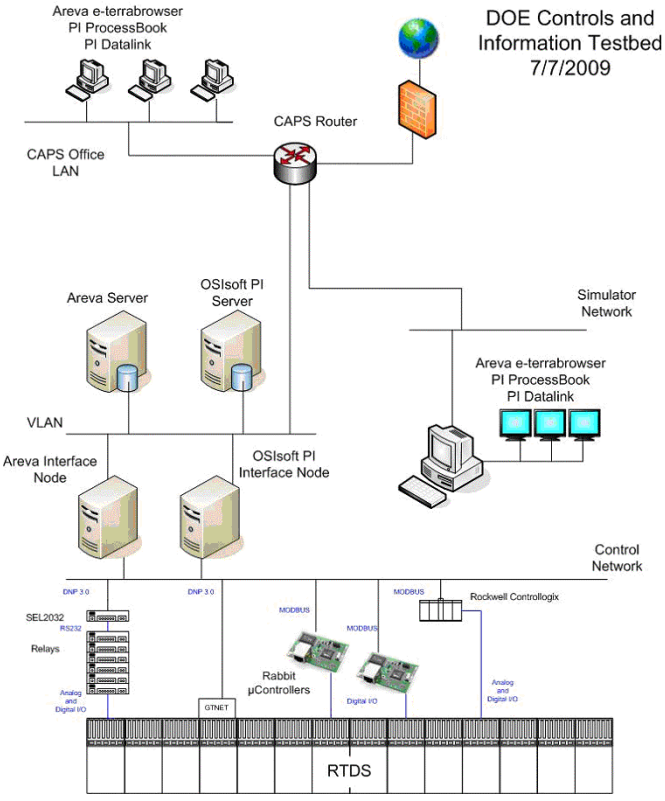

Figure 5. Control and information network architecture

WORKSHOPS, CONFERENCES, AND OUTREACH

CAPS Electric Power Research Laboratory Facilities Open House

On 2/23/2009 and 2/27/2010, CAPS hosted public open-house events, in conjunction with the National High Magnetic Field Laboratory, to provide the general public an opportunity to tour the CAPS facility and learn about electric power and the programs and facilities at CAPS through demonstrations, hands-on activities, and exhibits for all ages.

Figure 6. '76 Porsche 912 converted to all-electric, on display at CAPS Open House

Figure 7. Middle and high school student science fair competition at CAPS Open House

In addition to exhibits involving the permanent CAPS research facilities, the 2010 Open House included electric vehicle exhibits, including a Porsche 912 (Figure 6) and a City of Tallahassee Electric Utility all-electric truck, and, a student science fair competition, where middle and high school students recently competing in Leon County school system science fair competition entered energy-related projects in the CAPS competition, displayed and discussed their projects during the CAPS Open House, and were recognized with awards selected by a panel of distinguished judges (Figure 7). The Open House events also featured exhibits from companies with energy-related services or technologies, including displays of large solar PV plants operating at Florida Power and Light and Colorado State University (Figure 8).

Figure 8. Solar PV plant operating displays at CAPS Open House

Town Hall Meeting on Energy

On 3/4/2009, a town hall meeting and capital energy forum was held at the Doubletree Hotel in Tallahassee, Florida. The purpose of the event was to bring together government, the academic and research community, and industry for a public discussion on "Energy and Economic Development – Making the Connection". The event was attended by approximately 130 people. Organizers included FSU CAPS, the State of Florida Governor's Energy Office, the Tallahassee-Leon County Economic Development Council (EDC), the American Society of Mechanical Engineers (ASME), and the Institute of Electrical and Electronics Engineers (IEEE). Distinguished panelists and speakers for the event included Tallahassee Mayor John Marks, Dr. John Adams, President and CEO of Enterprise Florida, Representative Paige Kreegal, Chair of the Energy and Utilities Policy Committee, Commissioner Nathan Skop, Florida PSC, Dr. Tim Anderson, Director of the Florida Energy Systems Consortium, Mr. Jack Sullivan, President of the Florida Research Consortium, Mr. Don Markley, Vice President of Southeast Renewable Fuels, and Mr. Ben Stuart, Economic Development Lead for the Governor's Energy Office. The event was moderated by Ms. Lynda Keever, Group Publisher for Florida Trend Magazine, and, taped for broadcast on public television by WFSU-TV. Cost sharing for the event was provided by the ASME Tallahassee Section and the ASME Washington Office, the IEEE Tallahassee Section and IEEE Washington Office, and several industry sponsors.

Figure 9. Panelists at the 2009 Town Hall Meeting on Energy, Tallahassee, FL.

Florida Smart Grid Workshop

The first *Florida Smart Grid Workshop* was held Monday, 9/28/09, at the Embassy Suites, University of South Florida campus in Tampa, FL (Figure 10), preceding the Florida Energy and Climate Commission (FECC) meeting on 9/29 and the Florida Energy Systems Consortium (FESC) 1st Annual Summit on 9/29-30. The purpose of this workshop was to begin a dialogue, process, and stakeholder community engagement towards producing a Smart Grid Roadmap for Florida.

The workshop was attended by close to 100 people representing electric utilities, universities and other stakeholder groups, and was organized by FSU CAPS and USF's Power Center for Utility Explorations (PCUE). Katherine Hamilton, President of the Gridwise Alliance, provided the keynote talk. Panelists included representatives involved in smart grid initiatives from the North American Electric Reliability Corp. (NERC), Florida Power and Light (FPL), Jacksonville Electric Authority (JEA), Tampa Electric Co., Gulf Power Corp., Draper Labs, MetroCore, LLC., and Kitson & Partners/Family Lands Remembered. Sponsors sharing cost included the Gridwise Alliance, Areva T&D and FESC.

Figure 10. Florida Smart Grid Workshop, Tampa, FL, 9/28/2009.

In conjunction with the Florida Smart Grid Workshop, a memorandum of understanding, initially between FSU CAPS and USF PCUE, was executed and announced, establishing the *Intelligent Energy Grid Alliance*, as a basis for collaboration in electric power systems and smart grid.

Stakeholder Community Engagement

This project has helped support the involvement, engagement and contributions of CAPS personnel in various electric power stakeholder organizations and initiatives to advance electric power technology and grid modernization efforts. CAPS has been involved in and contributing to the following:

- CIGRE A3.23 Working Group, "Application and feasibility of fault current limiters in power systems".[2]
- IEEE Task force on Fault Current Limiter Testing.[2]
- IEEE 1547.7 Standard, "Draft Guide to Conducting Distribution Impact Studies for Distributed Resource Interconnection".[2]
- North American Synchrophasor Initiative (NASPI) Work Group
    - Data & Network Management Task Team (D&NMTT)
    - Research Initiatives Task Team (RITT)
- The Gridwise Alliance
    - Implementation Work Group
    - Education and Workforce Work Group
    - Legislative and Policy Work Group
- American Society of Mechanical Engineers (ASME) National Energy Committee

In addition, S. Dale and R. Meeker produced an article for EnergyBiz Magazine on possible justification and concepts for an overarching electric transmission grid in North America.

[2] see discussion under Distributed Energy Resources Integration section of this report

RESEARCH ACTIVITIES AND RESULTS

Distributed Energy Resource Integration

Testing Requirements and Methods for Fault Current Limiters

(M. Steurer)

Introduction

Continuously increasing demand for power transmission and distribution combined with new regulatory constraints require utilities to face long term decisions regarding their strategies for managing increasing fault current levels in their systems. With the prospect of some of the fault current limiter (FCL) technologies currently under development for the medium and high voltage range it is expected that these devices may soon be applied in utility systems. While the development of FCL's move forward through many projects around the world, such as several DOE co-funded projects pursuing superconducting FCL's (SCFCL's), very little is still understood about how these devices should be tested before utilities accept them in their systems. The difficulty lays in the fact that a FCL dynamically changes its impedance shortly after the onset of a fault. Hence, the device is different from a line reactor. However, many FCL technologies, especially SCFCL's do not interrupt the current. Hence, it is different form a circuit breaker. Therefore, none of the existing standards for testing power equipment (C37.06 for circuit breakers, C57.12.00 for transformers, C57.16 for line reactors) apply directly.

Cryogenic Dielectric Issues

An additional complication is that the insulation medium for most SCFCL's is liquid nitrogen (LN2). However, during the current limiting phase large energy is dissipated in to the LN2 environment, which almost certainly generates N2 gas bubbles. Except for a few spot checks of specific cryogenic system designs, and some basic work surveying the applicability of existing standards, no good understanding about the relevant testing requirements exists for SCFCL's. In particular, such requirements should take the physics of the dominant breakdown mechanism into account and not only pick the most applicable requirements from one of the existing standards.

Modeling and Simulation Issues

Dynamic modeling and simulation of FCL's for system level studies .is important to understand system-device interactions under different system conditions. In addition to the good understanding of the transient behavior of FCL's under various fault conditions other conditions may be all of particular interest: transformer inrush, large motor inrush, follow current behavior for protection coordination, transient recovery voltage of adjacent circuit breakers (as they may be influenced by the impedance and capacitance of the FCL), and insulation coordination studies (high frequency travelling wave phenomena). However, there is no clear understanding of the required model fidelity for the various studies. Since it is not always feasible to utilize the highest fidelity physics based model it is very desirable to research the degree of fidelity required and recommend the findings tot the FCL and utility community.

Testing of FCL's

(co-sponsored by Office of Naval Research, ONR)

With respect to testing FCL devices during development as well as for type acceptance before field deployment a fundamental difficulty from the inherently large energy dissipation occurring during the fault current limitation phase exists. In fact, today no testing facility exists anywhere capable of testing a 138 kV/1200 A SCFCL at full fault current. It is not clear is synthetic testing such as the methods applied to test circuit breakers may be applied for FCL testing.

The newly emerging method of power hardware in the loop (PHIL) simulation may be a very useful tool for FCL testing. In principle, it allows for testing the FCL in a realistic, but virtual power system environment, which is simulated in real time on a specialized computer. It is expected that such capability, even if applied only at a downscaled device (i.e. reduced voltage) can become a critical asset for FCL development in the future. CAPS has recently commissioned a 6.25 MVA/4.16 kV rated PHIL facility utilizing a power electronics converter system as the high power amplifier for signals simulated by the state of the art real-time power system simulator RTDS. This facility provided an excellent opportunity to investigate how the method of PHIL simulation can be applied for FCL development and acceptance testing.

For example, some of the SCFCL programs currently under way utilize copper shunt coils to accept the major part of the fault current after the superconductor quenches. Currently, the only way to test the interaction between the superconductor and the shunt coil is to subject the entire assembly to the full fault current which typically ranges up to 80 kA peak or more. Investigations like this are particularly important for understanding the recovery under load behavior of SCFCL's. Unfortunately, this requires of the test site a very large current capability. However, only few and rather expensive sites are available with such capability. Therefore, it would be very desirable to be able to conduct experimental testing of the superconductor elements without the need to supply these large currents. With PHIL simulations it becomes possible to model the dynamic behavior of shunt (i.e. increase of shunt resistance with energy intake) in the simulated environment. Hence, the PHIL method potentially allows the researchers to subject the superconducting element to the same electrical environment as it exhibits in a complete assembly. While the PHIL may not replace the need for a full-scale test of entire FCL devices at very high power it may become a very valuable tool for the development of SCFCLs.

For the first time, a 5 MW, variable voltage source (VVS) converter at CAPS was utilized to conduct a power hardware-in-the-loop (PHIL) experiment with a non-liner apparatus. In this case we used a superconducting fault current limiter (FCL) element provided by a visiting scientist from the Karlsruhe Research Center (Karlsruhe, Germany) to investigate the feasibility of PHIL for such applications. Figure 11 illustrates this concept. The current as simulated by the virtual system on the RTDS was driven through the FCL element by the VVS. In this case we used a series connected resistor (not shown in Figure 11) to achieve the current source behavior of the CAPS VVS. In return, the voltage across the FCL element was fed back into the simulated environment in order to complete the PHIL structure. The advantage of this method is that parameter and topology changes in the virtual test circuit can be implemented very quickly on the RTDS. This allows evaluation of the superconducting FCL element under a wide range of system conditions. Of particular interest to the ongoing superconducting FCL projects will be the ability to investigate recovery under load for different shunts (Z_{shunt} in Figure 11).

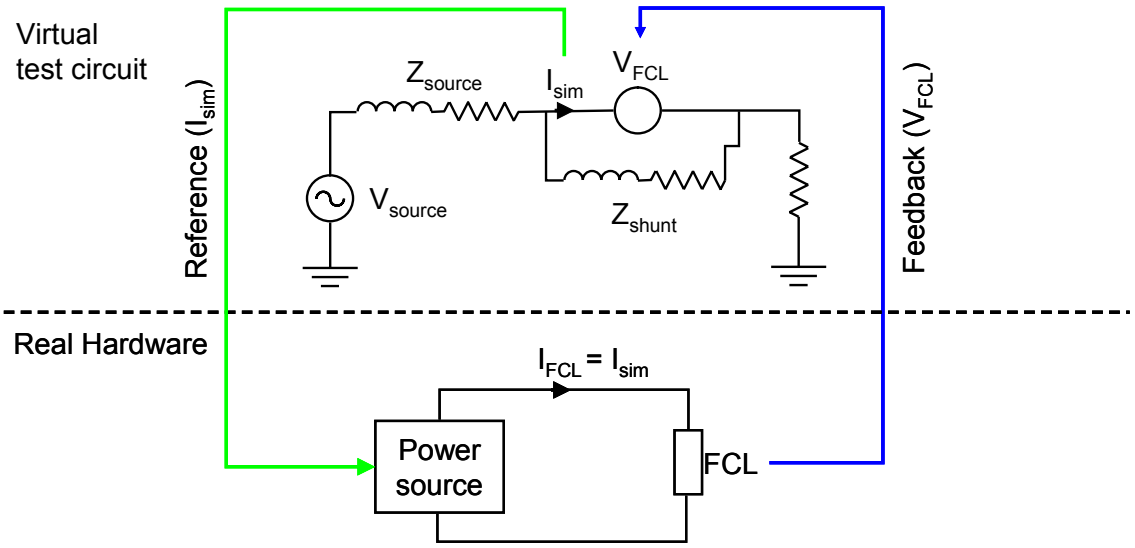

Figure 11. PHIL setup of experiments with superconducting FCL element

The experiments were successful since the simulated current waveform could be reproduced by the VVS with a good accuracy as shown in Figure 12. However, under certain system conditions we encountered stability problems, which will be investigated further in the future.

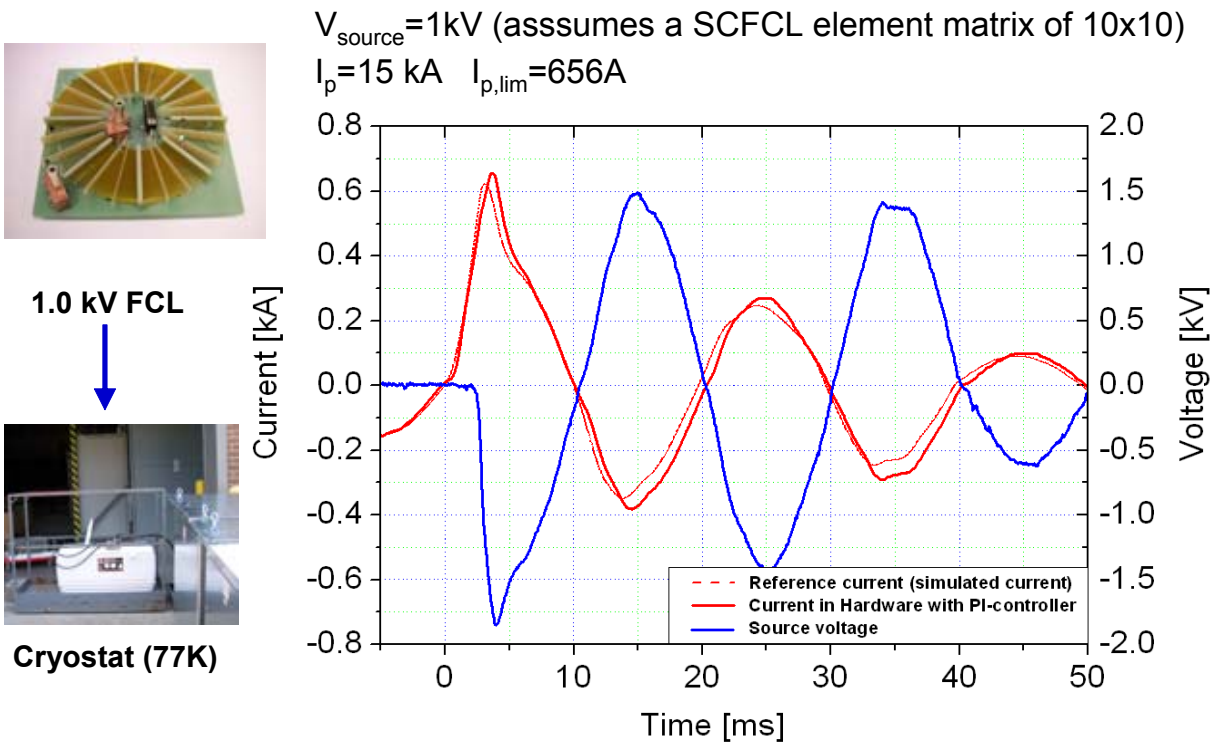

Figure 12. Results from PHIL experiment with superconducting FCL element

Outreach and Stakeholder Community Support

A panel session was organized for the IEEE OPES General Meeting held in Pittsburgh, July 20-24 2008.

Substantial input (including a gap analysis) was provided to production of the report titled "An Assessment of Fault Current Limiter Testing Requirements" to the DOE under contract to the Oak Ridge National Laboratory. The report was published March 2009, with M. Steurer as a co-author.

M. Steurer attended the kick-off meeting of the new CIGRE WG A3.23 on September 3-4 2008 in Erlangen, Germany, where he presented a summary of the FCL related activities at FSU. (The CIGRE Working Group A3.23 holds two meetings per year - spring and autumn.)

Heino Schmitt, the convener of this WG, explained the scope of the CIGRE Working Group A3.23 as it has been defined by the CIGRE Study Committee A3:

This WG builds upon the previous work of WG A3.10 and WG A3.16 with regard to the application of fault current limiters from a technical point of view and will draw to a close A3's investigations into FCL's. The working group makes use of the results of the previous working groups and will investigate and summarize the following topics:

- location of FCL installation
- different types of FCL (conventional and novel) and their limiting behaviour and drawbacks
- experience from former and new pilot projects in order to give a realistic picture
- feasibility of the application of conventional and novel FCL technologies to HV (e.g. technical and economic possibilities, extrapolation from MV to HV?)
- acceptance issues and how to overcome them
- customer system requirements with respect to fault level, insulation coordination, power quality, stability, etc.
- interactions with protection and other control and power devices
- potential economical savings (examples from utility experiences….)

The testing of fault current limiters was not within the scope of the existing Working Group. It was established that the subject would be treated by the formation of other Working Groups more focused on FCL testing (e.g. IEEE, CIGRE (Joint CIGRE Working Group A3/C4/D1)).

By drafting the outline of the report the group distributed the responsibilities for various chapters to different WG members. M. Steurer accepted responsibility for the chapter on "System Analysis and Tools"

M. Steurer and F. Lambert (NEETRAC) developed a scope for a new IEEE Task Force (TF) on Fault Current Limiter (FCL) Testing. The TF is sponsored by IEEE Switchgear ADSCOM and was approved to hold a first meeting in January 2009 during the IEEE joint technical committee meeting in Atlanta, GA.

The goal of the TF is to develop a guide for testing novel FCL technologies

Scope:

- Identify FCL testing requirements from a utility point of view
- Identify specific testing needs regarding the different FCL technologies (e.g. superconducting vs. power electronics)
- Identify applicability of existing power equipment testing standards
- Recommend additional tests and testing procedures as needed

- Identify gaps in availability of testing capabilities and recommend power requirements for upgrading

Approach:

- Study and review novel fault current limiter (FCL) technologies for medium and high voltage systems.
- Map testing requirements against the needs by different FCL technologies
- Map testing requirements against existing power equipment testing standards
- Map testing requirements against available laboratory capabilities
- Coordinate with other technical committees, groups, societies and associations as required.

The first meeting of the new IEEE Task Force (TF) on Fault Current Limiter (FCL) Testing, sponsored by IEEE Switchgear ADSCOM, was held on January 15 2009 during the IEEE joint technical committee meeting in Atlanta, GA. The second meeting of the new IEEE Task Force (TF) on Fault Current Limiter (FCL) Testing, sponsored by IEEE Switchgear Committee ADSCOM, was held on May 6 2009 during the IEEE Switchgear Committee meetings in Asheville, NC. The third meeting of the IEEE Task Force (TF) on Fault Current Limiter (FCL) Testing, sponsored by IEEE Switchgear Committee ADSCOM, was held on September 29 2009 during the IEEE Switchgear Committee meetings in Denver, CO.

The project authorization request to IEEE to become a working group as drafted by the TF was approved by the IEEE Switchgear Committee ADSCOM for submission to IEEE. A web site was created to provide information about the Task Force (TF) on Fault Current Limiter (FCL) Testing: http://www.caps.fsu.edu/fcl-testing.html

M. Steurer was invited to present about the IEEE Task Force (TF) on Fault Current Limiter (FCL) Testing during the CIGRE Workshop on Test Techniques and Procedures for HTS Power Applications, held May 13-15, 2009, at the Noyori Materials Science Laboratory, Nagoya University, Nagoya, Japan (the presentation was delivered by Isidor Sauers, Oak Ridge National Lab, USA, on behalf of M. Steurer). Steurer was also invited to present about the IEEE Task Force (TF) on Fault Current Limiter (FCL) Testing during the HTS DOE Peer review, to be held August 4-6 2009 in Alexandria, VA. In May 2009 Steurer was invited to review the HTS Framework that Navigant Consulting has developed for DOE. Subsequently, Steurer attended several tele-conferences and provided feedback to Navigant Consulting in support of this request. Steurer attended the third meeting of the CIGRE WG A3.23 “Application and feasibility of fault current limiters in power systems” Sept 9-10 in Zurich, Switzerland.

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Contributions to the development of the guideline for IEEE p1547.7

(O. Faruque, M. Steurer)

Background

IEEE 1547 (2003) is the basic standard that deals with interconnection of distributed resources with electric power systems. It has a series of standards that are being developed by Standards Coordinating Committee 21 on Fuel Cells, Photovoltaics, Dispersed Generation, and Energy Storage concerning distributed resources interconnection [1]. In that series, 1547.7 deals with the development of a guide to conducting distribution impact studies for distributed resource interconnection. This guide describes the criteria, scope, and extent for impact studies on electric power systems when a distributed resource or aggregate distributed resources are connected to that area electric power distribution system [2].

CAPS role and activities

CAPS has volunteered to play a constructive role in the development of the guide which will later be used as an standard for impact studies for interconnecting distributed resources. The guide will allow distributed resource owners, interconnection contractors, area electric distribution power system owners and operators, and regulatory bodies to have a standard methodology for when distribution system impact studies are appropriate, what data is necessary, how they are performed, and how the study results are evaluated [2]. Since CAPS has the experience of performing most of the required impact studies through off-line simulation, hardware-in-the-loop simulation and experimental validation, our objective is to share the experience and wisdom that we gained over time. In addition, CAPS facility is also suitable for performing impact studies that may be needed for distributed resources interconnection, as has been explored and demonstrated in prior phases of this DOE-supported effort. CAPS can play a vital role in the development of the guide by providing inputs based on scientific research and evidence.

In line with our objective and the scope for contribution to the impact study, the following activities were performed so far:

1. Sanjeev Srivastava attended the first meeting that took place in Las Vegas in February 2009 and introduced CAPS to the contributing members. In the first meeting, the scope, limitation and criteria of the guide were determined. Sanjeev actively participated there for CAPS and contributed in the development of the structure of the guide.
2. Omar Faruque attended the second meeting in August 2009 in San Francisco. In that meeting, the first draft was presented for discussion. CAPS took part in the discussion of reports, restructuring and re-writing of some parts of the report. CAPS also emphasized the need for detailed impact studies, which become increasingly important with ever increasing penetration levels and diversity of distributed resources being considered for interconnection.
3. Mischa Steurer and Omar Faruque attended the 3rd meeting that took place in Atlanta in last October (6th and 7th). CAPS actively contributed in the discussion of various aspects of the guide, especially in the discussion of restructuring the guide. Various technical issues were discussed and we contributed there by providing inputs from our research experience. CAPS has also volunteered to re-write/edit some parts of the report and will present these at the next meeting. CAPS has also committed to provide a case study on impact of energy storage (battery system) integration with the distribution line.

Future contributions

In support of further development of the guideline/standard for IEEE 1547.7, FSU CAPS representatives continue commitments and efforts in the following areas:

- Continuation of the effort in rewriting/editing various part(s) of the guideline, including active contributions to chapters 7, 8, and 9.

- Attend/organize the teleconferences to discuss various related technical and editing issues associated with those parts of the guideline.
- Work on the case study of impact of energy storage integration with the distribution network
- Present progress and contributions to the committee (attended and presented at the October 2009 and February 2010 meetings)
- Any subsequent work that might be required to complete the guide.

Analysis of a STATCOM Application for Wind Resource Integration

(L. Qi, J. Langston, M. Steurer)

With 2005/2006 funding from the DOE, Office of Electricity Delivery and Energy Reliability, FSU CAPS made significant contributions to a collaborative project with Bonneville Power Administration, Tennessee Valley Authority, NC State University, Sandia National Labs, EPRI, the DOE OE Energy Storage program, and others, to understand and develop solutions to voltage and reactive power support around weak systems and in particular a remote induction-generator based wind farm in eastern Oregon, including development and implementation of an ETO-based STATCOM from NCSU. That project led to a subsequent contract with EPRI for FSU CAPS to test the STATCOM controller in a dynamic real-time hardware-in-the-loop simulation-based test environment.

Outside the scope of the EPRI contract, but, a part of the Distributed Energy Resource integration focus of this project was an effort to study and understand the broader system integration and protection issues associated with active power electronics controllers for improvement of stability and control around wind-farms, and especially, continuing to look at the specific Bonneville power system case for which much data and validated dynamic models are now available as a result of the prior work. This describes activity in verification of the voltage support function of STATCOM in the BPA wind farm system.

Wind farms are becoming important distributed renewable energy resources. However, voltage stability issues with wind farms employing fixed-speed induction generators may require such systems to be augmented with dynamic compensation devices, such as STATCOM units. In preparation for deployment of a 10 MVA STATCOM at an existing wind farm, shown in Figure 13 [3], in the Bonneville Power Administration (BPA) system, the STATCOM controller, whose diagram is shown in Figure 14, is to be tested through hardware-in-the-loop simulation with a real-time digital simulator, which will model both the BPA system and wind farm with high fidelity, transient models. This research presents groundwork conducted in preparation for the dynamic testing of the controller, including studies of the stability improvement facilitated by the introduction of the STATCOM into the BPA system.

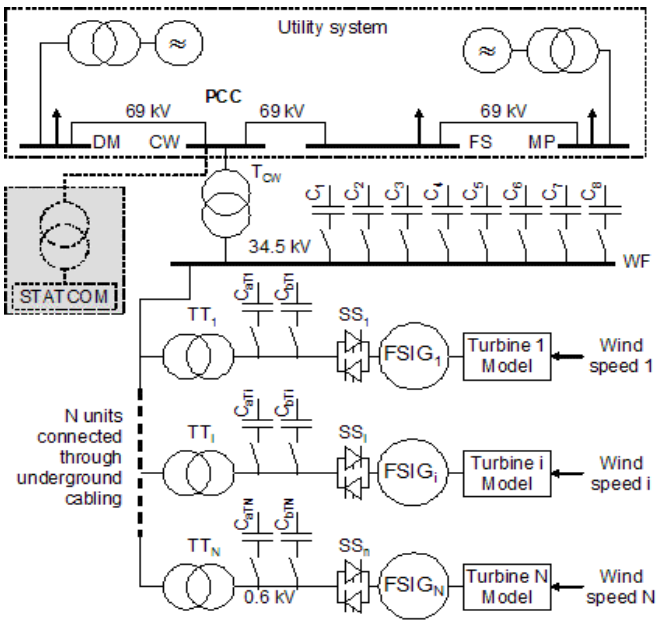

Figure 13. Basic system layout used for RTDS model (adopted from [3])

The enhancement of voltage stability and induction generator stability by the STATCOM is studied analytically by power-voltage and torque-slip relationships of a simple wind power system, as well as through simulation studies with the real-time simulation to be used for testing of the controller. Simulation results from both approaches are compared and illustrate the potential benefit of the STATCOM in preventing voltage collapse caused by serious network changes, such as opening a line, as well as improvement of the Fault Ride Through capability of the wind power system.

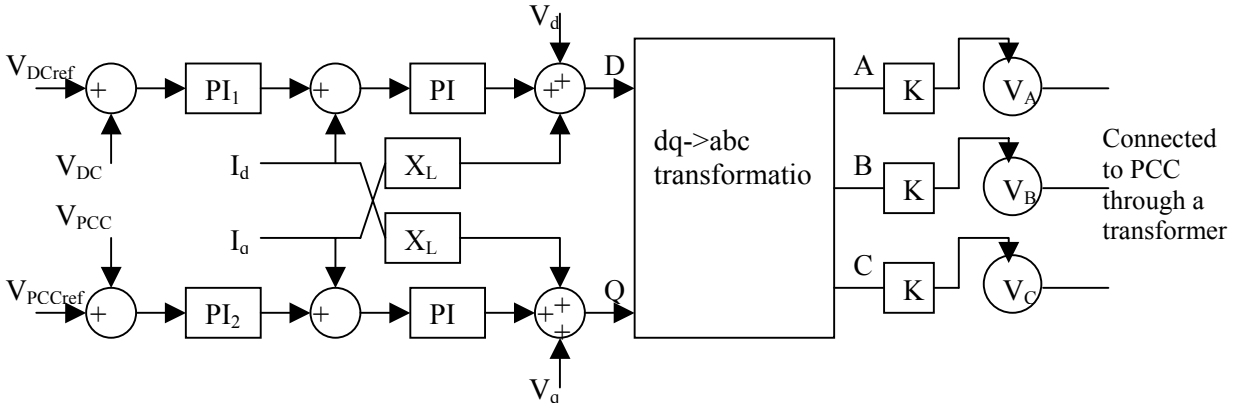

Figure 14. A generic STATCOM and its controller

Simulation studies were carried out with the RTDS simulation for the test system described in the previous section. The dynamic behavior of this test system was obtained for two network disturbances. For one of the scenarios, one of the lines serving the wind farm is abruptly opened. For the other scenario, a three-phase fault is applied at a nearby substation. The dynamic voltages at the PCC with and without the STATCOM are compared. The improvement of the dynamic response provided by the STATCOM shown in the simulation is compared with analytical results.

Opening of Line. In this case, a severe condition for voltage recovery analysis is considered in which the line between the buses labeled DM and CW in Figure 13 is opened. Due to the increase of the equivalent line reactance, extra reactive power is needed in order to maintain the voltage at PCC. While switched capacitor banks can supply this reactive power, the additional reactive power is supplied in discrete steps, which may cause undue voltage fluctuations. Furthermore, the reaction time of the capacitor bank controls may be too slow to provide adequate support for such a dynamic event. Therefore, the STATCOM is expected to provide this extra reactive power support dynamically with continuous change of output quickly enough for voltage recovery when the line opens.

Figure 15 illustrates the ability of the STATCOM to mitigate a voltage collapse scenario. In this scenario, the wind farm produces around 37 MW (0.74 pu of its 50 MW rating), when the line is opened. In the present situation, with only power factor correction capacitors available, this would eventually lead to a voltage collapse if no other corrective action were taken (e.g. tripping out the wind generators). With less than 5 MVAr dynamic reactive power injection from the 10 MVAr STATCOM (i.e. 0.5 pu of its rating), the voltage collapse is avoided, and the power for the wind farm might be more gradually reduced to a safer operating point until the line is put back in service. The figure also shows the reactive power contribution from the STATCOM in per unit values of a 10 MVAr rated STATCOM.

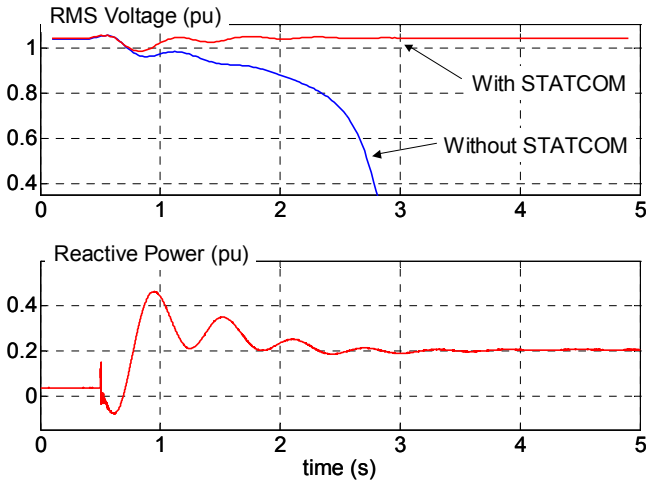

Figure 15. Mitigation of voltage collapse and associated reactive power injected by a 10 MVAr STATCOM

Using the equations for a simplified equivalent circuit approach, the PV curves of the simplified system without and with the line open, with and without contribution from the capacitor bank, and at different levels of STATCOM compensation currents, are shown in Figure 16. From this analysis we see that if the wind farm output is at or exceeds approximately 0.62 pu the system will experience voltage collapse after the line is opened, even with the capacitors providing adequate reactive power support prior to the event. With the STATCOM providing additional reactive power support, the system can maintain voltage stability until the maximum allowable power reaches approximately 0.82 pu. These estimated power limits are close but noticeable smaller than the power limits of 34 MW (0.68pu, with only one line connected) and 44 MW (0.88pu, with both lines connected) derived from RTDS simulations under quasi steady-state operations. Simplifications in the analytical model, such as the use of only one equivalent induction generator model and a constant current injection for the STATCOM may contribute to the smaller power limits obtained from this approach. In comparison, the more detailed RTDS model uses 40 induction generators and a better representation of the utility system.

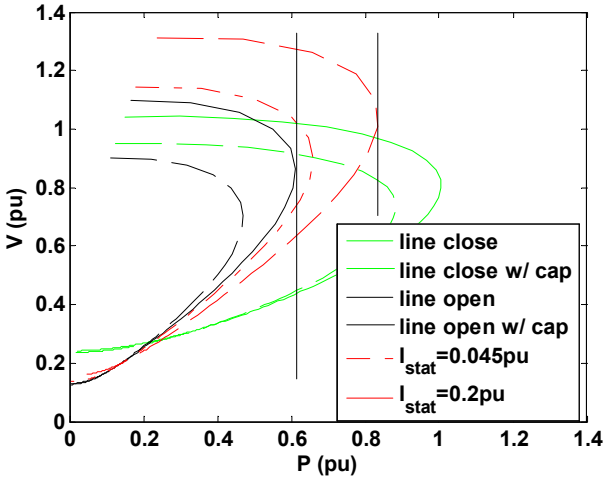

Figure 16. PV curves from analytical analysis

Three Phase Fault. For this scenario, a severe condition of fault recovery is considered in which a three-phase short circuit is applied at a bus close to the wind farm PCC. During a fault, the stator of the induction generator is demagnetized due to subsequent drop in voltage at the PCC while the rotor speed increases. Since the rotor flux cannot change immediately, the machine experiences a transient and delivers a large amount of reactive power into the system. At the same time, the real power delivered to the utility system becomes small and the rotation speed increase significantly because of excess energy from the constant wind turbine power. After the fault is cleared, the machine consumes a large amount of reactive power due to the re-magnetization and the increased speed during the fault. If the increased speed is above the maximum allowable speed corresponding to the CCT, the large amount of required reactive power may induce voltage collapse.

Wind generators are required to remain connected and supply real power to the electrical system immediately after network faults. This capability of wind generators is called Fault Ride Through (FRT) capability. According to the Low Voltage Ride Through (LVRT) standard by FERC [4], which is shown in Figure 17, the induction generators should stay connected when the voltage at the PCC is as low as 15% of its nominal value for 0.625 s. Furthermore, the wind farm must remain online as long as the voltage at the PCC reaches 90% of its nominal value within 2.375 s after the fault has been cleared.

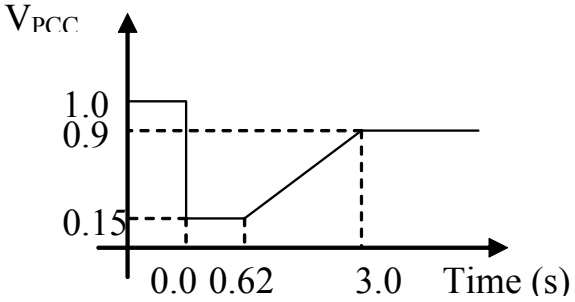

Figure 17. FRT requirement by FERC

One way to increase the FRT capability is to install a STATCOM at the wind farm terminals. While during a fault, a relatively small STATCOM contributes little to support voltage it may provide sufficient reactive power after the fault clears to extend the FRT capability.

Figure 18 illustrates the support by the STATCOM in recovery from a fault. For this scenario, the wind farm was supplying about 37 MW (.74 pu) when a three-phase fault is applied to the 69 kV bus at a nearby substation. The fault is cleared after 9 cycles. Without the STATCOM, the wind farm would be unable to recover and requires to trip off line in order to prevent voltage collapse. With the STATCOM, however, the wind farm is able to recover successfully. As illustrated in Figure 13, the STATCOM control was commanded zero reactive power during the fault in order to avoid additional fault current contribution into the utility system.

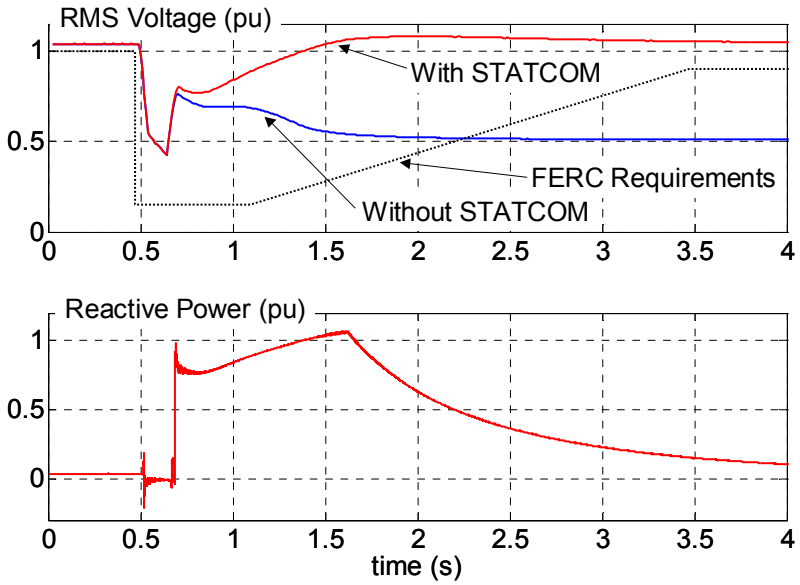

Figure 18. Support of FRT capability of the wind farm by the 10 MVAr STATCOM

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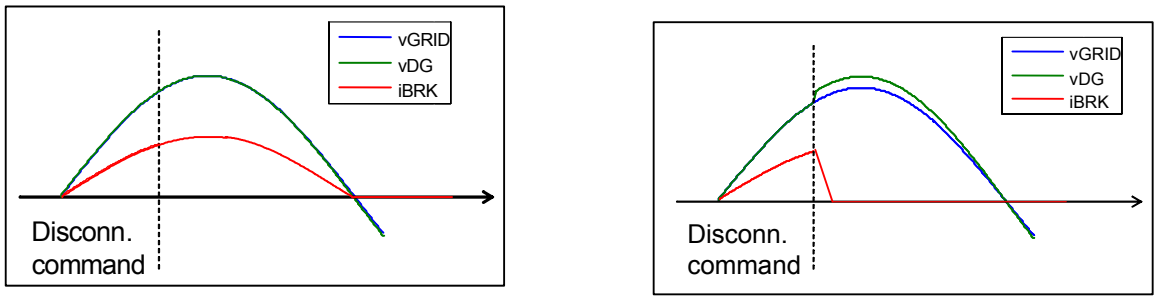
A Grid-interactive inverter with Energy Storage Elements

(H. Li, L. Liu)

Introduction

Background

Grid-interactive inverters converting renewable DC power sources such as photovoltaic or fuel cells to AC grid systems are gaining considerable popularity as the energy crisis and environmental concern becomes the driving force for alternative energy. Grid-interactive inverters expect sufficient reactive power regulation to improve grid voltage quality and power quality besides controllable real power [5]. And energy storage elements (ESE) integrated in such inverters can help distributed energy sources (DES) schedule real/reactive power flow responding to grid-side demand. Grid-connected inverters with energy storage systems (ESS) for small distributed power generation (DG) system have been gaining popularity due to the following advantages: (1) power quality can be improved; (2) voltage regulation capability can be improved; and (3) grid stability can be enhanced. In the reported one, a mixed operation of real/reactive power in a wide region was achieved [6]. However, much attention was paid to provide either pure dynamic real power to improve transient grid stability or pure reactive power to meet power quality requirement [7-8]. It is necessary to develop a grid-connected inverter merges notable techniques such as "single-stage", "multilevel" and "transformerless", but not the inverters adopting multiple-stage or transformer [9], to improve in efficiency, cost, reliability, weight, size, etc. In addition, the reported grid-connected inverters with ESS [10-15] require multiple conversion stages. The DC-side shunted topology has been used in [10-12], which can achieve flexible real power management but suffer the limited reactive power compensation due to the limited AC output voltage. The AC-side shunted topology has been used in [13-15], which can implement the wide real and reactive power management but increase the complex and cost of the whole system. Cascaded multilevel inverters with ESS [16-19] have been used to achieve single-stage energy conversion, but suffer inadequate DC voltage usage and limited analysis on real and reactive power allocation. In addition, energy storage is required to compensate the variation of renewable energy source when it operates at stand-alone mode. For sensitive and mission critical local loads, a seamless transition between two operation modes of grid-interactive system is also valuable, especially for the transition from grid-tied mode to stand-alone mode in the case of utility fault. The traditional method needs a half cycle to disconnect from the utility in the worst scenario, since the current through the static transfer switch has to be naturally reduced to zero [20], as shown in Fig.19 (a). Methods based on the voltage amplitude and voltage phase regulation [21] were proposed to reduce the transition time, but the load voltage of these methods becomes discontinuous during transients and it will cause mechanical vibration for electric machine loads, as shown in Fig.19 (b).



(a) *(b)*

Fig.19. The traditional transfer control from grid-connected mode to stand-alone mode

Problem Definition

The main difficulties to implement wide range reactive power compensation and maintain power quality are: (1) how to separate the real and reactive component of inverter output voltage; (2) how to properly distribute the reactive power between distributed energy source (DES) and ESS; (3) how to achieve the voltage balance within ESS; (4) how to achieve fast and smooth seamless transfer from grid-connect mode to standalone mode without output voltage distortion.

Relevance to DOE

Besides the already mentioned interest on grid-connected inverter for DG system due to improved stability and increased efficiency, another incentive to integrate ESS into DG system is the ever-increasing need to achieve energy conversion reduction, as well fast and smoothing real and reactive power compensation at local position with help of ESS. The DG system with wide range real and reactive power compensation poses severe challenges in the development of new inverter topology and minimizing energy conversion stages; so novel inverter topology with combined ESS is attractive to DOE mission and the future of DG system.

Expected Improvement over the Current State-of-the-Art

This main goal is to develop a single stage grid-interactive transformerless inverter for DG system with ESS. The advantages of the proposed inverter are: (1) improved efficiency and lower cost by single stage conversion; (2) transformerless design; (3) higher dc boost ratio; (4) reduced switching loss by using hybrid phase-shift PWM; (5) fast and smooth seamless transfer. In addition, the topology can provide: (1) a wide range of real and reactive power compensation; (2) fast dynamics for real and reactive power requirement; and (3) rejection capability against grid voltage disturbance and grid current distortion.

Research Activities and Results

Topology development:

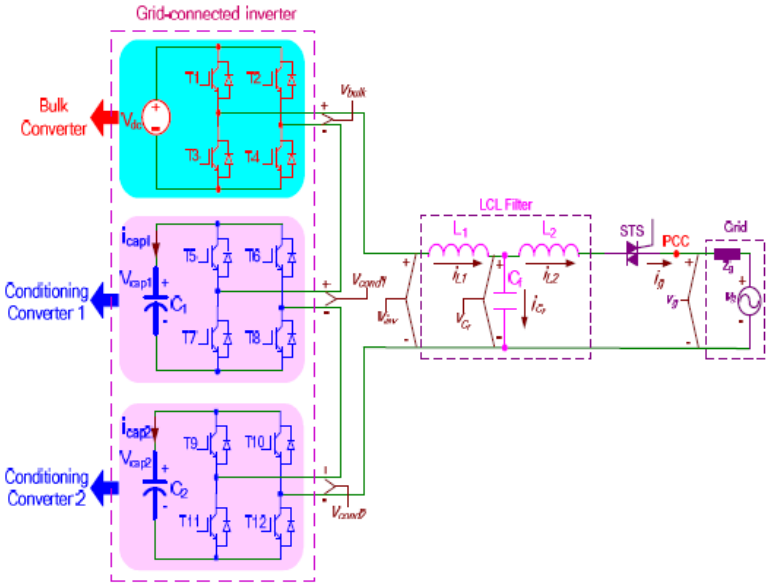


Fig.20. Grid-connected inverter-based system configuration

Fig.20 exhibits the system configuration based on the developed grid-connected inverter. This inverter consists of 3 H-bridges in cascade with one bulk converter linked to distributed energy source (DES) (PV, FC, etc.) and the other two conditioning converters tied to energy storage elements (ESE). As the first step research, the capacitor is used as ESE. Voltage ratio of DES, ESE1 and ESE2 is 2:1:1 for optimal input consideration. As an efficiency-increasing scheme, the hybrid carrier based phase-shift (HCBPS) PWM in use enables bulk converter to work at line frequency and the conditioning converters to operate at reduced switching frequency. Output current is refined by a LCL filter, and then is injected to the PCC through a static transfer switch (STS).

Power flow interaction analysis:

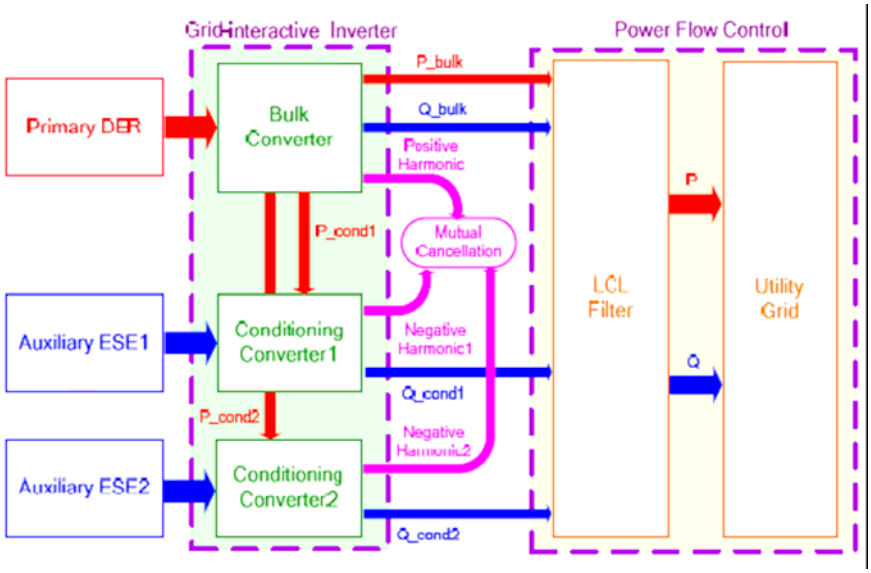


Fig.21. System Power Flow Interaction

Fig.21 illustrates the system power flow interaction. In DC side: bulk converter extracts all real power and partial reactive power from DES; and conditioning converters absorb the remaining reactive power from ESE. Inside the inverter: little real power from DES compensates losses consumed by both conditioning converters; and low-order voltage harmonics resulting from fore-mentioned hybrid modulation strategy are mutually cancelled. In AC grid side, most real/reactive power is injected to the grid after deducting a slight quota used by LCL filter.

Hybrid modulation strategy analysis

The proposed hybrid modulation strategy can reduce the switching loss and expand the switches' lifetime. However, the over-modulation problem is demonstrated in Fig.22 using one example when converter V_{dc}=200V, V_{cap}*=100V, V_{inv}*=200V. The modulation index and switching angle for the bulk inverter are:

$$M = \frac{V_{inv}^*}{V_{dc}} = \frac{200}{200} = 1,\ \theta_1 = \arccos(\frac{V_{inv}^*}{V_{dc}} \cdot \frac{\pi}{4}) = \arccos(\frac{200}{200} \cdot \frac{\pi}{4}) = 38.24^\circ \quad (1)$$

Fig.22 (a), (b), (c) describes the total output voltage $V_{inv}^* = MV_{dc}\sin\omega t = 200\sin\omega t$, output voltage command of bulk inverter and conditioning inverter, respectively. The V_{cond}* in Fig.22 (c) exceeds the capacitor voltage V_{cap}* (100V) at four electric degree intervals. So V_{cond}* can't be replicated and the actual

V_{cond} is shown in Fig.22 (d). The phenomenon is defined as over-modulation in the conditioning inverter, which will cause the distortion of output voltage shown in the left side of Fig.22 or bring in low order harmonics.

Since the over-modulation is caused by the fact that the voltage command V_{cond}^{*} exceeds the capacitor voltage. If capacitor voltage magnitude can be controlled, the over-modulation problem can be solved. Fig.23 (a) shows the desired capacitor voltage control trajectory and the corresponding switching angle to solve the over-modulation problem. If the capacitor voltage is requested to be constant, e.g., $0.5V_{dc}$, the effect of over-modulation on the THD will depend on different switching schemes and the THD from optimized switching scheme is shown in Fig.23 (b). If modulation index range is chosen from 0.5 to 1.2, the THD of output voltage will meet IEEE519.

The optimized switching scheme can be found from Fig.24, which shows single switching of the bulk inverter requires minimum capacitor voltage, compared with multiple switching, to avoid the over-modulation problem.

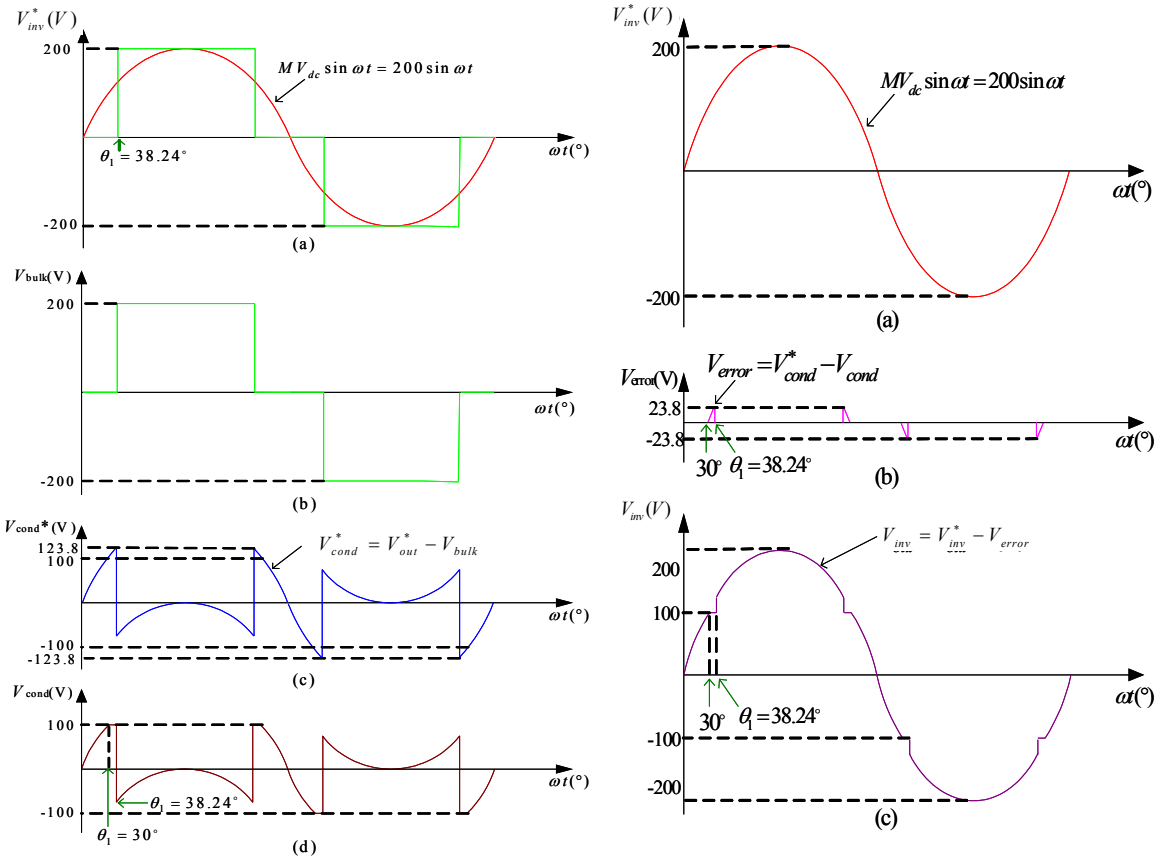
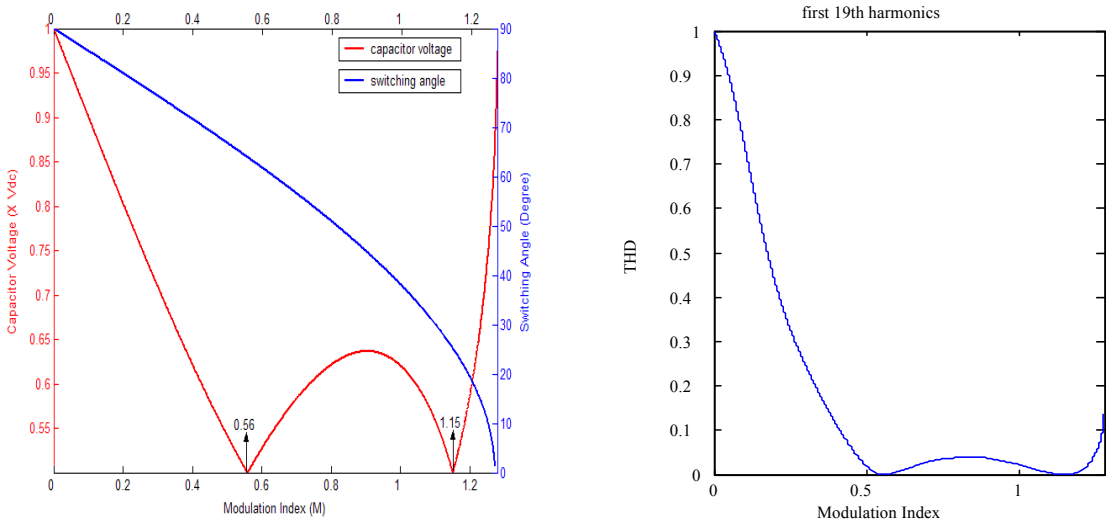


Fig.22. The over-modulation problem



(a) *(b)*

Fig.23. Over modulation effect analysis

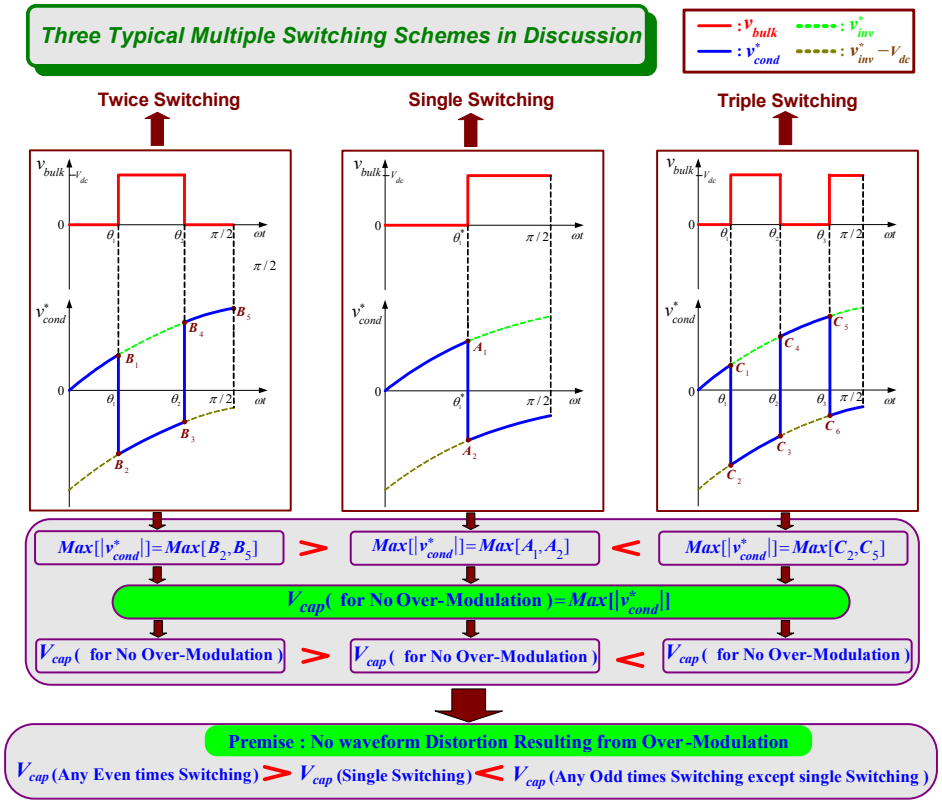
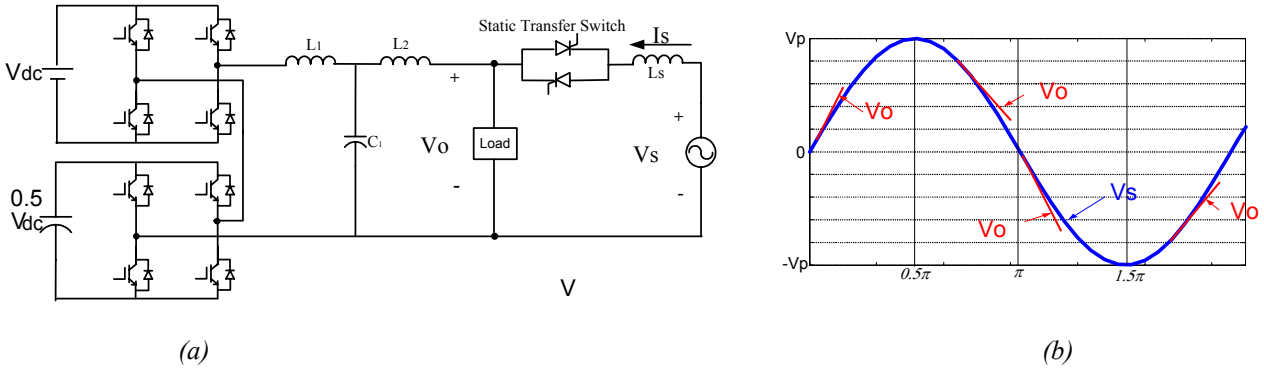


Fig.24. Optimized modulation strategy

Fig.25 (a) shows a single phase with two cascaded inverters to demonstrate the proposed seamless transfer control algorithm. A voltage difference thus can be generated between V_s and V_o to force the current i_s to zero from grid-connected mode to stand-alone mode. In order to make the transition time shorter, the voltage V_o needs to be well regulated. The voltage amplitude regulation and voltage phase regulation methods can make time shorter but the voltage waveforms in these methods become discontinuous which lead to the mechanic vibration for electric machine load. Instead of control voltage phase angle, the voltage frequency is regulated to achieve the same goal. The advantage of the voltage frequency control is now the voltage waveform become continuous since the phase angle is the integral of the frequency.

Fig.25 (b) shows the change tendency of output voltage V_o if a disconnection signal is received at different phase angle of one cycle. By regulating the output voltage frequency, the current i_s is forced to zero in less than ¼ cycle at worst-case and with continuous load voltage as well. The detailed frequency regulation logic is illustrated in Fig.26. Depending on the instant phase angle, every one cycle of the breaker current is divided into five zones (0-4). In zone 1 to 4, the frequency of V_0 is either controlled to increase or decrease for a period of half a cycle. In zone 0, no extra frequency regulation is activated since the natural turn-off of the breaker current is already very fast. One thing to be mentioned here is the concept of "dead band". As shown in Fig.26, the four control zones differ from the four quadrants of the current by a dead band of dΦ. This band should be large enough to assure the breaker current to be extinguished before it enters into the next quadrant. Otherwise, the control method may exacerbate the breaker current when it spans quadrants.

Fig.27 shows that the output voltage control of the utility-interactive interface is divided into four different operation modes. In each mode, the magnitude and the frequency of the modulation voltage are separately controlled. In the "stand alone" mode, the inverter is operating with constant 1 pu voltage magnitude and 60 Hz frequency. When the utility connection is requested, the interface enters into the "synchronization" mode. In this mode, the inverter adjusts its output voltage to follow the waveform of the grid voltage. Only when both the magnitude and phase differences are within the given threshold for a minimum amount of time can the transfer switch be closed and the inverter enters into the "online operation" mode. In this mode, the reactive power going out of the inverter is controlled to be zero that indicates a unity power factor. The active power is controlled to the desired value. When the inverter is disconnected from the grid, the proposed frequency regulation control is activated to extinguish the current as soon as possible. This mode is called the "disconnection" mode.



(a) *(b)*

Fig.25 (a) Single-phase utility-interactive inverter and (b) controlled V_o *tendency during one full cycle*

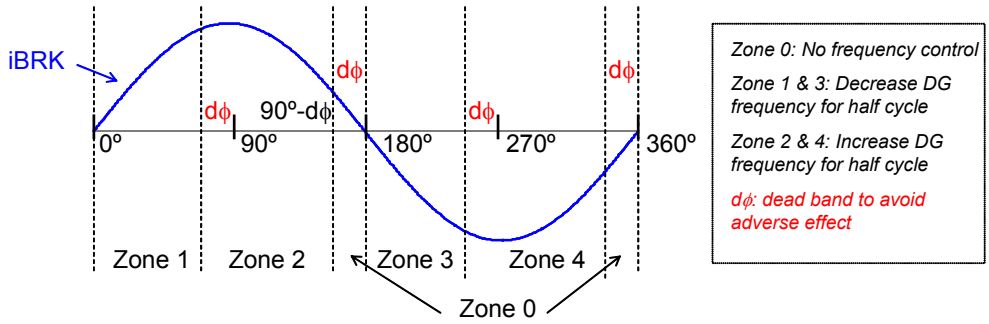


Fig.26. The frequency regulation logic for fast current extinguishing control

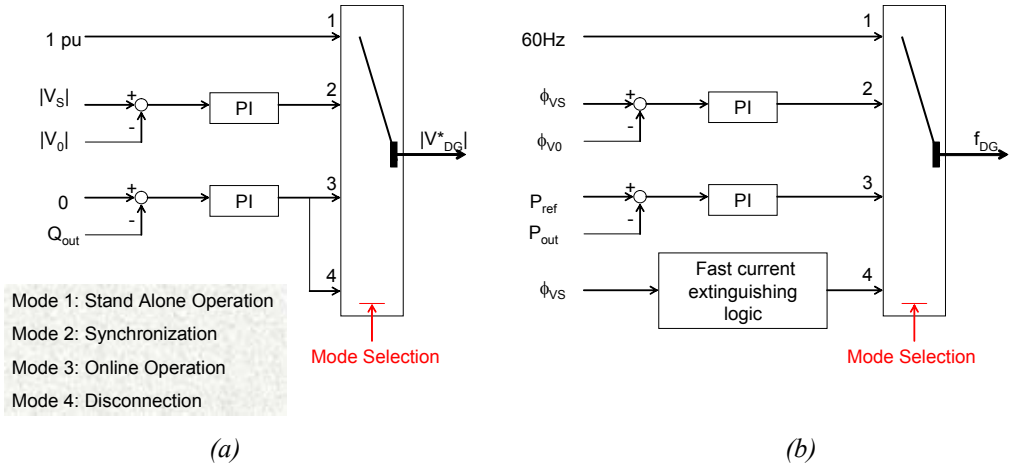
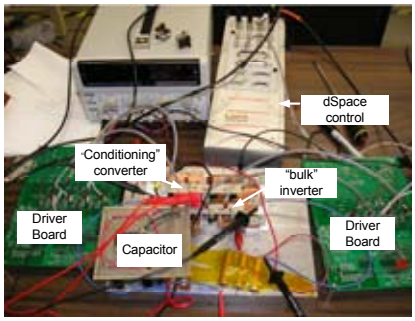


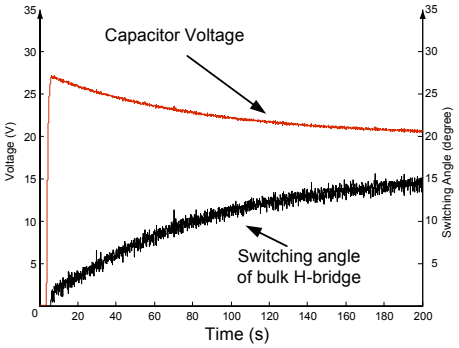
Fig.27. The control logic of the utility-interactive inverter (a) magnitude control algorithm and (b) frequency control algorithm

Seamless transfer method hardware verification

The research results have been verified using a single-phase utility-interactive hybrid cascaded inverter prototype of Fig.28 (a) for resistive load with a scaled-down power rating. The LCL filter and the thrysitor are not shown in Fig.29. The control signal is generated using dSPACE DS1104 controller board. V_{dc} is chosen as 40 Volts and V_{cap} is regulated as 20 Volts. The switching frequency of "conditioning" inverter is 15 kHz. Fig.28 (b) shows the experimental waveforms of capacitor is controlled to be 20 Volts and switching angles of bulk inverter is regulated to 15 degree. Fig.29 shows the single-phase experimental output voltage waveforms of cascaded H-bridge inverter with single dc source are consistent with those of simulation results. Fig.30 (a)-(b) shows the experimental results from grid-connected mode to stand-alone mode using frequency regulation method and traditional method at worst-case scenario. It is clear that proposed method forced current to zero much faster.

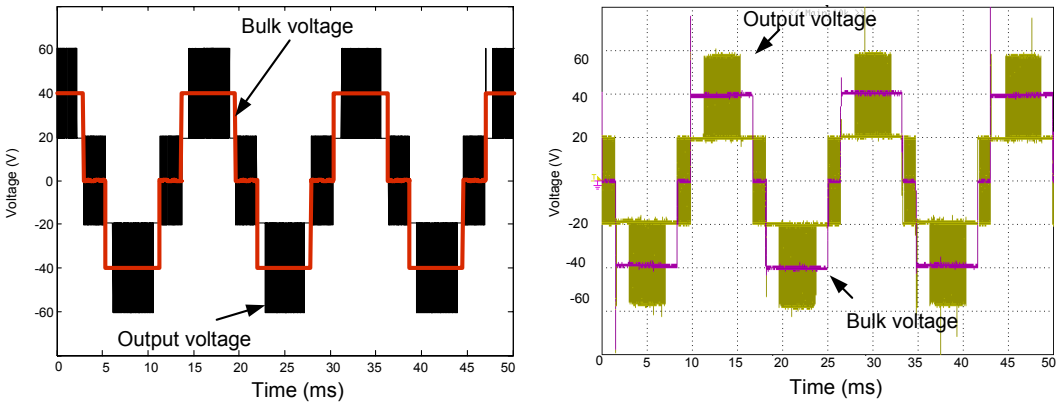
Fig.30 (c)-(d) gives the experimental results when the disconnection occurs at different phase angles. Both figures validate the effectiveness of the proposed method. One observation in the results is the magnitude separation (i.e., the magnitude of V_0 differs from the magnitude of V_S) after the turn-off of the current. This phenomenon roots from the poor voltage regulation of the source voltage. In our experiment setup, the source voltage is taken from the grid after a step-down transformer that has a fairly large leakage inductance. When the load transfer changes after the current extinguishes, the voltage drop on the transformer also changes and therefore the magnitude of the two voltages diverge from each other.





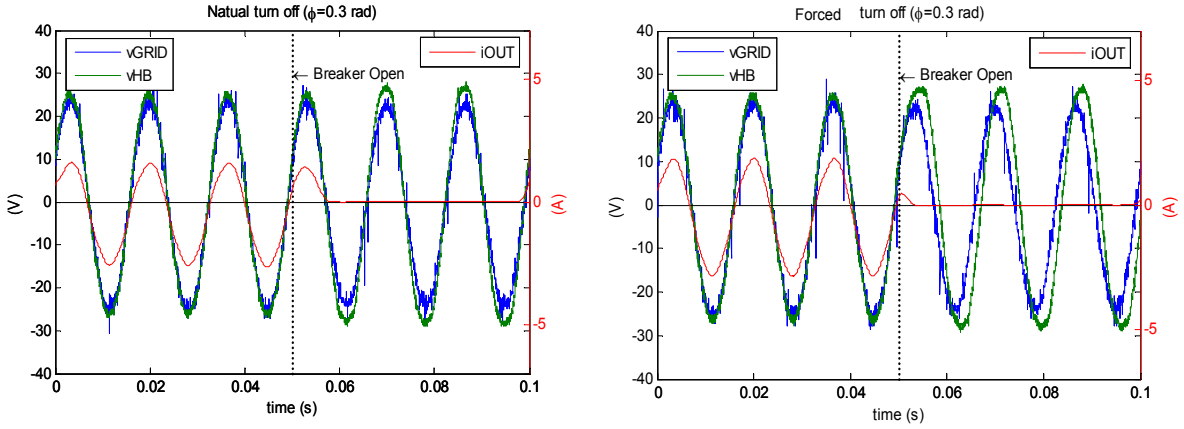
(a) *(b)*

Fig.28. (a) The photo of single- phase hybrid cascaded inverter and (b) The experimental waveforms of capacitor voltage and switching angle of bulk inverter

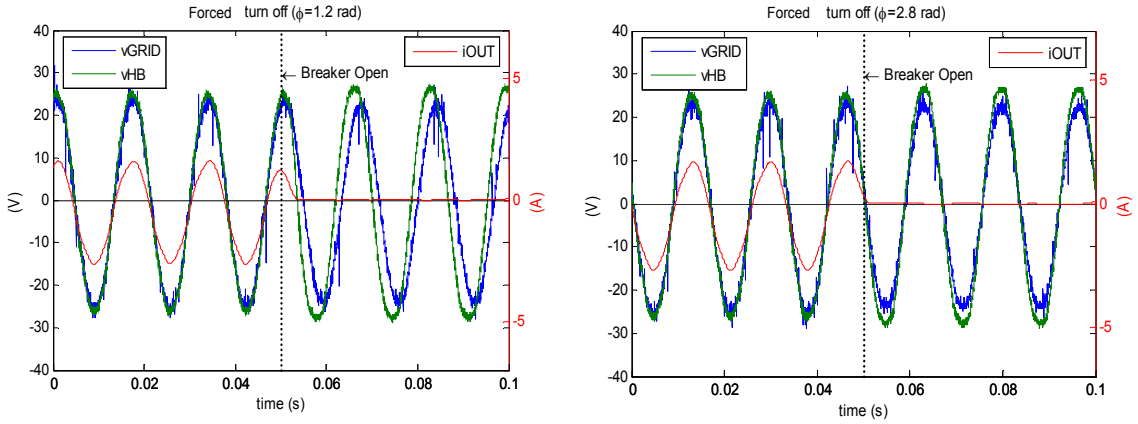


(a) (b)

Fig.29. Output voltage waveforms of hybrid cascaded H-bridge (a) simulation results and (b) experimental results



(a) *(b)*

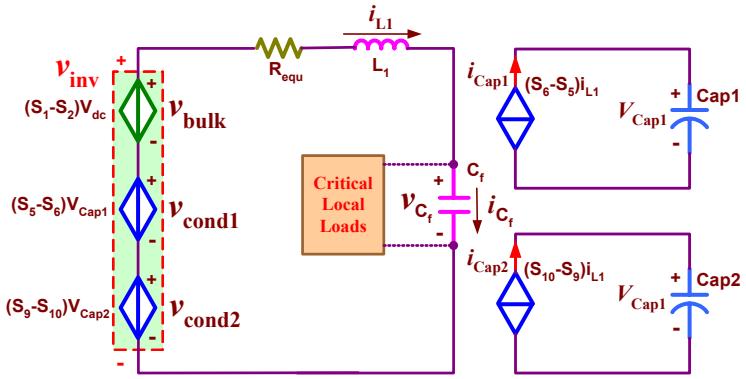


(c) *(d)*

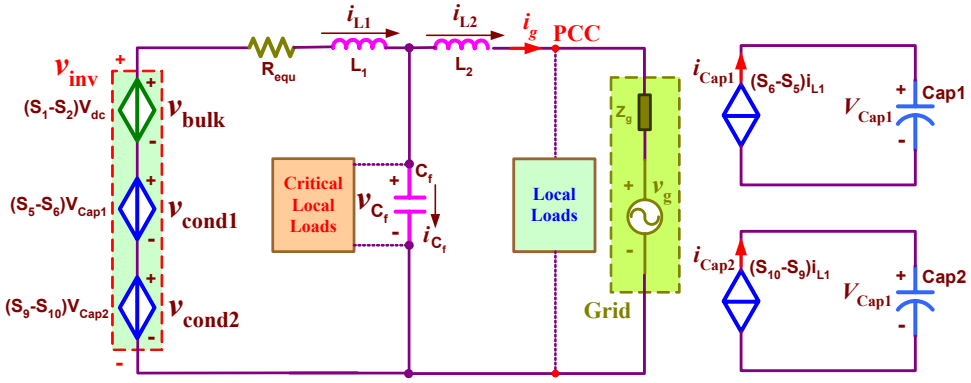
Fig.30. Experimental results from grid-connected mode to stand-alone mode using traditional method and the proposed frequency regulation method. (a) traditional method when Φ=0.3rad, (b) proposed method when Φ =0.3rad, (c) proposed method when Φ =1.2rad, (d) proposed method when Φ =2.8rad

System models development:

The nonlinear large-signal averaged models for proposed DG system with ESS are developed in stand-alone mode and grid-connected mode as shown in Fig.31. These models can be used to design controllers and conduct system dynamic simulation.



(a) Developed converter model at stand-alone mode



(b) Developed converter model at grid-connected mode

Fig.31. Proposed converter nonlinear large-signal averaged model in stand-alone mode and grid-connected mode

The average model in standalone mode is presented in Fig. 31(a). R_{equ} is equivalent inverter resistance. LC filter is used to attenuate high frequency voltage harmonics. Inverter voltage v_{inv} is modeled as three controlled voltage sources v_{bulk}, v_{cond1} and v_{cond2} in series. S1, S2, S5, S6, S9 and S10 are average switching functions. v_{bulk} is symbolized by S1&S2, v_{cond1} is symbolized by S5 and S6, and v_{cond2} is symbolized by S9 and S10. As to DC capacitor 1, controlled current source i_{cap1} is associated with S5, S6 and inductance current i_{L1}. Similarly as for DC capacitor 2, controlled current source i_{cap2} is related to S9, S10 and i_{L1}.

The average model in grid-connected mode is presented in Fig.31 (b). R_{equ} is equivalent inverter resistance. Different from the model in standalone mode, this model uses LCL filter and interconnects with main grid. LCL filter is selected here relying on higher attenuation around switching frequency, lower switching frequency and smaller size given the similar attenuation, and prevention of inrush current. three controlled voltage sources and two controlled current sources are involved in this model. S1, S2, S5, S6, S9 and S10 are average switching functions of corresponding converter legs.

Control system development

Considering the proposed system will be operated at stand-alone mode and grid-connected mode, the optimal control system should be designed at the two modes to guarantee the system operation.

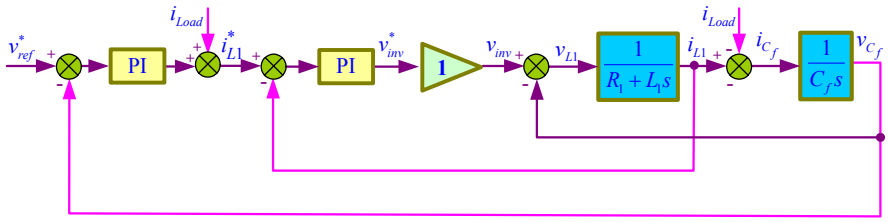
Design decoupled controller in AC side and DC side based on the developed models in standalone mode

The dynamic control system model at stand-alone mode is shown in Fig.32. It consists of capacitor voltage balance control and output voltage control jointed with converter model. As shown in Fig.32 (a), dual-loop PI controller is adopted to track output voltage instantaneously in AC side. Load current i_{Load} is treated as a disturbance. As shown in Fig.32 (b), three parallel PI controllers in DC side are used to control two capacitor voltages balance and stability during transient and steady state in order to ensure system stability. Hybrid PWM modulation produces average switching functions S1, S2, S5, S6, S9 & S10 to construct average model.

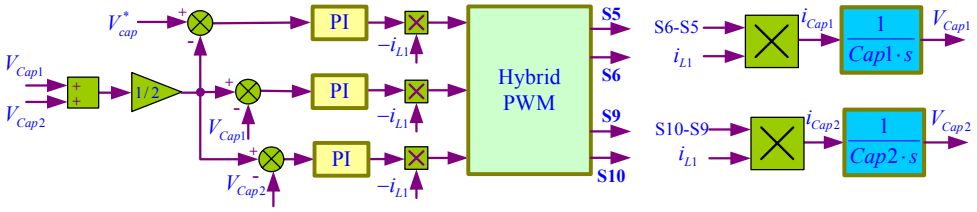
In order to access the parameters of the control system, the detail deduction is presented as follows.

PI for outer loop voltage regulation:

$$PI\_v_{C_f} = \frac{(k_{1p}s + k_{1i})}{s} \tag{2}$$



(a) AC-side controller diagram



(b) DC-side controller design diagram

Fig.32. Decoupled standalone mode control diagram in AC side and DC side

PI for inner loop current regulation:

$$PI\_i_{L_1} = \frac{(k_{2p}s + k_{2i})}{s} \tag{3}$$

Inner current open loop transfer function:

$$G_{op\_i_{L1}}(s) = \frac{C_f(k_{2p}s + k_{2i})}{L_1C_fs^2 + R_1C_fs + 1} \tag{4}$$

Inner current closed loop transfer function:

$$G_{cl\_i_{L1}}(s) = \frac{G_{op\_i_{L1}}(s)}{1 + G_{op\_i_{L1}}(s)} = \frac{C_f(k_{2p}s + k_{2i})}{L_1C_fs^2 + (R_1C_f + C_fk_{2p})s + 1 + C_fk_{2i}} \tag{5}$$

Outer voltage open loop transfer function:

$$G_{op\_v_{C_f}}(s) = \frac{(k_{1p}s + k_{1i})(k_{2p}s + k_{2i})}{s^2[L_1C_fs^2 + (R_1C_f + C_fk_{2p})s + 1 + C_fk_{2i}]} \tag{6}$$

Outer voltage closed loop transfer function:

$$G_{cl\_v_{C_f}}(s) = \frac{(k_{1p}s + k_{1i})(k_{2p}s + k_{2i})}{L_1C_fs^4 + (R_1C_f + C_fk_{2p})s^3 + (1 + C_fk_{2i} + k_{1p}k_{2p})s^2 + (k_{1p}k_{2i} + k_{2p}k_{1i})s + k_{1i}k_{2i}]} \tag{7}$$

Load disturbance closed loop transfer function:

$$G_{cl\_i_{Load}}(s) = -\frac{s^2(L_1s + r)}{L_1C_fs^4 + (R_1C_f + C_fk_{2p})s^3 + (1 + C_fk_{2i} + k_{1p}k_{2p})s^2 + (k_{1p}k_{2i} + k_{2p}k_{1i})s + k_{1i}k_{2i}]} \tag{8}$$

System transfer function for AC side control:

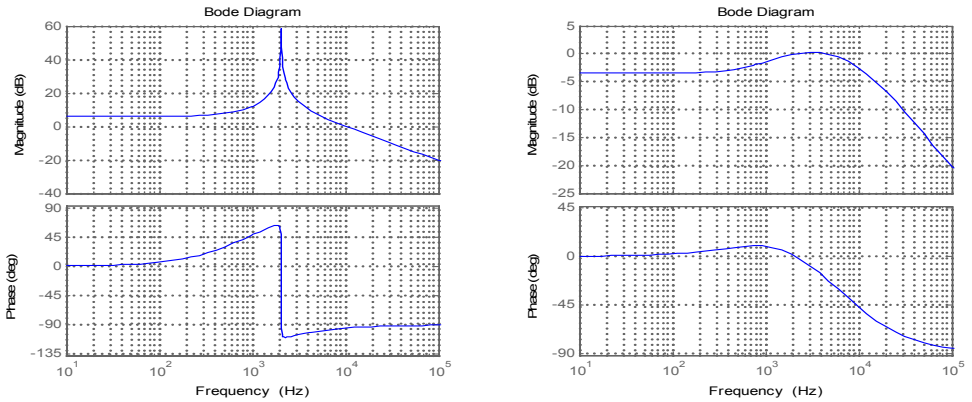
$$\begin{aligned} v_{C_f}(s) &= G_{cl\_v_{C_f}}(s)v^*_{ref}(s) + G_{cl\_i_{Load}}(s)i_{Load}(s) \\ &= \frac{(k_{1p}s + k_{1i})(k_{2p}s + k_{2i})}{L_1C_fs^4 + (R_1C_f + C_fk_{2p})s^3 + (1 + C_fk_{2i} + k_{1p}k_{2p})s^2 + (k_{1p}k_{2i} + k_{2p}k_{1i})s + k_{1i}k_{2i}]}v^*_{ref}(s) \\ &\quad - \frac{s^2(L_1s + r)}{L_1C_fs^4 + (R_1C_f + C_fk_{2p})s^3 + (1 + C_fk_{2i} + k_{1p}k_{2p})s^2 + (k_{1p}k_{2i} + k_{2p}k_{1i})s + k_{1i}k_{2i}]}i_{Load}(s) \end{aligned} \tag{9}$$

Controller design based on pole-assignment of 4-order system:

$$\begin{aligned} &L_1C_fs^4 + (R_1C_f + C_fk_{2p})s^3 + (1 + C_fk_{2i} + k_{1p}k_{2p})s^2 + (k_{1p}k_{2i} + k_{2p}k_{1i})s + k_{1i}k_{2i} \\ &= L_1C_f(s - p_1)(s - p_2)(s - p_3)(s - p_4) \end{aligned} \tag{10}$$

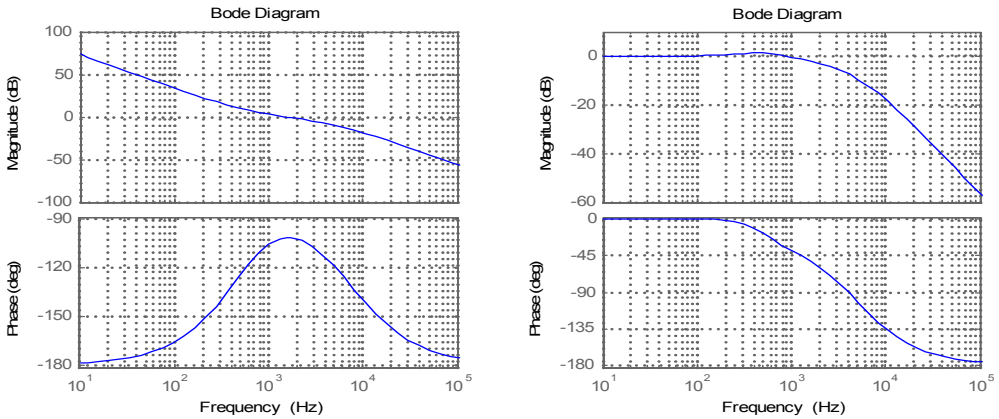
Where: $p_1 = -\varepsilon\omega_r + j\omega_r\sqrt{1-\varepsilon^2}$, $p_2 = -\varepsilon\omega_r - j\omega_r\sqrt{1-\varepsilon^2}$, $p_3 = p_4 = -m\varepsilon\omega_r$; p_1, p_2 are dominant poles; p_3, p_4 are non-dominant poles.

For pre-set damping ratio ε, natural frequency ω_r & m as well as L_1=1.2mH, C_f=5uF, R_1=0.1Ω, controller parameters k_{1p}, k_{1i}, k_{2p}& k_{2i} can be derived. Here, $\varepsilon = 0.8$, $\omega_r = 3500$, m=10.



(a) Inner current open loop frequency response *(b) Inner current closed loop frequency response*

Fig. 33. Inner current loop frequency response



(a) Outer voltage open loop frequency response *(b) Outer voltage closed loop frequency response*

Fig. 34. Outer voltage loop frequency response

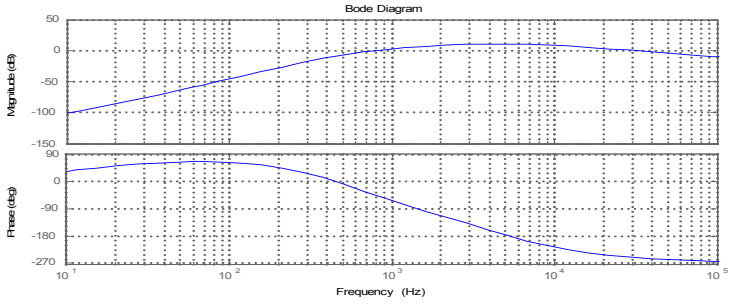


Fig. 35. Load disturbance closed loop frequency response

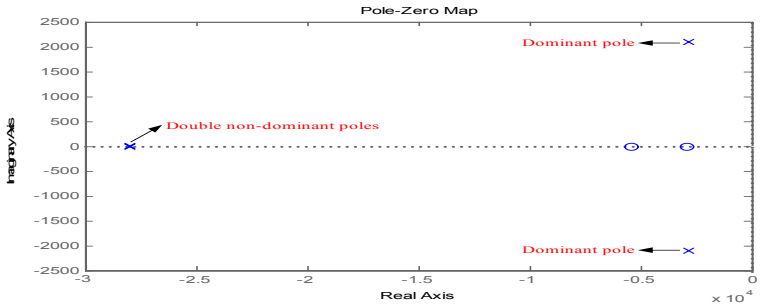


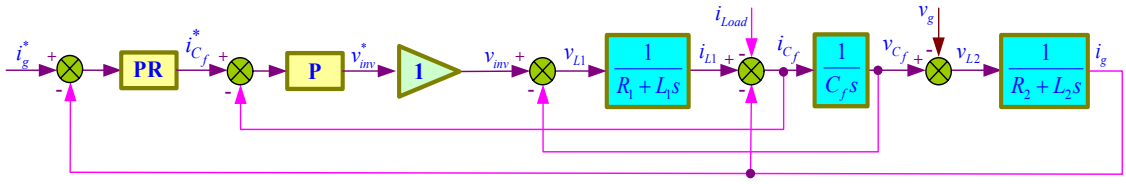
Fig.36. Pole-zeros placement of closed-loop voltage control

From Fig.33~Fig.36, the inner PI current regulator enhances the phase margin to above 80 degree, which improves system stability, and also extends the bandwidth of inner current loop that increases fast response. Outer voltage loop ensures big phase margin to 78 degree. Gain of fundamental component in dual closed loop system approaches 1.0 that denotes slight stable error. High attenuation in low-frequency band seen in Fig.35 reveals strong suppression on load disturbance. Fig.36 shows the pole-zeros placement of the whole closed-loop system that contains two pre-set dominant poles and one non-dominant pole.

Design decoupled controller in AC side and DC side based on the developed model in grid-connected mode

The dynamic control system model at grid-connected mode is shown in Fig.37. It's composed of capacitor voltage balance control and grid current control jointed with converter model. Capacitor voltage balance control (CVBC) can make up for unequal conducting and switching losses in separate DC capacitor. As for CVBC, the average value of real capacitor voltage is fed back to follow preset voltage v^*_{cap}, and simultaneously commands each capacitor voltage v_{cap1}&v_{cap2}. Finally through three PI regulators and three multipliers, all balance instructions are imported to hybrid PWM with power distribution to participate in reference generation for conditioning converters. By this means, each capacitor voltage can be kept constant. As to grid current control, LCL filter likely endangers the system stability owing to hazardous resonance. So a dual loop controller is adopted to track grid current. It consists of outer grid current feedback loop and inner filter capacitor current regulating loop. Proportional + Resonant (PR) controller is used to follow instantaneous grid current with zero-steady-state error, and P controller is chosen to actively damp resonant peak. Hybrid PWM modulation with power distribution produces average switching functions S1, S2, S5, S6, S9 & S10 to build average model.

In order to access the parameters of the control system, the detail deduction is presented as follows.



(a) AC-side controller diagram

(b) DC-side controller design diagram

Fig.37. Decoupled grid-connected mode control diagram in AC side and DC side

PR for outer loop grid current regulation:

$$PR\_i_g(s) = k_p + k_i \frac{s}{s^2 + \omega_1^2} \tag{11}$$

P for inner capacitor current regulation

$$P\_i_{C_f}(s) = k \tag{12}$$

Inner capacitor current open loop transfer function:

$$G_{op}\_i_{C_f}(s) = \frac{kL_2C_fs}{L_1L_2C_fs^2 + L_1 + L_2} \tag{13}$$

Inner capacitor current closed loop transfer function:

$$G_{cl}\_i_{C_f}(s) = \frac{G_{op}\_i_{C_f}(s)}{1 + G_{op}\_i_{C_f}(s)} = \frac{kL_2C_fs}{L_1L_2C_fs^2 + kL_2C_fs + L_1 + L_2} \tag{14}$$

Outer grid current open loop transfer function:

$$\begin{aligned} G_{op}\_i_g(s) &= (k_p + k_i \frac{s}{s^2 + \omega_1^2}) \cdot G_{cl}\_i_{C_f}(s) \cdot \frac{1}{C_fs} \cdot \frac{1}{L_2s} \\ &= (k_p + k_i \frac{s}{s^2 + \omega_1^2}) \cdot \frac{kL_2C_fs}{L_1L_2C_fs^2 + kL_2C_fs + L_1 + L_2} \cdot \frac{1}{C_fs} \cdot \frac{1}{L_2s} \\ &= \frac{k_pks^2 + k_iks + k_pk\omega_1^2}{L_1L_2C_fs^5 + C_fL_2ks^4 + (L_1L_2C_f\omega_1^2 + L_1 + L_2)s^3 + kC_fL_2\omega_1^2s^2 + (\omega_1^2L_1 + \omega_1^2L_2)s} \end{aligned} \tag{15}$$

Outer grid current closed loop transfer function:

$$\begin{aligned} G_{cl}\_i_g(s) &= \frac{G_{op}\_i_g(s)}{1 + G_{op}\_i_g(s)} \\ &= \frac{k_pks^2 + k_iks + k_pk\omega_1^2}{L_1L_2C_fs^5 + C_fL_2ks^4 + (L_1L_2C_f\omega_1^2 + L_1 + L_2)s^3 + (kC_fL_2\omega_1^2 + k_pk)s^2 + (\omega_1^2L_1 + \omega_1^2L_2 + k_ik)s + k_pk\omega_1^2} \end{aligned} \tag{16}$$

Grid voltage disturbance rejection transfer function:

$$\begin{aligned} &G_{dis}\_v_g(s) \\ &= -\frac{L_1C_fs^4 + C_fks^3 + (L_1C_f\omega_1^2 + 1)s^2 + kC_f\omega_1^2s + \omega_1^2}{L_1L_2C_fs^5 + C_fL_2ks^4 + (L_1L_2C_f\omega_1^2 + L_1 + L_2)s^3 + (kC_fL_2\omega_1^2 + k_pk)s^2 + (\omega_1^2L_1 + \omega_1^2L_2 + k_ik)s + k_pk\omega_1^2} \end{aligned} \tag{17}$$

System transfer function for AC side control:

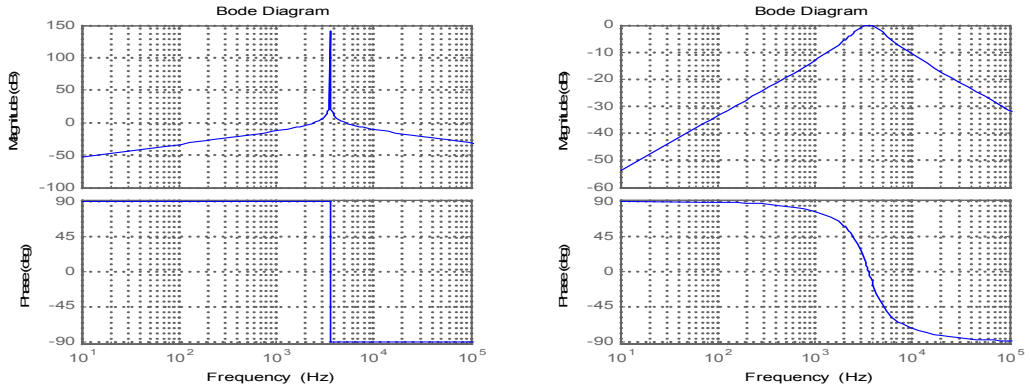
$$i_g(s) = G_{cl\_i_g}(s) i_g^*(s) + G_{dis\_v_g}(s) v_g(s)$$

$$= \frac{k_p k s^2 + k_i k s + k_p k \omega_1^2}{L_1 L_2 C_f s^5 + C_f L_2 k s^4 + (L_1 L_2 C_f \omega_1^2 + L_1 + L_2) s^3 + (k C_f L_2 \omega_1^2 + k_p k) s^2 + (\omega_1^2 L_1 + \omega_1^2 L_2 + k_i k) s + k_p k \omega_1^2} i_g^*(s)$$

$$- \frac{L_1 C_f s^4 + C_f k s^3 + (L_1 C_f \omega_1^2 + 1) s^2 + k C_f \omega_1^2 s + \omega_1^2}{L_1 L_2 C_f s^5 + C_f L_2 k s^4 + (L_1 L_2 C_f \omega_1^2 + L_1 + L_2) s^3 + (k C_f L_2 \omega_1^2 + k_p k) s^2 + (\omega_1^2 L_1 + \omega_1^2 L_2 + k_i k) s + k_p k \omega_1^2} v_g(s)$$

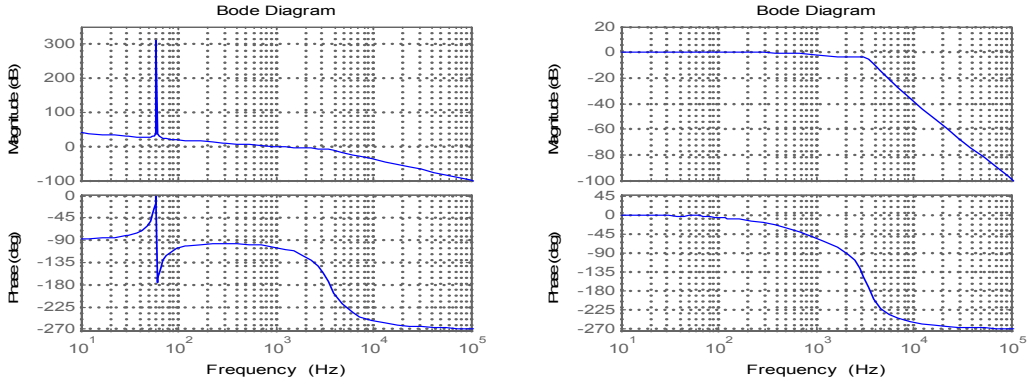
(18)

For L_1=1.2mH, C_f=5.0uF, L_2=0.6mH, controller parameters are selected as kp=0.5, ki=50, k=20. And related frequency plot is shown as follows:



(a) Inner current open loop frequency response (b) Inner current closed loop frequency response

Fig.38. Inner capacitor current loop frequency response



(a) Outer current open loop frequency response (b) Outer current closed loop frequency response

Fig.39. Outer grid current loop frequency response

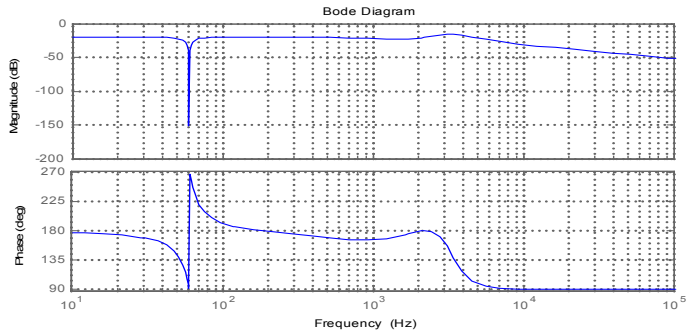


Fig. 40. Grid voltage disturbance rejection capability

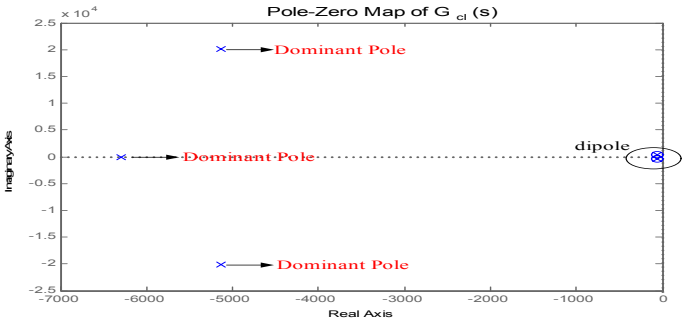


Fig. 41. Pole-zeros placement of closed-loop grid current control

It can be seen from Fig.38 that inner P regulator damps high peak value around resonant frequency introduced by LCL filter, which contributes to improve the system stability. As shown in Fig.39, PR controller holds big phase margin to 77 degree and gain margin to 9.5dB that shows excellent stability. Very huge gain at fundament frequency exhibits precise current tracking in steady state. Wide current bandwidth is obtained to achieve fast response to grid current reference. As depicted in Fig.40, high attenuation at fundamental frequency shows that fundamental grid voltage has slight effect on grid current. Fig.41 indicates that the closed-loop system contains three dominant poles and some dipoles canceled each other.

Reactive power allocation (RPA) Strategy Development

One advantage of cascaded structure is that the dc voltage of each inverter cell can be reduced. However, the reduced dc voltage will affect reactive power generation capability. In order to achieve wide range reactive power compensation, it is desirable to have the reactive power is provided by all the inverter cells instead of a single inverter cell. How to distribute the reactive power among inverter cells is designed based on the proposed RPA strategy.

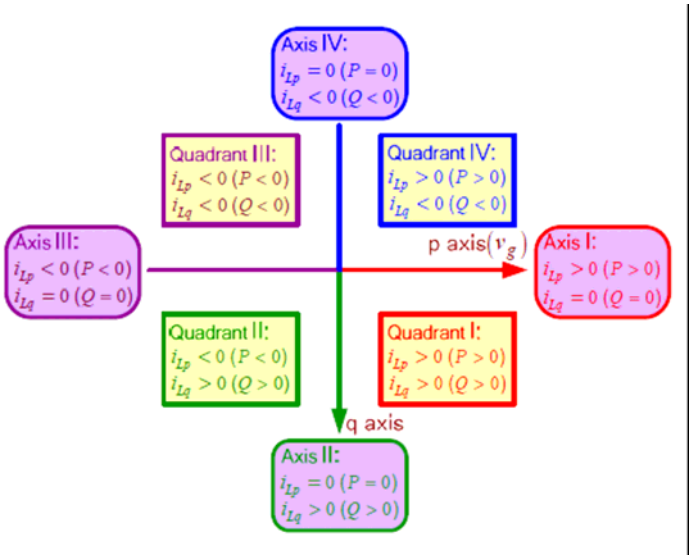


Fig. 42. System power region classification

The *p* axis indicating real power component is fixed in phase with grid voltage, and *q* axis denoting reactive power component lags 90 degree behind p axis. According to such *pq* axis definition, inverter power flow is classified into 4 quadrants and 4 axes as shown in Fig.42. Inductive lagging reactive power is positive, and capacitive leading reactive power is negative. And a wide power region covering quadrant I, IV and axis I, II, IV is investigated.

Unified real/reactive power with unit pu is expressed:

$$P' = \frac{P}{P_{rated}}, Q' = \frac{Q}{Q_{rated}} \tag{19}$$

Fig.43 illustrates vector analysis of RPA strategy. A *p′q′* coordinate is established with a phase shift relative to original *pq* framework. *p′*axis reflecting real power component is fixed in phase with inductor current i_L, and *q′* axis indicating reactive power component leads 90 degree to *p′* axis.

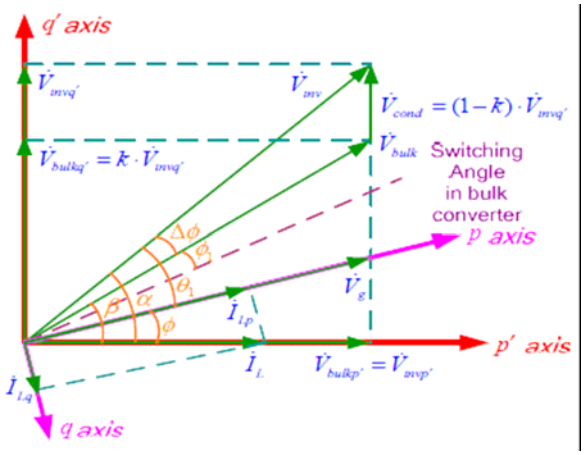


Fig.43. Vector analysis of RPA strategy

k ($0 \le k \le 1$) is defined as reactive power allocation coefficient (RPAC) that implies reactive power weight within converters. At a given k, bulk converter accounts for k of all reactive power, and conditioning converters covers 1-k of that. Thus, bulk converter voltage and conditioning converters voltage can be expressed in the form of $p'q'$:

$$\begin{cases} v_{bulkp'} = v_{invp'} \\ v_{bulkq'} = k v_{invq'} \end{cases}, \begin{cases} v_{condp'} = 0 \\ v_{condq'} = (1-k) v_{invq'} \end{cases} \tag{20}$$

Assume that inductor current is $i_L = I_L \sin \omega_1 t$ and v_{inv} leads α to i_L , then bulk converter voltage can be written as:

$$v_{bulk} = v_{invp'} + k v_{invq'} = V_{invp'} \sin \omega_1 t + k V_{invq'} \cos \omega_1 t = V_{bulk} (\sin \omega_1 t + \beta) \tag{21}$$

B is the leading phase angle of v_{bulk} to $i_{L:}$

$$\begin{cases} \sin \beta = \dfrac{k \sin \alpha}{\sqrt{(\cos \alpha)^2 + (k \sin \alpha)^2}} \\ \cos \beta = \dfrac{\cos \alpha}{\sqrt{(\cos \alpha)^2 + (k \sin \alpha)^2}} \\ \tan \beta = k \tan \alpha \end{cases} \tag{22}$$

V_{bulk} is the fundamental amplitude in bulk converter:

$$V_{bulk} = V_{inv} \sqrt{(\cos \alpha)^2 + (k \sin \alpha)^2} \tag{23}$$

Φ_1 is the first switching angle in bulk converter relative to its fundamental voltage. From (5), the following equation holds:

$$\frac{4V_{dc}}{\pi} \cos \phi_1 = V_{bulk} = V_{inv} \sqrt{(\cos \alpha)^2 + (k \sin \alpha)^2} \tag{24}$$

From (24), 4 switching angles in bulk converter relative to its fundamental voltage are derived with radian unit:

$$\begin{cases} \phi_1 = \cos^{-1}\left(\dfrac{\pi V_{inv}}{4V_{dc}} \sqrt{(\cos \alpha)^2 + (k \sin \alpha)^2}\right. \\ \phi_2 = \pi - \phi_1 \\ \phi_3 = \pi + \phi_1 \\ \phi_4 = 2\pi - \phi_1 \end{cases} \tag{25}$$

$\Delta\Phi$ is the leading phase angle of inverter voltage v_{inv} to bulk converter voltage v_{bulk}:

$$\Delta \phi_1 = \alpha - \beta \tag{26}$$

Considering phase shift $\Delta\Phi$, switching angles relative to inverter voltage v_{inv} are calculated:

$$\begin{cases} \theta_1 = \phi_1 + \Delta\phi \\ \theta_2 = \phi_2 + \Delta\phi \\ \theta_3 = \phi_3 + \Delta\phi \\ \theta_4 = \phi_4 + \Delta\phi \end{cases} \tag{27}$$

Also, the RPA strategy conveyed in above formulae can be illustrated by Fig.44.

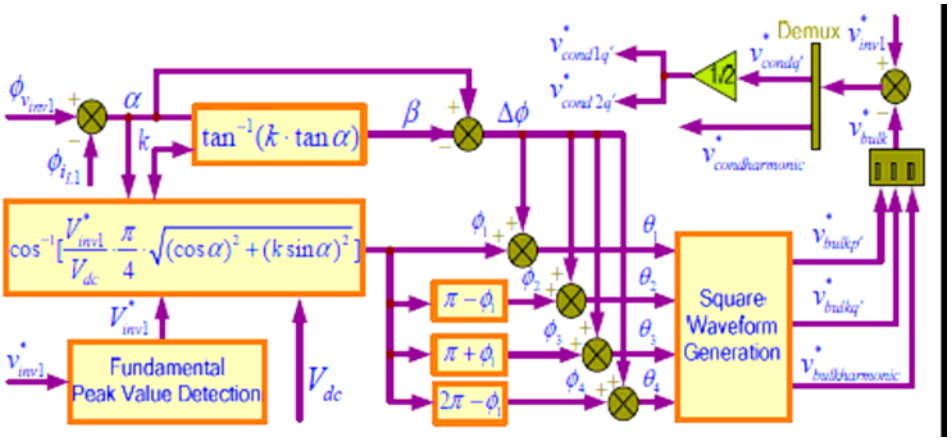


Fig.44. Reactive power allocation strategy diagram

Designed power circuit parameters are summarized into Table 1 that is used for the following analysis.

TABLE I Designed power circuit parameters

Side	Parameter	Symbol	Value
Inverter	DC Bus Voltage	V_{dc}	140 V
	Capacitor Voltage	$V_{cap1,\,2}$	70V
	Capacitance	C_1, C_2	60mF
	Filter Inductance	L_1	1.2mH
		L_2	0.6mH
	Filter Capacitance	C_f	5μF
	Equivalent Resistance	R_{equ}	0.1Ω
	Switching Frequency	f_{sw}	4.8KHz
Grid	Frequency	f_1	60Hz
	Rated RMS Voltage	V_g	120V
	Rated Real Power	P_{rated}	3.5KW
	Rated Reactive Power	Q_{rated}	3.5KVAR

As shown in Fig.45, unified inverter voltage magnitude manifests the total voltage boost capability given in (28):

$$V_{inv}^{'} = \sqrt{\left(V_g + 7000\omega_1 LQ^{'}/V_g\right)^2 + \left(7000\omega_1 LP^{'}/V_g\right)^2} \Big/ V_{dc} \tag{28}$$

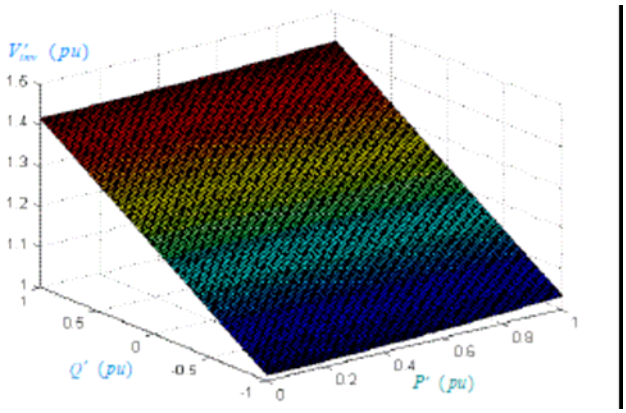


Fig.45. Total voltage boost capability V'_{inv}

As shown in Fig.45, the maximum value of V'_{inv} =1.426pu, which indicates the inverter can realize a considerable voltage boost. Maximum voltage boost reaches 142.6% at rated real power and rated inductive reactive power. This function rewards the inverter with a reduced input voltage.

To avoid saturated operation in bulk converter, RPAC *k* has to be lower than one limit as given in (29) and Fig.46.

$$k_{\lim it} = \sqrt{\left(\frac{4V_{dc}}{\pi}\right)^2 - V_g^2 \frac{P'^2}{P'^2 + Q'^2}} \Bigg/ \left| V_g \frac{Q'}{\sqrt{P'^2 + Q'^2}} + \frac{7000\omega_1 L}{V_g}\sqrt{P'^2 + Q'^2} \right| \qquad (29)$$

From Fig.46, $k_{limit} \geq 0.826$ holds for the whole defined power region, which implies that duty cycle saturation in bulk converter never happens under RPAC $k \leq 0.826$. However, this saturation would appear in partial power area provided that $k > 0.826$.

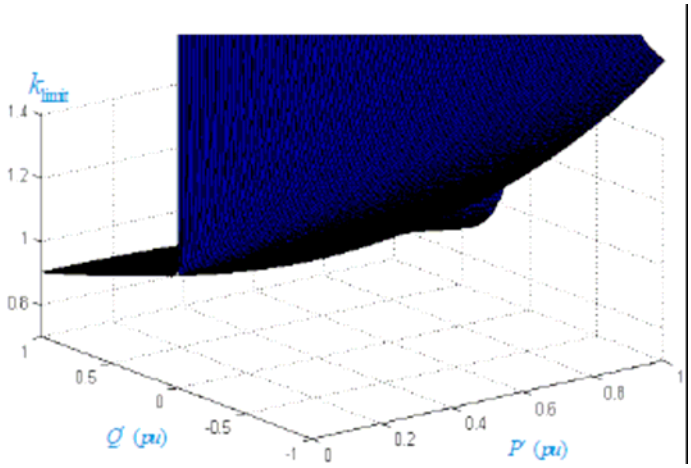


Fig.46. RPAC limit for instauration in bulk converter

For conditioning converters, duty cycle instauration is desired for proper operation. This requires absolute voltage maximum in conditioning converters shouldn't be greater than V_{dc}. Probable absolute maximum arises in switching angles θ1~θ4. Due to the symmetry, candidates of absolute maximum are acquired at θ1 & θ2. All candidates and unified absolute maximum are given:

$$\begin{cases} V_{cond1} = \left| V_{inv} \sin\theta_1 \right|, V_{cond2} = \left| V_{inv} \sin\theta_1 - V_{dc} \right| \\ V_{cond3} = \left| V_{inv} \sin\theta_2 \right|, V_{cond4} = \left| V_{inv} \sin\theta_2 - V_{dc} \right| \end{cases} \tag{30}$$

$$V'_{cond\max} = \max\left(V_{cond1}, V_{cond2}, V_{cond3}, V_{cond4}\right) / V_{dc} \tag{31}$$

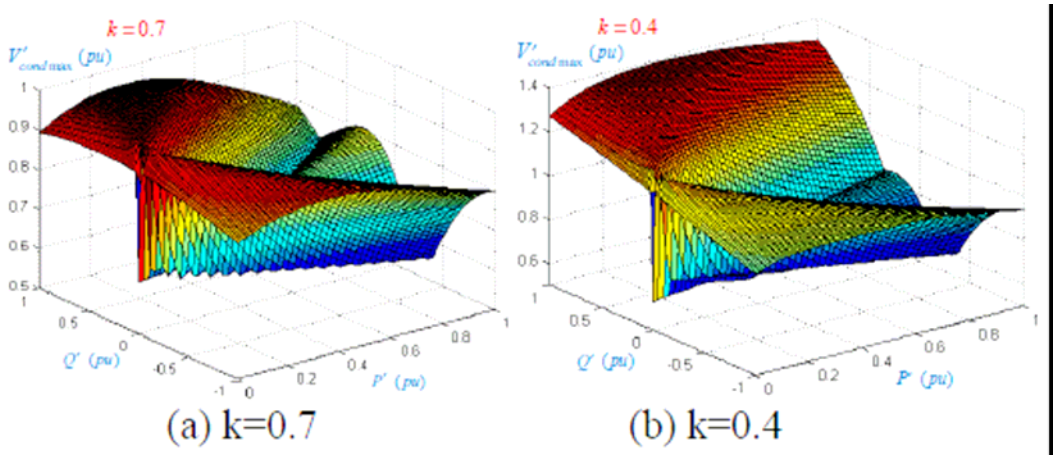


Fig.47. Example of absolute voltage maximum V'condmax

In sum, appropriate RPA strategy requires insaturated duty cycle not only for bulk converter but also for conditioning converters. So the following constraint condition must be met:

$$\begin{cases} \dfrac{\pi}{4} \dfrac{V_{inv}}{V_{dc}} \sqrt{\left(\cos\alpha\right)^2 + \left(k \sin\alpha\right)^2} \le 1 \\ V'_{cond\max} \le 1 \end{cases} \tag{32}$$

Power region satisfying the constraint condition (32) is defined as PQ effective area. Fig.48 describes examples of such areas. From Fig.48 (a), colorful effective area under k=1.0 only covers part of power region. This implies that only bulk converter can't afford all reactive power in some power region, and conditioning converters are indispensable to reactive power supplement. From Fig.48 (b), k=0.8 enables the inverter to work well in any defined power operation point.

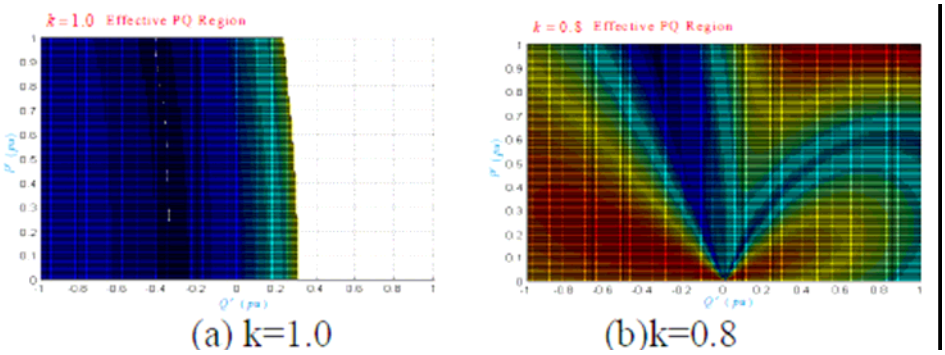


Fig.48. Examples of PQ effective area

System Simulation model building

Main circuit model in PSIM

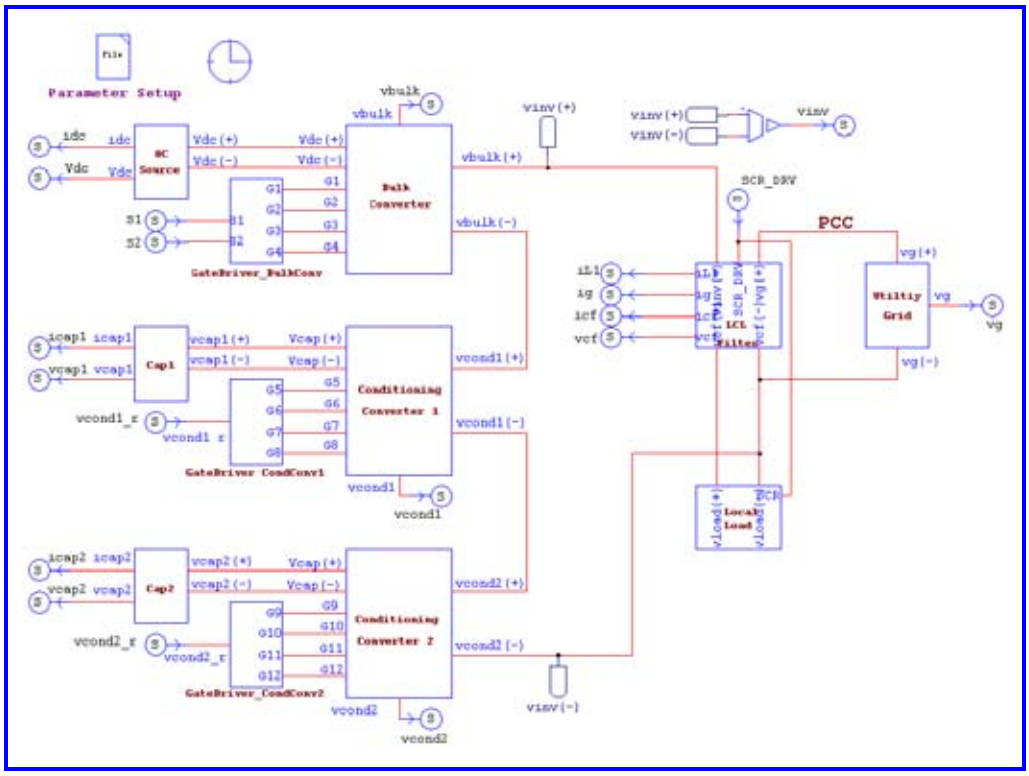


Fig.49 Main circuit system model in Matlab/Simulink

Control system model in Matlab/Simulink

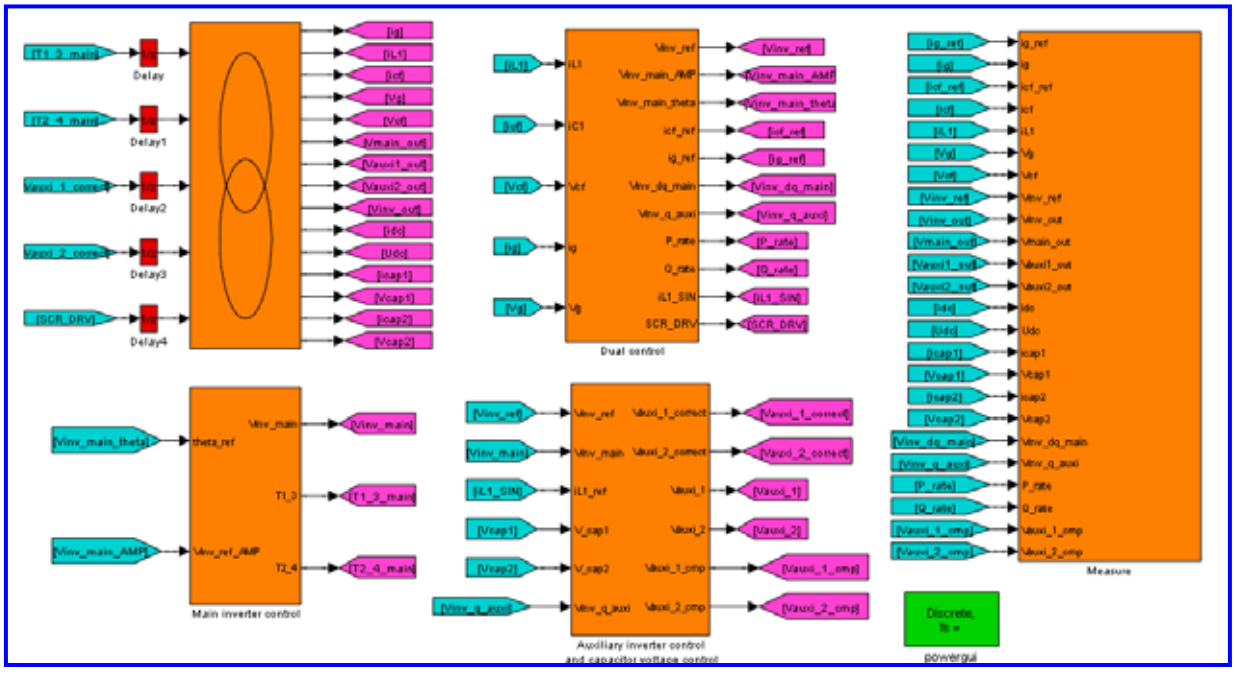


Fig.50. Control system model in Matlab/Simulink

Figures 49 and Fig.50 show the system simulation block diagram respectively where the main circuit is simulated in PSIM and the control system is implemented in Matlab/Simulink. The PSIM simulation software can be integrated with Matlab/Simulink to provide the whole system performance. The main circuit simulation includes multilevel inverter circuit model with filter and their driver model. The control system model includes the interface model to main circuit, bulk inverter control block, conditioning inverters control block and measure block.

Simulation results

The proposed RPA technique for extensive power flow regulation is tested in simulation. The combination of rated real power and different amount of reactive power (large, medium, small) is selected as the demonstration. These cases focus on power quality analysis and the validation of reactive power quota.

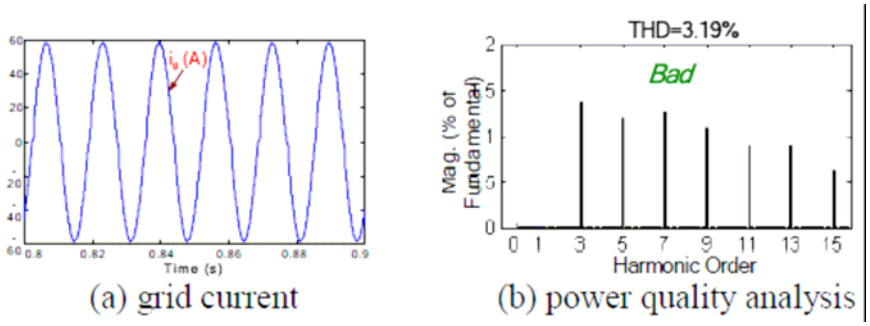


Fig.51. Simulation results with RPAC k=0.4 for rated real power and large reactive power (1.0pu)

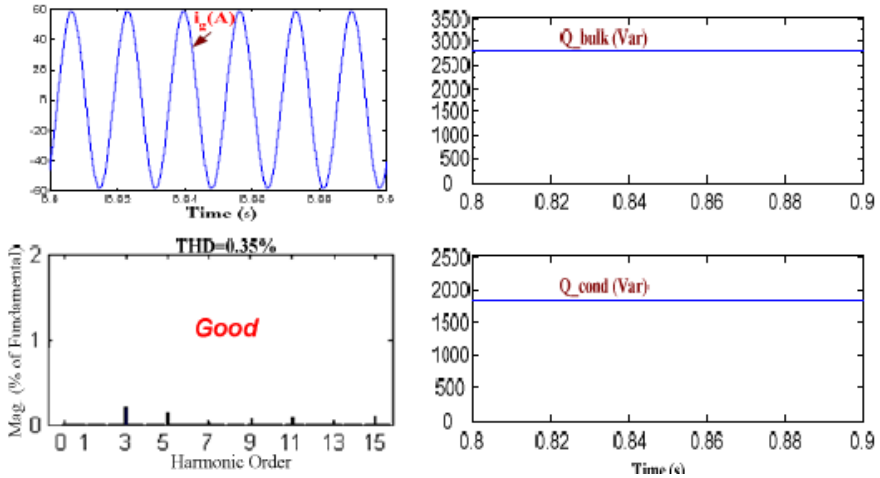


Fig.52. Simulation results with RPAC k=0.6 for rated real power and large reactive power (1.0pu)

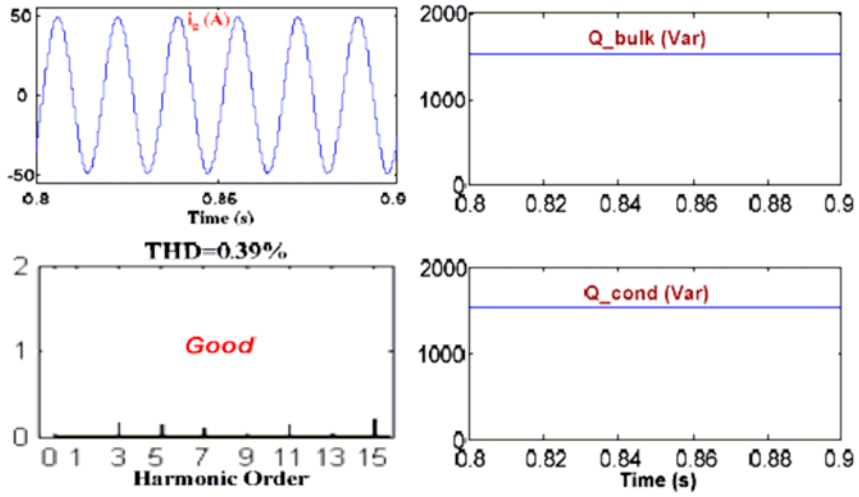


Fig.53. Simulation results with RPAC k=*0.5 for rated real power and medium reactive power (0.65 pu)*

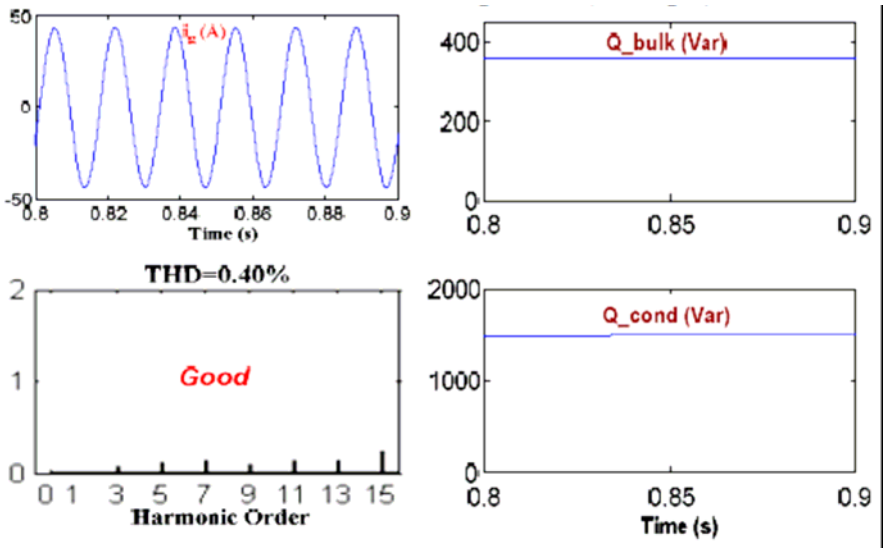


Fig.54. Simulation results with RPAC k=0.2 for rated real power and small reactive power (0.35 pu)

Fig.51 demonstrates that power quality is degraded by low-order current harmonics once k isn't properly chosen. These harmonics are caused by saturated operation of the inverter. Compared to Fig.51, Fig.52 displays good results under the same power point owing to suitable k selection. Also based on rational k selection, Fig.53 and Fig.54 exhibit fine power quality under medium or small reactive power together with rated real power. In addition, it's confirmed from Fig.52~Fig.54 that all reactive power quotas inside the inverter agree with pre-set RPAC k.

Conclusions

- A grid-connected inverter with energy storage system was developed for the small distributed power generation system.
- A novel reactive power allocation strategy was proposed to achieve the wide range power generation.
- The system power flow was analyzed in detail and four quadrants power flow regions were accessed.

- A nonlinear large-signal averaged model for proposed system in stand-alone mode and grid-connected mode was explored to design the controllers and conduct system dynamic simulation.
- A decoupled controller in AC side and DC side of the proposed system was developed based on the developed mode in stand-alone mode to achieve voltage balance of ESS, fast dynamics and zero steady state error
- A decoupled controller in AC side and DC side of the proposed system was developed based on the developed mode in grid-connected mode to achieve fast and smooth real power and reactive power regulation
- A proper reactive power allocation coefficient was selected based on the vector analysis and two critical operation conditions
- A detailed system simulation test bed using Matlab/Simulink and PSIM was constructed including main circuit model and control model investigate different system dynamic scenarios. The simulation results confirmed the effectiveness of proposed power conversion topology and control.
- A controller-in-loop simulation and test arrangement for the proposed system was developed to further verify the performance of the system.
- The proposed DG system with energy storage system can achieve single stage energy conversion and improve the system efficiency.
- The proposed DG system with energy storage system can access wide range real and reactive power compensation, and enhance the system stability and reliability.
- The proposed DG system with energy storage system has low cost due to the transformerless design and higher dc boost ratio due to the cascaded topology and hybrid modulation strategy.
- Short transition time from grid-connected mode to stand-alone mode and minimum voltage fluctuation on the load.
- The proposed methods can be easily applied to multi-bus micro-grid system with least modification

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Simulation-Assisted Advancement of Microgrid Understanding and Applications

(M. Steurer, A. Domijan, J. Langston, O. Faruque, K. Schoder, R. Meeker, A. Islam)

An information survey and review was conducted of several micro grid projects having a sufficiently rich environment of hardware in order to support RTDS simulation activities. Some candidate circuits for study which were initially identified are summarized in Table 2.

Project Name	Location	Description
CERTS Micro Grid	Columbus, Ohio	Three 100 kW microturbines (with 60 kW inverters) and 4 load banks (each with loads of up to 100 kW and 20 kVAR), interfaced to AEP utility system through static switch.
CESI RICERCA DER Test Facility	Milan, Italy	Mix of generation, load, and storage (350kWe, 250kWth)
SCE Avanti circuit of the future	Los Angeles, CA	A 12 kV distribution circuit serving 2000 customers, incorporating new hardware and protection schemes and utilizing high speed, fiber communication.

Table 2. Initial survey of candidate microgrid circuits for simulation

M. Steurer visited CESI RICERCA and the SCE Avanti circuit of the future where he established contact to key personnel. Especially, SCE is very interested to collaborate with FSU on testing a controller for a novel distribution level SVC (d-SVC) soon to be installed on that circuit.

The team also established contact with Joe Eto of the Environmental Energy Technologies Division of the Lawrence Berkeley National Laboratory and Ben Schenkman of Sandia National Laboratories as the key persons for any work in support of the CERTS Micro Grid.

Circuit of the Future and d-SVC

(Collaborators: Christopher R Clarke and Juan Castaneda at SCE, Ted Klimek and Matt Pugh at AMSC)

Southern California Edison (SCE) operates the "Circuit of the Future", a 10 MVA rated 12 kV distribution circuit powering approximately 1,500 customers in SCE's service territory in San Bernardino County, CA. The circuit has been specifically adapted to facilitate field-testing of novel distribution class devices such as fault current limiters, advanced protection and metering, and reactive voltage support. SCE is in the process of installing and commissioning a new device for reactive voltage support developed by American Superconductors (AMSC) called dSVC. The dSVC is a self-contained, air-cooled Static VAR Compensator designed for use on underground distribution systems. This project presented an excellent opportunity to evaluate how to employ the controller-hardware-in-the-loop (CHIL) method for the de-risking of installation and commissioning of such a novel device on the grid.

Therefore, a working relationship was established with Southern California Edison (SCE) aimed at modeling the SCE "Circuit of the Future". As a result, CAPS received a notional representation of the circuit from SCE suitable for unrestricted work within this project. The circuit representation was provided by SCE in form of a PSCAD/EMTDC model depicted in Figure 55.

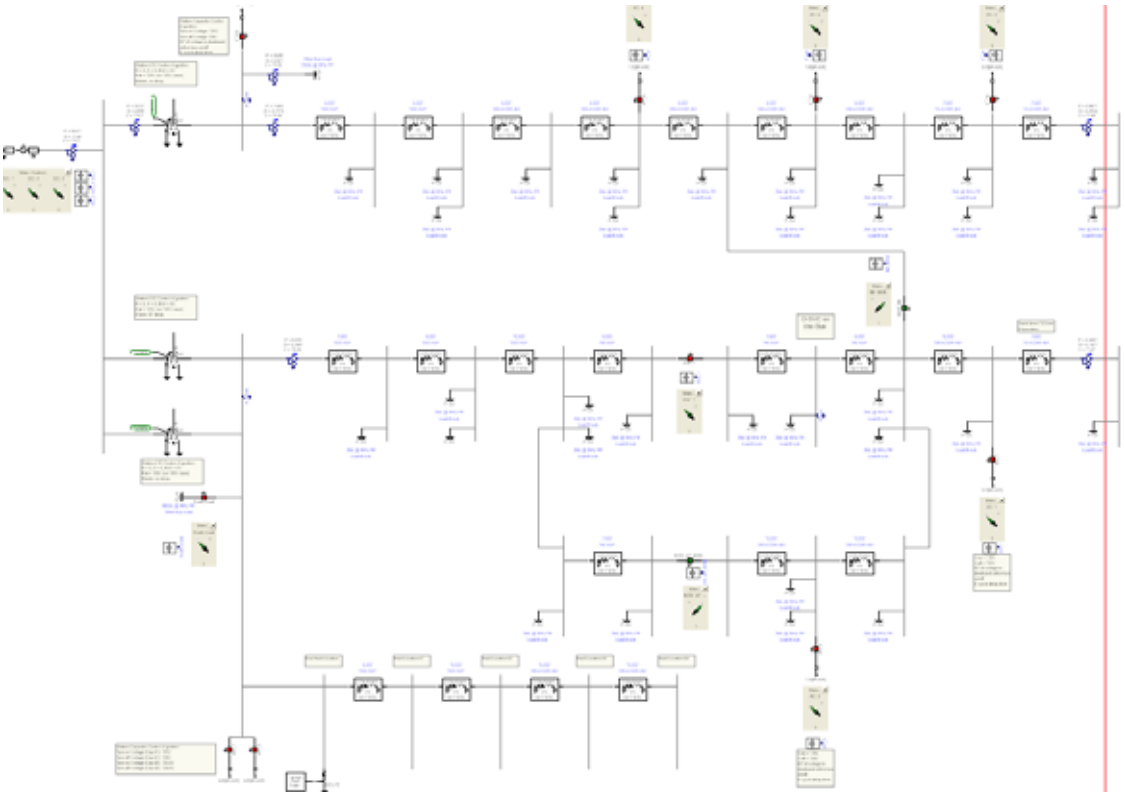


Fig. 55: Notional representation of SCE's "Circuit of the Future"

In addition, a PSCAD/EMTDC model of the dSVC from AMSC was received by CAPS, which provided the necessary details to allow porting the model into RTDS.

The next steps in the project are to

- Implement a representative version of the system depicted in Figure 55 and the dSVC in RTDS
- Revive the dSVC controller an commission the CHIL setup at CAPS
- Develop a test plan together with SCE and AMSC
- Conduct test according to the plan and report the findings

In cooperation with Southern California Edison (SCE) and American Superconductor (AMSC), the controller for a distribution level static VAR compensator (dSVC), associated with the Avanti distribution circuit of the future project, was tested using hardware-in-the-loop experimentation. The intent of this effort was to test the dSVC controller in a realistic environment before the dSVC was deployed in Southern California Edison's (SCE) system.

For the dSVC controller HIL testing project, a PSCAD model of the dSVC was provided by American Superconductor (AMSC), the developer of the dSVC, and this model was implemented for RTDS, the real-time simulator to be employed for the testing. A PSCAD model of a notional distribution circuit, providing some representative characteristics of SCE's "circuit of the future," was provided by SCE. However, as the circuit provided by SCE contained too many busses to be represented within a single subsystem in RTDS and no transmission lines of sufficient length to provide decoupling were present, the system was reduced to allow for real-time implementation. The reduced system that was actually implemented is illustrated in Figure 56. While simplified from the originally proposed circuit, this system

provides a flexible environment in which to the exercise the dSVC and study it's interaction with other voltage controls in the system including capacitor banks and transformer tap changers. This simulation model also provides the ability to study the response of the dSVC to voltage sags induced by faults in the system.

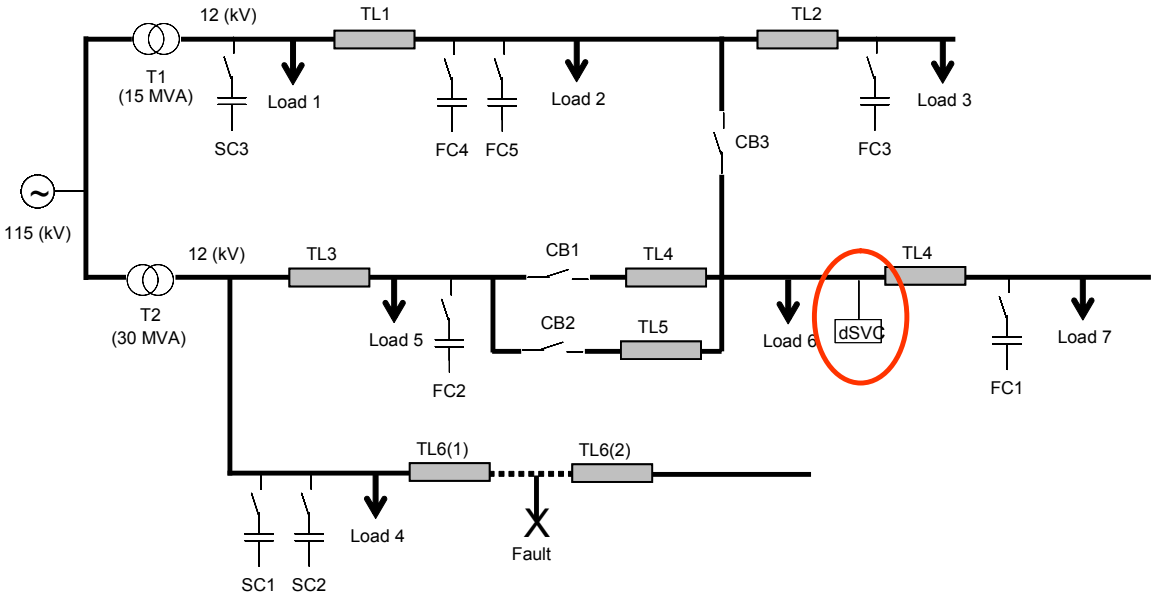


Figure 56. Notional Distribution System for HIL Testing of dSVC Controller

The actual controller to be used with the dSVC was delivered to the Center for Advanced Power Systems (CAPS) and interfaced to the RTDS system, the platform on which the real-time electromagnetic transient simulation of the dSVC and utility system was implemented. The setup is illustrated in Figure 57.

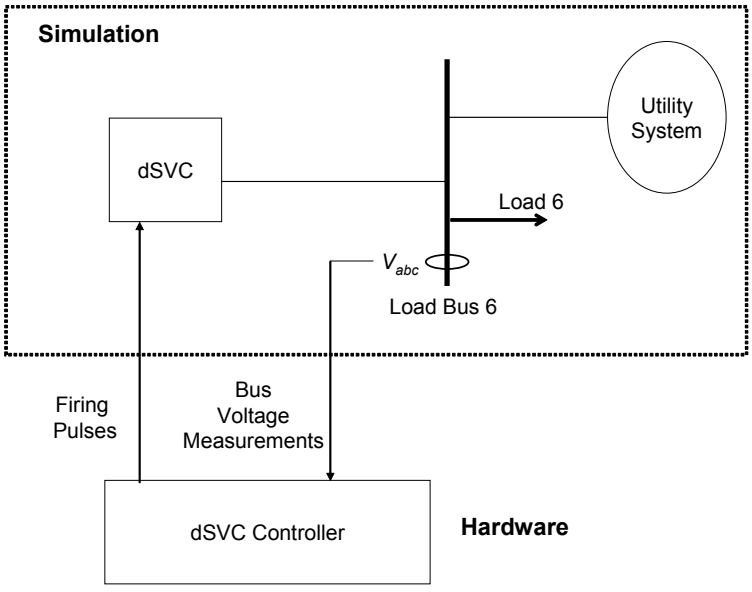


Figure 57. Hardware-in-the-Loop (HIL) Setup

Once interfacing issues were resolved, tests based on a test plan developed by SCE were scripted for execution, and over 500 tests were carried out over a period of a week. The tests included slow ramps of loads for different system conditions and configurations and for scenarios in which short circuit faults were applied in the system at different locations and for different durations. Figure 58 shows results from one of the fault tests, illustrating the RMS voltage at Load Bus 6 for a 10-cycle fault applied at 25% of the line length of transmission line TL6. As expected, the dSVC provides voltage support throughout the voltage sag and ceases voltage support once the bus voltage is back within the dead band region.

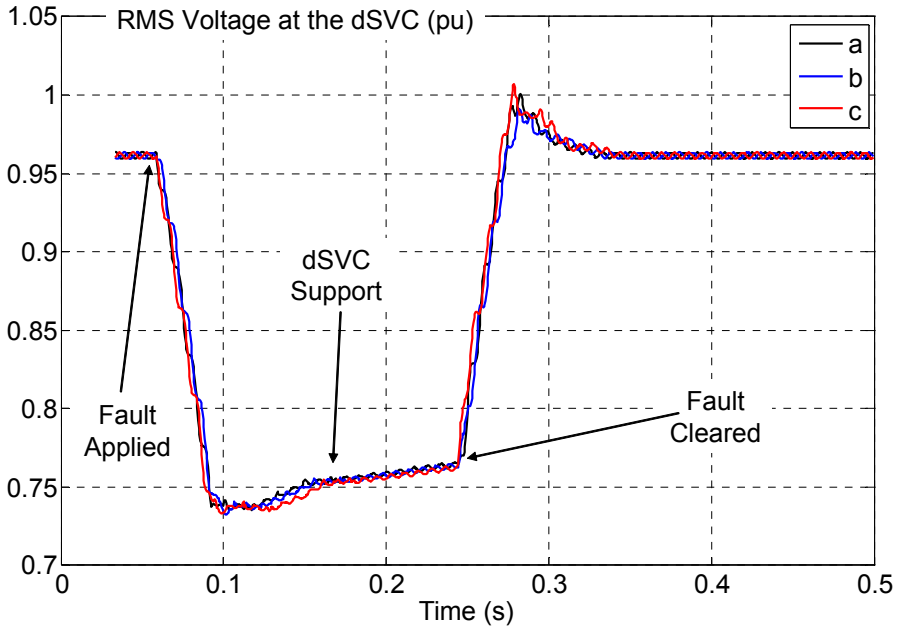


Figure 58. RMS Voltages at Load Bus 6 for a 10 Cycle Fault

In addition to the tests with the system of Figure 56, some tests were also conducted with the system illustrated in Figure 59. This system includes variable source impedance and capacitors for boosting the system voltage at the load. In this case, the load is modeled as a large induction machine, and, depending on the system impedances and loading, the system may have difficulty recovering from voltage sags. Tests were performed to assess the ability of the dSVC to mitigate such problems with systems involving significant induction machine loading. Figure 60 shows results from two of the tests with this system in which a three second fault is applied. In one case, without the compensation of the dSVC, the system is not able to recover from the voltage sag. However, with the dynamic reactive power compensation of the dSVC, the system is able to ride through the voltage sag and recover, illustrating the value of dynamic compensation in such cases. At the conclusion of the testing period, the dSVC controller was sent to SCE.

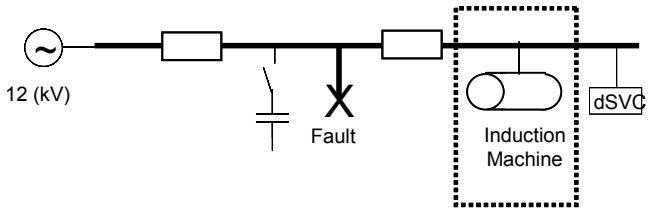


Figure 59. Notional System for Testing dSVC Performance with Induction Machine Loads

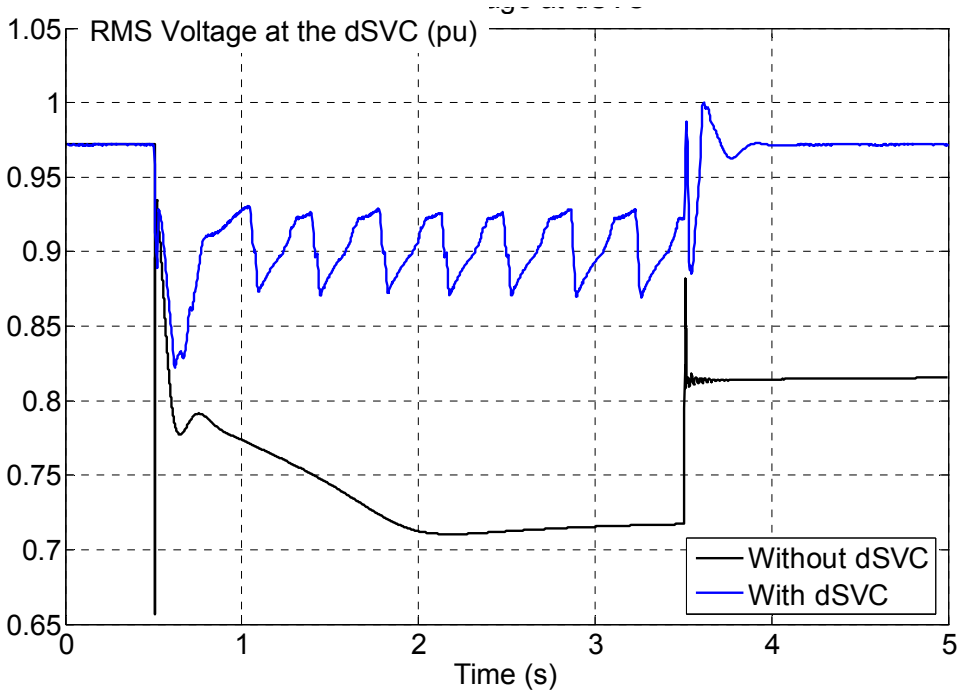


Figure 60. Results from Tests with Induction Machine Loads Illustrating the System Behavior With and Without the Reactive Power Compensation of the dSVC

Distributed Energy Storage System (DESS) Testing and Characterization

(T. Chiocchio, J. Hauer, M. Steurer, FSU CAPS; in collaboration with V. Beaston and M. Chen-Young, of Greensmith, and USF PCUE)

In collaboration with the Power Center for Utility Explorations (PCUE) at the University of South Florida (USF), FSU CAPS worked with GreenSmith Energy Management Systems ("Greensmith"), a developer of Lithium-Ion battery systems, to facilitate a power-hardware-in-the-loop (PHIL) test program of one of GreenSmith's prototype distributed energy storage systems (DESS) at CAPS. These tests evaluated the battery system for application in the Sustainable Electric Energy Delivery Systems (SEEDS) installation project within the Progress Energy Florida (PEF) distribution system in St. Petersburg, FL. Steps in carrying out this testing initiative included:

- Develop a test plan jointly with USF and GreenSmith
- Facilitate the PHIL interface according to the GreenSmith system requirements
- Temporarily install and commission the GreenSmith battery in the CAPS laboratory for testing
- Carry out testing according to the plan

The automatic algorithm in the battery's energy management system was updated in order to optimize the battery operation. The aging effects on the battery parameters were studied to establish a prediction model.

Background

The goal of this effort is to test various aspects of a 5kW distributed energy storage system (DESS) (Figure 61), supplied by Greensmith and intended for installation in the Progress Energy Florida (PEF) distribution system in St. Petersburg, FL.

The testing of the DESS is comprised of two basic categories: IEEE 1547 [1][22] testing and system modeling / characterization testing. IEEE 1547 tests are concerned with the interconnection of the DESS to the grid. It should be noted that this testing is a sample of the testing required by IEEE 1547 and is not meant to be a rigorous testing of the device.

Figure 61. Greensmith Distributed Energy Storage System (DESS)

Unit under Test (UUT)

The DESS was sent to FSU CAPS by the University of South Florida (USF) to test the basic capabilities of the unit. Greensmith, USF and CAPS all agreed that the unit should be tested according to IEEE 1547 and that unit should be characterized about its nominal rating.

The DESS is a low voltage (single phase, 220 V rated) distribution system level battery energy storage system. It consists of a battery pack of 15 cells of lithium-ion iron phosphate (LPF) batteries, two inverters and two chargers. The LPF batteries are rated at 400Ah and connected in series for a possible voltage range of 37.5 V – 63.75 V. The DESS' control, however, limits the voltage range to about 44 V – 49.5 V during discharging and about 49 V-56 V during charging. The pair of inverters shares the load when the batteries are discharging more than 60 A. Their total rated current is 120 A, and, the maximum DC power is, therefore, about 6 kW. Similarly, the chargers share the power with high charging currents. The maximum input charging current per charger is 16 A RMS. More information about the Greensmith system is available at http://greensmith.us.com/product.html.

CAPS low power PHIL testing Facilities used in this project

The DESS is connected to the grid directly and through power hardware in the loop testing. The direct connection is at 3-phase 208 V. This connection is used for part of the IEEE 1547 testing and all of the modeling / characterization testing.

Power Hardware in the Loop Testing

Power hardware in the loop aims to test a device apart from its system as if it is in the system, under realistic dynamic conditions at the power terminals of the device, in full interaction with a high-fidelity simulation of the target system. The system model to be run as a computer simulation is interfaced with the unit under test (UUT), generally as shown in Figure 62.

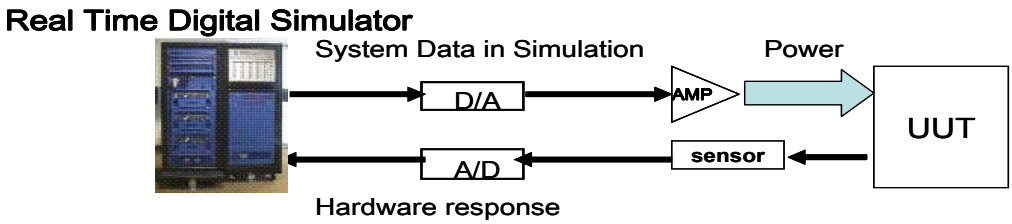


Figure 62. Power Hardware in the Loop (PHIL)

The device is provided an amplified voltage according to the voltage of the device in simulation. The device's representation in simulation is then a current source according to the measured current of the device. This interface provides a closed loop between hardware and simulation.

The power hardware in the loop (PHIL) test setup for the DESS is similar to Figure 62. The DESS is connected to a simulated grid using the real-time digital simulator (RTDS) and using a switched mode AC-DC-AC converter, which acts as an amplifier during charging and current sink during discharging. The PHIL test setup is used only to test the response of the DESS to abnormal grid conditions. The clearing times of the DESS are only tested during discharge when it is considered to be a DR. The hardware setup is depicted in Figure 63. The RTDS provides the voltage reference for the converter.

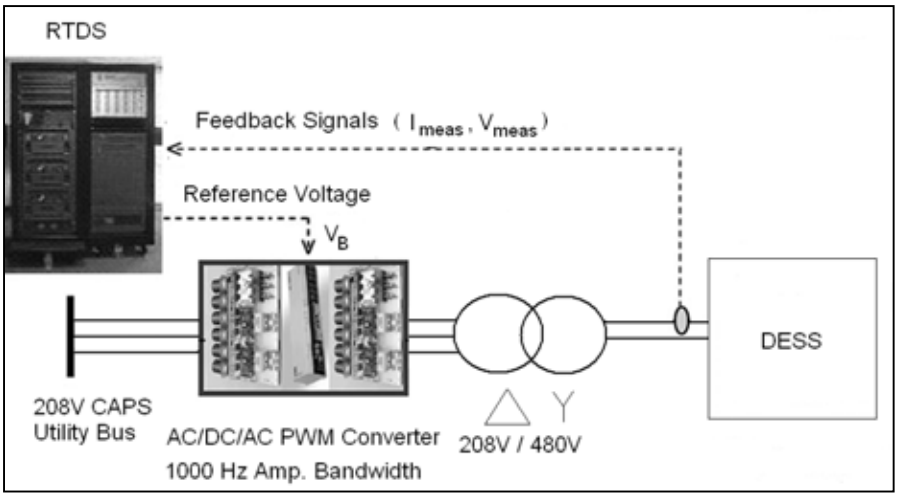


Figure 63. Test Hardware Configuration

Summary of Results

The goal of this effort is to test various aspects of the distributed energy storage system (DESS) by Greensmith. The testing of the DESS is comprised of two basic categories: IEEE 1547 testing and system modeling / characterization testing. IEEE 1547 tests the interconnection of the DESS to the grid. It should be noted that this testing is a sample of the testing required by IEEE 1547 and is not meant to be a rigorous testing of the device. The interconnection of the DESS meets the specifications of IEEE 1547-2003 [1] in all cases except one. While the the clearing time met the IEEE 1547 requirement when the frequency was stepped up or down, the clearing time did not meet the requirement in the case of ramping up and ramping down in source frequency. The reason that DESS does not clear in time during a ramp in frequency could be that ramp is too slow for the DESS to quickly detect the change in frequency.

The steady state behavior of DESS has been characterized. The unit can be modeled on the DC side as a variable voltage source in series with a variable resistance. The voltage and resistance depend on the state of charge of the battery. The AC side would then be a power source with its power proportional to the DC power. The DESS has been tested to assure that unit neither excessively charges nor discharges the battery. The maximum discharge and charge power are estimated.

IEEE 1547 Testing

The DESS is a distributed resource since it is capable of supplying power to the grid when discharging and it should be tested according to [1] and [22]. IEEE 1547-2003 [1] provides an overview of

interconnect tests as well as the specifications for an acceptable test result. IEEE 1547-2005 [22] provides details about the interconnection tests.

Response to Abnormal Grid Conditions

The DESS may be subject to abnormal grid conditions and its response should be tested and clearly understood. The inverters of the DESS check the voltage and frequency and discontinue discharging if the grid is out of their allowable limits. The inverters' grid voltage lower and upper limits are programmable from 180 V-220 V and 225 V-265 V. IEEE 1574 specifies the maximum clearing times that all distributed resources should require to disconnect from the grid in the cases of voltage and frequency deviations beyond allowable limits. The specified limits are shown below in Table 3 and Table 4.

Voltage Range (pu)	Maximum Clearing Time (s)
V < 0.50	0.16
0.50 < V < 0.88	2.0
1.10 < V < 1.20	1.0
V > 1.20	0.16

Table 3. Voltage Deviation Clearing Times from [1]

Frequency Range (Hz)	Maximum Clearing Time (s)
f < 59.3	0.16
f > 60.5	0.16

Table 4. Frequency Deviation Clearing Times from [1]

The harmonic distortion of the simulated voltage needs to be less than 2.5% according to Section 4.6.1 of [22]. The voltage waveform and a table of the harmonic distortion are provided in Figure 64 and Table 11 where the peak fundamental voltage is 341.8 V. The voltage THD is calculated to be about 2.0 %. The sampling rate is 25 kHz.

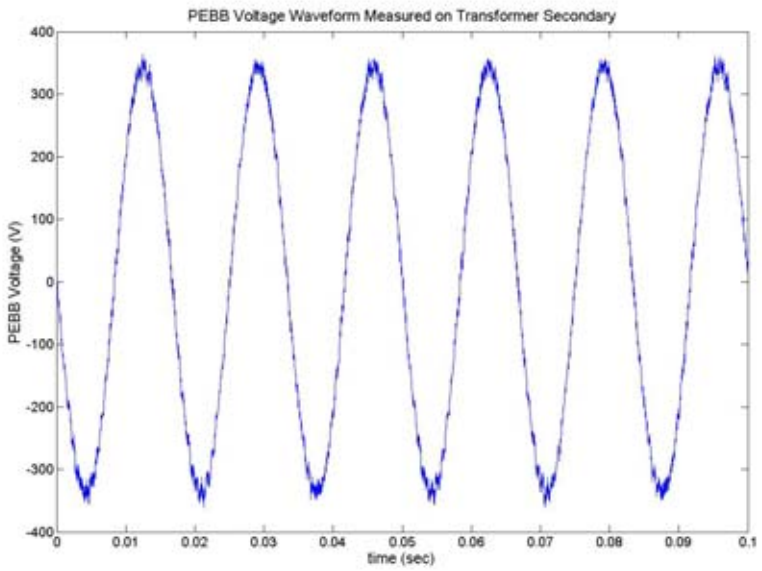


Figure 64. Amplifier (PEBB) Voltage Waveform

The DESS is subjected to steps and ramps in voltage and frequency to tests the clearing times.

The DESS Response to Step Changes in Source Voltage & Frequency

The DESS is provided a simulated voltage through the hardware configuration of Figure 63. The PEBB provides a voltage that the DESS perceives as the grid. The difference between this scenario and an actual connection to the grid is the relative high impedance between the converter and the DESS. The result of this impedance is that the unit must significantly increase its voltage (about 30 V) in order to discharge its nominal current. DESS is tested by stepping down the voltage below the threshold and by stepping up the voltage above the threshold. The base voltage in these tests is 250 V. The grid voltage lower and upper limits are set to 220 V and 265 V. The frequency is also stepped up and down as the voltage. The grid frequency lower and upper limits are set to 59.3 Hz and 60.5 Hz.

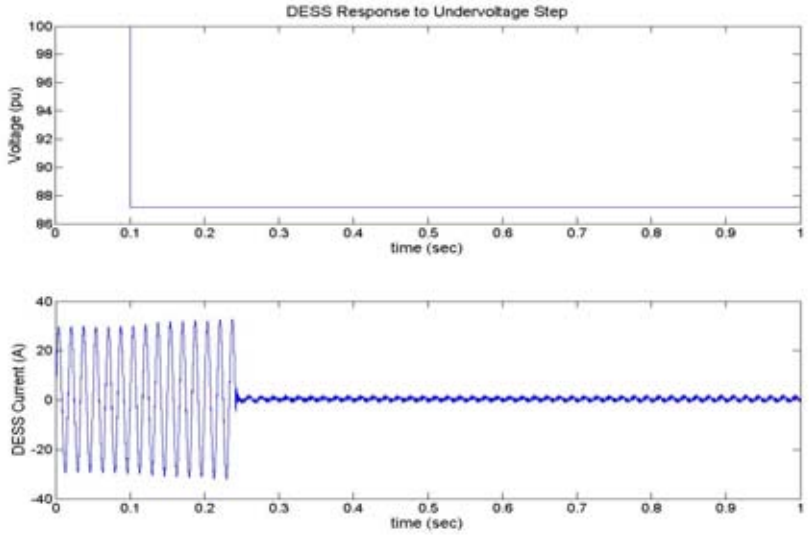


Figure 65. Under-voltage Trip

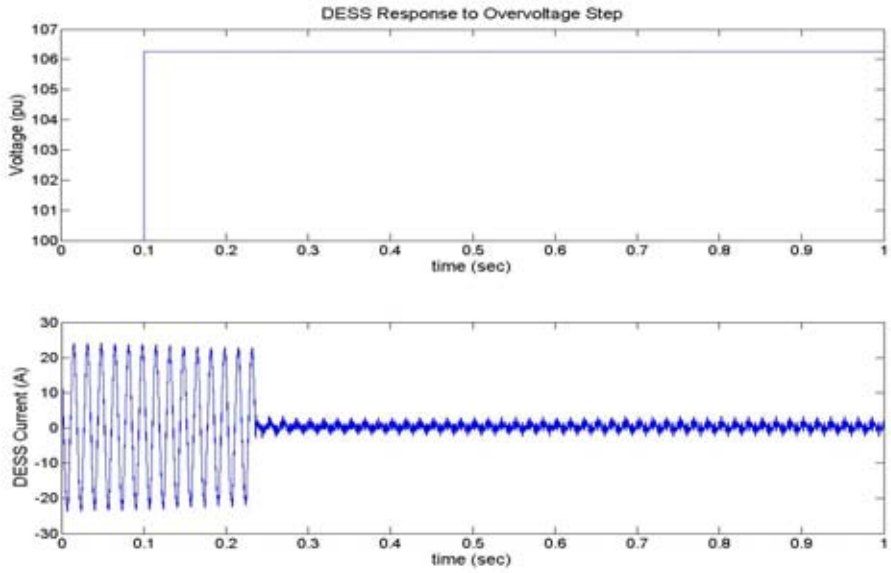


Figure 66. Over-voltage Trip

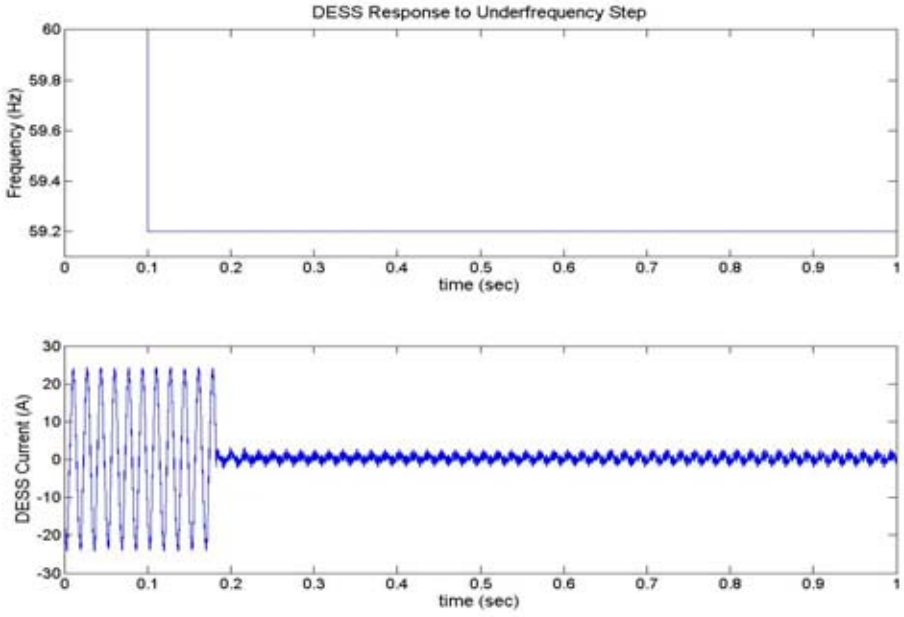


Figure 67. Under-frequency Trip

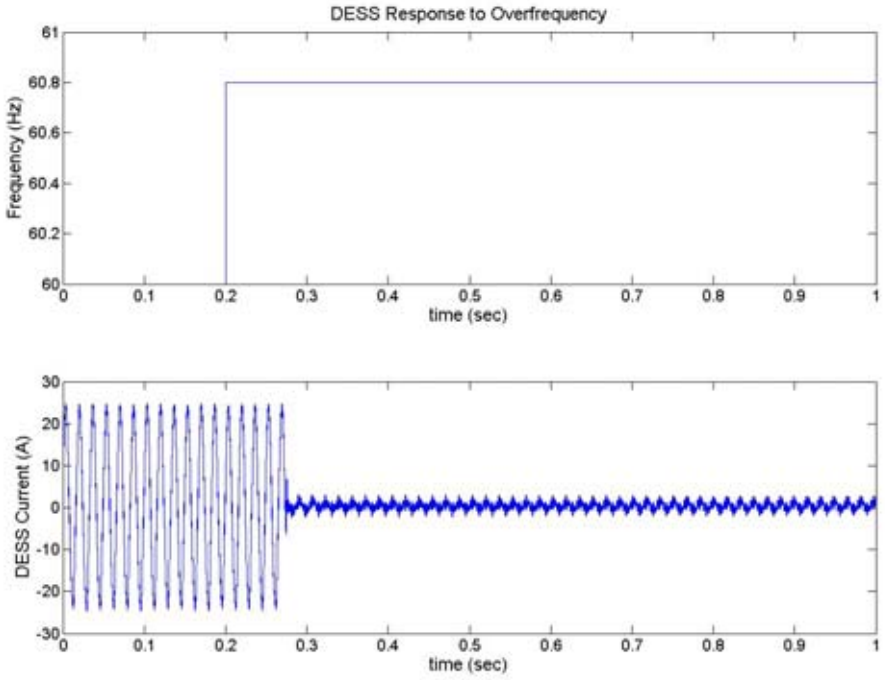


Figure 68. Over-frequency Trip

The DESS Response to Ramps in Source Voltage and Frequency

As before, the AC-DC-AC converter provides a voltage that the DESS perceives as the grid. Additionally, the simulation incorporates a PI-based voltage control that maintains a set voltage at the DESS. DESS is tested by ramping down the voltage at a rate of 3.71 V/s until it reaches the lower threshold and then by ramping up the voltage at a rate of 3.14 V/s to the upper threshold. The base voltage in these tests is 220 V. The grid voltage lower and upper limits are set to 194 V and 242 V. The frequency is also ramped up and down as the voltage. The ramp rate in both cases is 0.14 Hz/s. The grid frequency lower and upper limits are still set to 59.3 Hz and 60.5 Hz.

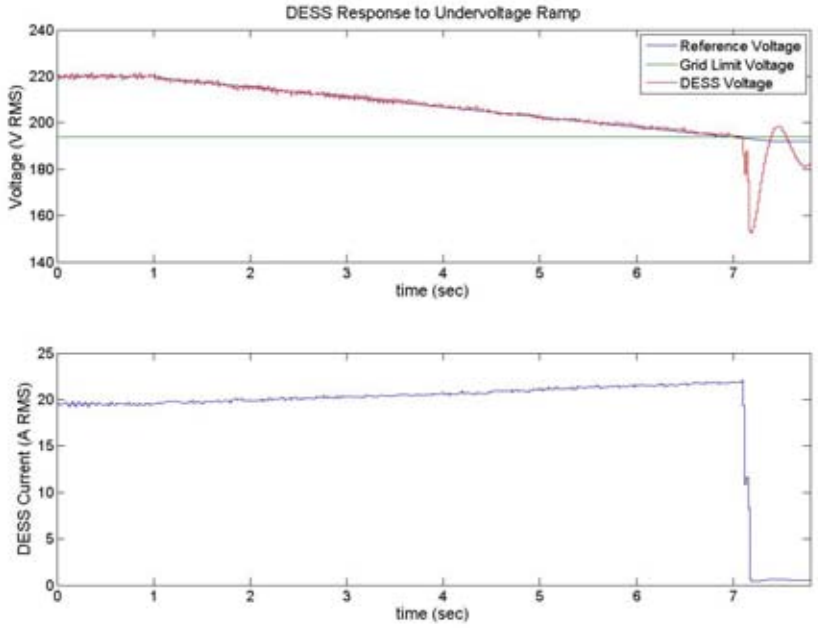


Figure 69. DESS Response to Under-voltage Ramp

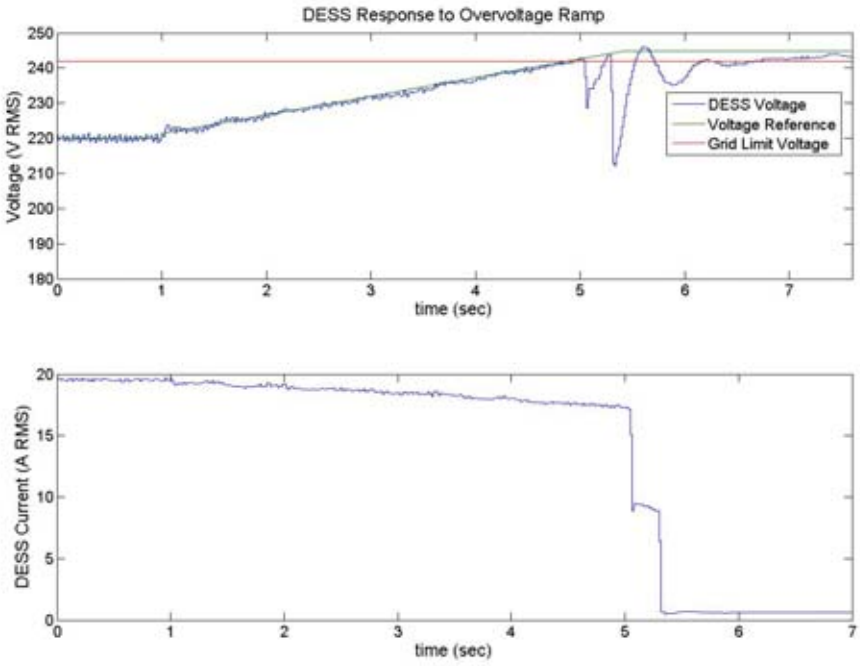


Figure 70. DESS Response to Over-voltage Ramp

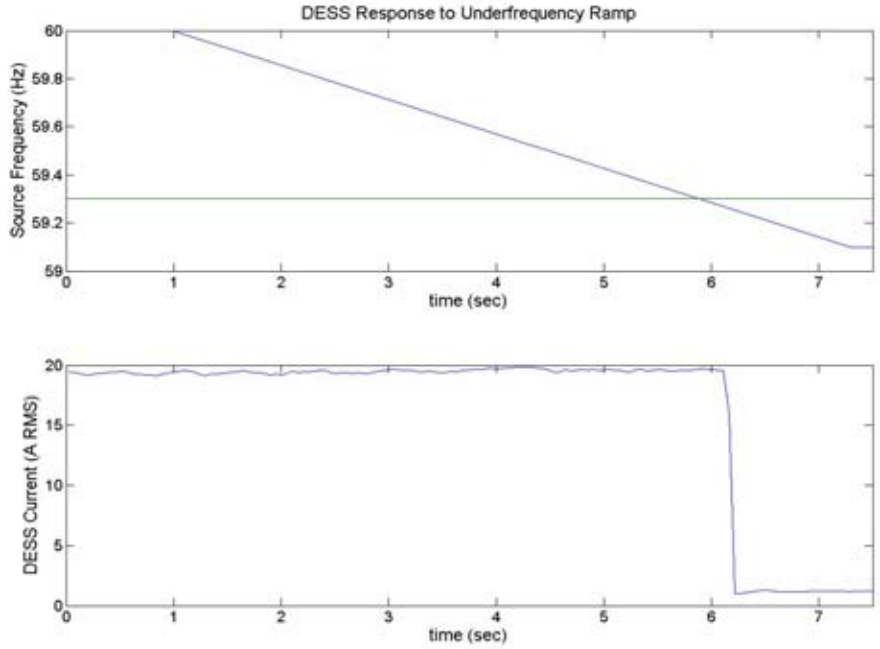


Figure 71. DESS Response to Under-frequency Ramp

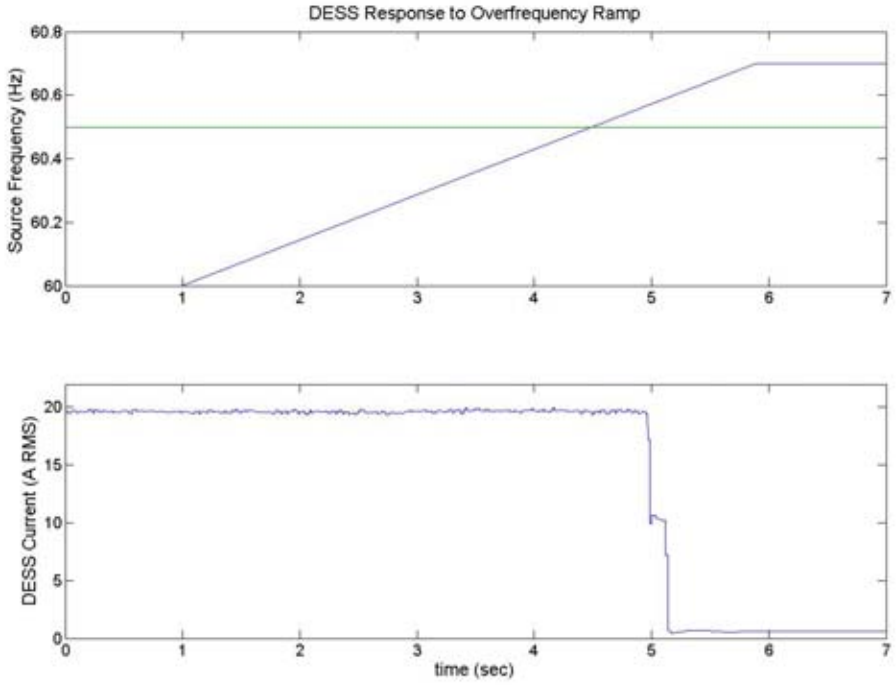


Figure 72. DESS Response to Over-frequency Ramp

Test Type	Input Type	Clearing Time (ms)	Passed Test (Y/N)
0.5 pu < V < 0.88 pu	Step	143.6	Y
1.1 pu < V > 1.2 pu	Step	135.5	Y
f < 59.3 Hz	Step	82.3	Y
f > 60.5 Hz	Step	76.0	Y
0.5 pu < V < 0.88 pu	Ramp	89.0	Y
1.1 pu < V > 1.2 pu	Ramp	340.0	Y
f < 59.3 Hz	Ramp	321	N
f > 60.5 Hz	Ramp	640	N

Table 5. Summary of Response to Abnormal Grid Tests

The DESS clearly passed the test in most of the cases. It did not appear to pass the test in the case of a ramp in frequency. The clearing time in general is measured from when the converter reference reached the threshold to when the DESS had less than 2 A of current. The clearing time may be off if the converter frequency poorly tracks the frequency reference. A high resolution recording was done in the case of over-frequency in order to check the tracking of the source frequency. The sampling rate is at 25 kHz. The results show that calculated frequency tracks the reference frequency well. It is expected that DESS would have problems responding in time if the frequency rate were too slow because of the resolution of the unit's frequency measurement. The frequency ramp rate, however, is quite reasonable at 0.14 Hz/s.

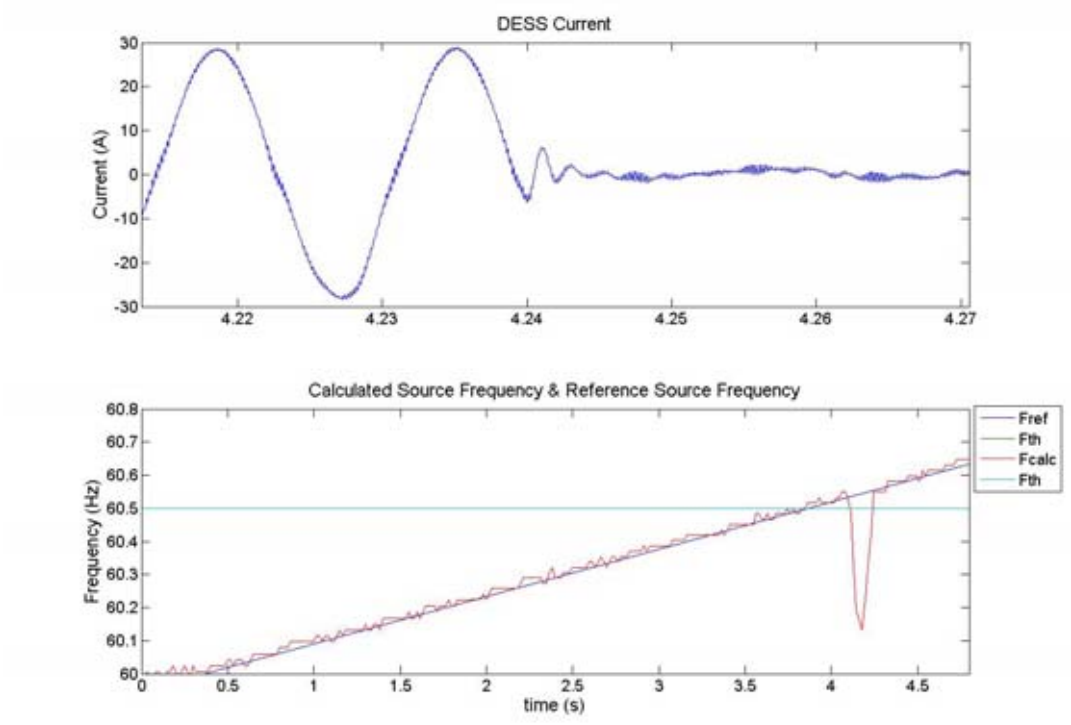


Figure 73. Calculated Source Frequency vs. Reference Frequency

Synchronization

The startup or inrush current drawn by the DESS is shown in 74. The peak startup current is 4.78 A, which is only 13 % of the unit's rated current. The sample rate of the capture is 2 kHz or 33.33 samples per cycle.

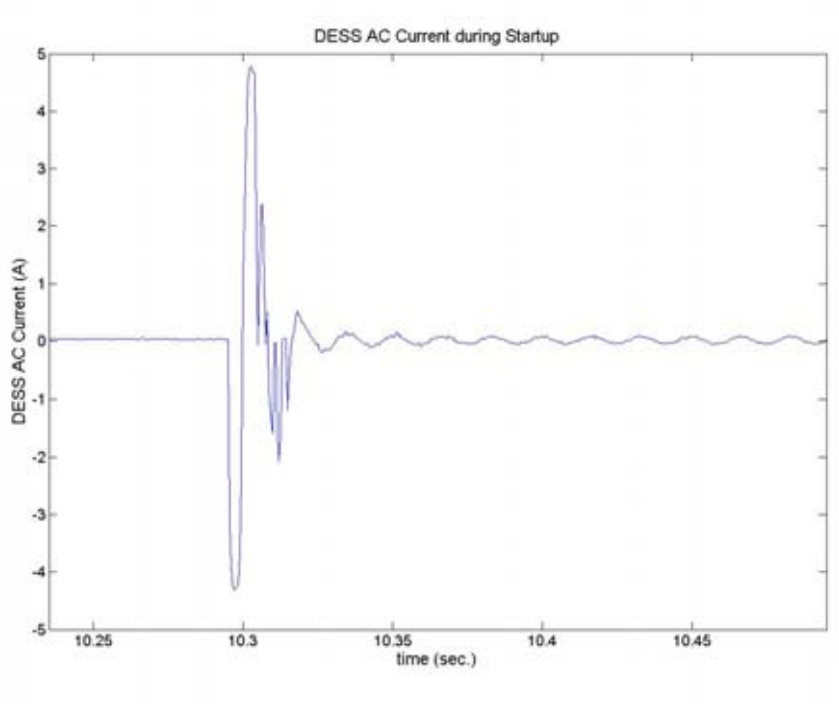


Figure 74. Startup Current

Harmonics

IEEE 1547 [1] requires that the current harmonic content of the first 40 harmonics of the distributed resource (DR) be within certain limits. The harmonics are converted into percentages by dividing by the rated current of the DR. The rated current of the distributed energy storage system (DESS) is calculated as follows:

$$I_{rated,pk} = \frac{P_{rated} * \eta_{inv}}{V_{rated,RMS} * \sqrt{2}} = \frac{6000W * 0.95}{220V * \sqrt{2}} = 36.64A$$

The sample rate is 40 kHz. The harmonics are measured at 30.3 A, 20.7 A and 11.8 A. All of the harmonics are within the specified limits except the 23rd harmonic at 11.8 A. The results are displayed in Table 12.

DC Current Injection

The DC current injection of the DESS is evaluated at 4518 W, 3043 W and 1737 W. The RMS voltage and current and as well as the DC component of the current are recorded every 10 cycles or 166.7 ms at

each of the power levels. The average value of the RMS and DC components are given in Table 6. The DC component should be below 0.5 % of the rated current of 36.64 A.

	Avg. RMS Current (A)	Avg. DC Component (A)	Avg. DC Comp. (%)	Avg. RMS Voltage (V)
4518 W	21.51	0.050	0.14	210.09
3043 W	14.53	0.103	0.28	209.45
1737 W	8.30	0.179	0.49	209.29

Table 6. Average of DC Current Injection Test Values

DESS Modeling & Characterization

Introduction

The steady state behavior of distributed energy storage system (DESS) can be modeled as shown below in Figure 75. The equivalent series resistance and open circuit voltage are functions of the state of charge (SOC) of the battery. The average model converter component provides AC current while accounting for the efficiency of the converter.

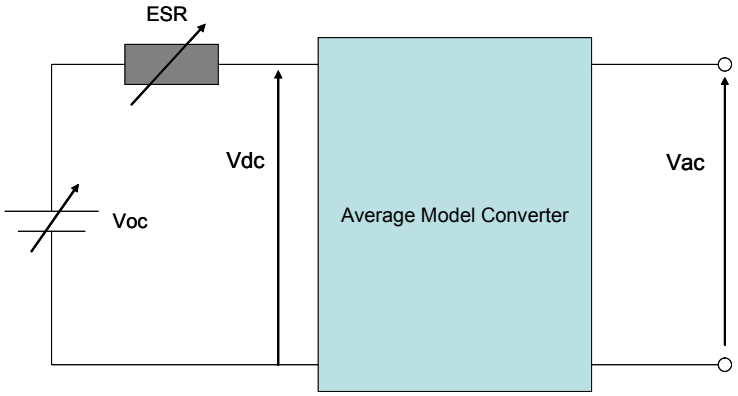


Figure 75. System Model

Battery Modeling

The battery pack voltage and resistance as a function of the SOC can be estimated by discharging the batteries in short intervals as shown below in Figure 76.

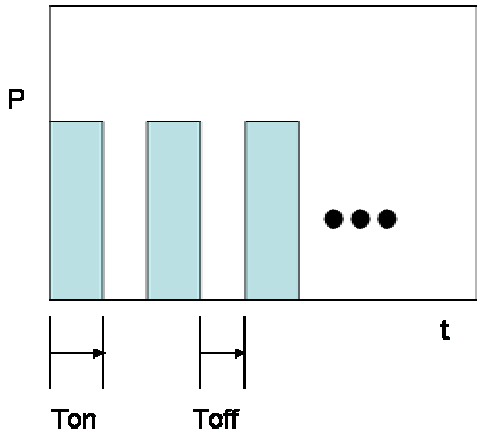


Figure 76. Interval Discharging

The time between discharging periods, T_{off} was set to 15 minutes, which allows the battery pack to reach its open circuit voltage. The DESS was discharged at two different rates on the DC side: 3750 W and 4725 W. The discharging period, T_{on} for those two rates was set to 23 minutes and 20 minutes, respectively. The period is chosen such that the SOC of the DESS decreases in 10 % increments with each discharge. For example, the battery system was requested to run at 4 kW, which ran at 3750 W. The total runtime, R is calculated with the assumption that the estimated available energy in the DESS is 15 kWh:

$$R = \frac{15kWh}{4kW} = 3.75h = 225\,\text{min}$$

The discharging period was therefore chosen to be 23 minutes. The corresponding voltage, current and temperature profiles at 3750 W are shown in Figure 77, Figure 78, and Figure 79. The sample rate is 4 times per minute or 0.0667 Hz for the voltage and current. The temperature measurements are taken at 1 Hz.

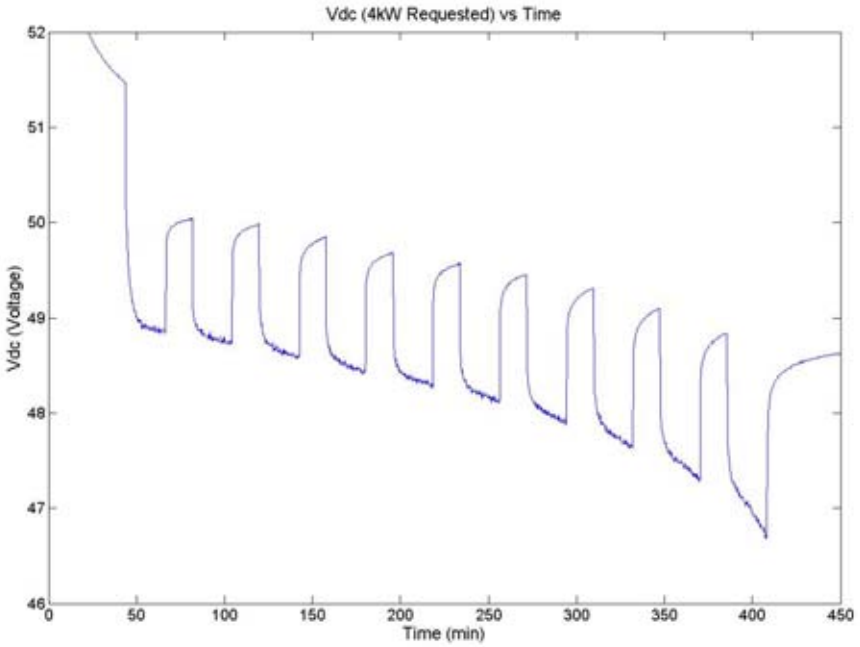


Figure 77. DC Voltage at 4 kW Requested

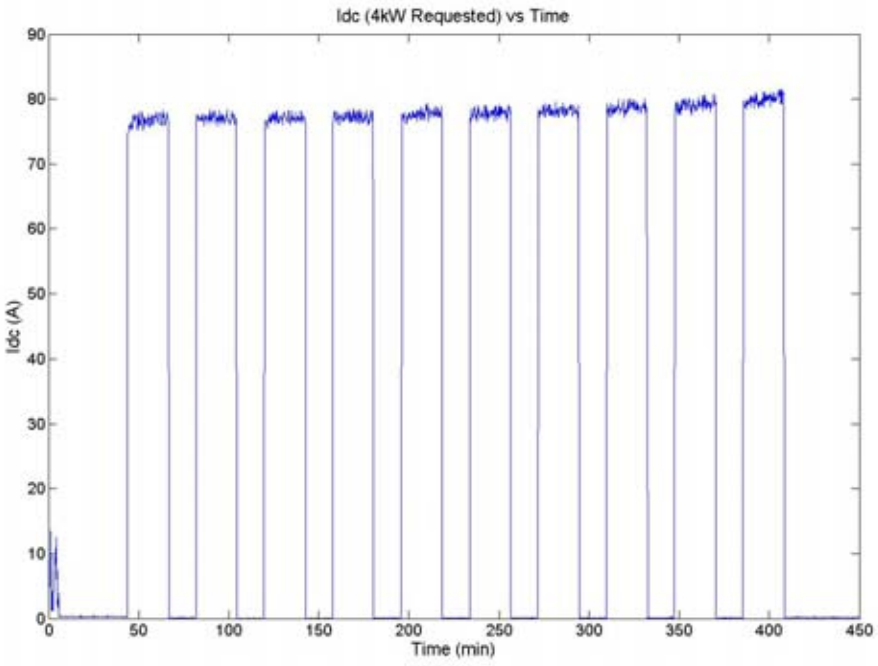


Figure 78. DC Current at 4 kW Requested

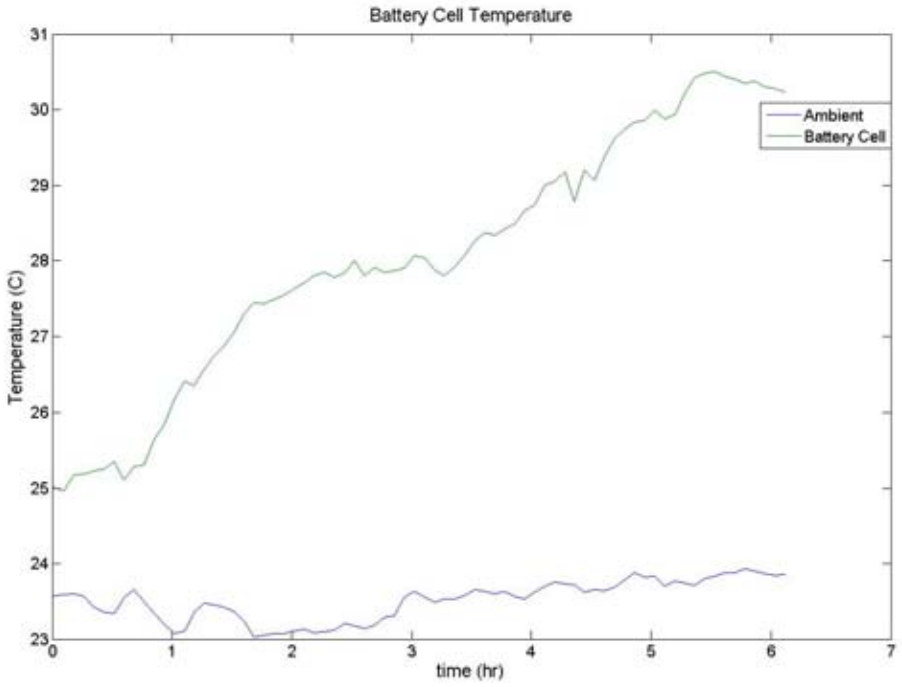


Figure 79. Battery Cell Temperature at 4 kW Requested

The battery pack resistance is estimated by measuring the voltage under load and without load using the following equation:

$$R = \frac{V_{OC} - V_{LOAD}}{I}$$

The measured values and the calculated resistance are listed in Table 7.

V_{OC} (V)	V_{LOAD} (V)	I (A)	R (milliohm)
51.47	50.28	74.71	15.928
50.04	48.88	76.7	15.124
49.99	48.75	77.14	16.075
49.85	48.6	76.03	16.441
49.68	48.43	78.09	16.007
49.57	48.26	77.36	16.934
49.45	48.11	78.73	17.020
49.31	47.89	78.99	17.977
49.1	47.63	78.73	18.671
48.84	47.29	79.14	19.586
48.63	46.7	81.02	23.821

Table 7. Extracted Data Points for 4 kW Run

The state of charge of the battery pack is estimated by integrating the current. The plot of the used capacity or charge vs. time is shown below in Figure 80.

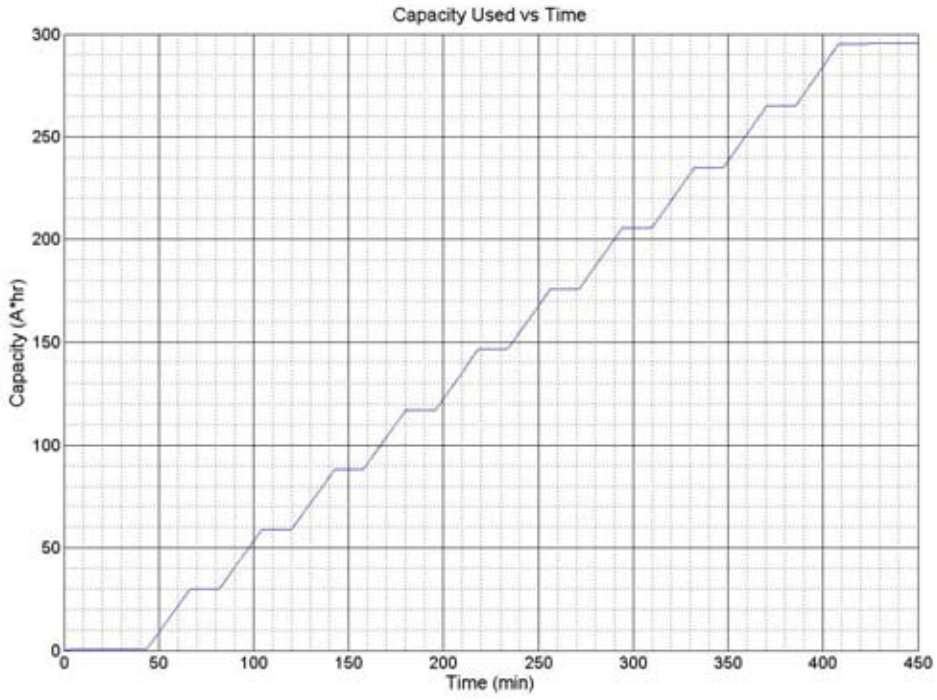


Figure 80. Used Capacity vs. Time

The eleven data points correspond to the eleven levels of plot of the capacity such that the open circuit voltage and resistance can be easily plotted versus the battery pack capacity (Figure 81, Figure 82).

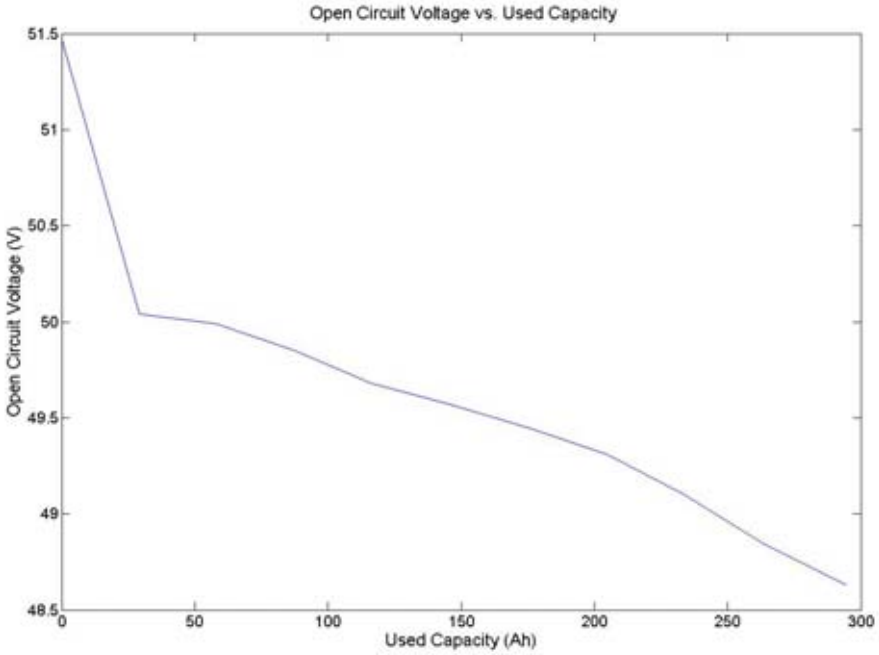


Figure 81. Open Circuit Voltage vs. Used Capacity

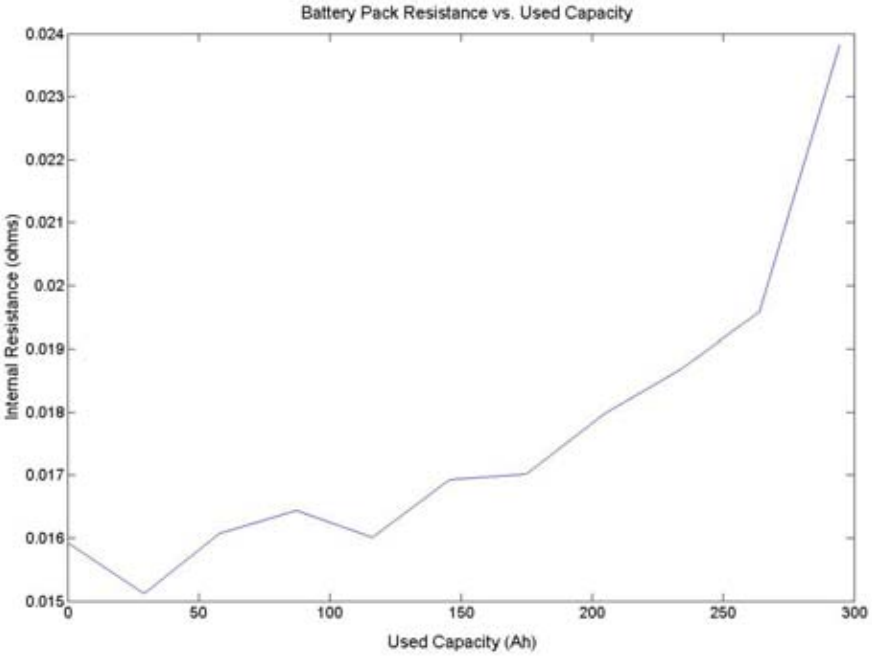


Figure 82. Battery Pack Resistance vs. Used Capacity

The same analysis is done for the run at 4725 W. The voltage, current and temperature profiles are shown in Figures 83-85. Unfortunately, the temperature data acquisition was interrupted when the data acquisition system lost power.

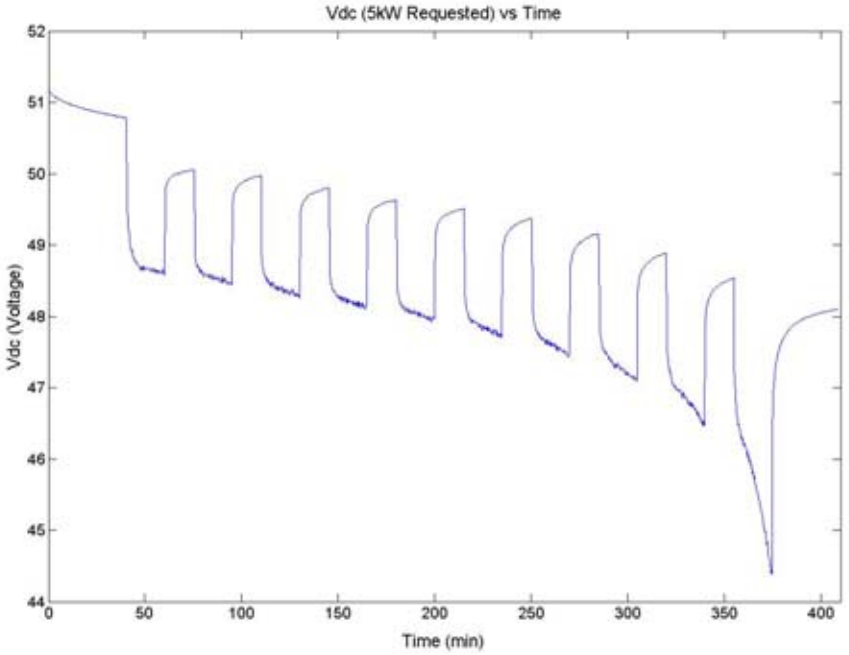


Figure 83. DC Voltage at 5 kW Requested

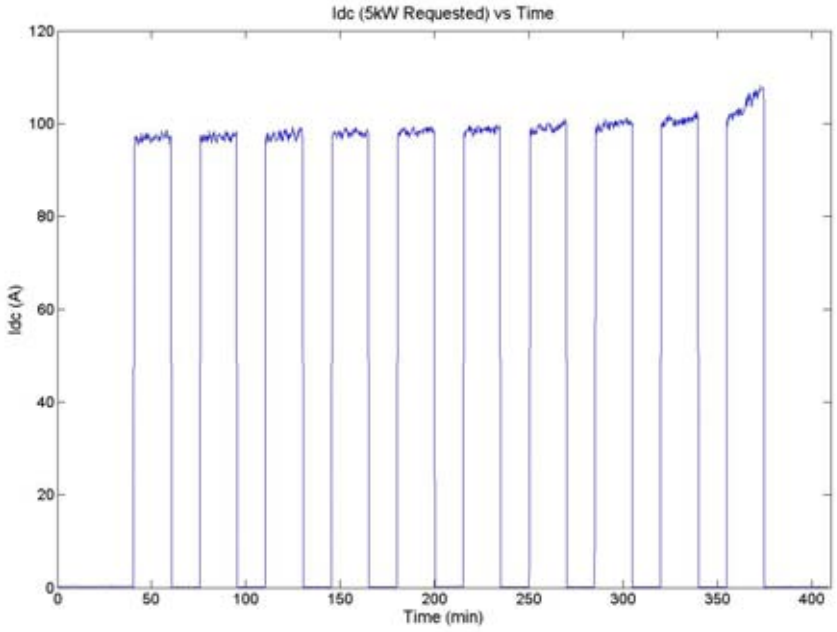


Figure 84. DC Current at 5 kW Requested

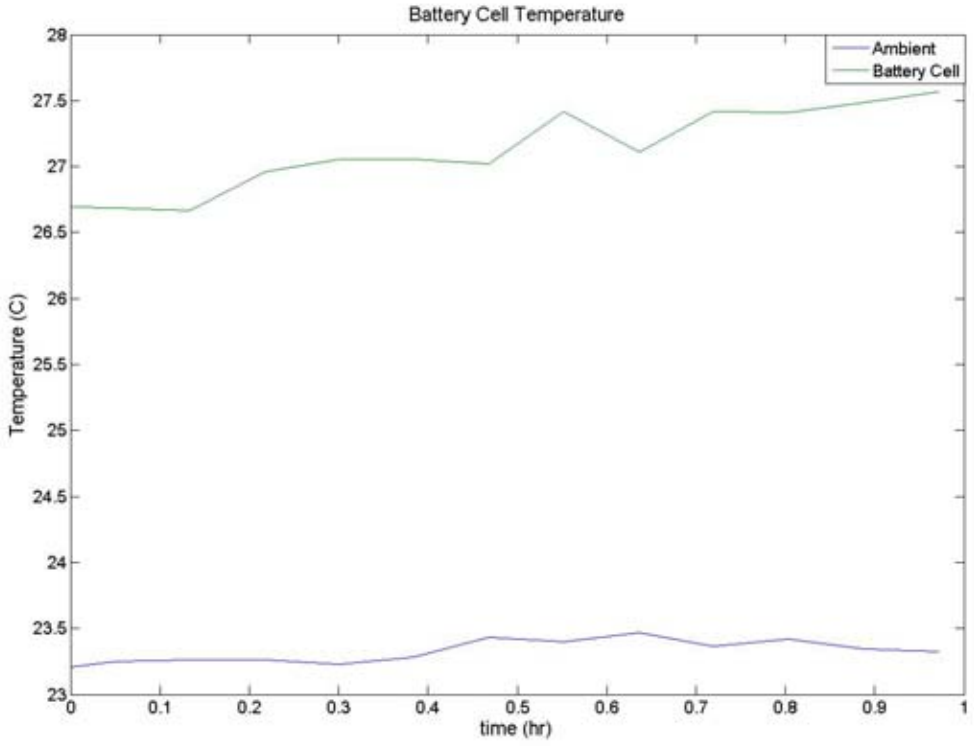


Figure 85. Battery Cell Temperature at 5 kW Requested

The measured values and the calculated resistance for the 4725W run are listed in Table 8.

V_{OC} (V)	V_{LOAD} (V)	I (A)	R (milliohm)
50.78	49.35	95.67	14.947
50.05	48.57	97.15	15.234
49.97	48.46	96.88	15.586
49.79	48.25	97.28	15.831
49.63	48.15	98.16	15.077
49.51	47.97	97.89	15.732
49.37	47.71	98.83	16.797
49.16	47.46	100.2	16.966
48.89	47.12	100.0	17.700
48.54	46.47	101.5	20.394
48.09	44.43	107.7	33.983

Table 8. Extracted Data Points for 5 kW Run

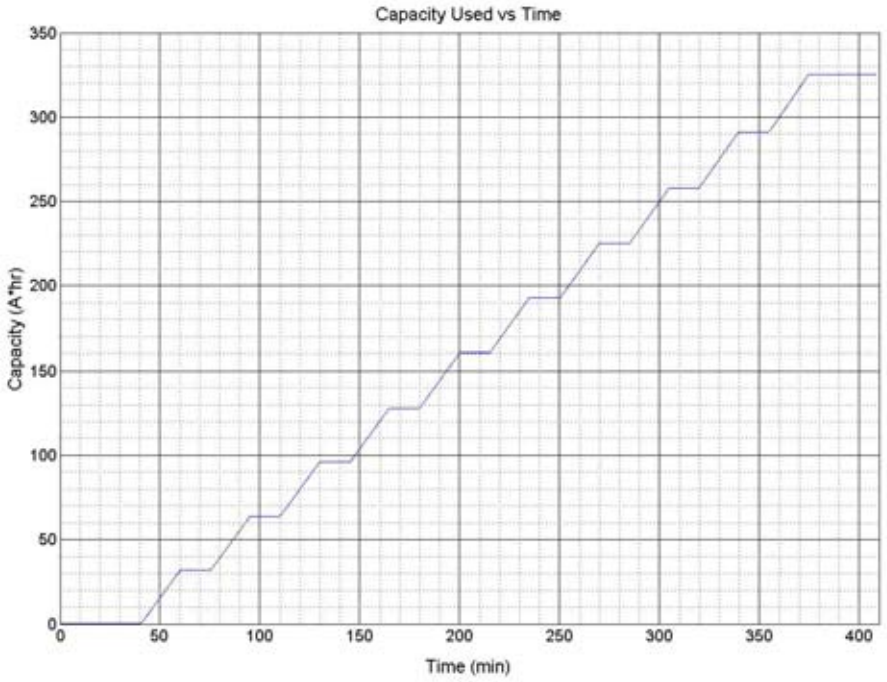


Figure 86. Used Capacity vs. Time

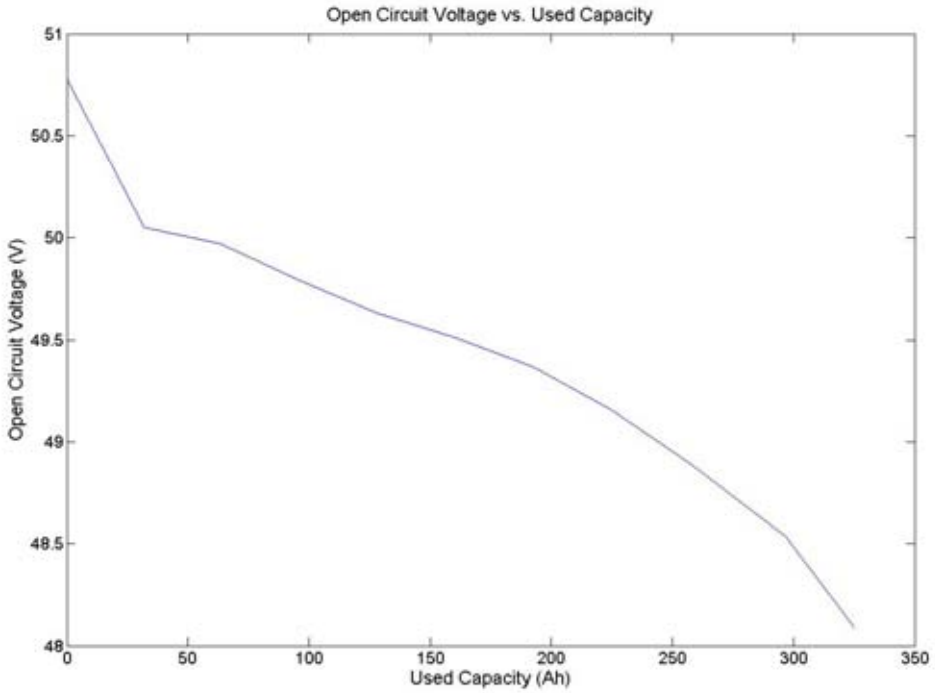


Figure 87. Open Circuit Voltage vs. Used Capacity

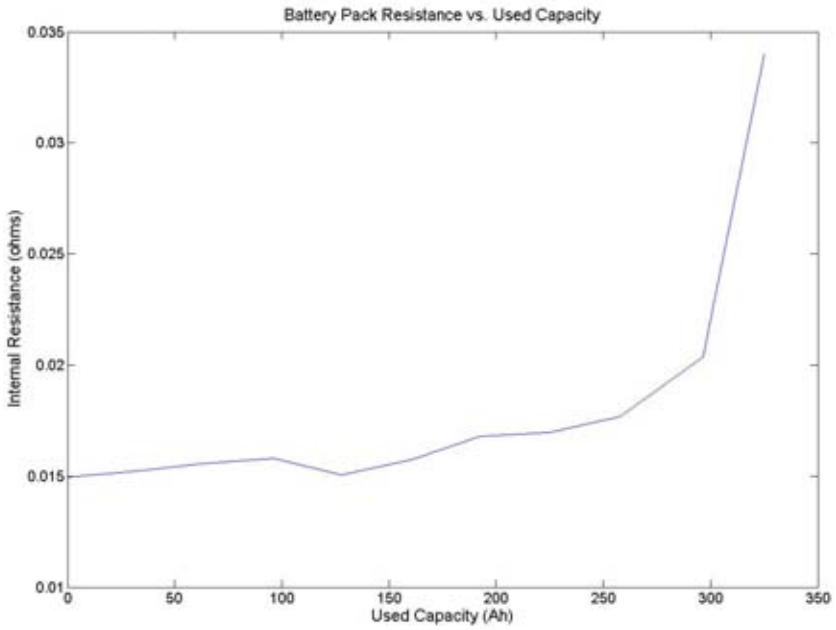


Figure 88. Battery Pack Resistance vs. Capacity

The open circuit voltage plots that are derived from the 3750 W and 4725 W runs are plotted on top of each other in Figure 89. Except for the first data point, there is good agreement between the two plots. The discrepancy is due to the fact that the voltage had not settled down completely before the 3750 W run began. The battery pack resistance plots are also plotted on top of each other in Figure 90. They also match quite well.

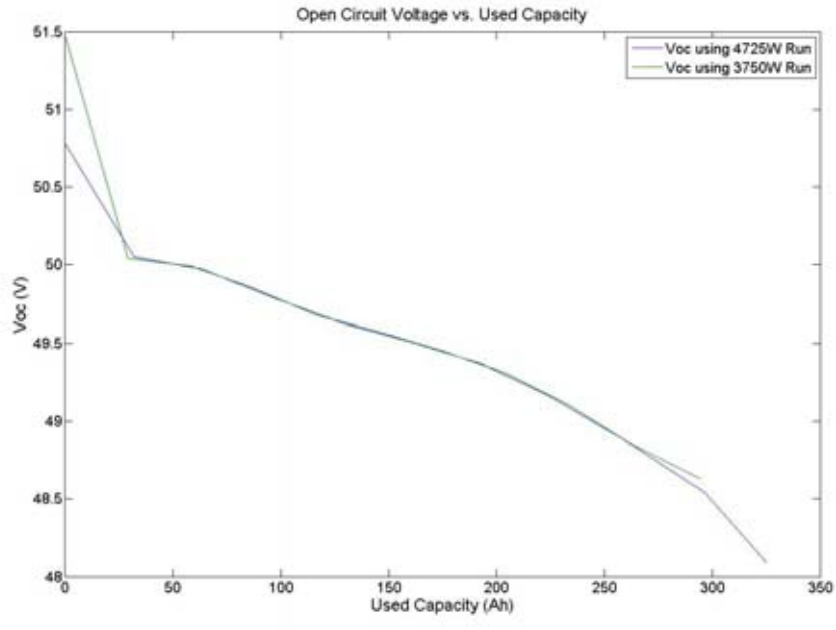


Figure 89. Comparison of Open Circuit Voltage Curves

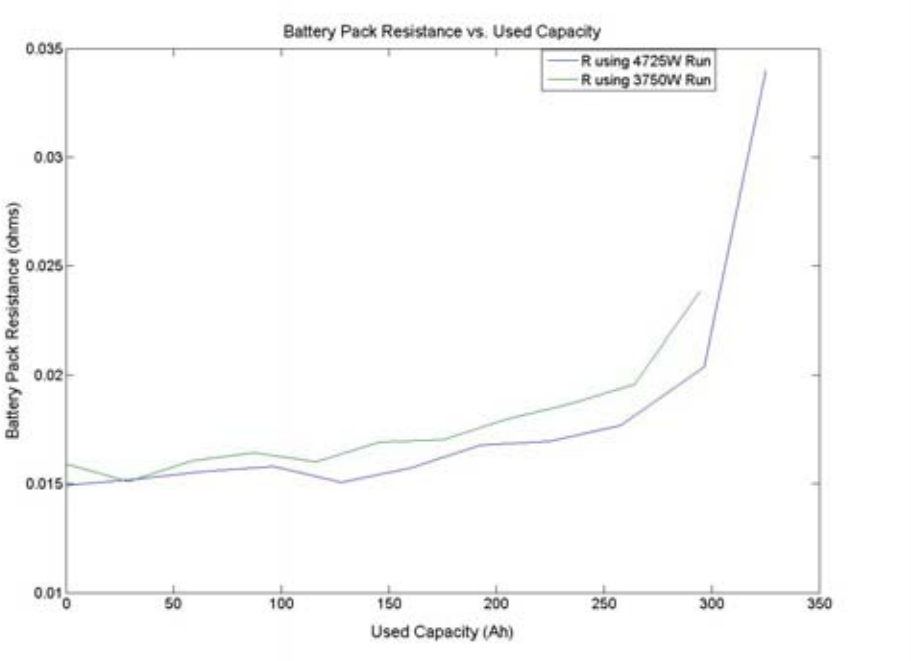


Figure 90. Comparison of Battery Pack Resistance Curves

Converter Modeling

The DESS is equipped with two chargers and two inverters for charging and discharging the battery pack, respectively. The simplest way to model them is to lump them together into one converter that has a charging efficiency and a discharging efficiency. There were two battery cycles that were used to characterize the converter efficiencies. One cycle was run with a requested power of 4.5 kW. The other cycle was at 3.5 kW with part of the charge at 1.2 kW.

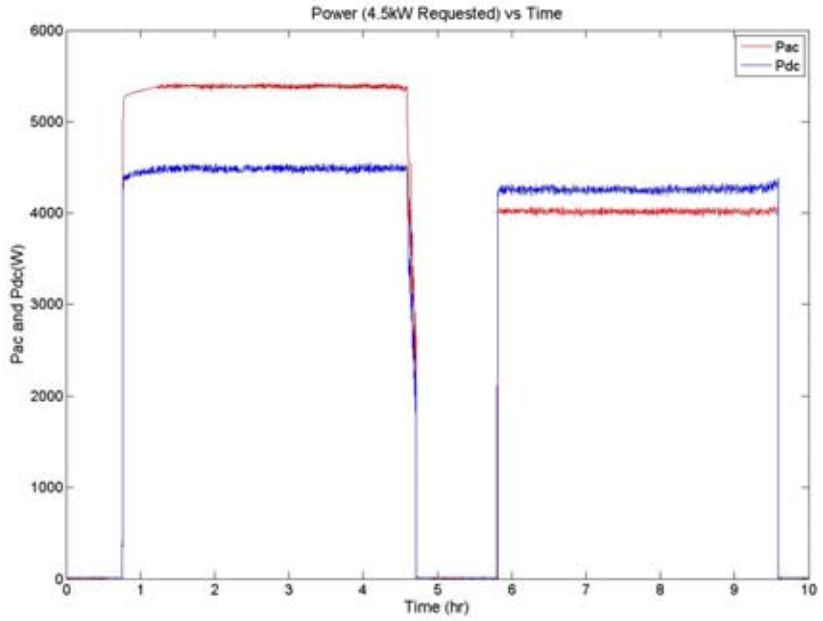


Figure 91. Power (4.5 kW Requested) vs. Time

	AC Energy (kWh)	DC Energy (kWh)	Efficiency (%)
Charge	21.042	17.520	83.26
Discharge	15.173	16.089	94.31
Round trip Eff.	-	-	72.11

Table 9. Power & Efficiency at 4.5 kW Requested

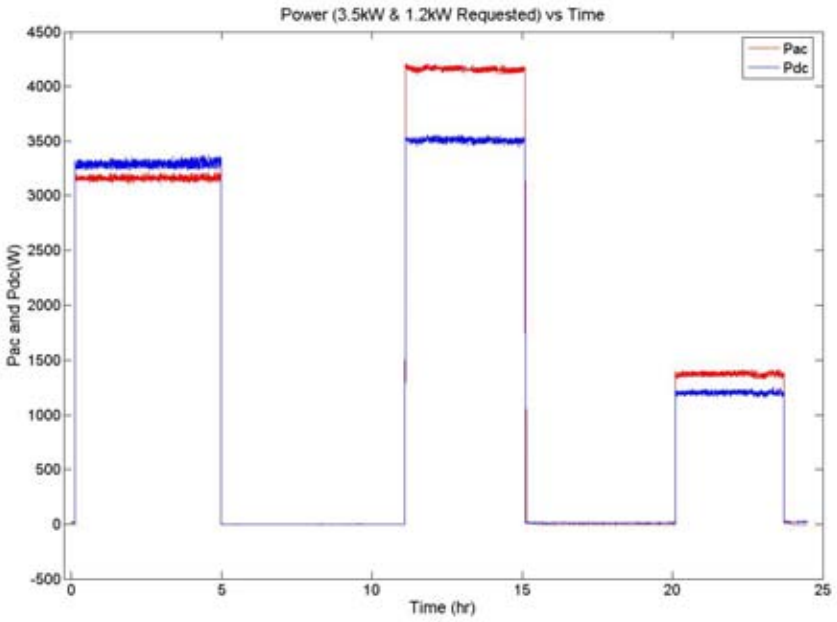


Figure 92. Power (3.5 kW Requested) vs. Time

	AC Energy (kWh)	DC Energy (kWh)	Efficiency (%)
Charge	21.617	18.440	85.30
Discharge	15.378	16.012	96.04
Round trip Eff.	-	-	71.14

Table 10. Power & Efficiency at 3.5kW Requested

System Protection

The DESS protects itself during charging and discharging. The battery cells are rated at 400 Ah and therefore should definitely not be allowed to discharge more than 400 A. Greensmith limits the discharge at 0.3CA or 120A, which increases the battery pack's life time as well as the capacity. The current limit derives from the 60A current rating of each inverter or 120A with 2 inverters in parallel. The discharge DC current seems to be limited to about 112-113A as demonstrated by Figure 93. The figure shows that 7.7% increase in requested power does not provide a proportional increase in current and power. It

appears that the inverters are near their limits as the efficiency is decreasing in the run at 6437W requested power as the current increases as shown in Figure 94. The ratios of the AC to DC power at the two endpoints are 0.949 and 0.929.

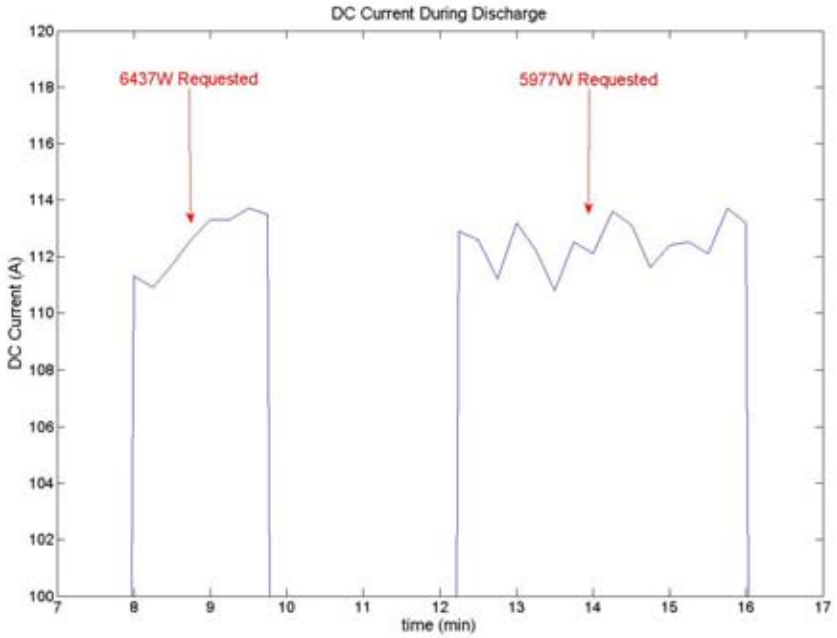


Figure 93. Apparent DC Current Limit

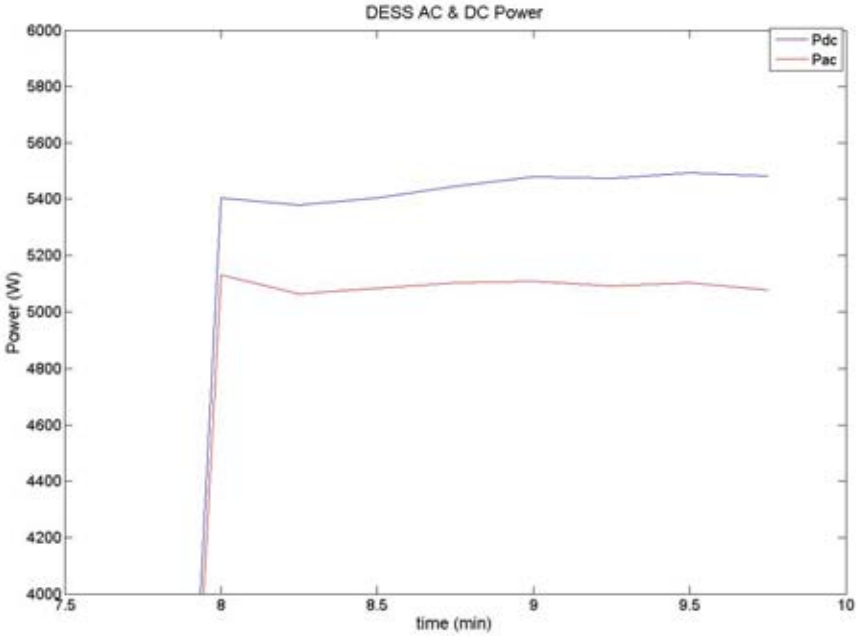


Figure 94. AC & DC Power near Inverter Limits

The current is limited during charging by the two chargers. Greensmith specifies that the maximum input current to each charger is 16A. This limit is reachable as shown below in Figure 95.

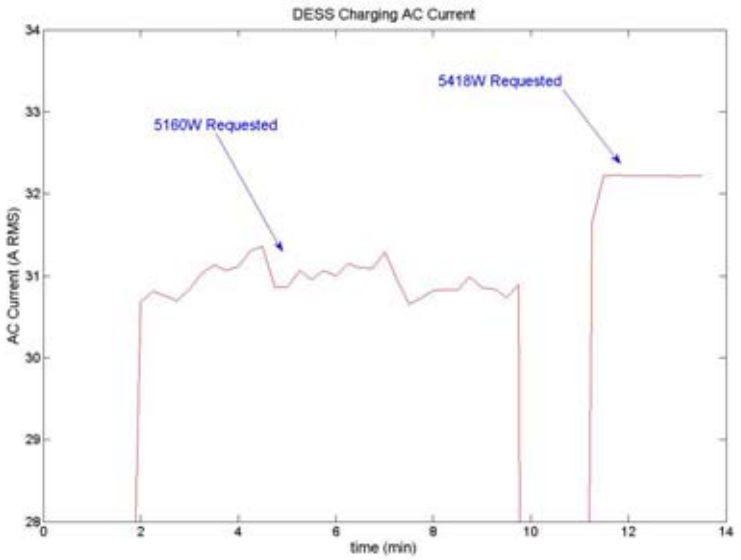


Figure 95. DESS Charging AC Current

It does not appear to be near the limit of the chargers as the current increases proportionally. The efficiency also seems to be constant as shown in Figure 96.

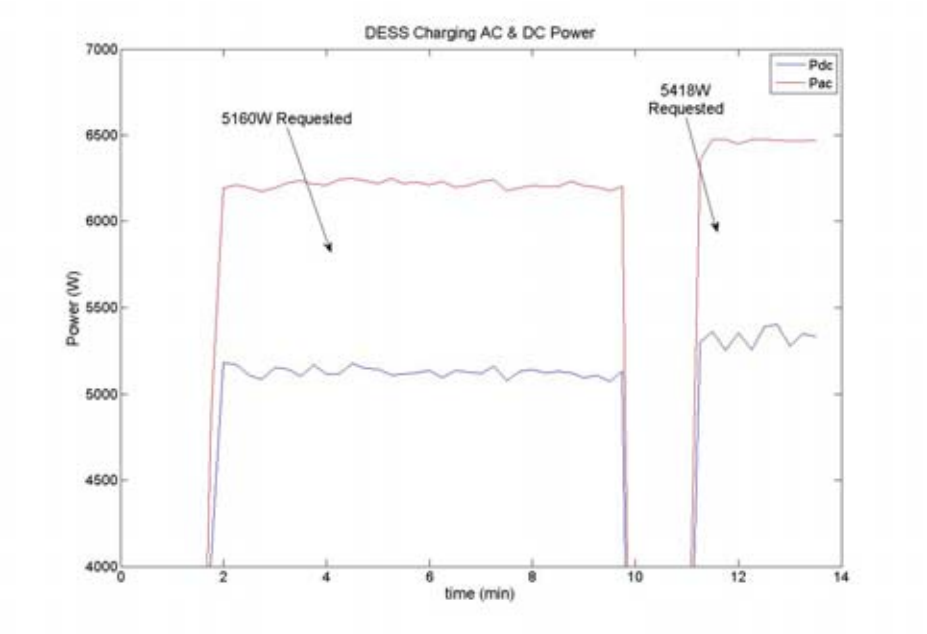


Figure 96. DESS Charging AC & DC Power

The battery manufacturer specifies the operating voltage of each cell as 2.5V minimum during discharge and 4.25V maximum during charge. This corresponds to a 37.5V to 63.75V range for a 15 cell battery pack. The DESS limits the minimum discharge voltage to about 44V and the maximum charge voltage to about 56V as shown in Figure 97. These limits correspond to a minimum voltage of 2.933V per cell and a maximum voltage of 3.733V per cell.

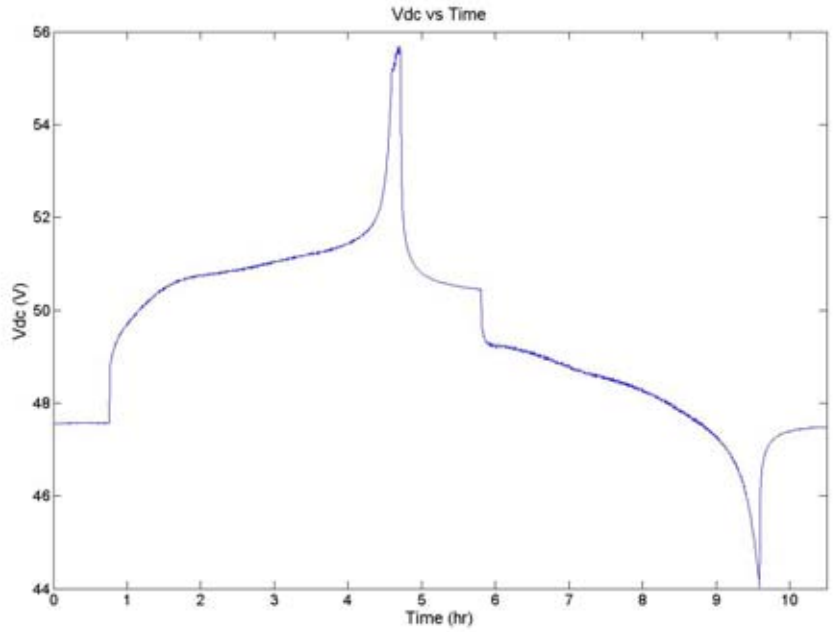


Figure 97. DC Voltage during Battery Cycle

Harmonic Number	Measured Harmonic Voltage (%)
2	0.7112
3	0.5085
4	0.2463
5	0.1273
6	0.1949
7	0.2115
8	0.2262
9	0.1375
10	0.2194
11	0.1337
12	0.2932
13	0.0492
14	0.0886
15	0.1311
16	0.2703
17	0.1755
18	0.3511
19	0.1214
20	0.2929
21	0.3964
22	0.4865
23	0.3221
24	0.4043
25	0.9035
26	0.6808
27	0.1132
28	0.1978
29	0.23
30	0.5097
31	0.1044
32	0.0936

Harmonic Number	Measured Harmonic Voltage (%)
33	0.1703
34	0.2885
35	0.0723
36	0.0559
37	0.0497
38	0.0541
39	0.0448
40	0.0951
THD_V	**1.99**

Table 11. PEBB Voltage Harmonic Distortion

Harmonic Number	Max. harmonic current (%) according to [1]	Measured harmonic current (%) I_{fund} = 30.28A	Measured harmonic current (%) I_{fund} = 20.65A	Measured harmonic current (%) I_{fund} = 11.78A
2	1.0	0.2792	0.1943	0.1749
3	4.0	0.5938	0.7873	1.1743
4	1.0	0.0379	0.0327	0.0423
5	4.0	2.0034	1.7499	0.7257
6	1.0	0.0993	0.1837	0.1446
7	4.0	1.3042	1.3525	0.4814
8	1.0	0.0499	0.006	0.0633
9	4.0	0.3954	0.3662	0.4165
10	1.0	0.0761	0.0415	0.0131
11	2.0	0.9538	0.905	0.3403
12	0.5	0.0202	0.015	0.0306
13	2.0	0.3564	0.4375	0.3826
14	0.5	00347	0.0958	0.0311
15	2.0	0.3998	0.3414	0.1094
16	0.5	0.0502	0.0087	0.0308
17	1.5	0.5264	0.4413	0.3867
18	0.375	0.0221	0.0478	0.009
19	1.5	0.1419	0.1089	0.325

Harmonic Number	Max. harmonic current (%) according to [1]	Measured harmonic current (%) I_{fund} = 30.28A	Measured harmonic current (%) I_{fund} = 20.65A	Measured harmonic current (%) I_{fund} = 11.78A
20	0.375	0.0327	0.0464	0.0142
21	1.5	0.1689	0.1103	0.3862
22	0.375	0.0336	0.0865	0.0368
23	0.6	0.0931	0.083	0.884
24	0.15	0.0180	0.0385	0.0685
25	0.6	0.1004	0.1157	0.3575
26	0.15	0.0677	0.0543	0.0671
27	0.6	0.1796	0.0442	0.3886
28	0.15	0.0115	0.06	0.0764
29	0.6	0.1987	0.1818	0.1528
30	0.15	0.0344	0.0535	0.0491
31	0.6	0.0303	0.1206	0.2511
32	0.15	0.0516	0.0505	0.0235
33	0.6	0.1706	0.1209	0.1354
34	0.15	0.0489	0.0519	0.0240
35	0.3	0.1998	0.1621	0.1367
36	0.075	0.0087	0.0439	0.0139
37	0.3	0.0922	0.0991	0.1045
38	0.075	0.0038	0.0906	0.0158
39	0.3	0.1779	0.1190	0.1542
40	0.075	0.0134	0.0196	0.0237
TDD	5.0	2.84	2.69	2.07

Table 12. Harmonic Testing Results

Integrating Solar Energy with Storage

(A. Domijan, A. Islam, USF {subaward})

The primary goal of this project is the integration of solar energy to grid, which is safe to share load on demand and is isolated from faults on the grid. Solar energy is seen as a potentially abundant and environmentally friendly alternative source in general. Due to its intermittent and deregulated output, it is usually accompanied by local electrical storage system that not only stores energy but also regulates the

share of load with the aid of electronic converters and local control system. The design goals include maintaining safety precautions, real and reactive power balance and disconnection upon failure to maintain the connection standard while operating.

The output power at the inverter is recorded continuously in the form of time interval data to observe the solar trajectory, climate and weather conditions. Data is collected from the site on a monthly basis and is analyzed to model the PV as in the same fashion as a signal generator. It is clearly observed that the PV output power is indicating predominant deterministic distribution with addition of uncorrelated randomly distributed weather effects superposed on it. As a result battery operation algorithm must take it into consideration this distribution pattern. The estimation of the worst-case scenario also depends on how accurately the PV output is modeled.

The PV panel output is modeled. The predefined Time Of Use (TOU) events are set to accompany the PV output as a complete input to our simulation program. The only thing remaining is the real time critical signal modeling, which requires more input from utilities. While it is being worked out the battery will be simulated virtually without the real time critical signal effect. However, it is important to include that in the simulation since it may play vital role to extract the worst-case information related to AESS reliability on peak load. The PV output analysis follows.

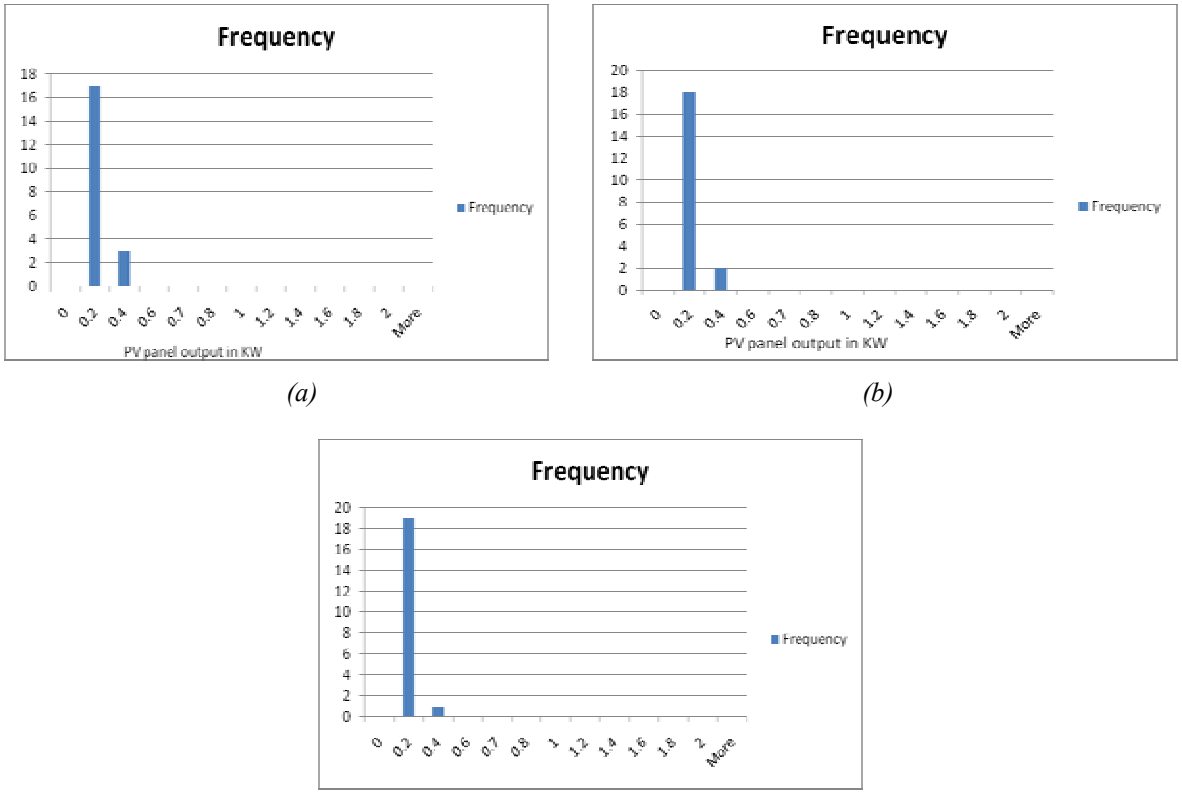
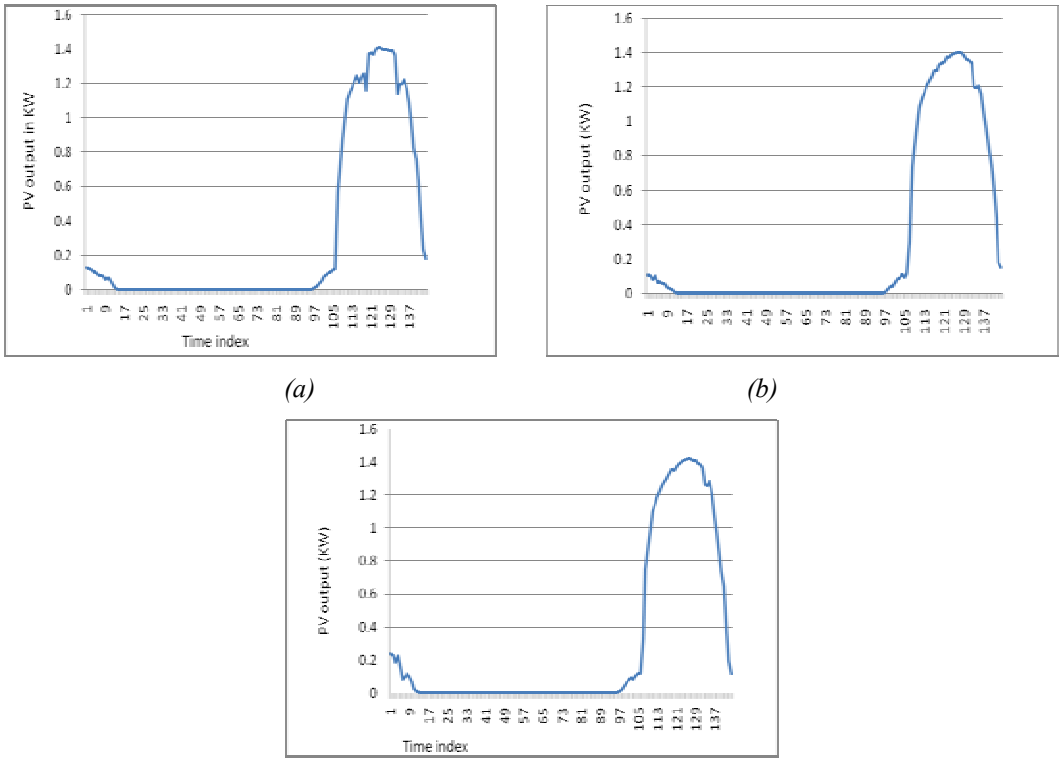


Fig. 98. (a), (b) and (c) is the histogram of the data 3 consecutive timestamp for 48 days.

The histograms (Fig. 98) clearly nullified the possibility of Gaussian distributed random sample. Instead it indicates Weibull or Gamma distributed samples due to shape and unbalance of the samples around the mean.



(a) *(b)*

(c)

Fig.99. (a), (b) and (c) PV output for three consecutive days.

The daily output is dominantly deterministic with random distributed noise (Figure 99).

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Grid Reliability and Security Support

(L. T. Baldwin, P. McLaren, R. Meeker)

With the assistance of the DOE Office of Electricity Delivery and Energy Reliability, CAPS reached out to the Florida Reliability Coordinating Council (FRCC) to, 1.) offer additional tools, resources, and expertise to the investigation and analysis effort associated with Feb. 2008 Florida system disturbance event, and, 2.) seek opportunities for learning from this rare event data more about system dynamics and wide area affects beyond the basic cause investigation that is the focus of the FRCC Event Analysis Team (FEAT) [23].

Event summary

On 2/26/08, the Florida bulk power system experiences a wide area disturbance initiated by a delayed clearing of a three-phase fault in a 138kV no-load switch at the Flagami substation in the FPL Miami area at 13:09h. Isolation of the event led to the following:

- opening of (22) transmission lines, (6) 230 kV lines, (15) 138 kV lines, and (1) 69 kV line
- shedding of 1350 MW of customer load in the local area
- loss of 2500 MW of generation near the fault location
- shedding of an additional 2300 MW of distribution-level customers across Florida by automatic underfrequency load shedding program
- loss of an additional 1800 MW of generation across FL

Figure 100. Flagami substation, aerial view (source: Google Maps)

The disturbance was observable on system frequency and PMU measurements at points all across the Eastern Interconnect.

Activities

CAPS met with FRCC in Tampa on 10/17/08 to discuss utilization of unique university capabilities such as those at CAPS in reliability coordination and outage investigation, and the possibilities for FSU CAPS contributions on the Florida outage investigation. In early communications (3/2008), FRCC and DOE contemplated the possibility of utilizing CAPS simulation capabilities in subsequent stages of the investigation. Interim results from FRCC's initial investigation were shared at the Tampa meeting, and, very shortly thereafter, on 10/30/08, the event analysis team issued its final report on the 2/26/08 disturbance. Also discussed at the meeting were the possibilities for real-time simulation-enhanced operator training to support existing and evolving NERC training and continuing education requirements for Certified System Operators.

Figure 101. Flagami substation, side view (source: Meeker)

The FEAT conducted a thorough investigation into the causes of the disturbance, documenting the causes in detail and producing 24 recommendations to address them and prevent future occurrence. With such a widespread and rare disturbance of this type, there exists a substantial and unique opportunity to better understand the system dynamics and interdependencies for stability and control, particularly in the southeast region and the Eastern Interconnect, and to validate existing understanding and modeling and simulation approaches. To that end, CAPS has worked to develop a closer working relationship with the FRCC, NERC, DOE and the utilities involved in reliability coordination and event investigation activities, including establishing the necessary mechanisms and approvals for accessing additional data to produce research-appropriate grid models and to study disturbances and perform model validation. In continued efforts to support regional electric power reliability activities with R&D, simulation and test

facility, and education resources, CAPS has continued communications and formal and informal meetings with the FRCC, and particularly the FRCC Planning Committee and Operating Committee. This cooperation and communication continues as CAPS seeks to develop collaborative modeling and simulation efforts that provide the means and foundation to rapidly and effectively engage the specialized resources of CAPS and the electric power systems research community to supplement those existing capabilities within the industry and the reliability organizations.

High Temperature Superconductivity (HTS)

The development of high temperature superconductors has made significant progress and has led to the necessity of AC characterization for their use in applied technologies. CAPS proposed research focused on AC losses, quench behavior, and mechanical behavior of HTS tapes. Mechanical behavior tasks were deleted from the program to prioritize and allow sufficient effort to produce more complete results in the AC loss and quench areas.

Further, because HTS materials require operation in cryogenic environments it is important to study behavior of dielectrics under those conditions. The data obtained from the studies has been applied to the understanding of practical issues related to the real world application and use of HTS devices and cables.

The emphasis of AC loss measurements at CAPS has been to generate the critical data on AC losses of commercial BSCCO and YBCO conductors. This research effort has produced AC loss experimental data in particular for (2-G) YBCO conductors, as function of a variety of parameters. AC loss measurements were proposed under the following conditions:

- Temperature range: 30 – 77 K
- Frequency range: 50 Hz – 3.0 kHz
- Transport current range: 0 – up to I_c of the conductor
- Magnetic field amplitude: 0 – 300 mT
- Magnetic field frequency: 50 – 1.0 kHz
- Magnetic field orientation: any angle with respect to the conductor

The measurements performed have been produced using primarily calorimetric methods.

In the process, laboratory capabilities and processes for conducting these types of measurements have been continuously improved.

Calorimetric AC loss measurements using liquid nitrogen boil-off method

(S. Pamidi)

Introduction and Background, Proposed Work

Variable temperature ac loss measurement techniques were established from previous funding from the Department of Energy. The current funding was used to enhance the measurement capabilities and to understand the manifestation of ac losses in coils of 2 G conductor. The focus of AC Loss characterization studies has been to establish a versatile technique for measuring the losses over a wide parameter range on not only on tape samples, but also on several coils to understand the extent and implication of the losses in designing superconducting magnets and power system components.

Results and Accomplishments

Enhancements of the existing AC loss measurement techniques at FSU-CAPS was continued with a design and fabrication of a set up suitable for transport loss measurements on coils of 2G conductor. The design was based on liquid nitrogen boil off measurements and would be suitable to measure medium size coils. The set up has been designed, components procured, parts machined, and assembled. The design was versatile to enable measurements on small to medium size coils with diameter of up to 14 cm length of 20 cm. The length of 2G conductor in a coil could be as long as 100 m. The current leads, nitrogen gas flow rate measurement meters are designed to enable up to 150 A transport current through the coils. The power supply for the measurement will allowed transport currents with variable frequency in the wide range of 20 – 2 kHz.

The initial design was modified until the system performed with high accuracy, reliability, and reproducibility.

Figures 102 and 103 depict a schematic and a photograph of the calorimeter, respectively.

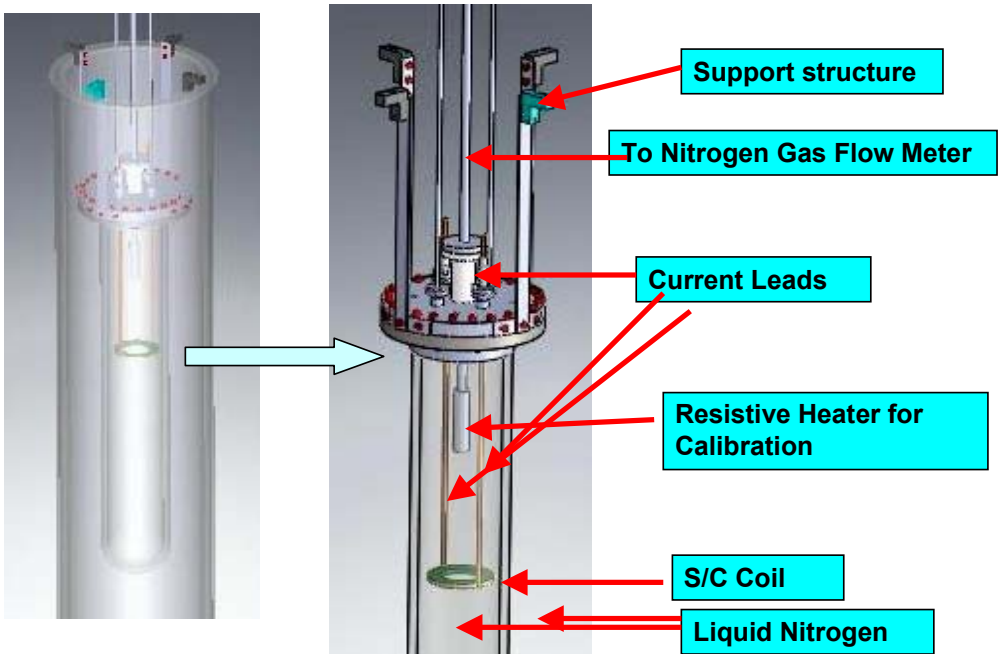

Figure 102. A schematic of the calorimeter used for ac loss measurements of superconducting coils.

Figure 103. Photographs of the calorimeter used for ac loss measurements of superconducting coils.

The calorimeter was calibrated using a resistive heater coil to the reliability of the measurement technique and the apparatus. The response of the calorimeter was linear up to 150 W as evidence by the linearity of the flow rate versus heat input into the calorimeter. The reliability is evidence by the slope of the calibration curve, which is equal to the theoretical value of 0.248 SLPM/W. Figure 104 depicts a typical calibration data set.

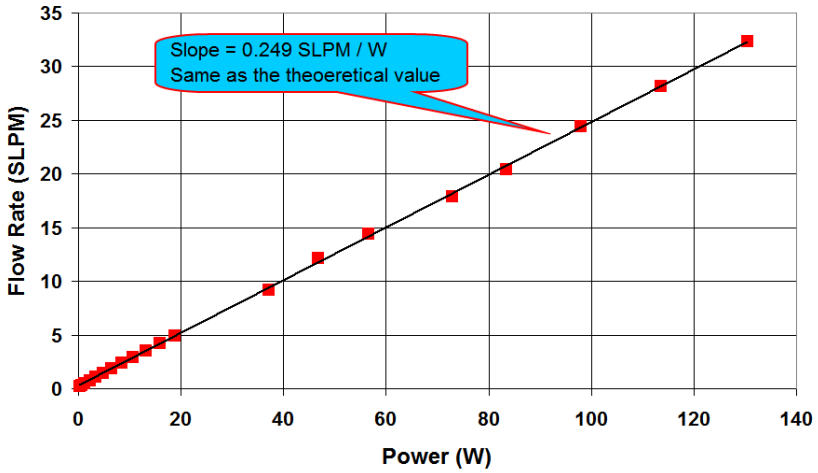

Figure 104. Nitrogen gas flow rate versus heat input of the calorimeter use for ac loss measurements of superconducting coils.

After confirming the veracity of the calorimetric measurement set up, several coils were fabricated using the conductor from both the manufactures of 2G superconducting tape. The coils fabricated ranged from solenoids with small self-field on the conductor to 125 turn pancake coils with significant perpendicular self-field on the conductor. Superconducting tape was insulated with GE warmish-based coating using a technique developed at the national High Magnetic Field Laboratory, Tallahassee. Figure 105 shows the pictures of some of the coils fabricated for AC loss characterizations.

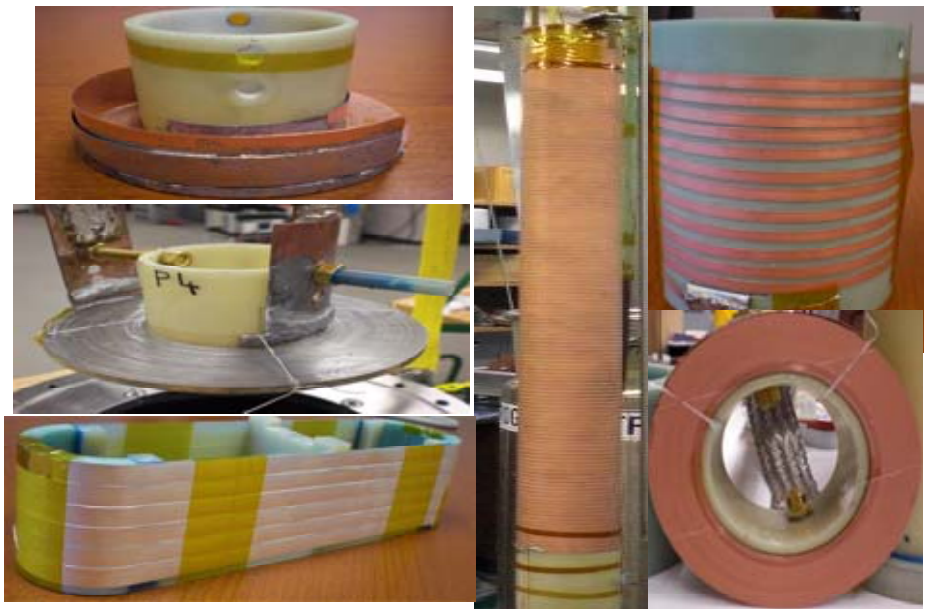

Figure 105. Superconducting coils fabricated using 2G superconducting tape for AC loss measurements.

After fabricating the coils, the coils were first characterized for self-field critical current density at 77 K before measuring the ac losses. Figures 106 and 107 show the superconducting transition and the corresponding critical current density of the coils.

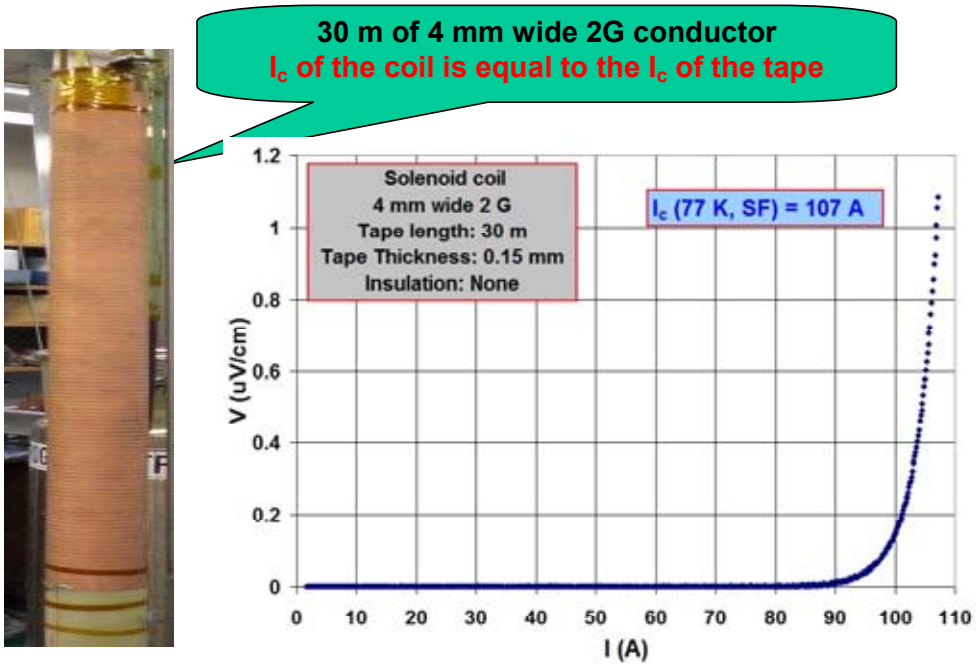

Figure 106. Voltage versus current behavior of one of the solenoid coils fabricated using 2G superconducting tape for AC loss measurements. The coil had 30 m of the tape and had an Ic of 107 A.

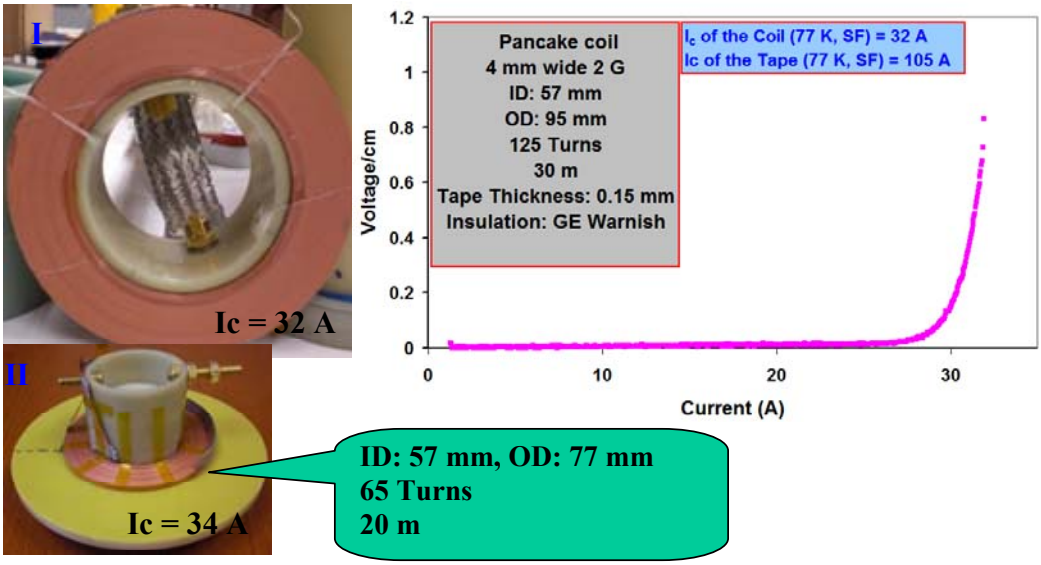

Figure 107. Voltage versus current behavior of one of the pancake coils fabricated using 2G superconducting tape for AC loss measurements. The coil had 20 m of the tape in 65 turns and had an Ic of 34 A.

Significant differences were noticed between coils of equal number of turns but made from conductor from different manufacturers. For example a 125 turn pancake coil has a critical current of 70 A, where as a coil with the same 125 turns but from another manufacturer had critical current of only 34 A. The differences were interesting and forced us to perform electromagnetic modeling and detailed tape characterization. A combination of the electromagnetic models and detailed Ic(B) characterization enabled explanation of the difference measured between the coils. Figure 108 lists the electromagnetic characteristics of the two coils.

SCS4050 - 125 turns pancake coil

125turns pancake coil	Inner diameter	57mm
	Outer diameter	95mm
	Turns	125turn
	Inductance	1.479mH
	Total wire length	29.79 meter
	Center magnetic field	0.00175T/Arms
	Max. parallel magnetic field	0.00552T/Arms
	Max. perpendicular magnetic field	0.00355T/Arms
Superpower 2G HTS wire Critical current : 107A @ 77K, sf	Width = 4mm, thickness = 0.15mm (insulated)	

344C - 125 turns pancake coil

125turns pancake coil	Inner diameter	57mm
	Outer diameter	123mm
	Turns	125turn
	Inductance	1.557mH
	Total wire length	35.47 meter
	Center magnetic field	0.00178T/Arms
	Max. parallel magnetic field	0.00395T/Arms
	Max. perpendicular magnetic field	0.00214T/Arms
AMSC 2G HTS wire Critical current : 107A @ 77K, sf	Width = 4.35mm, thickness = 0.265mm (insulated)	

Figure 108. Electromagnetic characteristics of two coils with 125 turns. The tape used for each coil was manufactured by a different firm.

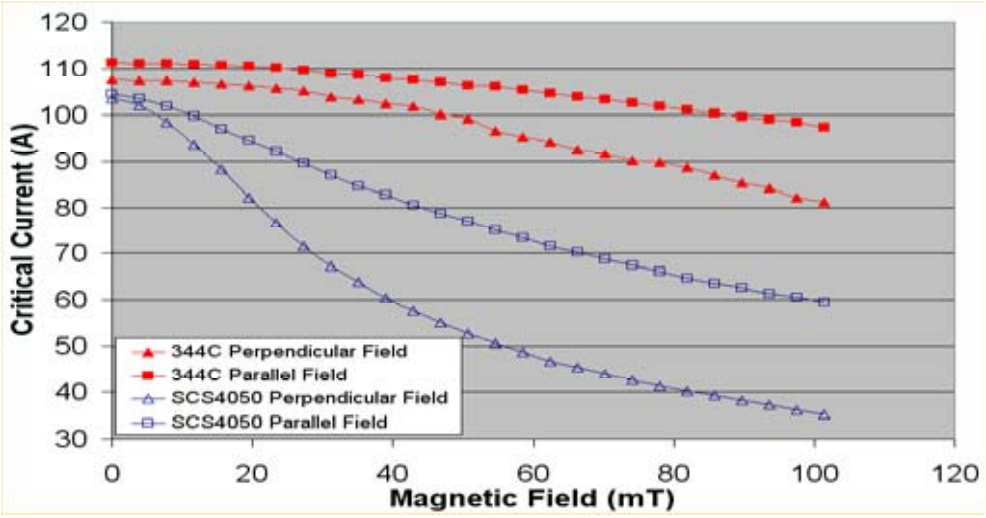

Figure 109. Shows the differences in Ic(B) characteristics of the tapes used for the coils described above.

As can be seen in Figure 109, both the tapes have almost similar critical current density in zero applied magnetic field, but are significantly different in their critical current density as the magnetic field increased to 100 mT. This difference manifests in the large variation observed in the coil critical current values.

AC losses were measured as a function of transport current through the coils as various frequencies. The losses were significant at higher currents and frequencies. Figure 110 shows losses for one of the coils at various currents as the frequency is increased.

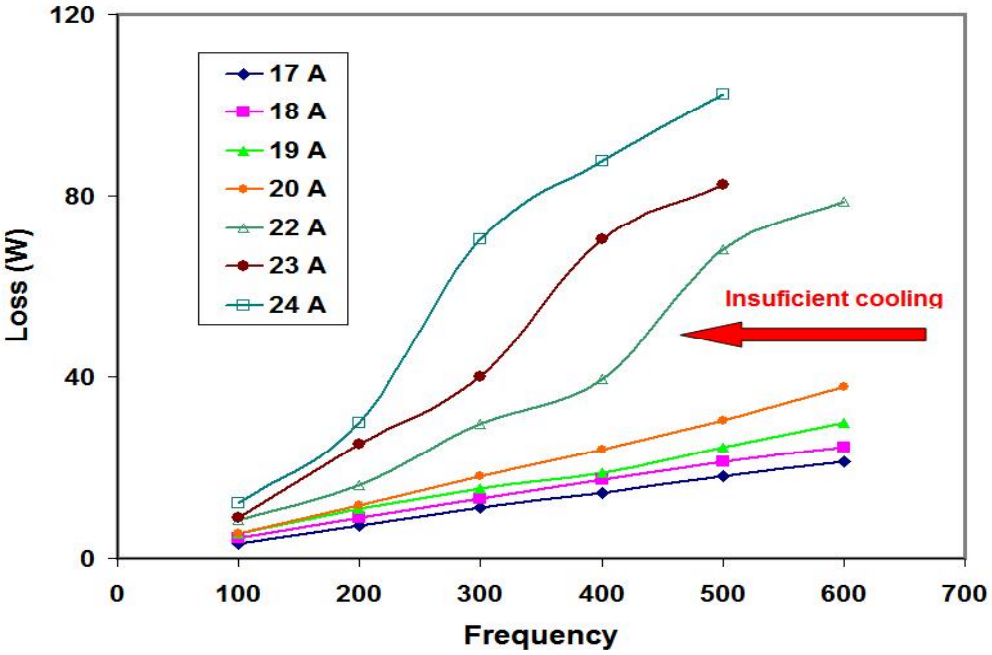

Figure 110. Ac losses in Watts for a 65 turn coil at various currents as the frequency is increased.

From Figure 110, it is clear that the losses are linear with frequency for current up to 20 A. The loss curves deviate from linearity for higher currents, suggesting that either the loss mechanism is changing or there is insufficient cooling of the coils. If the cooling is insufficient, the coil is operating at temperatures higher than 77 K, causing the critical current density to lower values. To understand the reason for the measured behaviors, thermal sensors were mounted on the coil and the temperature of the coil was measured at multiple locations as transport current is injected into the coil. As shown in figure 111, the temperature of the coil increases above 77 K reaching 80 K at some locations. The results of temperature measurements suggest that the cooling was insufficient for the coils in spite of the coils in a pool of nitrogen.

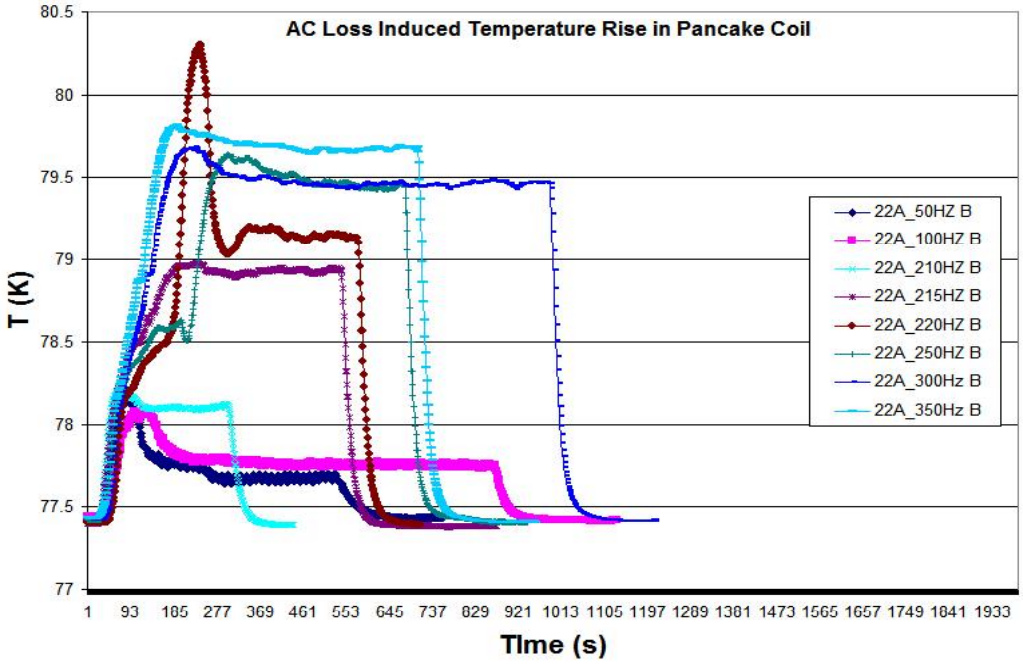

Figure 111. Loss-induced temperature rise in coil.

The consequence of insufficient cooling is thermal runaway condition causing the coils to undergo catastrophic damage if the losses are high enough to cause cooling problems.

Summary

A versatile technique has been established for ac loss measurements of superconducting coils. Many coils were fabricated and characterized. The coils performed well under DC current. AC losses of the coils fabricated from commercial tape materials are high and in some situations can cause catastrophic failure due to a combination of large ac losses and insufficient cooling. Temperature increase was noticed in coils when injected with ac current at high frequencies. Failure was noticed in coils subjected to 70-80% of the critical current at 300 Hz or higher frequency. The results suggest that there is a need for concerted effort in understanding of ac loss behavior of superconducting coils and development of low ac loss conductor.

Supporting Industry

Many measurements were performed to support SuperPower in their efforts to develop low ac loss conductor.

Supporting DOE

Sastry Pamidi regularly reviews DOE SBIR/STTR proposals on superconductivity and related topics.

Sastry Pamidi participated in workshops to identify research needs in high temperature superconductivity programs.

Other supporting activities

Sastry Pamidi organized short courses in conjunction with Applied Superconductivity conferences and started a new course on AC loss measurements and other characterization techniques.

Sastry Pamidi in on the editorial boards of Applied Superconductivity Conferences and Cryogenic

Engineering conferences and frequently reviews papers submitted for many scientific journals.

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Current Density and Current Limiting Mechanisms in Coated Conductors

(D. Larbalestier, D. Abraimov, P. Li)

Background to the Project and Global Objectives:

The primary thrusts of our ongoing work supported by DOE-OETD are to provide critical understanding of how best to enhance the current-carrying capacity of coated conductors. A portion of this total effort is supported under this subaward through CAPS-FSU. It specifically concerns the use of a Low Temperature Scanning laser Microscope built up in the Applied Superconductivity Center (ASC) to study the current limiting effects of grain boundaries.

Local identification of current limiting mechanisms: We built and now operate a low temperature laser scanning microscope (LTLSM) which provides a 2D map in coated conductors. It thus allows us to identify their principal sources of dissipation. This is part of a suite of instruments in ASC and techniques to identify current limiting mechanisms in coated conductors. The LTLSM is part of a suite of instruments, which provides a unique capability worldwide. The LTLSM is the tool that enables us to identify the local electric field produced by the supercurrent, while magneto optical imaging (MOI) shows the local supercurrent path. Both guide use of a dedicated field emission high-resolution scanning electron microscope (HRSEM) equipped with full analytical and orientation image mapping (OIM) capabilities. This machine, a Zeiss 1540, has a full focused ion beam (FIB) capability with gas injectors for C, W, and Pt deposition and an Omniprobe TEM surgical TEM sample fabrication and lift out tool. The key and unique feature of this suite of tools is that we can locate local regions of specially good or bad superconductivity using the LTLSM or MOI and then bring the HRSEM and TEM to bear on exactly those local regions of interest.

As noted above, all of these thrusts have been integrated into close working relations with the national labs, especially closely with members of the Wire Development Group (AMSC, ANL, ORNL, LANL and FSU), where our collective goal is to decisively impact the production of YBCO coated conductors. It is well known, though less well described in the literature, that all attempts to proportionately increase I_c of coated conductors by just thickening the YBCO layer run into difficulty for multiple reasons associated with various issues like progressive loss of epitaxy, irregular YBCO nucleation, chemical segregation, unwanted 2nd phase etc. Our capability has been particularly valuable for collaborations within the WDG, where grain boundary limitation of the I_c in MOD RABiTS is an important factor that depends on the local grain-to-grain misorientation and specific aspects of the grain boundary morphology, such as the planarity and segregation to the GB. There is recent controversy that goes to the heart of what the RABiTS approach to template engineering is supposed to do. Experience within the WDG says that minimization of both out-of-plane (OOP) and in-plane (IP) misorientations is important to gaining high I_c. Indeed a crucial feature of earlier ASC work within the WDG was our observation [24] that one of two crucial reasons for greatly enhanced J_c in RABiTS-MOD coated conductor is that the OOP component of the misorientation $\Delta\omega$ is significanlty reduced by the MOD growth of YBCO on a given RABiTS, while there is just almost perfect replication of the template $\Delta\omega$ with an *in situ* process like PLD YBCO. The underlying reason is that the PLD and MOD growth processes produce columnar and laminar YBCO grain structures, respectively. In the MOD-processed sample with full-width critical current density Jc(0 T, 77 K) = 3.4 MA/cm^2, electron back-scatter diffraction (EBSD) revealed an improvement in both the in-plane and out-of-plane alignment of the YBCO relative to the template that resulted in a significant reduction of the total grain boundary misorientation angles. YBCO GBs produced by MOD also meandered extensively about their corresponding template GBs and through the thickness of the film. In contrast, the PLD-processed film (full width J_c(0 T, 77 K) = 0.9 MA/cm^2) exhibited nearly perfect epitaxy, replicating the template grain orientations without any observable GB meandering. Direct transport measurement of the intra-grain J_c(0 T, 77 K) values of PLD and MOD-processed films on RABiTS revealed values up to 4.5 and 5.1 MA/cm^2, respectively. As the intra-grain J_c values were similar, the significantly higher full-width J_c for the MOD-processed sample was directly correlated to the improved grain alignment and extensive GB meandering [24]. These conclusions are widely accepted

within the WDG as showing a huge value of using an *ex situ* process, especially MOD, for making YBCO (full width J_c 3.4 versus <1 MA/cm^2), but they have now been implicitly challenged by Held *et al.* [25], who compare the differing effect of low angle tilts, ~5-10º, of two types, [001] and [100] using PLD-grown bicrystal films. They show that the OOP tilts of [100] type have significantly higher J_c than IP tilts of the more common [001] type. In our view, these results, though interesting, suffer from not being compared to our earlier work on single grain boundaries isolated within the YBCO grown by PLD and MOD on the same RABiTS, and also ignore the very positive enhancement in J_c (perhaps half of the 3.4 times increas noted above) produced by grain boundary meandering [26]. The LTLSM is an even more effective instrument for resolving this controversy than the single GB tests pursued by Feldmann *et al.* [26], since multiple GBs can be measured at one time using 1D tracks patterned on to RABiTS templates. This is the work that we have taken on in FY09.

Determining I_c as a function of in-plane and out-of-plane GB misorientation

During the present quarter we developed a LabView based program with which we can separate the in-plane, out-of-plane (including twist and tilt) misorientations from OIM data and export profiles of the components of the GB misorientation. We can apply this to all data that we have previously measured with OIM, including those that we took on quasi-1D MOD AMSC CC grown on RABiTS.

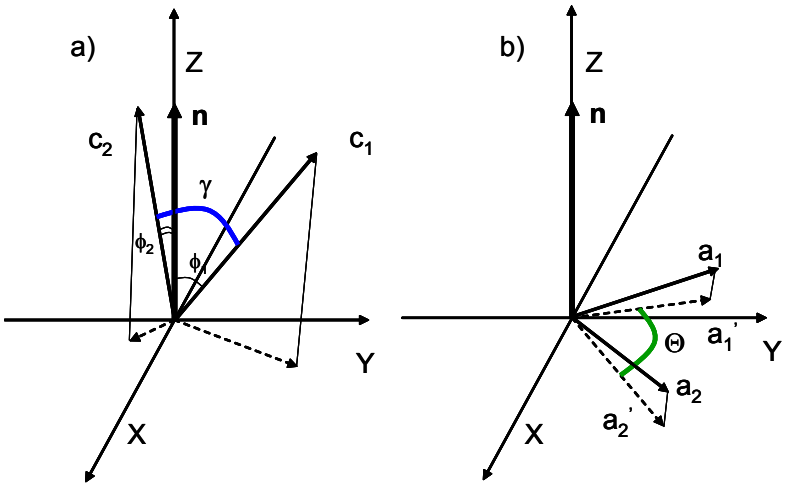

Fig. 112. Definition of misorientation angles. X-Y is the specimen plane. (a) Out-of-plane misorientation where γ is the angle between two c-axes; (b) In-plane misorientation, where Θ is the angle between the projection of two a-axes to the specimen plane.

The OIM data were collected with the standard TSL program and exported as a data file to our LabView-based program. Our program reduces the Euler angles to minimum misorientations between neighboring points, applying the usual tetragonal (a = b) symmetry simplification to the YBCO unit cell. Since GBs in CC grown on RABiTS are much more random compared to PLD films grown on bicrystal substrates. As shown in Fig. 112, we define the out-of-plane misorientation angle γ as the minimum angle between the c-axes of neighboring OIM data points. This angle entangles both pure [100]-tilt and [100]-twist components. Figure 112b shows how we define the in-plane misorientation angle Θ as the minimum angle between projections of the a-axis on the sample plane. For small out-of-plane misorientations, the misorientation is indeed very similar to a pure [001]-tilt. The rotation angle was calculated in the standard way and corresponds to the minimum angle required to bring two neighboring crystal lattices into coincidence around the common axis.

Since our aim is to study influence of low angle GBs, we used SEM images to select regions without

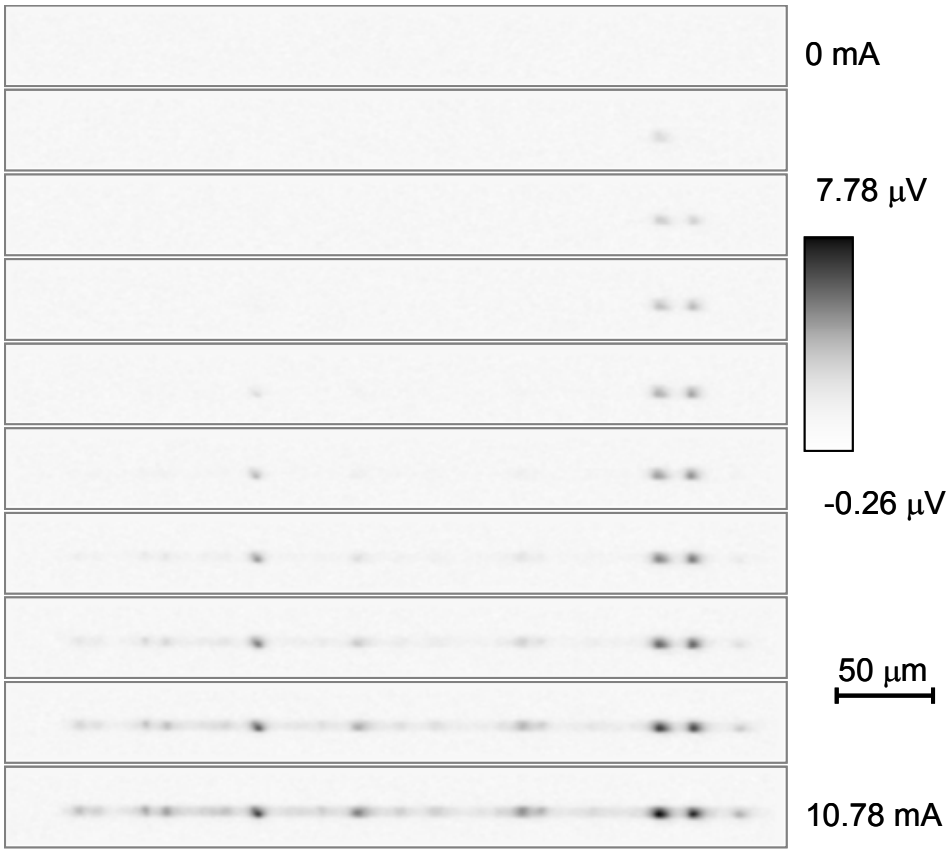

Fig. 113. Selection of voltage response maps used for I_c profile calculation. T=77 K, B= 2 T. The bias current is ranging from zero to 10.78 mA.

obvious major defects such as scratches or a-axis grains before patterning the quasi-1D links. We used AMSC 0.8 μm thick MOD CC on RABiTS for the studies. The ~6 μm wide quasi-1D link was cut with the FIB and the pattern finished with laser ablation.

In additional experiments, the bias current (I_{bias}) was increased in small steps: ΔI_{bias}=0.3 mA. About 35-37 automatic dV scans were taken at each magnetic field. The I_{bias} ranged as high as ~20 I_c. The dV measurements were repeated for different field values up to 5 T. In all measurements the field was perpendicular to the sample plane.

Comparison of in-plane and out-of-plane disorientation maps calculated for two different YBCO films

We analysed OIM maps taken on YBCO CCs grown on different RABiTS substrates. One YBCO film was 0.3 4μm thick with $\Delta\omega \approx 5^o$, $\Delta\varphi \approx 6^o$. It was grown by an ex-situ BaF_2 technique (grown by Ron Feenstra, ORNL) on older RABiTS from AMSC. Another 0.55 μm thick YBCO PLD film with $\Delta\omega \approx 2.5^o$, $\Delta\varphi \approx 5^o$ was grown on a more modern RABiTS from AMSC (grown by Pei Li). To preserve flatness, both films were glued on Cu plates with Stycast. Using a Nd-YAG laser we patterned arrays of dots with spacing about 150 μm on both films. Each dot is about 6 μm in diameter. These arrays define the area where we did the OIM scanning and were used to correlate the OIM and SEM images. To reduce number of misindexed points, the top ~10-12 nm of YBCO, which was potentially damaged, was removed by Ar milling. No mechanical polishing was used. The OIM scanning was done with a Carl Ziess 1540 EsB SEM. The scanning area was about 460 μm X 160 μm and was scanned with 1 μm steps. We studied 8 areas of YBCO on old RABiTS and 8 areas of PLD YBCO on modern RABiTS.

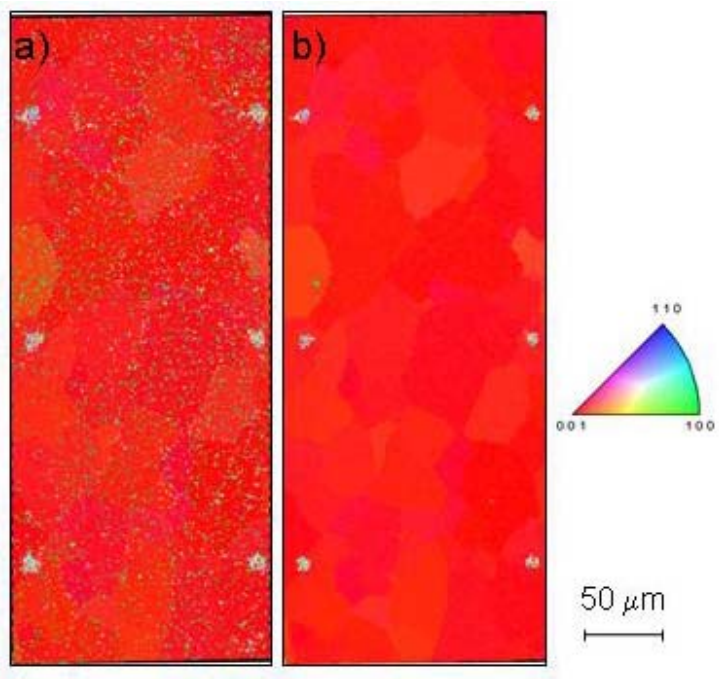

Fig. 114. Inverse Pole Figures and IP GB maps for YBCO grown on older RABiTS. (a) IPF before cleaning the data. Most of green [100] oriented data points correspond to misindexed data due to the similarity of EBSD patterns for the [100] and [001] orientations. Clusters of strongly misoriented data points near the edges of the scanned areas are the laser-cut alignment marks. (b) IPF after one iteration of dilation cleaning. Triangular color scale on the right is valid for both maps. The length marker is the same for both maps. YBCO area about 410 μm X 170 μm was scanned with 1μm. per step.

The data acquisition parameters for the TSL-OIM program were adjusted toward larger binning pattern size, longer time constants, and lower camera gain to get higher quality Kikuchi diffraction patterns. For indexing purposes, YBCO was considered to be tetragonal. To get the average c-axis direction perpendicular to the sample plane the raw OIM data were manually rotated (about 1^o-3^o) in the TSL program.

It is well known that EBSD patterns are similar for perpendicular orientations [27] in YBCO. Therefore the presence of noise in the diffraction Kikuchi patterns causes some fraction of the EBSD data points to appear as though they are rotated by 90°. Figure 114 shows inverse pole figures (IPF) plotted using raw and processed data that had been cleaned up. Data points that are rotated 90° due to the noise points are expected to be misindexed [27] and are not clustered except in very small area (see the left middle part of Fig. 114b). Almost every one of these misindexed points is surrounded by correctly indexed points, which allows us to use the standard grain dilation cleaning (one iteration) to get a clean IPF map (Fig. 114b). To illustrate the fraction of such misindexed points in the raw data is really small, in Fig. 115 we plot number fraction of <100> indexed directions as a function of the alignment angle with respect to the direction normal to the sample plane. Only ~4.2% of the points are due to grains that were miscalculated to have their normal direction between 0° and 10° rather than between the proper angles of 80°-90°.

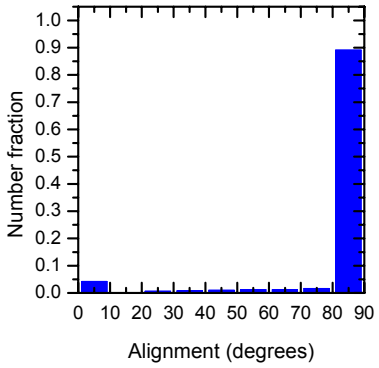

Fig. 115. Crystal direction graph <100>[001] generated with the TSL program before the cleaning procedure was applied. The plot shows the number fraction of <100> indexed directions that are rotated at angle "Alignment" to the normal direction ([001]) of the sample. Only 4.2% of <100> appeared aligned with their normal direction within angles between 0° and 10°. Here we used the same OIM data that was used for Fig. 114.

Splitting In-Plane (IP) and Out-Of-Plane (OOP) maps and analyzing them

Cleaned data were exported from the TSL program as a file containing Euler angles for use with a LabView-based program we wrote to separate the IP and OOP portions of the widely used relative rotation disorientation angle. Here we use the definitions for misorientation and disorientation from V. Randal and O. Engler [28]. Misorientation is the orientation difference between two individual orientation measurements, usually of the same phase. Disorientation is the lowest angle crystallographically-related solution of a misorientation. To calculate disorientation angles from TSL data we start with two sets of Euler angles (φ_1,Φ,φ_2) and ($\varphi`_1,\Phi,\varphi`_2$) for neighboring cells from the data file. Treating the YBCO unit cell as tetragonal, each set of Euler angles is reduced to get the minimum rotation angle Θ_1 between the crystal main axes and specimen coordinate system. Here we consider the **a** and **b** axes to be indistinguishable. Then we apply a procedure we described in the Q-1 report for to calculate the OOP disorientation angles and procedures that utilize the Rodriguez vector to calculate IP disorientation angles. Typical GB disorientation maps for both film types are plotted in Fig. 116 with the same spatial and discrete angle scales. It takes about a two minutes to calculate the IP and OOP maps in Fig. 116 with our program. Such maps are useful to compare with electric field distribution maps, which may help improve our understanding of current limiting effects due to different GBs. The relative rotation angle maps (Figs. 116a and 116b) show the minimum rotation angles for neighboring OIM points. Small, highly misoriented clusters near the scan edge are due to the laser dots described earlier. Note that the disorientation varies by 2°-3° along the GB. The background of Fig. 116a corresponds to 0°-2°, in contrast to 0°-3° for the PLD sample (Fig. 116d). This may be related to differences in the YBCO thickness, growth process, and quality of buffer layers. IP maps are qualitatively similar for both films consisting of continuous GB networks for film grown on modern (Fig. 116b) and on older (Fig. 116e) RABiTS.

The background is also similar for the IP maps. GBs in CC strongly affect transport properties by limiting supercurrent therefore it is the *continuous GB networks* that are more critical to investigate than scattered segments, since supercurrent may avoid the scattered GB segments. We observe striking differences between the OOP GB maps for the two films. The OOP GB map (Fig. 116c) for YBCO grown on older

RABiTS is a continuous network with many OOP GB angles >3°. In this sample the OOP GB network is more extended (Fig. 116c) than the IP GB network (Fig. 116b). In contrast, the OOP GBs in the YBCO

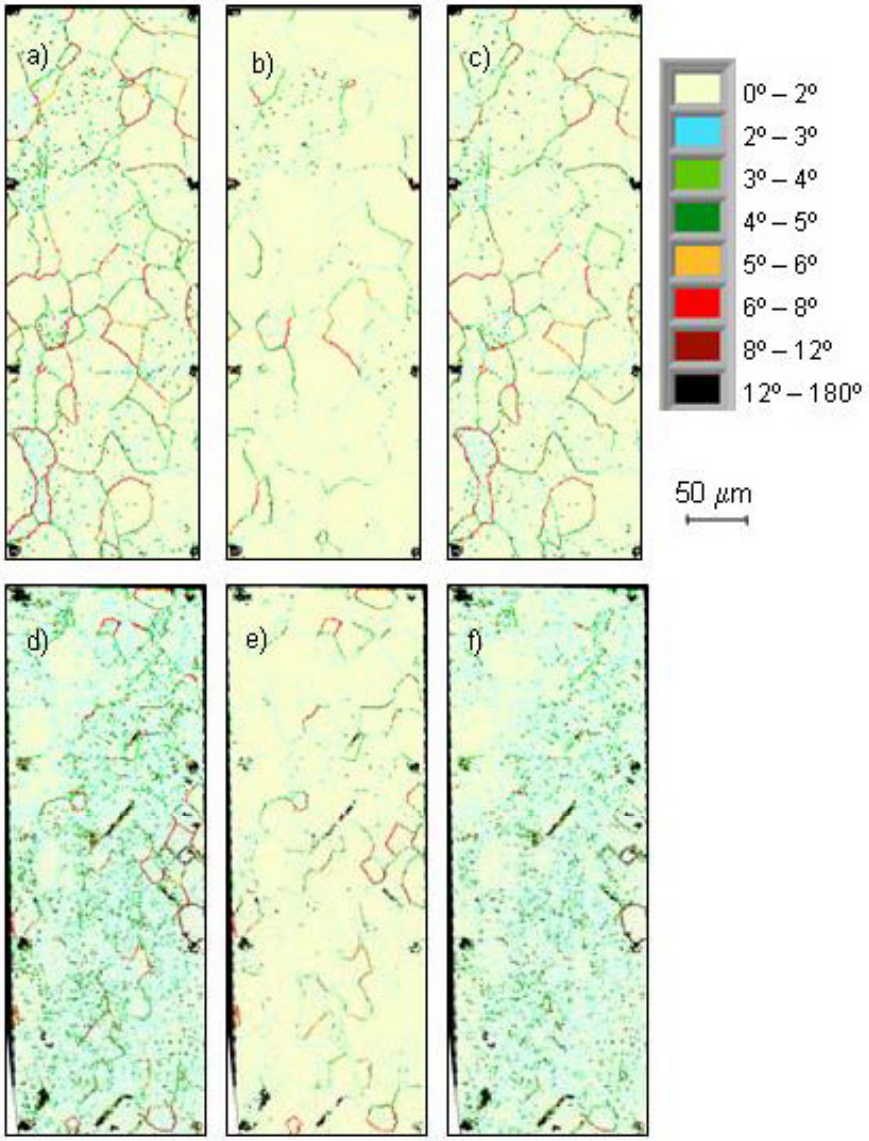

Fig. 116. GB maps from different CC. The upper row of GB maps were calculated for YBCO CC grown on the older RABiTS. The bottom row of GB maps were calculated for YBCO on modern RABiTS. (a,d) Rotation angle maps. (b,e) IP misorientation GB maps; (c,f) OOP misorientation GB maps.

on the newer RABiTS are widely dispersed with rare exceptions, and do not form a continuous network (Fig. 116f) The enhanced background is attributed to the OOP GB type as from comparing IP and OOP maps for YBCO on modern RABiTS. Scattered GBs in the YBCO sample on newer RABiTS expected to be less influential to transport properties of the CC, *because the supercurrent can go around these individual GBs.* These GB features are common for all measured areas.

Statistics of IP and OOP angles

To visualize statistics of the IP and OOP GB types in Fig. 117 we plotted the number of GBs as function of IP and OOP components for the same two samples shown in Fig. 116. The plots in Fig. 117 are entirely new way to present the IP and OOP data that we developed using our new LabView based program. In Fig. 117 white corresponds to a higher density of the specific type of GB (IP or OOP), blue corresponds to a lower intensity, black means there are no GB with these IP or OOP angles. For both samples the density of OOP GBs is larger than the number of IP GBs. Also the maximum density of OOP GBs have less than 1^o of rotation angle. However the distribution is different: for YBCO on the modern RABiTS more IP GB appear for larger rotation angles than in the YBCO on the older RABiTS. We calculated the ratio (R_{tot}) between the total number of GBs with a larger OOP component and the total number of GBs with a larger IP component for all measured samples and present the data in Table 13. For YBCO on modern RABiTS the R_{tot} is larger than for YBCO on older RABiTS. However it is opposite for the ratio $R_{\Theta>3}{}^o$ calculated for the selection of GBs with the rotation angle $>3^o$. The OOP is still dominant for YBCO on modern RABiTS above 3^o.

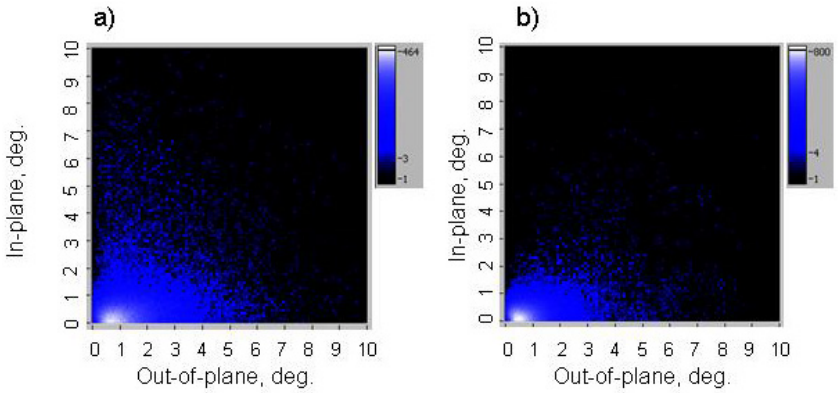

Fig. 117. Number of GBs as a function of IP and OOP misorientation components: (a) for YBCO grown on modern RABiTS; (b) for YBCO grown on older RABiTS.

Type of RABiTS	R	Sample Number								<R>	R_{SE}
		1	2	3	4	5	6	7	8		
modern RABiTS	R_{tot}	6.12	6.09	6.9	5.11	7.44	6.85	5.92	6.60	**6.37**	**0.25**
	$R_{\Theta>3}{}^o$	2.11	3.02	2.24	1.86	2.91	2.08	2.88	2.64	**2.46**	**0.16**
old RABiTS	R_{tot}	4.02	5.01	3.92	4.22	4.04	3.83	4.65	3.73	**4.17**	**0.16**
	$R_{\Theta>3}{}^o$	4.34	3.87	3.44	4.21	3.38	2.27	3.32	3.01	**2.93**	**0.24**

Table 13. The ratio $R_{tot} = N_{OOP}/N_{IP}$ is shown for all measured samples as well as ratio $R_{\Theta>3}{}^o$ for selection of GB with the rotation angle larger then 3^o. <R> is the average R over samples and R_{SE} is the standard error.

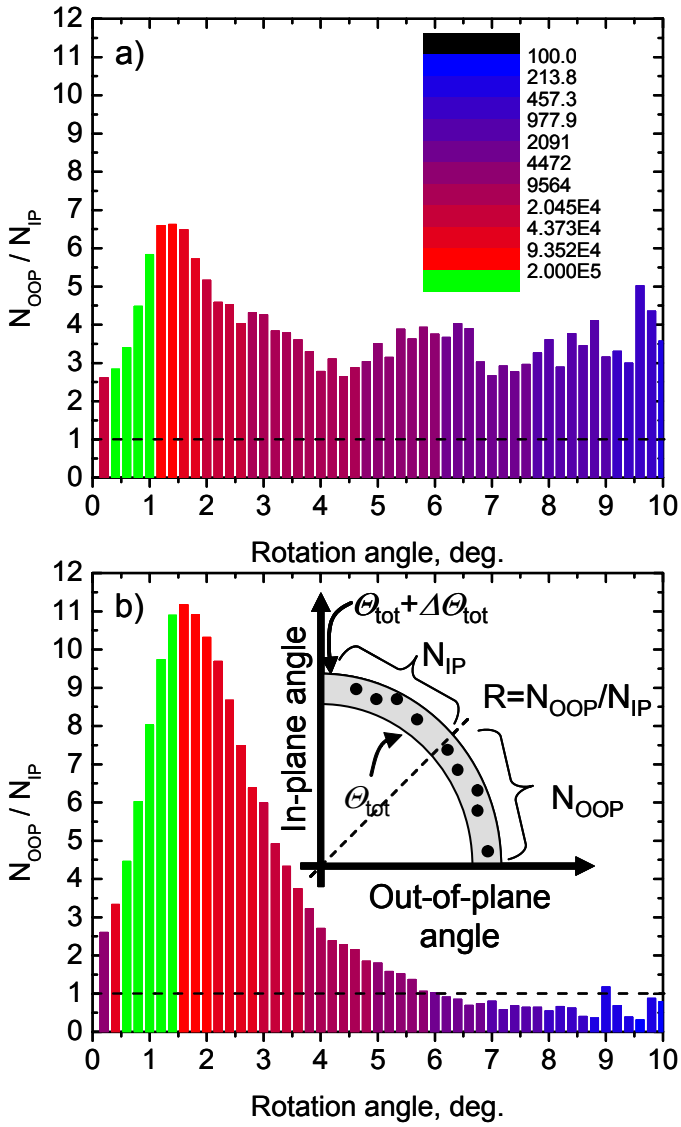

Fig. 118. The ratio N_{OOP}/N_{IP} as a function of the relative rotation angle (Θ_{tot}) plotted for YBCO on the two RABiTS substrates. The ay to calculate this ratio is clarified in the insert of (b), where a graph like that in Fig. 4 is shown schematically. Data for these graphs came from all scanned areas. Color marks the density of the total number of GBs per 10^6 μm^2. The area was scanned with 1 μm steps. (a) The ratio for the YBCO sample on older RABiTS is above 2.64 for $\Theta_{tot}<10^o$. (b) N_{OOP}/N_{IP} for YBCO grown on modern RABiTS is considerably larger for the low-angle region $\Theta_{tot}<3^o$, but it decreases below one for $\Theta_{tot}>5.75^o$.

GBs with low rotation angle disorientation do not effectively reduce J_c. As is well known from transport measurements, the critical rotation angle at which a GB effectively reduces J_c is about 2^o-3^o. Therefore we calculated the ratio R as function of Θ_{tot}. The number of GBs with larger OOP component from the layer $[\Theta_{tot}; \Theta_{tot}+\Delta\Theta_{tot}]$ is divided into the number of GBs with a larger IP component within the same range of

rotation angle; here $\Delta\Theta_{tot} = 0.2^o$. This definition is graphically shown in the inset of Fig. 118b. For ex-situ BaF_2 film on older RABiTS the OOP component dominates for all rotation angles (see Fig. 118a). We observed that the $R(\Theta_{tot})$ for YBCO on older RABiTS is above 2.64 for $\Theta_{tot}<10^o$ and has two local maximums at $\Theta_{tot}\approx1.5^o$ and at $\Theta_{tot}\approx6^o$. A much larger ratio $\mathbf{N_{OOP}/N_{IP}}$ was observed for PLD on modern RABiTS for low relative rotation angles, but it sharply decreases below one at $\Theta_{tot}>5.75^o$.

Associated work of interest to this program but supported by other funds:

S. Lee, J. Jiang, J. D. Weiss, C. M. Folkman, C. W. Bark, C. Tarantini, A. Xu, D. Abraimov, A. Polyanskii, C. T. Nelson, Y. Zhang, S. H. Baek, H. W. Jang, A. Yamamoto, F. Kametani, X. Q. Pan, E. E. Hellstrom, A. Gurevich, C. B. Eom, D. C. Larbalestier, "Weak link behavior of grain boundaries in Co-doped BaFe2As2 pnictide superconductors" accepted for Applied Physics Letters 2009.

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Cryogenic Dielectric Research and Test Facility

(H. Rodrigo)

Introduction, Background

We have investigated the electrical breakdown behavior of several materials, namely; ThermaVolt, Polymethyl Methacrylate (PMMA), PMMA + 5% by weight of Barium Titanate (BTA) and G10 at both room temperature (293 K) and liquid nitrogen temperature (77 K). Also presented are results of tanδ measurements (dielectric loss) for ThermaVolt , PMMA, PMMA +5% BTA at these temperatures. 60 Hz AC high voltage surface flashover measurements have been done for G10 cylindrical samples. For all other materials, electrical breakdown measurements have been done at 60 Hz AC high voltage and under lightning impulse voltages whose waveform is 1.2/50μs.

Proposed Work / Purpose and Objectives

We have studied the dielectric properties of three materials two of which are used extensively in the manufacture of transformers, cables, motors and magnets. One of the materials we have fabricated. The known materials are: Thermavolt and G10. Theremavolt was supplied by L-3 Communications, of California. G10 is a material used extensively in particular under cryogenic conditions. The material which we have fabricated is a nano-composite consisting of PMMA (Polymethylmethacrilate) + 5 % BTA (Barium Titanate).

The host resin being PMMA and the nano material being BTA, whose average particle size is 100 nm. PMMA is used as an insulating medium over a wide range of temperatures (77 K to 350 K). It exhibits high dielectric strength of the order of 13.5 MV/cm at around 77 K decreasing to about 7.5 MV/cm at around 325 K [29]. BTA has a very high relative permittivity, which is very sensitive to temperature and frequency; in addition it varies widely depending on the direction of the electric field to its crystal axis.

Approach and Results:

1. Figure 119 shows the experimental fixture used for AC breakdown measurements, under uniform field. Measurements were performed on Thermavolt, PMMA (Polymethyl Methacrylate), and PMMA with additive (5% weight) of Barium Titanate (BTA). Figure 120 shows the experimental arrangement for surface flashover in cylindrical G10. Measurements were carried out on cylindrical samples of G10, which were 5 mm long and diameters of 19 mm, 12.7 mm and 9.59 mm. All measurements were done at both 293 K and 77 K. The room temperature measurements were done in a bath of transformer oil (293 K), and, the measurements at 77 K were done in a bath of Liquid Nitrogen (LN). The electrodes used were made of Stainless Steel. They were 25 mm in diameter with Bruce profile. A fresh charge of oil was used after each breakdown. New electrodes were used for each experiment.

Figure 119. Sample Holder

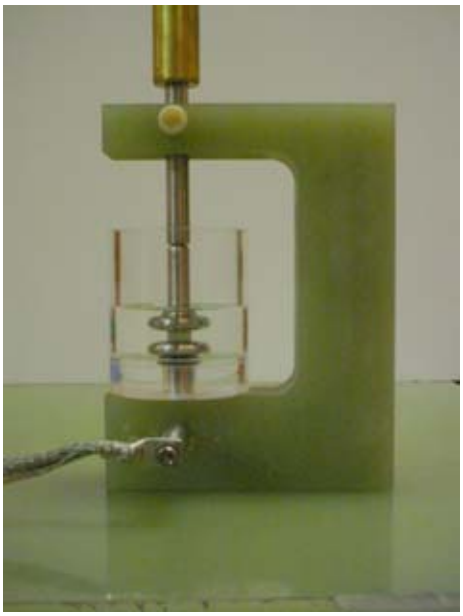
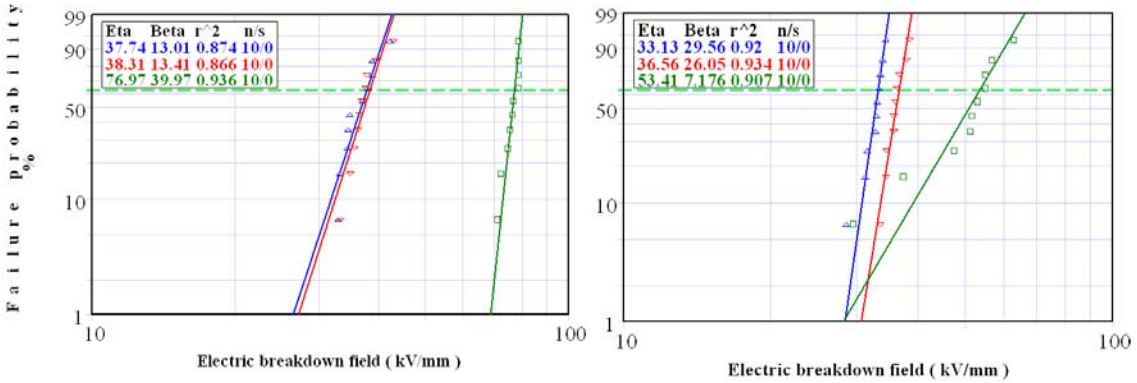


Figure 120. G10 Sample In Holder

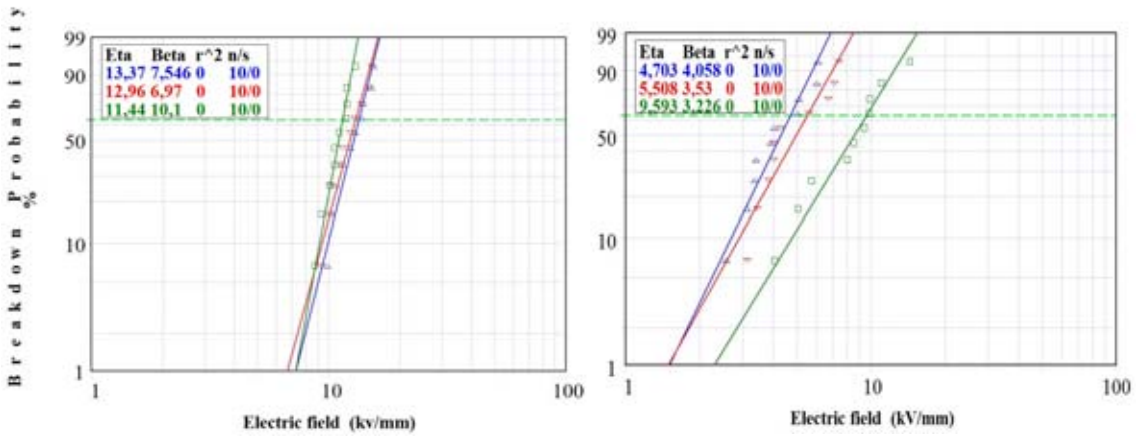


Δ – PMMA + 5% BTA

∇ – PMMA

□ – Thermvolt

Figure 121a and 121b. Weibull Plot for AC Breakdown; a: 77 K, b: 293 K



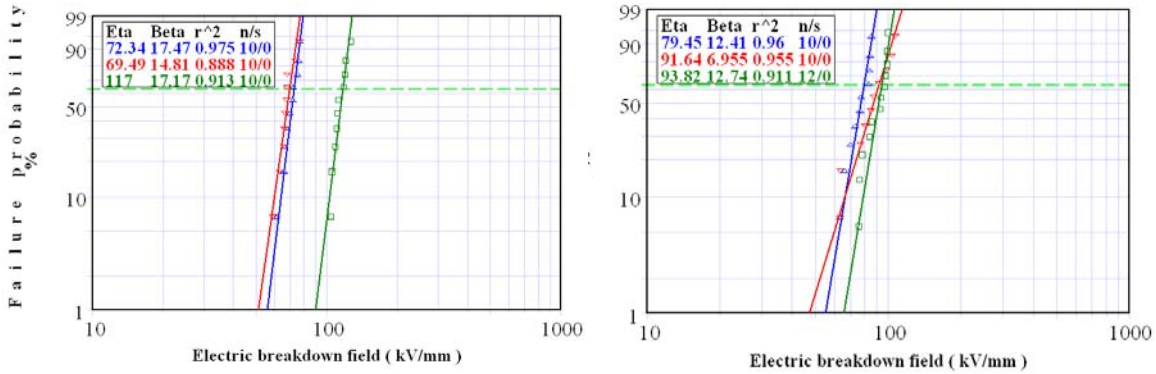
Δ – diameter 9,59mm

∇ – diameter 12,70mm

□ – diameter 19,00mm

Figure 122a and 122b. Weibull Plot for AC Breakdown of G10 cylinders; a: 77 K, b: 293 K

2. Lightning impulse measurements were done at the temperatures as stated above. The samples and electrode configuration used were identical in dimensions to the ones above.



Δ – PMMA + 5% BTA

∇ – PMMA

□ – Thermvolt

Figure 123a and 123b. Weibull Plot for Impulse Breakdown; a: 77 K, b: 293 K

3. The results obtained were analyzed using Weibul statistics for all measurements that were taken. The results have been presented in both graphical and tabular form.

   Figure 121(a) & (b) show the results for AC breakdown for neat PMMA, PMMA +5% BTA, and Thermavolt. Figures 122(a) & (b) show AC breakdown voltage results for cylindrical G10. Figures

123(a) & (b) show the results for impulse breakdown of neat PMMA, PMMA + 5% BTA, and Thermavolt.

	$(E_{b/d})_{63.2\%}$ (kV/mm)		β (shape factor)	
	293 K	77 K	293 K	77 K
Thermavolt	53.41	76.97	7.18	39.97
PMMA	36.56	38.31	26.05	13.41
PMMA+BTA	33.13	37.74	29.56	13.01

Table 14. Weibul Parameters for AC Breakdown

	$(E_{b/d})_{63.2\%}$ (kV/mm)		β (shape factor)	
	293 K	77 K	293 K	77 K
Thermavolt	93.82	117	12.74	17.17
PMMA	91.64	69.49	6.96	14.81
PMMA+BTA	79.45	72.34	12.44	17.47

Table 15. Weibull Parameters for Impulse breakdown

4. Dielectric loss measurements were done for PMMA, PMMA + 5 % BTA and Thermavolt, using the same electrode configuration on samples that were identical in dimension to those stated above and the measurements have been done at the two temperatures stated above. Figure 6 shows the experimental arrangement for tanδ measurements. Figures 125(a) & (b), 126(a) & (b), 127(a) & (b) show the results for tan δ as a function of voltage for Thermavolt, neat PMMA, and PMMA + 5% BTA, respectively, at temperatures 293 K and 77 K. Table 16 gives the relative permittivity values at the two different temperatures for all the materials studied.

Figure 124. Tan Delta Measurement System

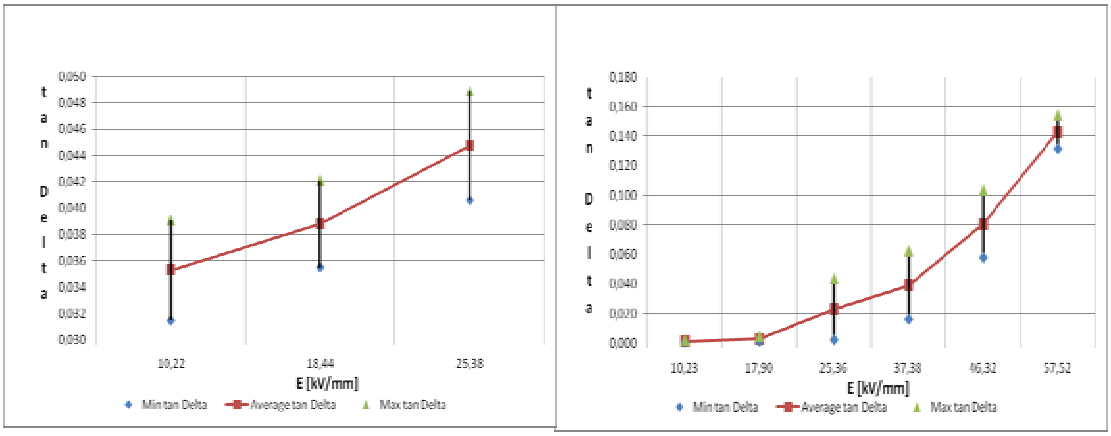


Figure 125a and 125b. Tan Delta vs. Electric field for Thermavolt; a: 293K, b: 77 K

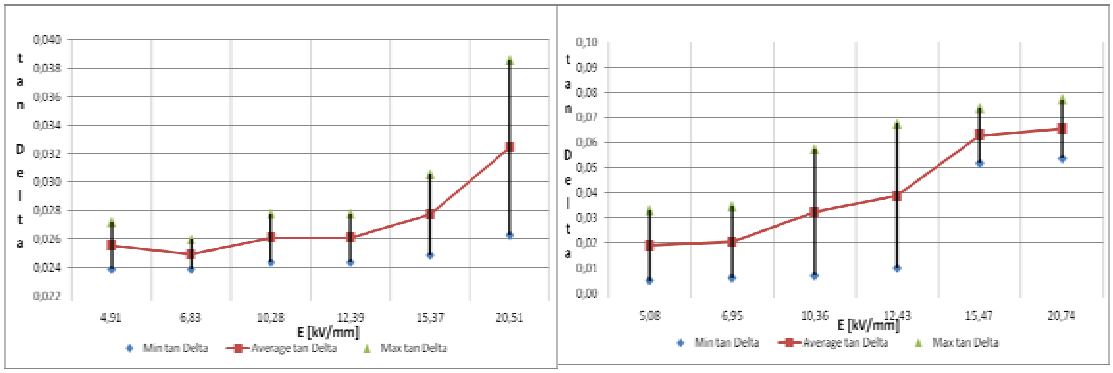


Figure 126a and 126b. Tan Delta vs. Electric Field for PMMA; a: 293 K, b: 77 K

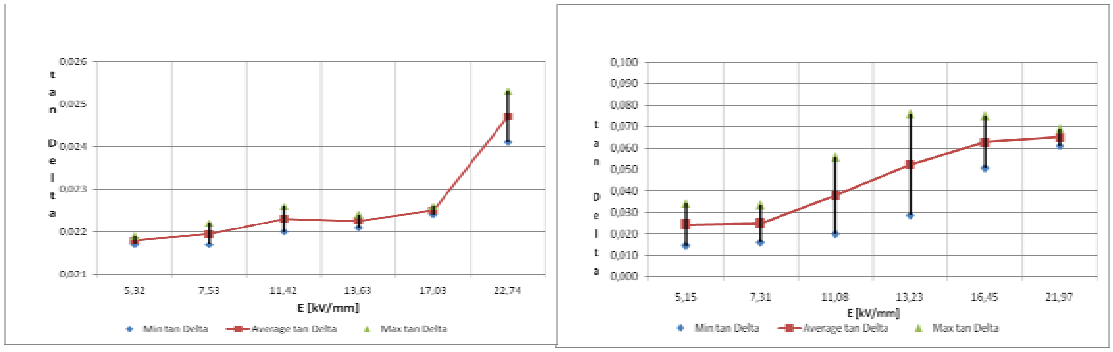


Figure 127a and 127b. Tan Delta vs. Electric Field for PMMA + 5% wt. BTA; a: 293 K, b: 77 K

	293K	***77 K***
Thermavolt	1.31	1.10
PMMA	2.72	2.64
PMMA+BTA	2.30	2.47

Table 16. Relative Pemittivity (ε_r)

Technology Transfer, Collaboration, Partnerships

We have made breakdown and dielectric loss measurements at 77 K and 293 K on transformer insulating material (ThermaVolt) supplied by L3 in California.

We have made contact with SuperPower for collaboration on studying suitable dielectric materials for the next generation of HTS wire. A similar collaborative effort has been established with the National High Magnetic Field Laboratory. Dielectric measurements have been carried out.

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PUBLICATIONS, PRESENTATIONS, AND PANEL/PAPER SESSIONS

Summarizing for all project areas:

Publications

Distributed Energy Resource Integration

1. Marchionini, B., Fall, N.K., Steurer, M., "An Assessment of Fault Current Limiter Testing Requirements" by Energetics, Inc., for U.S. Dept. of Energy, Office of Electricity Delivery and Energy Reliability, February 2009.
2. C. Schacherer, J. Langston, M. Steurer, and M. Noe, "Power Hardware-in-the-Loop testing of a YBCO Coated Conductor Fault Current Limiting Module," accepeted for publication in the IEEE Trans. Appl. Superconductivity, presented at Applied Superconductivity Conf., Chicago, IL, Aug. 2008.
3. L. Qi, J. Langston, and M. Steurer, "Applying a STATCOM for Stability Improvement to an Existing Wind Farm with Fixed-Speed Induction Generators", in Proc. of the IEEE Power Engineering Society General Meeting, Pittsburg, PA, Jul. 2008.
4. Zhichao Wu, Liming Liu, Hui Li, "Extensive Real/Reactive Power Flow Control for a Single-stage Grid-connected Inverter Integrating with Micro Storage," *Proc. 6th International Power Electronics Conference, -ECCE Asia- (IPEC-Sapporo 2010)*, Sapporo, Japan, 2010

Grid Reliability and Security

1. Dale, S., Meeker, R., "Let's Build a Superhighway, "Moving to a Better Power Grid", EnergyBiz Magazine, November 2008.

High Temperature Superconductivity

1. Sastry Pamidi, Doan Nguyen, Guomin Zhang, David Knoll, Ulf Trociewitz, Justin Schwartz, "Variable Temperature Total AC Loss and Stability Characterization Facility," IEEE Transactions on Applied Superconductivity 19(2007) 3179
2. Guo Min Zhang, D.C. Knoll, D.N. Nguyen, P. V. P. S. S. Sastry, Justin Schwartz, "Temperature Dependence of Critical Currents and AC Transport Losses in (Bi, Pb)2Sr2Ca2Cu3Ox and YBa2Cu3Oy Tapes,", Supercond. Sci. and Technol. 20 (2007) 516
3. Doan N. Nguyen, Pamidi V. P. S. S. Sastry, and Justin Schwartz, "Numerical calculations of the total ac loss of Cu-stabilized YBa2Cu3Oy coated conductor with a ferromagnetic substrate," J. Appl. Phys. 101 (2007) 053905
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5. D. Abraimov, A. Gurevich, A. Polyanskii, X.Y. Cai, A. Xu, S. Pamidi, D. Larbalestier, and C.L.H. Thieme, "Significant Reduction of AC Losses in YBCO Patterned coated conductors with transposed filaments," Superconductor Science and Technol., 21 (2008) 8/2004.

6. D. Nguyen, S. Pamidi, D.C. Knoll, and J. Schwartz, "Temperature Dependence of Total AC Loss in High Temperature Superconducting Tapes", IEEE Transactions on Applied Superconductivity, 19 (2009) 3637
7. Guo Min Zhang, Liang Zhen Lin, Li Ye Xiao, Yun Jia Yu, Sastry V. Pamidi, Justin Schwartz, "Quench Behavior of Bi2Sr2Ca2Cu3Ox/Ag Tape with AC and DC Transport Currents and a Comparison with YBa2Cu3Ox Conductors, " IEEE Transaction on Applied Superconductivity Vol. 20, No. 3, June 2010, 2146.
8. D. C. van der Laan, T.J. Haugan, P.N. Barnes, D. Abraimov, F. Kametani, D. C. Larbalestier and M.W. Rupich, "Effect of strain on grains and grain boundaries in $YBa_2Cu_3O_{7-\delta}$ coated conductors", invited paper to special edition on YBCO Supercon. Sci. and Technology, 2010.
9. J. Kvitkovic, J. Voccio and S. V. Pamidi, "Shielding of AC Magnetic Fields by Coils and Sheets of Superconducting Tapes," To be published in IEEE Transactions on Applied Superconductivity (Accepted for Publication).

Cryogenic Dielectric Research

1. H. Rodrigo, W. Baumgartinger, A. Ingrole, Z (Richard) Liang, D.G. Crook and S.L. Ranner, "Dielectric Breakdown of Transformer Insulation Materials Under Cryogenic and Room Temperatures", Proceedings of Materials Research Society, Symposium BB paper number BB3.10, June 2009.
2. H.Rodrigo[1,a], G.H.Heller[1,b], A.Ingrole[2,c], Z (Richard) Liang[2,d], D.G.Crook[1,e], S.L.Ranner[1,f], "Electric Field Breakdown of Polymer Based Nano-Composite at Room and Cryogenic Temperatures", 12th International Conference on Modern Materials, June 6 – 11 2010 , Italy (in press).

Presentations, Panels, Paper Sessions

In the previous section, any authored papers for conference proceedings were all accompanied by presentations at the respective conferences for which they were authored; these are not repeated in this section.

Distributed Energy Resource Integration

1. M. Steurer, "Task Force on Fault Current Limiter Testing", Eighth Annual EPRI Superconductivity Conference, Oak Ridge, TN, November 12 – 13, 2008.

High Temperature Superconductivity

1. "Integration and Application of Cryocoolers for Advanced Characterization of high Temperature Superconducting Components," Presented at the International Cryocooler Conference, , Long Beach California, June 9-12, 2008.
2. S. Pamidi, "AC Loss Characterization of HTS Materials," 2008 DOE Peer Review, Washington DC, July 29-31, 2008.
3. Presentations to D. Haught, visiting ASC and CAPS, January 21, 22, 2009.
4. "Measurement of AC Losses in Superconducting Tapes and Coils Using Liquid Nitrogen Boil-off Technique," Sastry. Pamidi, 2009 CEC-ICMC, Tucson, AZ, June 27-July2, 2009.

5. “Measurement of AC Losses in Superconducting Tapes and Coils Using Liquid Nitrogen Boil-off Technique”, 2009 CEC-ICMC, Tucson, AZ, June 27-July2, 2009.
6. D. C. van der Laan, T.J. Haugan, P.N. Barnes, D. Abraimov, F. Kametani, D. C. Larbalestier and M.W. Rupich, “Effect of strain on grains and grain boundaries in $YBa_2Cu_3O_{7-\square}$ coated conductors”, invited paper to special edition on YBCO Supercon. Sci. and Technology. Accepted to appear 2010.
7. D. Abraimov, E. Hellstrom, and D. Larbalestier, “Integrated study of current density and current limiting mechanisms in coated conductors”, DOE Peer Review, , Alexandria, VA, Aug. 2009.
8. D. Larbalestier, “Superconductors for future high field use: Why not multifilamentary YBCO - or something even better?”, Institute for Technical Physics Colloquium, Research Center Karlsruhe, Germany, September 8, 2009.
9. S. Pamidi, “AC Losses Measurements in Superconducting Tapes and Coils Using Liquid Nitrogen Boil-off,” The 9th European Conference on Applied Superconductivity, EUCAS 2009, Dresden, Germany, September 13-17, 2009.
10. S. Pamidi, “AC loss Measurements in 2G Coated Conductor Coils Using Liquid Nitrogen Boil-off and Electrical Methods”, Presented at the 2009 KEPRI-EPRI Joint Superconductivity Conference, Daejeon, Korea , November16-18, 2009.
11. S. Pamidi, “AC Characterization of Superconducting materials”, 14th US-Japan Workshop on Advanced Superconductors, Tallahassee, Florida Dec. 14-15, 2009.

Cryogenic Dielectric Research

3. H. Rodrigo, Z.(Richard) Liang, A. Ingrole, S.L. Ranner and D.G. Crook, “Characterization of Dielectric Materials Under Cryogenic Conditions”, Applied Superconductivity Conference, Chicago, August 2008.
4. H. Rodrigo, W. Baumgartinger, A. Ingrole, Z.(Richard) Liang, D.G. Crook And S.L. Ranner, “Dielectric Breakdown Of Transformer Materials At Room And Cryogenic Temperatures”, Materials Research Society, Annual Fall Meeting, December 2008.
5. H.Rodrigo, W.Baumgartinger, G.H.Heller, D.G.Crook and S.L.Ranner, “Surface Flashover Voltage of Cylindrical G10 Under AC and DC Voltages at Room and Cryogenic Temperatures”, to be presented at Applied Superconductivity Conference, Washington DC August 2010.
6. H. Rodrigo, G. Heller, R.E. McClellan J. Kvitkovic, and S. Pamidi, “Inter-turn dielectric properties of YBCO coils”, to be presented at Applied Superconductivity Conference, Washington DC August 2010.

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PATENT AND INTELLECTUAL PROPERTY (IP) ACTIVITY

1. "A Grid-interactive inverter with Energy Storage Elements". The co-PI (H. Li) is filing a Disclosure and Florida State University is filing a Provisional Patent Application, with intent to file a Utility Patent Application for invention(s) described in this section related to improved grid-interactive converter/inverter system control, performance, and cost.

COLLABORATIONS

INITIATIVE	*COLLABORATORS*
Distributed Energy Resource Integration	American Superconductor (AMSC) Bonneville Power Administration (BPA) Electric Power Research Institute (EPRI) Greensmith Energy Management Systems North Carolina State University (NCSU) Oak Ridge National Laboratory (ORNL) Sandia National Laboratory (SNL) Southern California Edison (SCE) Tennessee Valley Authority (TVA) University of South Florida (USF)
Grid Reliability and Security	Florida Reliability Coordinating Council (FRCC)
HTS AC Loss and Quench Propagation	Applied Superconductivity Center at the National High Magnetic Field Laboratory Several magnetization loss measurements were carried out as part of collaboration with Applied Superconductivity Center, National High Magnetic Field Laboratory in support of low ac loss conductor design. Super Power Collaborative work on AC losses. A new sample holder to measure AC losses on long samples has been designed to suit the needs of Super Power. Staff scientists from Super Power will visit in the second quarter to make some measurements and to discuss potential long-term collaborations. AC loss measurements were performed on several coils and tape samples of YBCO superconductor in collaboration with Super Power as part of cost-share agreement.

INITIATIVE	*COLLABORATORS*
	Ohio State University VAMAS round robin measurements on a series of Z-stack samples of YBCO coated conductors. The program is organized by the Ohio State University to establish and recommend measurement techniques for magnetization loss measurements on YBCO coated conductors.
	Launch Point Technologies Inc. Assistance with high frequency losses in high-purity copper cryogenic temperatures for extremely low-friction transport for high-speed transportation and electromagnetic launch applications.
Current Density and Current Limiting Mechanisms in Coated Conductors	American Superconductor (Li, Rupich) Argonne National Laboratory Oak Ridge National Laboratory (Feenstra) Los Alamos National Laboratory
Cryogenic Dielectrics	L3 Communications Furnishing insulating samples (typically used in transformers) for ac breakdown measurements. National High Magnetic Field Laboratory Certain measurement (e.g. SEM) and lab capability development support.

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