Final Report

Sections 1 and 2

Project Title: “Thin, High Lifetime Silicon Wafers with No Sawing; Recrystallization in a Thin Film Capsule”

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Section 3: Executive Summary

Overview for general public. The project fits within the area of renewable energy called photovoltaics (PV), or the generation of electricity directly from sunlight using semiconductor devices. PV has the greatest potential of any renewable energy technology. The vast majority of photovoltaic modules are made on crystalline silicon wafers and these wafers accounts for the largest fraction of the cost of a photovoltaic module. Thus, a method of making high quality, low cost wafers would be extremely beneficial to the PV industry. The industry standard technology creates wafers by casting an ingot and then sawing wafers from the ingot. Sawing rendered half of the highly refined silicon feedstock as un-reclaimable dust. Being a brittle material, the sawing is actually a type of grinding operation which is costly both in terms of capital equipment and in terms of consumables costs. The consumables costs associated with the wire sawing technology are particularly burdensome and include the cost of the wire itself (continuously fed, one time use), the abrasive particles, and, waste disposal. The goal of this project was to make wafers directly from molten silicon with no sawing required.

The fundamental concept was to create a very low cost (but low quality) wafer of the desired shape and size and then to improve the quality of the wafer by a specialized thermal treatment (called re-crystallization). Others have attempted to create silicon sheet by recrystallization with varying degrees of success. Key among the difficulties encountered by others were: a) difficulty in maintaining the physical shape of the sheet during the recrystallization process and b) difficulty in maintaining the cleanliness of the sheet during recrystallization. Our method solved both of these challenges by encapsulating the preform wafer in a protective capsule prior to recrystallization (see below). The recrystallization method developed in this work was extremely effective at maintaining the shape and the cleanliness of the wafer. In addition, it was found to be suitable for growing very large crystals. The equipment used was simple and inexpensive to operate. Reasonable solar cells were fabricated on re-crystallized material.

Further details. The fundamental concept was to encapsulate a preform wafer in a thin film capsule, typically of SiO_2 , which capsule would then retain hold the silicon melt in shape during re-crystallization.

The crystallographic and dislocation density characterization of the re-crystallized material and the fabrication and testing of solar cells on this material were two of the areas of focus for the effort. We were commonly able to produce cm sized grains. Occasionally a full sample of 25 x 100mm was a single crystal. Dislocation densities were demonstrated to be lower than

industry-standard cast multicrystalline material. Small champion solar cells had efficiencies of 15% based on active area (with no light trapping texture on the front).

A great deal of attention was paid to the nature and effect of the thin film capsule used. Two refereed journal papers resulted from the development of an understanding of the interaction of the capsule material and the silicon. One primary tool was to assess the degree of undercooling that a given capsule material would sustain and this was found to correlated well with the ability of the capsule to result in low nucleation and large grains.

Another area of work was the design and construction of the re-crystallization furnace itself. This furnace went through at least five iterations and its design was guided by the goal of operation in air – a huge opportunity for the technology to achieved which was enabled by the fact that the thin film capsule protects the silicon from oxidation.

The modeling and measurement of the temperature profiles during re-crystallization was also a major focus and fueled an iterative approach to modification of heating and cooling profiles so as to attain improved properties in the re-crystallized material. A novel technique for measuring wafer temperature was developed in which a wafer was implanted with opposing species of dopant (one n-type and one p-type) and then subjected to the temperature profile in question. Sheet resistance measurements maps were then used to infer the temperature profile. A refereed journal paper was published on this method.

Section 4. Comparison of the actual accomplishments with the goals and objectives of the project.

From SOPO : Task 1: *Modeling and Verification of Temperature and Stress profiles*. The cooling profile plays a key role in determining the thermal stresses that are generated during recrystallization and in consequence, the dislocation density. The cooling profile will be modeled using available heat transfer modeling packages. We will measure the temperature profile, both using tracing thermocouples and using methods that allow for temperature measurement with a wafer in place. We will recrystallize wafers under different cooling profiles, etch and measure dislocation densities. The goal will be to achieve dislocation densities lower than $1E5/cm^2$ by end of year 1 and lower than $3E4/cm^2$ by end of year 2.

Accomplishments: We were quite successful in both measuring and modeling of the temperature profiles in the recrystallizing material using conventional methods (thermocouples) and also using a novel method based on diffusion of dopants within the material and reported on later in this document (and in a journal paper). Stresses in the recrystallized material were found to be low – as inferred from good handling of the material. A wide variety of cooling profiles were used and dislocation densities routinely measured below $1E5$ per cm^2 .

From SOPO Task 2: *Design, Construction and Control of Recrystallization Furnace*. Materials of construction will be chosen and tailored for use in our furnace such that the environment remains clean. Control based on radiometric pyrometers will be implemented.

Accomplishments: We went through several generations of design of the recrystallization furnace as described in the document below. A key aspect was to retain the ability to operate the furnaces in air (rather than under inert gas). A new type of insulation was developed (made of silicon carbide) which allowed for clean operation in air. Heaters were developed. Pyrometers were used for closed loop control of the furnace

Task 3. *Superior Electrical Properties*. We will investigate and seek to control grain nucleation, grain size, and dislocation density through control of cooling profiles. We will characterize these properties. We will also measure minority carrier lifetimes and correlate to these properties.

Accomplishments: We were quite successful at control of grain size. In fact some single crystal samples were created. We did extensive work on different capsule materials and studied their effect on nucleation – resulting in two journal papers. As mentioned above, dislocation densities below $1E5$ were routinely observed.

Task 4. *High Efficiency Devices*. We will investigate and seek to control impurity levels. We will fabricate and measure cell performance.

Accomplishments: 15% efficient cells were fabricated based on active area.

Section 5. Summary and Discussion of Project Activities

5.1 Technical Approach

Our approach is to produce wafers without sawing, by using rapid solidification to first define the wafer geometry and then, in a subsequent step, to recrystallize the wafer in order to create large, high quality grains. An enabling invention provides for geometric and chemical integrity of the wafer during recrystallization. The key idea underlying this program is to encapsulate the wafer to be re-crystallized capsules in a thin film capsule, typically made of SiO_2 . In a typical procedure, the wafer to be recrystallized was placed in a tube furnace and an oxide film was grown over the entire wafer so as to encapsulate it. This film was typically micron thick, although even thinner capsules were found to work. This thin film capsule was found to have sufficient integrity to hold the silicon in place as it was melted and then re-solidified during the recrystallization. The capsule also serves to protect the wafer from the ingress of impurities during the re-crystallization process. Importantly, the re-crystallization can be run in a wide range of atmospheres, including ambient air. This is because the silica capsule heals itself by oxidation, should any crack develop.

The graphics below illustrates the basic concept. Figure 1 shows the rapid solidification to produce the wafer pre-form. Figure 2 shows the recrystallization.

Figure 1. A wafer preform is made by rapid solidification against a cold substrate. This pre-form has the right geometry, but the grain size is VERY small, due to the rapid solidification. Thus, the material is not yet suitable for use in photovoltaics. It must be re-crystallized.

Figure 2 . The wafer pre-form is placed in a tube furnace and a thin film capsule is grown which encases the wafer. The wafer is then placed between backing plates and passed through a heated zone so as to melt the silicon and allow it to re-crystallize, thereby growing the grains. The backing plates are necessary to maintain the flatness of the wafer during re-crystallization. While the capsule effectively contains the molten silicon it is very thin, and so, cannot independently retain its flatness.

Our focus in this program was entirely on the re-crystallization portion of the technology, as this was felt to be the most critical part – the highest risk part. The work performed in this program fell into several tasks/categories and each is described in a section below. The categories are:

- Thin Film Capsule
- Backing/Support Plates
- Furnace Design and Construction
- Thermal modeling and measurement
- Results of re-crystallization
- Electrical results

5.2. Thin Film Capsule:

The concept of re-crystallization in a thin-film capsule was originally invented with a silica capsule in mind. The majority of the silica capsules were grown on the wafer pre-form by either dry thermal oxidation or wet thermal oxidation, with the majority grown by dry oxidation. Typically 1 micron of oxide was grown, although capsules with oxides as thin as .25 micron served to adequately contain the molten silicon.

SiO₂ has a number of advantages in consideration for use as the capsule material. These advantages include:

- It can be grown very cleanly.
- It is known to be acceptable in contact with molten silicon
- It has good tear strength at the melting point of silicon.
- Any tear or rupture will heal itself if the re-crystallization is done in air.
- It has a low tendency to nucleate grains when silicon solidifies against it.

An extensive part of the research done under this contract concerned the nucleating properties of silica. The crucial point is that there is a significant contact area between the silicon and the capsule and thus, if there is a high propensity to nucleate grains at the interface between the silicon and the capsule, the resulting re-crystallized wafer will have very small grain size. Thus, it is important that the material of the capsule have a low tendency to nucleate grains.

Accordingly, a significant effort was spent on understanding and characterizing work on nucleation with various capsule materials. Two journal articles were written, one entitled *Nucleation Properties of Undercooled Silicon at Various Substrates*, J. Applied Physics, **109**, 084916 (2011). And the other entitled *The effect of Substrate Material on Nucleation Behavior of Molten Silicon for Photovoltaics*, J. Crystal Growth, **312** (2010) 1297-1300, both excerpted herein.

In these papers, small samples of silicon wafer were encapsulated with different materials and by different methods, including SiO₂ by wet oxidation, SiO₂ by dry oxidation, silicon nitride by PECVD and silicon oxynitride by PECVD. Stacks of capsule materials were also tested. The propensity to nucleate was assessed by measuring the amount of undercooling that a capsule material could sustain during cooling of the encapsulate silicon from a molten state. This undercooling was measured using a Differential Scanning Calorimeter (DSC). It was found that the oxide sustained the highest degree of undercooling, often of over 100K. This certainly supported the experimental observation that oxide capsules resulted in the lowest amount of grain nucleation in the re-crystallization step.

Excerpts from:

“Nucleation Properties of Undercooled Silicon at Various Temperatures”,

Appapillai, A., Sachs, C., and Sachs, E., *J Applied Physics*, 109
084916 (2011)

I. INTRODUCTION

In order to reduce the cost of crystalline silicon photovoltaics, it is important to maximize the electronic and structural quality of wafers without increasing their cost. Manufacture of multicrystalline silicon wafers typically involves a directional solidification process in order to maximize grain size. In any directional solidification process, the preferred mechanism of solid silicon crystallization is continuous growth from the already-solidified region of the crystal, rather than nucleation of a new grain at the wall upstream of the crystal-melt interface. The character of this crystallization depends on the temperature profile imposed upon the wafer, but also on the interfacial energy between substrate and melt, which will lower the energy barrier for nucleation of the solid. The nucleation properties of the wall material become especially important when the surface area-to-volume ratio becomes large, such as in zone-melting recrystallization,¹ ribbon growth on substrate,² or crystallization on dipped substrate.³ We can differentiate between substrates by measuring the amount of undercooling below the melting temperature that molten silicon will undergo before heterogeneously nucleating on the substrate. A substrate that allows a large level of subcooling before molten silicon nucleates will be less likely to provide nucleation sites for a directionally solidifying crystal.

Several studies have attempted to measure the homogeneous nucleation behavior of silicon by reducing contact with foreign materials that could cause nucleation. Studies have measured up to 350 °C of undercooling for levitated silicon droplets⁴ and silicon surrounded by a liquid flux of SiO₂-BaO-CaO.⁵ Dutarte⁶ found a maximum undercooling of 240 °C for silicon in contact with SiO₂ layers created by

both thermal growth and chemical vapor deposition; however the use of optical detection of solidification and separate thermocouple measurement led to large margins of error in undercooling determination, and the performance of other substrate materials was not investigated. The goal of this research is to determine how much the nucleation barrier and the level of undercooling is reduced as a function of the substrate material, as well as determine causes for, and thereby reduce, variability in this undercooling.

One approach to measurement of interfacial energies is to study the liquid-substrate behavior in a gaseous medium, such as air or vacuum. Several researchers have measured the wetting behavior of molten silicon using the sessile drop method,⁷⁻⁹ either in vacuum or inert atmosphere. Whalen et al. reported a contact angle for molten silicon of 40° ± 5° on SiC and 43° on hot pressed Si₃N₄ at ~1427°, the latter decreasing to 10° as temperature was increased to 1482 °C. However, Croll *et al.* measured the contact angle of molten silicon on substrates coated with various powder coatings, as often used in cast silicon manufacturing, and obtained measurements of 10°, 80°, and 150° for powders of Si₃N₄, SiO₂, and BN powders, respectively.⁸ A powder substrate will show higher contact angles than a solid substrate, but the relative behaviors of the different materials tested should be the same. This behavior would indicate that Si₃N₄ had the lowest interfacial energy of the three powders tested, and BN the highest of the three. However, because this study of liquid-silicon/substrate relationship was conducted with the third phase being vacuum atmosphere, it is difficult to translate the findings into a prediction of the behavior of a liquid-silicon/solid-silicon/substrate system, because changing that third component can have varying effects on the relative interfacial energies which cause the wetting angles. However, this reported data implies that silicon has a low interfacial energy with silicon nitride, which would make it the

most favorable material upon which to nucleate. In contrast, the data indicates that Si-SiO₂ has a high interfacial energy, such that nucleation of solid silicon would be less favorable.

In order to specifically determine the nucleation behavior of liquid silicon on various substrate materials, this study measures the amount of undercooling below the melting temperature that molten silicon is able to reach before it nucleates in contact with the substrate. The larger the undercooling below T_m , the less likely the substrate material is to cause new nucleation sites in a recrystallizing sample and thereby initiate new grains of solid silicon.

II. EXPERIMENTAL

Differential scanning calorimetry (DSC) was used to measure the level of undercooling below the melting temperature for various substrates of interest. The DSC technique involves measuring the heat flow to a sample, as compared to a reference, as a function of temperature during heating or cooling at a controlled rate. Because the surface properties of the substrate are of interest, each silicon sample was coated with a thin film of the material under investigation, rather than an independent piece of the substrate material placed in contact with the silicon. This configuration allows only the material being studied to touch the molten silicon, in thin-film form, reducing sources of error. Samples were tested on a Netzsch STA 449 Jupiter with DSC and thermogravimetric analysis capabilities.

Samples consisted of double-side-polished float zone wafers cut into 4.2-mm squares, and the substrate under investigation was applied as a coating on the sample. Sample preparation has been described in detail previously.¹⁰ Before each coating was applied, samples were cleaned using the standard RCA I process and etched in an HF/HNO₃/HCOOH solution to soften the sharp cut corners. To study the grain structure of resolidified samples, they were first embedded in clear epoxy and polished to a smooth finish in preparation for texture-etching in a 70 °C NaOH solution to reveal the grain structure.

Various coatings on the silicon samples were tested for their influence on nucleation. Dry thermal oxide was grown at 1100 °C under flowing dry oxygen in a quartz tube furnace. In some cases, a two-part oxidation process was applied, in which samples were rotated halfway through the oxidation, to reduce the oxide thickness nonuniformity caused by contact with the holder. Wet thermal oxide was grown at 1000 °C in a saturated steam environment in a quartz tube furnace. Silicon nitride was deposited by plasma-enhanced chemical vapor deposition (PECVD). The deposition process was repeated twice for each sample after switching the orientation of the sample relative to the sample holder, to ensure even coatings on both sides. The deposited amorphous nitride layer had a refractive index of 2.1, and was deposited using a gas flow ratio,¹¹ R_G , of 0.46. Silicon oxynitride was also deposited by PECVD using a 2:1 ratio of N:O gases to yield a thin film with a refractive index of 2.0.

Each sample was placed in a CVD SiC-coated graphite crucible with an alumina lid in the DSC to be heated to 1450 °C and cooled in air at a rate of 10 °C/min. The

difference in temperature between the onset of melting during heating and the onset of freezing during cooling represents the undercooling for each sample.

The concentration of interstitial oxygen and precipitated silicon oxide was investigated by Fourier transform infrared spectroscopy (FTIR). A float zone wafer was used as reference material. Two samples with an initial coating of 2 μ m dry oxide and a 25 mm $\times$ 25 mm center piece of a zone melting recrystallized sample were embedded into a mounting adhesive. To obtain coplanar faces and sufficient surface quality, the samples were ground and polished from both sides.

III. RESULTS

A. Dry oxide coating results

Undercooling results of silicon samples coated with various thicknesses of dry thermal oxide are shown in Fig. 1. The first data set, samples with a 1- μ m layer of dry oxide, has been reported previously and is shown here for comparison.¹⁰ The data shows a bimodal distribution, with samples having very high levels (>100 °C) of undercooling and samples with much lower (<60 °C) undercooling. The presence of high ΔT samples prove that the dry oxide material is not the cause of nucleation at lower ΔT , and that it is capable of sustaining large undercooling before solid nuclei are stable enough to grow continuously. However, some samples may have another factor, such as a foreign particle or a microcrack, that might cause nucleation before a larger undercooling is reached.

A previous hypothesis for causing nucleation at low undercooling levels was the deformation of some samples while molten.¹⁰ To probe this theory of deformation-caused nucleation, samples were prepared with a thicker dry oxide layer of 2 μ m, grown continuously in an oxygen atmosphere at 1100 °C for $\sim$ 130 hours, to see if the increased coating thickness could consistently constrain the sample shape. The results for this set of samples is shown in the second column of Fig. 1. It is clear that the proportion of samples with small undercooling levels is lower than that of the 1 μ m samples,

FIG. 1. Undercooling results for dry thermal SiO₂ coatings. Black asterisks represent mean values of each data set. Third column of data represents samples oxidized in two parts with opposite orientations relative to sample holder for a total of 40 hs, for minimum 1 μ m film thickness.

and the mean value of undercooling, shown as gray asterisks, has also increased. However, there was no clear correlation between oxide thickness and overall sample deformation from the original shape, as high undercooling levels were measured for both deformed and nondeformed oxide-coated samples, but the frequency of high undercooling did increase with the thicker oxide.

Another possible reason for the variation in undercooling data is nonuniformity of the oxide coating, given that the thermal growth is conducted with samples resting on a quartz sample holder. Regions of the sample in contact with the holder may have more limited access to the oxygen environment and thus local oxide growth may be slower. To avoid this scenario, a batch of samples was prepared with a two-part oxidation, with each sample rotated 180° relative to the sample holder after 20 hs at 1100 °C, for a total of 40 hs of growth. In this case, every point on the sample surface should have at least 1 μm of oxide, having had a minimum of 20 hs with unconstrained access to flowing oxygen. The data from this sample set is shown in the third column of Fig. 1. While the spread of the undercooling data is more evenly distributed, there were no samples with $\Delta T < 20^\circ\text{C}$, and the mean value of the set was higher than that of the 2 μm samples, as shown by the gray asterisks. These results indicate that a full 2 μm oxide is not necessary to improve the consistency of high undercooling, which is important because the long time required to grow such an oxide is not practical in many industrial situations. Overall, dry oxide looks promising because it will not be a cause for nucleation unless the recrystallizing silicon is cooled 120 °C below T_m , which is unlikely to occur in most crystallization processes.

As measured by FTIR, the concentration of interstitial oxygen in the samples coated with 2 μm dry oxide is about $2.4 \times 10^{18} \text{ cm}^{-3}$ and about $2.2 \times 10^{18} \text{ cm}^{-3}$ in the zone-melt recrystallized samples. Significant amounts of silicon oxide precipitates could not be detected.

The solubility of oxygen in silicon melt close to the melting point is about $2 \times 10^{18} \text{ cm}^{-3}$ for nondoped silicon¹² and increases to about $4 \times 10^{18} \text{ cm}^{-3}$ for boron concentrations of $5 \times 10^{20} \text{ cm}^{-3}$. The dissolution rate of silicon oxide in liquid silicon of about 2 nm/s, the high surface-to-volume ratio and the inability of the samples to release oxygen as silicon monoxide results in the silicon melt becoming rapidly saturated with oxygen during zone melting and the melt phase in the DSC temperature cycle.

Because of the absence of silicon oxide precipitates the high oxygen concentration in the silicon melt is unlikely to affect its nucleation behavior.

B. Wet oxide coating results

The undercooling behavior of wet thermal oxide coatings is shown in Fig. 2. The first wet oxide coating, a 1 μm layer grown at 1000 °C for 4 hs, has been reported previously.¹⁰ The high maximum indicated that wet oxide had the potential to suppress nucleation, as seen with the dry oxide, and similar steps were taken to improve undercooling repeatability, such as growing a thicker oxide and performing the oxidation in a two-step process. The thicker wet oxide layer

FIG. 2. Undercooling results for wet thermal oxide coatings. Black asterisks represent mean values of each data set.

was grown for 20 hs total at 1000 °C, significantly increasing the maximum undercooling to $\Delta T = 123^\circ\text{C}$, and the average to 79°C . Samples with two-part wet oxidation, for a total of 20 hs at 1000 °C, showed improved ΔT consistency, with a maximum of $\Delta T = 131^\circ\text{C}$. As with dry oxide samples, the increase in coating thickness had a negligible effect on sample deformation, further weakening the tie between macro-scale deformation and nucleation behavior.

These results support the idea that a uniform oxide coating of the silicon is required for the best performance in non-nucleation. This data also indicates that wet SiO_2 is practically equivalent to dry SiO_2 in terms of nucleation properties, which is beneficial since wet SiO_2 can be thermally grown at higher rates and is therefore more conducive to a high-throughput manufacturing process. Although fast oxidation under steam conditions has been reported to create dangling bonds at the oxide-silicon interface,^{13,14} it appears to have little effect on the nucleation behavior as compared to dry oxidation.

C. Silicon nitride coating results

Undercooling results for silicon nitride coatings are shown in Fig. 3. As reported previously,¹⁰ the 160 nm silicon nitride layer yielded consistently low undercooling results—less than 17°C . The 160 nm nitride-coated samples very

FIG. 3. Undercooling results for silicon nitride coatings. Black asterisks represent mean values of each data set.

consistently deformed into more rounded shapes with rough, colorful surfaces, and poorly defined corners.¹⁰

The 160 nm SiN_x coating consistently resulted in sample deformation, so a thicker nitride layer of 600 nm was applied to a set of silicon samples. In this case, the nitride was thick enough to maintain the rectangular shape of the sample throughout the experiment, as shown in Fig. 4(b). However, the 600 nm nitrided samples did not reach undercooling levels greater than 17 °C below T_m, shown in the second column of Fig. 3, which indicates that the sample deformation was not responsible for the low undercooling of the thinner nitride coating. In fact, these results indicate that the nitride material itself is unable to sustain contact with metastable supercooled silicon and causes nucleation of the solid phase before $\Delta T = 17^\circ\text{C}$. These results imply that the SiN_x substrate material will cause the most nucleation during crystallization.

While the nitride coatings displayed much lower undercooling levels than the thermal oxides, the nitride material has a beneficial quality of releasing from SiC crucibles without sticking. To utilize this property, a batch of samples was prepared with a 500 nm SiO_xN_y coating composition deposited by PECVD to see if moving the coating composition closer to that of silicon dioxide improved the undercooling behavior. As seen in the data shown in the third column of Fig. 3, this oxynitride layer yielded the smallest undercoolings of any materials tested, consistently less than 5 °C below the melting point. This oxynitride coating also had a unique texture post-melting, with parallel wrinkles oriented at 45° from the sample edges, shown in Fig. 5(b). This texture was much smoother and more uniform in color than that of a post-melting nitride-coated sample, shown in Fig. 5(a).

Due to the desirable nonstick characteristic of SiN_x relative to the crucible, several dry thermal oxide-coated samples were coated again with a 160 nm layer of SiN_x to protect the outside of the sample from sticking to the crucible while testing the nucleation properties of the oxide in contact with the silicon. While these samples indeed released cleanly from the crucible, they showed very small levels of undercooling between 19 °C and 26 °C, slightly higher than data for nitride coatings, but much less than the > 120 °C undercooling levels seen for dry oxide prepared in the same batch. The data is shown both in Fig. 1 and Fig. 3. It was suggested that the nitride layer might react with or diffuse through the oxide coating at high temperatures and form an

FIG. 4. (Color online) Morphology of silicon nitride-coated samples for coating thicknesses of 160 nm and 600 nm after melting and resolidifying.

FIG. 5. (Color online) Optical micrographs of morphology of silicon nitride and oxynitride-coated samples after melting and resolidifying.

oxynitride coating layer for the silicon, which would increase its tendency to cause nucleation. Several samples were tested using a faster heating rate of 30 °C/min to minimize the total time spent above 1000 °C, but no improvement in the undercooling level was measured. However, both layers are still able to be etched away in a dilute HF solution after recrystallizing, via undercutting of the nitride layer and etching away the oxide layer, as evidenced by clean removal of both layers with flakes of SiN_x floating in the solution. This behavior indicates that the two capsule layers are still separate and distinct. Therefore, the original SiO₂ was likely in sole contact with the silicon.

Another possible mechanism for the undercooling reduction caused by depositing SiN_x over the oxide capsule is high-temperature stress between the layers which could cause wrinkling or warping of their surfaces. Such wrinkles could create small topological features that would be favorable nucleation sites for undercooled silicon if their dimensions are on the order of the critical nucleus size for a particular temperature below T_m. An image of the surface texture of a sample with SiN_x over SiO₂ after recrystallization in the DSC is shown in Fig. 6. This side of the sample was facing the SiC-coated crucible, and a wrinkled texture can be seen. These wrinkles, shown larger in Fig. 6(b), consist of circular and straight features, which may have resulted from the differing high-temperature behaviors of the two capsule materials. These circular features were primarily seen on the bottom surface of the sample, which was likely

FIG. 6. Optical micrograph of bottom surface of DSC-recrystallized silicon sample coated with composite capsule of 160 nm SiN_x over SiO₂.

to have cooled down first due to its intimate contact with the cooling crucible; however, the final texture did not match the crucible texture and the sample released easily from the crucible, indicating that the SiC crucible did not affect the silicon melt inside the capsule. It is known that silicon nitride deposited by PECVD undergoes a densification process at high temperatures, during which the hydrogen incorporated in the film may be released.^{15,16} Cai *et al.* reported ~3–16% decreases in PECVD silicon nitride film thicknesses of different refractive indices after annealing at 650 °C, with a corresponding reduction in bonded hydrogen content, and it can be expected that annealing at higher temperatures could cause further densification of the films.¹⁶ SiO₂ also undergoes softening above 1000 °C, which might render it more susceptible to deformations due to thermally-induced stress from thermal expansion/contraction of SiN_x, causing wrinkles that act as favorable nucleation sites.

To minimize the possible influence of this structural change on the underlying SiO₂ capsule, the thickness of the nitride layer was reduced to 40 nm. This alteration resulted in an increase of the maximum undercooling level to 56 °C, as shown in the right-most column of Fig. 3. This result supports the idea that a densification and mismatched coefficients of thermal expansion of the composite coating layers was the cause for reduced undercooling, and that reducing the nitride layer thickness decreases its ability to apply stress to the oxide layer. Since the nitride layer is only needed as a release layer, its thickness can be reduced farther, to impart the least stress on the oxide layer, as long as a continuous layer is present to prevent sticking to the crucible or substrate. This capsule configuration looks the most promising for achieving large recrystallized grains without adhesion to supporting substrates during a directional recrystallization.

D. Grain structure

To get a closer look at the recrystallized grains in the DSC samples, they were cross-sectioned and texture-etched. High undercooling should result in small grains in the final structure,^{17,18} since the driving force for solidification is very high at such temperatures and nucleation rates increase with undercooling level.^{4,19} Faceted grains have been observed by various researchers for undercooling levels below 85 °C, and as undercooling increases, more dendritic growth has been seen.²⁰

The grain structure of a Si sample coated with 600 nm SiN_x that reached only 15 °C below T_m before nucleation occurred is shown in Fig. 7(a). Large, faceted grains can be seen, consistent with findings for low-undercooling silicon in the literature.^{20,21} Samples with this level of undercooling typically took ~60 seconds to completely solidify. Kuribayashi *et al.* have reported that silicon solidifying with undercooling levels of up to 100 °C typically solidify with stable {111} interfaces.¹⁸

Similar grain structures were seen for samples coated with a combination of dry oxide and SiN_x, an example of which is shown in Fig. 7(b). Two or three main grains are seen in this sample, and grain boundaries are slightly less faceted than those with the lowest undercooling. This sample

FIG. 7. Grain structure in resolidified Si samples which showed low levels of undercooling.

completed solidification in approximately 20 seconds, slightly faster than those with high levels of faceting, but is mostly likely dendrite-free because it is in the undercooling range of $\Delta T < 100$ °C.²²

The grain structure of a dry oxide-coated Si sample with ~120 °C undercooling before solidification is shown in Fig. 8. In this case, the grains are much less faceted and the grain boundaries are rougher, and these samples typically solidify within 10 seconds. At first glance there appear to be two main grains within the cross-section. However, a closer view of the structure, as seen in Fig. 8(b), reveals many small, irregular grains scattered throughout the sample. This increase in grain density corresponds with the literature for mid-range levels of undercooling, between ~100 °C and 250 °C.²² Nagashio *et al.* have reported that the dendritic growth of silicon undercooled by more than 100 °C typically results in grain refinement, due to fragmentation of the higher-order arms of the dendrites into small spheres.²³ This fragmentation may occur when the silicon recalesces to the melting temperature after nucleation, at which point the silicon tries to minimize the interfacial area between solid and liquid by breaking off high-order dendrite arms into spheres. Thus the small grains seen along the edge of another elongated grain in Fig. 8(b) may be the result of this fragmentation and refinement. Silicon undercooled by more than 250 °C often undergoes fragmentation of even lower-order dendrite arms, resulting in even finer grain structure.^{22,23} This grain refinement behavior is one reason to avoid high undercooling in the silicon melt during a recrystallization process, where large grains are desired and the molten silicon should not actually reach high levels of undercooling as it grows from the already-solid region at the leading edge.

FIG. 8. (Color online) Texture etched grain structure of high-undercooling 2-part dry oxide sample, $\Delta T = 120$ °C. Black dotted lines are residual scratches from the polishing process.

IV. DISCUSSION

Considering results from all types of samples, most data sets contained a bimodal distribution of undercooling levels for a particular sample type. The maximum undercooling can be considered as the true measure of nucleation behavior for a particular material, and the lower- ΔT group of data points were likely the result of other defects or impurity particles. The dry oxide coating sustained the highest maximum undercooling levels, up to 141 °C below the melting point, indicating a high interfacial stability with the molten silicon which should reduce the probability of unwanted heterogeneous nucleation. The wet oxide overall showed slightly lower levels of undercooling with a maximum of 130 °C, and the silicon nitride coating consistently showed low undercooling levels below 17 °C. This finding indicates that a nitride substrate would be more likely to cause nucleation of new grains at low levels of undercooling in a recrystallization process. However, deposition of a nitride layer over an inner dry oxide layer reduced the undercooling from the > 100 °C typical of dry oxide to a maximum of <60 °C, as discussed in the previous section.

The results of this nucleation study indicate that dry or wet thermal oxide films have the highest potential for being good non-nucleating coating/substrate materials. As long as the silicon has begun to solidify at one end that begins cooling first, further nucleation of new grains should not occur on the rest of the sample due to the oxide contact. In this situation it is reasonable to assume that the molten silicon will not have a chance to subcool far below the melting temperature since the leading edge has already provided a growing solid phase. Thus, the SiO₂ coating should not be a source for new nuclei. However, a coating of SiN_x would be a more favorable site for nucleation, which should manifest in an increased number of grains in a zone-recrystallized wafer.

To test these findings in an actual zone-melt recrystallization process, single-crystal silicon wafers (25 mm width, 100 mm length) were prepared with a 160 nm SiN_x coating and passed through a zone-melt recrystallization furnace between two supporting SiC backing plates. A 25 mm square piece was cut, polished, and etched in a saturated NaOH solution to reveal the grain structure of the wafer. The resulting grain structure is shown in Fig. 9(a). Grains are elongated and tend to increase in number toward the trailing edge, which is on the left. This arrangement indicates that new grains are nucleating as the solidification front moves toward the left. Multiple points of the coating are breached at the left side as silicon bursts through upon final solidification. Grain widths range from ~0.2–2.2 mm.

For comparison, another sample was recrystallized in the zone-melt furnace under the same conditions, but with a coating of SiO₂ grown in a two-step oxidation and an outer coating of SiN_x. The coating layers were etched off in a dilute HF solution, and the wafer was subsequently etched in an NaOH solution to reveal the grain structure, which is shown in Fig. 9(b). In this case, the grains are elongated but much wider due to decreased nucleation at the capsule. Grain widths range from ~1.8–6.0 mm and are generally increasing in width toward the trailing edge at the left side of the image. This clear difference in grain structure may result from the different

FIG 9. Grain structure in 25 mm section at trailing edge of Si sample coated with SiN_x or composite coating, recrystallized in zone-melt furnace.

nucleation properties of the two types of coating. The undercooling data indicates that the molten silicon would have to be undercooled at least 30 °C in order for the oxide-nitride composite coating to cause new grain nucleation, and this small shift in nucleation condition may have been enough to increase the resulting grain size by a factor of ~3. Since the undercooling data indicates that a thinner SiN_x film would increase the required undercooling to cause nucleation, it is probable that using a film of <40 nm could allow growth of larger grains. However, this effect depends on the level of undercooling reached by the recrystallizing silicon and the thermal profile to which it is subjected. If it is able to solidify by the growth of existing grains without experiencing any undercooling of more than 30 °C, then the 160 nm SiN_x outer coating may be sufficiently thin to avoid influencing nucleation of the molten silicon. For best results, the SiN_x outer layer should be reduced below 40 nm to reduce the possibly detrimental effects of inter-layer stresses.

V. CONCLUSION

The silicon nucleation behaviors in contact with silicon nitride and silicon oxides were revealed and sources of variation in undercooling results were reduced and discussed. Undercooling data sets showed bimodal distributions, with the maximum level of undercooling representing the real potential for a given material to suppress nucleation below silicon's melting point. Both dry and wet thermal oxides showed equally low propensity to cause nucleation of undercooled silicon, sustaining contact with molten silicon up to 141 °C and 131 °C, respectively, below T_{melt} before causing nucleation. In contrast, silicon nitride sustained small undercooling levels, with a maximum of 17 °C of undercooling, and enhanced nucleation. A silicon oxynitride coating yielded the lowest undercooling levels, consistently within 5 °C of the melting temperature. To utilize the nonreactivity of silicon nitride with supporting substrates, it was applied over a layer of dry oxide, which was suggested to have caused inter-layer thermal stresses and reduced undercooling levels to 19–26 °C, significantly lower than that of dry oxide alone. Reducing the silicon nitride layer to 40 nm improved performance to up to 56 °C undercooling, indicating that the thin nitride layer would cause less deformation of the oxide texture while acting as a successful release layer.

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1. Introduction

One of the major barriers for widespread implementation of photovoltaics is their high cost compared with traditional energy sources. Given that almost half the cost of a crystalline silicon-based solar module comes from producing the silicon wafer, including purifying the silicon, forming the ingot, and sawing into wafers [1], it would be desirable to reduce the cost of this part of the process. More than 80 percent of current solar cell production utilizes crystalline silicon [2], and the majority of those produces silicon by bulk methods, such as float zone, Czochralski, or cast multicrystalline processes, but all these methods require that the bulk piece of silicon be sawed into wafers. During the sawing process, basically half of the silicon is wasted as dust. Clearly, if the amount of purified silicon lost as dust can be reduced, the cost of the solar cell will be decreased.

One way to reduce this loss is to avoid the process of producing the bulk silicon ingot or block by either appropriately solidifying the silicon in a wafer shape, or by using a zone-melting process to grow an appropriate grain structure for photovoltaics in a preformed wafer. Several different approaches to this idea have been taken in the past. For example, in the ribbon growth on substrate (RGS) method, a crucible of molten silicon is spread onto a cooler substrate where it solidifies in a ribbon form [3,4]. Alternatively, several different approaches utilize a zone melting

technique, beginning with a wafer form supported by a substrate or sandwiched by layers of oxide, for example, and moving a zone heater across the wafer to recrystallize into a preferred grain structure [5]. The common factor in these different techniques is the contact between the molten silicon and a foreign substrate, having a large contact surface area compared with the area of the silicon solid-melt interface. The effect of this large contact area on the nucleation and growth behavior depends on the particular substrate material used.

In these types of processes, the preferred mechanism of solid silicon crystallization is continuous growth from the already-solidified region of the wafer, rather than nucleation of a new grain on the substrate material upstream of the solid-melt interface. The character of this crystallization depends on the temperature profile imposed upon the wafer, but also on the interfacial energy between substrate and melt, which will lower the energy barrier for nucleation of the solid. We can differentiate between different substrates by measuring the amount of undercooling below the melting temperature that molten silicon will undergo before heterogeneously nucleating on the substrate. Studies have shown up to 350 °C of undercooling for levitated silicon droplets [6] and silicon surrounded by a liquid flux [7]. Dutarte [8] found a maximum undercooling of 240 °C for silicon in contact with SiO₂ layers created by both thermal growth and chemical vapor deposition; however, the use of optical detection of solidification and separate thermocouple measurement led to large margins of error in undercooling determination, and the performance of other substrate materials is still unknown. The goal of this research is to determine how much the nucleation

barrier, and thereby the level of undercooling, is reduced as a function of the substrate material, as well as determine causes for and thereby reduce variability in this undercooling.

2. Experimental

Differential scanning calorimetry (DSC) was used to measure the level of undercooling below the melting temperature for each type of substrate. Samples were tested on a Netzsch STA 449 Jupiter with DSC and thermogravimetric analysis (TGA) capabilities. Samples consisted of double-side-polished float zone wafers cut into squares of 4.2-mm sides and the substrate under investigation was applied as a coating on the sample. The first coating was 1 μm of dry thermal oxide, grown at 1100 $^{\circ}\text{C}$ for 20 h under dry oxygen. The second coating was 1 μm of wet thermal oxide, grown at 1000 $^{\circ}\text{C}$ for 4 h in a saturated steam environment. The third coating was 160 nm of silicon nitride deposited by plasma-enhanced chemical vapor deposition (PECVD). Fig. 1 shows a photograph and representative schematic of the samples before entering the DSC. Each sample was placed in a silicon-carbide-coated graphite crucible in the DSC to be heated and cooled in air at a rate of 10 $^{\circ}\text{C}/\text{min}$. The difference in temperature between the onset of melting during heating and the onset of freezing during cooling represents the undercooling for each sample. Samples were subsequently characterized through optical microscopy.

3. Results and discussion

Fig. 2 shows an example of data collected showing undercooling of the sample, in this case, with a 1 μm dry oxide coating. The sample heats up along the lower grey curve, and the sample melting is signified by a downward peak representing the absorption of

Fig. 1. (a) Photograph and (b) schematic of prepared samples before DSC experiment.

Fig. 2. DSC signal vs. temperature for an example dry oxide-coated sample with a large undercooling of 122 $^{\circ}\text{C}$.

Fig. 3. Comparison of undercooling levels, ΔT , for various coatings on silicon.

latent heat. Once the sample reaches 1450 $^{\circ}\text{C}$, it begins cooling at 10 $^{\circ}\text{C}/\text{min}$ until the solidification peak is observed. In this particular data set, the large undercooling achieved by the sample led to a very rapid solidification and therefore very fast release of latent heat. The exothermic nature of this sudden reaction led to a slight increase in the measured temperature of the sample, shown by the retrograde character of the solidification peak, before the sample continued to cool according to the prescribed program.

The overall comparison of undercooling results is shown in Fig. 3. Clearly, the dry oxide coating sustained the highest undercooling levels, up to 141 $^{\circ}\text{C}$ below the melting point, indicating a high interfacial stability with the molten silicon which should reduce the probability of unwanted heterogeneous nucleation. The wet oxide overall showed lower levels of undercooling with a maximum of 77 $^{\circ}\text{C}$, and the silicon nitride coating consistently showed low undercooling levels below 20 $^{\circ}\text{C}$. This finding indicates that a nitride substrate would be more likely to cause nucleation of new grains at low levels of undercooling in a recrystallization process.

One possible factor affecting the spread in the undercooling data for each type of sample coating may be the deformation of some samples during the molten phase of the experiment. As

Fig. 4. Examples of deformation for samples coated with (a) dry oxide, (b) wet oxide and (c) silicon nitride, after undergoing melting and re-solidification in the DSC. Optical microscopy showed unique surface morphology for (d) dry oxide and (e) silicon nitride coatings after re-solidification.

shown in Fig. 4a, several dry oxide samples retained their rectangular form and subsequently achieved high undercooling levels. Similar results were seen for some wet oxide samples; however many of them instead showed folding deformations, shown in Fig. 4b, while molten. Many such folded samples had cracks in the oxide coating layer, and such deformations were seen for both wet and dry oxides. The variation in both final shape and level of undercooling could be related to micro-defects or impurities in some coatings, or slight variations in coating thickness due to samples touching a sample carrier during oxide growth.

The nitride-coated samples very consistently deformed into more rounded shapes with rough, colorful surfaces and poorly defined corners. It should be noted that the 1 μm thickness of the oxide coating was much larger than that of the 160 nm nitride coating, which may have also influenced the final shapes. Because the large deformation resulted in higher surface roughness, it may have provided an additional source of nucleation barrier reduction, preventing the nitride coating from reaching larger undercooling

levels. The performance of thicker nitride coatings is under investigation, as well as a reduction in the driving force for deformation by using more spherical samples rather than plates.

Optical microscopy revealed unique surface morphologies for the different coatings after re-solidification. In the case of the dry oxide coating with large undercooling, shown in Fig. 4d, there is an overall scale pattern, with each region having a central point from which striations radiate outwards; these central points may represent nucleation centers. These nucleation sites are very finely spaced near the sample edge, indicating that nucleation was initiated in this region, and as the released latent heat caused the sample temperature to increase, nucleation occurred with lower frequency in the inner areas of the sample, resulting in larger distances between nucleation sites there. In contrast, samples coated with silicon nitride revealed many small colorful circle morphologies, as shown in Fig. 4e, which suggest that these small portions around each nucleation site froze more quickly before the sample temperature was raised and the surrounding areas froze more slowly as heat was removed. However, due to

the small overall undercooling, nucleation sites did not grow fast enough to touch the next nucleation site as in the dry oxide case, which is consistent with studies of crystal growth velocity with undercooling level by Panofen and Herlach [9]. Polished cross-sections of these samples showed that the large-undercooling samples were multicrystalline with small grains, and the small-undercooling samples had one or a small number of grains, consistent with the literature [10]. It is evident that the type of coating has a significant effect on the nucleation behavior and subsequent growth, and further studies of the effect of coating thickness and exact composition are in progress.

4. Conclusions

It has been shown that the dry and wet oxide coatings enable much larger undercooling levels than the nitride coating, suggesting a higher interfacial stability and a lower propensity to cause heterogeneous nucleation at higher undercooling levels, which can be used to design recrystallization processes for a desired grain growth pattern. It is desirable to further increase the consistency of reaching those high undercooling levels, whether by using thicker coating layers or different initial sample shapes to reduce varied deformation while molten. Other coating materials of interest, such as silicon carbide and silicon oxy-nitride, will be investigated in future studies. This information can be used to tailor the grain nucleation and growth in the design of wafer recrystallization processes to more efficiently increase the quality of multicrystalline wafers for more competitive and lower cost solar cells.

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5.3. Support Plates

A crucial aspect of the re-crystallization process is the maintenance of wafer flatness and thickness. The issue is that while the capsule has enough strength to keep in the molten silicon, it does not have enough strength to maintain the flatness of a wafer, unless the entire capsule is supported by a plate – called a backing plate. Thus, at a minimum, a plate is needed under the encapsulated wafer. However, one plate under the wafer is not sufficient because the molten silicon can rearrange within the capsule, resulting in thickness variations in the final wafer. Thus, there must be something on top of the wafer as well. Most typically, we put a second backing placed on top of the encapsulated wafer.

Using a flat backing plate under the encapsulated wafer worked well, as the encapsulated wafer naturally lies flat on this plate. However the top plate could be more problematic. The issue is that the wafer is being melted sequentially and this provides an opportunity for the silicon to rearrange – resulting in no uniform thickness in the final product. This was especially true when the top plate was merely resting on the wafer and therefore free to move up and down (or tilt) as the wafer solidified. Accordingly, we experimented with different methods of holding the top plate. In some cases, the top plate was fixed at a particular distance from the boom plate. Typically, this resulted in a re-X wafer in which the silicon drained out of a portion of the capsule and filled in other portions so as to create a wafer in those zones which completely filled the space between the backing plates. This could be a manageable arrangement, especially if the liquid silicon were biased to flow in one direction so that the denuded area of the capsule would be in a known and predetermined location.

Significant experiments were performed with a different concept. In this concept, the top backing plate was replaced with a bed of powder. In this way, the powder bed would conform precisely to the top of the wafer preform – leaving none of the slight gaps that might be present with a flat backing plate. The diagrams below show two methods that were used to apply the powder bed on top.

In Figure 3, dry powder is poured over the top of the preform wafer and backing plate. This powder sinters together lightly on its way into the re-crystallization furnace, thereby gaining strength and allowing it to hold the molten silicon in place. In Figure 4, the powder is made into a slurry which is cast on top of the preform wafer and backing plate. These methods helped substantially with flatness and surface finish. However, the electronic performance of this material was lower than material re-crystallized with two backing plates. This is probably due to an increase in impurity content in the wafer due to the high surface area of the powder.

Figure 3: Schematic of the process for applying a powder to the wafer to preserve its geometry during recrystallization. Powder is poured over the backing plate and wafer, the shell contains the wafer during recrystallization, and the components are separated and the final wafer is removed.

Slurry Casting

Figure 4: Schematic of a powder shell created by pouring a liquid-powder mixture (slurry) over the wafer and backing plate. A rubber mold is placed onto of the backing plate surrounding the wafer. The slurry is then poured into the mold, creating a compact layer of powder over the wafer. Slurry casting provides a far superior compaction than vibration compaction. However, it is a wet process that results in slurry flowing underneath the wafer, disturbing the release layer, and allowing the wafer to stick to the backing plate during recrystallization.

5.4 . Furnace Design

A crucial aspect of the re-crystallization process is the design of the re-crystallization. The furnace design went through several stages and prototypes. A common thread that was maintained throughout was the goal of operating in air. Silicon furnaces generally operate under inert gas at atmospheric pressure or under partial vacuum with inert gas. This is necessary in order to prevent oxidation of the silicon. However, in the case of re-crystallization in a thin-film pouch, the silicon is protected from oxidation by the pouch and hence the option exists to run the furnace in air. This has tremendous operation and cost advantages. First, there is no need for a water cooled stainless steel shell – the normal way of creating an inert gas environment. Second, the expense of argon is eliminated. Third, it is easier to move product in and out of the furnace as load locks are not required. Thus, it was a guiding principle, that the re-crystallization furnace operate in air.

This in turn led to constraints on the choices of materials for all components that get hot as they must run in air without oxidizing. Heaters were made of silicon carbide rod. Hexoloy rod from St. Gobain was the material used. Heat distribution was then accomplished by arraying multiple rods as may be seen in Figure 5. Rough tuning was accomplished by the positioning of the rods, and fine tuning by having independent control over the electrical power to the rods. Figure 5 shows a layout with three pairs of rods. Each pair consists of a top and bottom rod and these rods are electrically connected in series. Each pair is independently controlled as described below. The substrate packages traverses from left to right, supported on silicon carbide rods, one of which is evident in Figure 5.

Figure 5: Interior view of furnace, with lid removed. Pyrometers point directly at the top 3 elements. The long bar running left to right is one of the sample slider bars.

Figure 6 shows the control schematic for a single rod. A pyrometer sites directly onto a furnace element. The analog signals from the pyrometer go to a PIC microcontroller where they are converted to digital signals. An algorithm then interprets these signals and gives a digital output representing the temperature. This is converted to an analog signal and fed to a stand-alone temperature controller which then controls the current through the heater through a current-control SCR pack. There are independent control circuits for each heater. It was decided to control the temperature of the heaters rather than the temperature of the substrate and backing plates as they move through the furnace because it was felt that more reproducible control could be had in this manner. Further, current control was used for the heaters, rather than voltage control because the silicon carbide heaters, being of a semiconductor material, have a negative temperature coefficient of resistance. Thus, under voltage control, the heater can run away as it warms up, while current control is stable.

Figure 6. Schematic of a single control loop in the furnace. There are 3 such loops. A pyrometer sites directly onto a furnace element. The analog signals from the pyrometer go to a PIC microcontroller where they are converted to digital signals. An algorithm then interprets these signals and gives a digital output representing the temperature. This is converted to an analog signal and fed to a stand-alone temperature controller which then controls the current through the heater through a current-control SCR pack.

The other challenge was the insulation material. In an inert gas silicon furnace the most common type of insulation is a rigid carbon fiber material. But of course, this will not withstand high temperatures in air. Accordingly, we began our work with commercial silica-alumina insulation boards. The open furnace in Figure 5 shows such insulation materials. However, out of concern for impurities, especially aluminum from the alumina, we developed our own insulation material made out of very pure silicon carbide powder. These materials are in use in Figure 7 which also shows a single pair of heaters lit up.

Figure 7: Our own silicon carbide based insulation material with a single pair of heaters glowing.

One of the great advantages of making our own insulation materials was that we were able to create very low density and highly insulative materials. In fact, the insulating properties of our materials were vastly superior to the industry-standard carbon materials. Thermal conductivities were measured in the apparatus shown in Figure 8 below and we found to be as much as 5 times lower than the standard materials. This both reduces power consumption and also provides for better temperature control.

Figure 8 The apparatus (admittedly rather crude) used to test the thermal conductivity of newly fabricated insulation. The material under test is the square on the top of the box.

5.5. Modeling and Measurement

Extensive work has been done in the program on modeling and measurement. Both simple analytical models and numerical models were used to predict the shape of the liquid/solid interface. The numerical modeling was performed with the aid of COMSOL Multiphysics Modeling. The great challenge in modeling of a solidification process is to determine the location of the solid-liquid interface. This is difficult because this interface represents an abrupt change in materials properties and there is a concentrated heat source at the interface due to the release of the heat of fusion. The problem then is highly non-linear. While some methods, such as phase field analysis, attempt to compute the position of this boundary, we used a different approach which is less computationally intensive. We assumed a shape for the solid-liquid interface and then ran the numerical simulation of the heat transfer that would result from this shape. Now we had the heat flux into and out of the interface as a function of position along the interface. This could now be compared with the heat generation that would result from the liberation of the latent heat of fusion. That is, at every position along the interface we should find that the heat conducted out – heat conducted in should equal the heat of fusion liberated at that position and at the targeted growth speed. The shape of the interface is then adjusted and the simulation repeated until the agreement is within an acceptable range.

The plot below shows the result of an iteration for one set of parameters.

Figure 9. The output of a numerical simulation which predicted the shape of the liquid-solid interface in re-crystallization as well as the temperature field and heat flow directions in the solidified crystal. The white lines are the direction of heat flow. This is a relatively low growth speed as can be seen from the relatively flat interface at the left.

The plot below shows a set of interface shapes as a function of the growth speed, as derived by the iterative method described above.

Figure10 Interface shapes corresponding to different rates of advance of the interface – that is, different growth speeds. At the growth speed increases, the interface extends further “downstream” and becomes more curved.

With predictions of the shape of the solidification interface, the heat transfer circumstances can be changed (different heaters, heater power levels, insulation...) so as to shape the interface as desired with the goal of propagating grains in the desired direction.

These models predict the temperature field within the re-crystallizing wafer. In order to test these models we were faced with the challenge of measuring the temperature field in the wafer during the process. The problem is that the standard approaches to temperature measurement were difficult or impossible. Radiometric measurements were impossible because there is no direct visual access to the wafer as it is held between backing plates. Thermocouples capable of operation at these temperatures and in air (typically platinum alloys) are incredibly fragile, and virtually unusable in the fine gauge wire that would be needed for this case. Accordingly, we developed a new method of measuring temperature of the wafers. The basic idea was to apply dopant at the surface of the wafer by ion implantation and then to let the wafer sit stationary in the temperature field and allow the dopant to diffuse. After withdrawal, measurements of the sheet resistance of the wafer are made and the temperature

inferred from these measurements. In order to increase sensitivity, two dopants were implanted one p-type and one n-type. The different rate of diffusion of the dopants increased the sensitivity of the measurement. This work is described in a paper entitled *A Method for Temperature Profile Measurement of Silicon Wafers in High-Temperature Environments*, Journal of Applied Physics, **109**, 034902 (2011). This method proved to be highly effective and might be of use in semiconductor processing in general.

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I. INTRODUCTION

Measurement of high-temperature environments often used in processing of silicon wafers can be difficult due to the reactivity of many materials at these high temperatures, and the small dimensions of such wafers can increase the sensitivity to perturbations by measuring instruments. Conventional invasive methods for measuring temperature above 1200 °C include platinum-rhodium thermocouples, which must be in contact with the object to be measured.¹ Kreider *et al.*² developed a platinum-palladium thin-film thermocouple array method for measuring two-dimensional temperature fields on silicon for rapid thermal processing applications, with an upper limit of 900 °C, which is an invasive technique requiring external connections to the wafer. Single-point temperature measurements of silicon near or at its melting point have also been conducted using optical fiber thermometry,^{3,4} which uses an optical fiber cable threaded into the molten zone, connecting a carbon-coated fused quartz sensor to an external photodiode. However, this method measures only a single location at any time, and a reaction between the molten silicon and quartz can alter the temperature data. Furthermore, the silicon volume must be large enough to surround a large sensor without significant perturbation of the temperature field, so such a technique would not be appropriate for wafer or thin film geometries.

Noncontact methods for temperature measurement include radiation pyrometry, which requires that either the emissivity of the object being measured is known, or that two radiation wavelengths are measured to reduce the effects of emissivity on the signal. Pyrometry can be particularly challenging in a high-temperature furnace where the presence of the heating elements can affect the signal measured, and furnace insulation may require rearrangement to provide a clear optical pathway for the radiation signal, thereby al-

tering the environment of interest. It can be difficult to have precise knowledge of variation in the spectral emissivity of silicon samples undergoing various process steps. Ripple pyrometry, which measures both the sample radiation and the ac-modulated heater radiation, decouples the emissivity and reflectivity of the sample *in situ* to get a more accurate measure of the sample temperature.⁵ However, this technique relies on a quick response time of the system, and requires multiple measurements and signal processing. Furthermore, for a thin sample with a small thermal mass, the modulated heating signal may also cause the sample temperature to ripple and obscure the desired measurement.

Thin films of silicon have been characterized near the melting point by Hatano *et al.*,⁶ who used the reflection and transmission of an excimer laser signal through a partially melted silicon film in conjunction with its conductance to determine its time-dependent temperature and phase change behavior, however, the setup is quite complex and resolution is limited by the size of the laser spot. Martan *et al.*⁷ have also used infrared radiometry and time-resolved reflectivity methods to measure the laser-induced melting of monocrystalline silicon, and these noncontact techniques require unobstructed optical pathways for signal measurement and would not be convenient in many furnace geometries.

In some cases, it is desirable to measure the two-dimensional temperature profile of a thin sample without perturbing the existing heat flow conditions and external structure of the high-temperature environment. In this work, a new method has been developed to characterize a two-dimensional temperature profile experienced by a silicon wafer under steady-state conditions near the melting temperature of silicon.

II. DESIGN OF NOVEL TECHNIQUE

The premise for this temperature profile measurement technique is to utilize the temperature dependence of the dif-

FIG. 1. Schematic representation of the effect of temperature variation on the dopant penetration into a silicon wafer from an initial surface dopant source.

fusivity of dopants in silicon. Solid state diffusivity of impurities in crystals increases with temperature, and the diffusivities of common dopants in silicon are generally well known.⁸ In addition, doping silicon with impurities such as boron or phosphorus in controlled concentrations results in a predictable change in electrical resistivity of the material.^{9,10} Therefore, introducing a given quantity of dopant atoms to the surface of an undoped silicon wafer and allowing them to diffuse in at a steady-state temperature field for a given period of time, hereby referred to as a soak step, will result in a repeatable change in sheet resistance of the wafer. Thus it should be possible to determine the temperature of the wafer during an isothermal soak step by measuring its final sheet resistance.

A benefit of this approach is that two-dimensional temperature maps can be generated by placing a large wafer into a high-temperature environment and measuring the sheet resistance at the wafer surface as a function of position, using a four-point probe of small probe-tip spacing. This feature is useful for situations where temperature varies over small distances and precise knowledge of temperature gradients may be critical to the quality of a wafer being processed. Wafer thickness should not affect resistivity results since dopant diffusion occurs within the top few micrometers from the surface, such that the most convenient wafer thickness can be chosen based on application.

A schematic representation of the concept of this method is depicted in Fig. 1, showing that an imposed temperature profile will cause a phosphorus surface dopant to diffuse into the wafer by a distance dependent on the local temperature at each point. For a single dopant, such as phosphorus, diffusing into an undoped wafer, the slope of the dopant concentration as a function of depth from the surface is relatively

small after a soak step in the temperature range near silicon's melting point, such that samples soaked at different temperatures have only small differences in their concentration profiles, since concentration gradients are small. Using a larger implant dose would increase the concentration gradient but due to the power law relationship between resistivity and dopant concentration (having a negative slope on a log-log plot), a change in concentration at high overall concentration leads to a relatively small change in resistivity.¹¹ Thus the ability to distinguish two different soak temperatures in that range requires high resolution in the resistivity measurement, and allows less tolerance for sample variability which might reduce precision of the T- ρ relationship.

To increase the sensitivity of the resistivity measurement above 1200 °C, the starting wafer can be uniformly doped with an initial concentration of one type of dopant, such as p-type boron. Next, an n-type dopant can be deposited on the wafer surface, and as it diffuses into the wafer during the soak, a p-n junction is formed where the two dopant concentrations are equal, as shown in Fig. 2(a). Using a four-point probe on the top region of the junction (where the n-type dopant source was deposited), applied current does not pass across the junction, and therefore, the properties of only this top region are measured. By measuring this sheet resistance at the top surface, which depends on the excess of the majority dopant, a relationship can be distinguished between temperature and measured sheet resistance. The presence of background doping allows higher implant doses to increase the concentration gradient without lowering the resistivity as discussed in the previous paragraph. The creation of this junction improves the sensitivity of measured resistance to temperature because the resistivity is now based on the difference in carrier concentrations between the two oppositely charged dopants.

As temperature increases, the position of the junction moves farther into the wafer and the excess dopant concentration at any given depth decreases—two trends that have opposing effects on measured resistivity. Increasing the junction depth causes the measured resistivity to decrease but decreasing the excess dopant concentration causes the resistivity to increase. The junction depth increases at a nearly exponential rate above ~900 °C, but the excess concentration decrease occurs at a lower rate, resulting in an overall decrease in measured resistivity, as the effect of the junction position is larger. To improve the temperature-resistivity sensitivity, one can lessen the rate of decrease in excess concen-

FIG. 2. Simulated dopant concentration profile after initial implantation of dopant source.

FIG. 3. Simulated concentration profile of surface-implanted boron and phosphorus after 30 min soak at various temperatures. Location of the junction, where local concentrations are equal, moves deeper into the wafer for higher temperature soak steps.

tration by implanting two dopants of opposite type at the same surface, as shown in Fig. 2(b). As phosphorus diffuses into the wafer, decreasing its local concentration, the boron (implanted at a lower dose) also diffuses inward, such that the excess concentration is decreasing more gradually than it would if the boron concentration were constant, as discussed previously. This behavior, illustrated in Fig. 3, leads to a steeper decrease in measured resistivity with temperature. In this case, because the resistivity depends on the high concentration of implanted ions very close to the surface, bulk resistivity of the starting wafer is not critical. This characteristic is beneficial since high resistivity ($>1000 \text{ } \Omega \text{ cm}$) wafers are typically more costly. The procedure for implantation and diffusion of two dopant species is described in the following sections.

III. EXPERIMENTAL

Single-side polished Czochralski p-type silicon wafers of $200 \text{ } \mu\text{m}$ thickness with a starting resistivity of $20 \text{ } \Omega \text{ cm}$ were used. Wafers were thermally oxidized for 3 h at $1000 \text{ } ^\circ\text{C}$ in dry oxygen to create a 100 nm oxide layer to act as a protective layer during ion implantation. Silicon oxide was chosen for this protective coating due to its high purity, to avoid introducing impurities that would interfere with the measurement and contaminate high-temperature environments, as well as its ease of application and well-known properties. Ion implantation was used to implant a uniform distribution of both boron and phosphorus ions across the entire front polished surface of each wafer. The implantation doses were $1 \times 10^{15} \text{ cm}^{-2}$ and $2 \times 10^{15} \text{ cm}^{-2}$ at implantation energies of 80 keV and 170 keV , for boron and phosphorus, respectively, in order to place the concentration peaks at the same depth from the surface. These doses were chosen such that the faster-diffusing phosphorus atoms would have a higher concentration in the top region of the wafer, and when the wafer is soaked at high temperatures, the concentration of both dopants decreases at every depth on the top side of the junction, but the top region of the wafer always remains n-type. This way the polarity of the junction never changes, reducing ambiguity in data interpretation. While a thermal damage removal step is often conducted after ion implantation, typically involving a 1 min rapid anneal at $900\text{--}1000 \text{ } ^\circ\text{C}$, this step was eliminated because the 30 min soak step at temperatures above $900 \text{ } ^\circ\text{C}$ would serve to include this damage removal in the initial seconds at high temperature.

After implantation, a 160-nm -thick layer of silicon nitride was deposited on the front side of the wafer using plasma-enhanced chemical vapor deposition, in order to prevent further oxidation of the surface during the soak process as well as block outdiffusion of the dopants. Although the nitride layer will densify after a high-temperature soak step, it is deposited on top of the existing oxide layer such that submersion in a dilute hydrofluoric acid will etch the oxide layer through defects in the nitride layer, undercutting and completely removing it. Implantation and soak processes were modeled using TSUPREM-4, to predict the changes in dopant concentration profiles under different process parameters and implant doses.

Calibration of the method was carried out by placing small samples, prepared as described above, into a tube furnace of constant temperature for 30 min for the soak step. Samples were then etched in a dilute HF solution with periodic agitation to remove the nitride and oxide layers. Sheet resistance measurements were taken across the top surface of the bare wafer using a Jandel square-array four-point probe with probe-tip spacing of 0.6 mm .

IV. RESULTS

A. Simulation of diffusion and resistance

After ion implantation, the boron and phosphorus profiles were mainly concentrated around 150 nm from the wafer surface according to simulation of the implantation in TSUPREM-4, as shown in Fig. 2(b). The dopant profiles extend into the oxide layer due to its presence during implantation, acting as a protective layer against implantation damage and a screening layer to ion channeling. The dopants create a p-n junction approximately 190 nm from the top surface, where the dopant concentrations are equal, with the n-type side at the surface. As the wafer is soaked for 30 min at various temperatures, the dopants diffuse deeper into the wafer depending on their different diffusivities at the given temperature. Phosphorus has a higher diffusivity than boron above $\sim 900 \text{ } ^\circ\text{C}$ (Ref. 8) but it is implanted in a higher dose so that the top side of the junction is always n-type. At higher soaking temperatures, the dopants diffuse farther into the wafer, decreasing the measured sheet resistance as the junction moves deeper into the wafer.

TSUPREM-4 was used to calculate the expected sheet resistance of the top layer of the junction. The results of this simulation with the chosen process parameters are displayed

FIG. 4. TSUPREM-4 modeling results of sheet resistance variation in top layer of junction with soak temperature, showing constant resistance at lower temperatures, where dopant motion is negligible, and increasing and decreasing behavior of resistance as temperature increases.

in Fig. 4. The simulation predicts a constant sheet resistance for soak temperatures below 700 °C, for which there is no significant movement of the dopants during 30 min due to lower diffusivities in silicon. For example, the characteristic diffusion length of boron and phosphorus at 700 °C over 30 min is approximately 1.3 nm and 0.42 nm, respectively, which is small, compared to the width of the implanted concentration profile, on the order of hundreds of nanometers. However, due to the presence of an oxide layer on the silicon surface during the soak step, the concentration of phosphorus in the silicon has increased where it contacts the oxide layer due to a segregation coefficient greater than unity.^{12,13} In contrast, the concentration of boron decreases at the silicon-oxide interface due to a segregation coefficient less than unity. The segregation coefficient represents a comparison of the equilibrium solubility of each dopant in silicon versus in silicon dioxide, which will dictate the concentrations on each side of the interface that will yield equal Gibbs free energy values of the dopant at the interface.¹⁴ The result of both segregation behaviors are shown in Fig. 5(a). The overall upward slope of the profile is due to the distribution of the implantation, shown more clearly at a larger scale in Fig. 2(b). This surface dopant redistribution causes very large

concentration gradients at the interface, thus driving faster diffusion relative to other locations in the depth profile of concentration.

The consequence of this segregation is that the most significant diffusion at temperatures below 900 °C is the movement of dopants to decrease this steep surface gradient, causing surface P concentration to decrease and surface B concentration to increase. Figure 5(b) shows the profile at 750 °C, where the dopants in the bulk wafer have not moved noticeably but the surface concentrations of boron and phosphorus have increased and decreased, respectively, compared to their profiles at 600 °C. A decrease in the excess number of n-type carriers at the surface leads to an increase in resistivity, shown in Fig. 4 by the increasing resistivity between 700 and 900 °C. For soak temperatures around 900 °C, shown in Fig. 5(c), the segregation-related surface gradients have basically flattened out, and further dopant movement is due to the overall concentration gradient of the implanted profile, with a peak at 190 nm. For soak steps above 1050 °C, shown in Fig. 5(d), bulk dopant concentrations are changing during the 30 min timespan and the junction moves further into the silicon, causing the measured sheet resistance to diminish with temperature. In this higher temperature range, the bulk movement of both dopants drives the location of the junction farther from the surface and resistance decreases due to this increasing volume of silicon with excess P concentration.

B. Calibration

To connect the simulated results with the actual prepared samples, calibration measurements were carried out at a range of temperatures between 800 and 1400 °C. These calibration measurements yielded the experimental relationship between temperature and sheet resistance of the top layer of the p-n junction. Several different samples were prepared and soaked at each temperature, with several resistivity measurements taken per sample, and the results of this calibration are shown in Fig. 6. Each point represents a different sample, and scatter in the data may be attributed to slight

FIG. 5. Simulation of dopant profiles near oxide-silicon interface after 30 min soak at various temperatures, showing relaxation of the segregation-induced surface gradients. Oxide is shown at $x < 0$, and silicon at $x > 0$. Phosphorus concentration is plotted in black, boron in gray. Dashed lines represent profiles before soaking.

FIG. 6. Calibration data measured from prepared samples soaked at various known temperatures show similar behavior to simulated sheet resistance results, as seen in Fig. 4.

variations in wafer placement within the tube furnace used for calibration. Each point includes several measurements taken from the central region of the sample to reduce the influence of spatial variations within the sample. The overall behavior of the resistance increase, maximum, and decrease with increasing temperature as predicted from the simulations was clearly shown by the calibration samples as well. The values predicted by the TSUPREM-4 model shows an overall shift to higher sheet resistance values for any temperature, as compared to the measured calibration data. One calibration sample was run with the tube furnace set at 1400 °C, which caused the sample to melt. Given that the known melting temperature of silicon is approximately 1415 °C, there may be a 15 °C shift in the tabulated temperatures from the actual temperatures of the calibration samples. However, the overall relationship between resistivity and temperature still applies.

The higher measured resistance values compared to simulated values were suggested to be due to oxidation occurring through the nitride layer during high-temperature soak steps, causing oxidation-enhanced diffusion (OED).¹⁵ Because both boron and phosphorus diffuse in silicon primarily by the interstitialcy mechanism,⁸ and the oxidation reaction injects interstitials into the underlying silicon, the diffusivities of both dopants in silicon are thus enhanced when oxidation occurs. Small amounts of oxidation may cause OED effects to be most pronounced at the surface, causing a larger rise in resistivity than predicted by the TSUPREM-4 model. Dopant diffusion enhancement by oxidation depends on the fraction of diffusion due to the interstitialcy mechanism, as opposed to the vacancy mechanism, for a particular dopant. Several researchers have measured this fractional contribution for boron and phosphorus, with varying results,^{15,16} but Antoniadis *et al.*¹⁷ suggest that phosphorus may have a slightly higher fraction of interstitialcy diffusion. In this case, the diffusivity of phosphorus would be more affected by the process of oxidation, and the phosphorus peak would diffuse more quickly than predicted, reducing the difference in concentration between dopants and increasing the resistivity.

FIG. 7. Simulated and measured depth profiles of B and P concentration in sample soaked for 30 min at 1000 °C in argon atmosphere (o) and in air atmosphere (x), compared to simulation results (—), showing a smaller surface concentration difference between dopants for the measured samples. Boron plotted in gray, phosphorus plotted in black.

Visual observation of samples after soaking above 1300 °C reveals a noticeable change in color, indicating a change in the oxide layer thickness. This fact suggests that oxidation is able to occur despite the protective nitride layer capping the wafer. It is likely that lower-temperature soak steps also incurred smaller amounts of oxidation.

To verify whether oxidation was causing this resistivity shift from predicted data, two samples were soaked for 30 min in a quartz tube furnace at 1000 °C under flowing argon. The sheet resistance of these samples was measured to be 170 Ω/sq, which is lower than that of samples soaked at the same temperature in air by ~30 Ω/sq. This supports the explanation that oxidation occurring in the air-soaked samples causes an increase in diffusion of the dopants. However, the argon-soaked sample still has higher resistivity than the simulations predict for that temperature.

To further determine the extent of oxidation, the depth profiles of air- and argon-soaked samples were measured using secondary ion mass spectroscopy (SIMS). As shown in X and O points in Fig. 7, both dopants have diffused farther from the wafer surface in the oxygen-soaked sample, indicating that even at 1000 °C, the OED is enough to affect the underlying dopant profile. The junction depth in the air-soaked sample is 36 nm farther from the surface than in the argon-soaked sample, and the phosphorus peak concentration is also lower for the sample soak in air.

Comparing the SIMS-measured depth profile of the argon-soaked sample to the simulated results in TSUPREM-4, shown in dashed lines in Fig. 7, it is clear that there is a significant difference in the profiles of both dopants between modeled and measured concentrations. Specifically, the difference in concentration between phosphorus and boron in the top 150 nm for the modeled profile is much larger than the difference in concentration for the measured sample. This profile difference should result in a higher resistivity for the calibration sample, and this is consistent with what is measured and shown in Fig. 6.

Above 1000 °C, the decrease in resistivity is due to a broadening of the top layer of the junction and overall decrease in both dopant concentrations at any position above the junction. The higher the temperature of the soak step, the

FIG. 8. High-temperature subset of measured calibration data for temperature and sheet resistance shown in black circles, with curve fit shown in solid line.

deeper the junction is and the lower the sheet resistance measured. This behavior corresponds well with the predictions of the TSUPREM-4 model discussed previously.

It is clear that this technique is appropriate for measurement of environments with temperatures above 800 °C, due to negligible movement of the dopants in a 30 min period at low temperatures. However a modification could be made by using longer soaking times such that dopant diffusion length is significant at slightly lower temperatures. For example, increasing the soak time to 300 min would shift the minimum temperature of the monotonic range to ~900 °C, from 1050 °C as shown for 30 min. However, such a long soak time may be impractical in some applications.

One way to achieve a strictly decreasing behavior is to use lower implant doses of dopants, on the order of $1 \times 10^{14} \text{ cm}^{-2}$, where simulation results indicate that diffusion of surface species due to segregation has a negligible effect on measured resistivity. This behavior may be due to the lower absolute magnitude of the concentration gradients at this lower implant dose, resulting in lower diffusion flux. However, this lower implant dose is less repeatable than implant doses of $1 \times 10^{15} \text{ cm}^{-2}$, and the consistency of higher doses was desirable for the development of the technique in this work.

For a monotonic relationship between temperature and measured resistance for the given parameters, the current method is restricted to temperatures above 1050 °C. This range of data is depicted in Fig. 8, which is a subset of the data shown in Fig. 6. A quadratic fit was made to the calibration data in the range of temperatures above 1050 °C, and was subsequently centered at 1260 °C and scaled by a factor of 100, given by

$$R_{sh} = -6.17T_o^2 - 43.7T_o + 127.6$$

where $T_o = (T - 1260 \text{ °C})/100$. It is clear that the scatter in the experimental data decreases as temperature increases, most likely due to the overall larger movement of the dopants at these temperatures, whereas low-temperature movement occurs over smaller distances, which is more subjective to small temperature variations between samples. This relationship was used to relate subsequently measured sheet re-

FIG. 9. Schematic of wafer in resistively heated zone furnace.

sistances to corresponding temperatures between 1050 and 1400 °C.

C. Application of technique

To apply this method in a high-temperature environment with a spatially varying temperature field, a rectangular wafer of 25 mm width and 100 mm length was prepared with dopants as previously described. This wafer, between two silicon carbide backing plates of 1 mm thickness, was placed centrally in the hot zone of a high-temperature furnace, defined by six resistive silicon carbide heater elements in two horizontal rows, with the wafer located between the two rows. The total width of the hot zone was ~50 mm. A schematic representation of the wafer's position in the furnace is shown in Fig. 9. The temperature of the heater elements was set at 1585 °C, controlled by a series of two-color pyrometers. Upon removal from the hot zone, it was observed that a small oval-shaped zone became molten during the 30 min soak. This region can be used as a reference point of known temperature.

The entire area of the sample can be measured using a four-point probe if a correction factor is used to adjust the sheet resistance measurement near the wafer edges. The correction factors, $C.F.$, for rectangular- and square-array probes are given by Catalano.¹⁸ In general, $C.F.$ deviates from unity only when the distance of the probe from the wafer edge is less than $4s$, where s is the spacing between probe tips. This edge-effect distance of $4s$ also indicates the lateral resolution of the measurement, dependent on the spacing of the probes being used, implying that the resistance measured will be affected by variations within $4s$ of the outermost probes. Probes in this measurement were 0.6 mm apart. Using resistivity correction factors near sample edges, a temperature map was generated from the sample resistance measurements. Shown in Fig. 10(a), the temperature reveals a hot zone of ~50 mm in length, corresponding to the location of the three heater element rods above and below the sample. Temperatures are greater than 1400 °C in this hot zone. The measurement has revealed that the hot zone has a central

FIG. 10. (Color online) Measured data of temperature profile showing a hot zone along furnace length, for heating elements set at two different temperatures. Temperature colorbar shown in °C.

maximum near the center heating element. While the temperature-resistivity relationship cannot be applied to the region that was molten during the process, it can be used as a check to make sure that the surrounding areas show temperatures approaching the melting temperature of silicon. Indeed, the measured points near this region show a reasonable approach to 1420 °C. It is also clear that the wafer center point is offset from the center of the hot zone, revealing more of the temperature profile on the right side of the furnace.

A second wafer was tested at different heater element settings to test the sensitivity of the furnace profile to variations in heater element temperatures. In this case, the elements were set to a constant temperature of 1530 °C and the entire sample remained solid during the process. The resulting temperature map is shown in Fig. 10(b). This wafer reached a maximum temperature of 1389 °C in the center with a ~50 mm hot zone with temperatures above 1375 °C. A comparison with the first sample shown in Fig. 10(a) shows that the 55 °C decrease in heater element setpoint results in a 25 °C decrease in hot zone temperature.

One common feature between both measured temperature profiles is the slight curvature in the isotherms across the width of the wafer. The slightly lower temperatures at the wafer edges are most likely due to a temperature gradient in the cylindrical heater elements across their length, which is approximately 50 mm, and the decrease in temperature as they touch the electrical contacts at the furnace walls. Clearly, these measurements have revealed the temperature

gradients surrounding the hot zone of the furnace and their dependence on heater setpoints, and such parameters can be critical to the final quality of zone-processed wafers. Similar characterization of wafer oxidation and diffusion furnaces could illuminate nonuniformities in the temperature distribution, facilitating furnace diagnosis, and improvement for consistent processing.

V. DISCUSSION

Using the specifications described in the previous sections, this method can be used to characterize temperatures above 1050 °C. As described in Sec. IV, these parameters yielded a nonmonotonic behavior of sheet resistance with increasing temperature due to the movement of surface concentrations due to segregation effects at the silicon-oxide interface. Consideration was given to switching the dopant species such that the phosphorus implant dose was lower than the boron dose, such that segregation-related movement at the surface would not cause an increase in sheet resistance for temperatures between 700 and 1000 °C. If this approach could achieve a monotonic relationship, it would increase the temperature range over which temperature profiling could be useful. However, the segregation effects still complicate the results—if the concentration of phosphorus is too close to the higher boron concentration, the segregation effects will cause the phosphorus to increase at the surface, above the surface level of boron, as shown in Fig. 11(a). This behavior actually creates a second junction near the surface, and changes the polarity of the surface region as the majority dopant is now n-type at the surface. Beyond the very surface, boron is the majority dopant up to a distance of ~190 nm, as implanted, and this junction at 190 nm is only one that should be present for this measurement. After a soaking step at a high temperature, these segregation effects diffuse away to leave a single junction as is desired but the diffusivities at lower temperatures are not sufficient for this to occur.

At a certain threshold temperature, the diffusivity of the dopants is high enough to diffuse away those surface effects in the 30 min period, resulting in a single junction. If the ratio of phosphorus to boron implant doses increases closer to unity, then the segregation effects cause a much larger surface excess of phosphorus, which increases that threshold

FIG. 11. Simulation of dopant concentration profile after initial implantation of dopants for higher dose of boron than phosphorus, showing surface effects of segregation, and consequent behavior of sheet resistance with soak temperature.

temperature at which diffusion is fast enough to diffuse away the surface effects. This behavior is reflected in Fig. 11(b), where the threshold temperature (the lowest-T plotted data point for X and O curves) is shown to increase as the ratio of P:B increases. Conversely, reducing the dose of phosphorus will decrease the impact of its presence at all, approaching the result for implanting only boron in an n-type wafer, shown in gray diamonds in Fig. 11(b). Above $\sim 1000^\circ\text{C}$, the resistance-temperature curve has a very flat slope, as seen in Fig. 11(b), making it poorly suited to measuring those temperatures. Therefore this technique produces better results when phosphorus is implanted in a higher dose than boron.

Another possible approach is to use two dopants with similar segregation behaviors, such that their movements at the oxide-silicon interface have the same trend with respect to resistivity as the overall movement of the implanted dopant peaks. For example, gallium is a p-type dopant with a segregation coefficient greater than unity, similar to phosphorus, which is n-type. Therefore, P and Ga could be a useful pairing for implantation, to potentially produce monotonic behavior of resistivity with temperature. To the same effect, the oxide layer could be etched away before any high temperature processing and replaced with a thin film cap that produces different segregation behavior in contact with silicon.

The concept of using the temperature dependence of dopant diffusivity to alter the resistivity of silicon could alternatively be applied in a lateral configuration for increased sensitivity. Specifically, instead of implanting dopants in a uniform layer across the wafer, they could be implanted in a two-dimensional array of islands across the surface. At high temperature, each island of highly concentrated dopant would diffuse laterally across the wafer plane as well as vertically, and the resulting resistivity would depend on the spacing and size of the implanted points, in addition to the temperature. The island array dimensions could be designed to suit the specific application. Further modeling and development is needed for this concept.

VI. CONCLUSION

In summary, a novel method has been developed and proven for characterizing the two-dimensional temperature profile experienced by a silicon wafer in a high-temperature environment. This new temperature profiling method has shown to be promising and useful for measurement of the high-temperature range field of thin silicon geometries. The simultaneous diffusion of two different dopants from the surface of the wafer was simulated using TSUPREM-4 and successfully calibrated to show the same behavior of sheet resistance as a function of increasing temperature. The technique was successfully implemented to show the effects

of variations in furnace heater conditions on the temperature fields experienced by silicon samples without altering the furnace geometry or heat flow conditions. This noninvasive, low-complexity method is promising for characterization of other constrained-geometry high-temperature environments in silicon processing, such as wafers in tube furnaces, where other methods are insufficient.

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5.6. Results of Re-crystallization

Hundreds of re-crystallizations were performed over the course of the program. Re-crystallization rates ranges from 10 mm/minute to 60 mm/minute. Experiment were performed with a wide array of temperature profiles as created by applying different amounts of power to the heaters used in the furnace. For the first two years of the program, the furnace had 3 pairs of heaters (a pair consists of a heater over the top backing plate and a heater under the bottom backing plate). In the last year of the program a fourth heater pair was added in order to exercise better control of the temperature profile in the cooling portion of the wafer traverse.

Initially samples of 25 x 25 mm were recrystallized and sometimes as large as 40 x 40 mm. Eventually we standardized on samples of 25 x 100 mm, with the 100mm direction aligned to the direction of travel. The purpose of these longer substrates was to follow the propagation of grains over a distance more representative of what would be the case for full length wafers of 156mm.

A huge variety of grain structures were observed over the course of the program. Rarely were grains of less than 5mm in extent observed – already large enough for solar cells. Figure 11 below shows a re-crystallized wafer which is representative of the wafers made toward the end of the program. The first to enter (and first to leave) is the right hand edge. That is, the wafer was travelling left to right. The wafer has been etched to reveal the grain structure. As can be seen initially there is a single grain which propagates as a single grain for a distance of approximately 35mm. An nucleation event takes place. The cause of this event iunknown. This event then leads to the expanding propagation of a new grain which continues until it has nearly replaced the original grain. Several smaller grains are also evident after the first nucleation event.

Figure 11. A 25 x 100 mm re-crystallized sample which was moving left to right. Note that the sample was initially single crystal and then underwent several nucleation events.

Remarkably, some fully single crystal samples were also made. This was not a common occurrence, but did repeat several times. Figure 12 shows a photo of such a sample. Yes indeed, this has undergone the same etching regimen used to reveal the grains in Figure 11. Again, this sample was travelling left to right.

Figure 12. A single crystal sample made by re-crystallization. The right edge was first in and first out of the furnace.

Dislocation etching was commonly performed to reveal the dislocation densities and their distribution. Generally, the dislocation densities were found to be lower than those of industry standard cast multicrystalline wafers. Figure 13 shows a case here a standard multi wafer was used as the preform and the recrystallization was stopped part way through the furnace. The furnace was cooled and the sample removed and then grain etched. What can be seen is that the portion of the wafer that was re-crystallized is significantly lower in dislocation density than the portion that was not re-crystallized.

Figure 13. A partially re-crystallized wafer which has been etched to reveal dislocations. The direction of travel was left to right. The right-most third of the wafer was been re-crystallized and is lower in dislocation density.

5.7. Solar Cell Results

We used standard processing to make 2 x 2 cm test cells to evaluate the re-crystallized material. The junction was made a POCL tube diffusion to a conservative sheet resistance of 60 ohm/square. The AR coating is an industry standard PECVD silicon nitride deposited by remote plasma in a Roth and Rau tool. The front grid is screen printed silver. The back is full area screen printed aluminum pastes which was co-fired with the front. A cell made on re-crystallized material is shown to the right in Figure 16.

Figure 16. A 2x2 cm cell on re-crystallized material

The IV curve and measured parameters for our champion cell is shown below. It should be noted that this wafer had no light trapping texture and such texture should be expected to increase the cell efficiency by at least 1% absolute. These are good results early in the development of a new wafer technology.

Section 6. Publications

Theses Completed under this Program:

Silicon Cast Wafer Recrystallization for Photovoltaic Applications

Eerik Hantsoo, Master of Science, MIT, June 2008

Geometry Control of Recrystallized Silicon Wafers for Photovoltaic Applications

Christopher Ruggiero, Masters of Science, MIT, June 2009

Nucleation and Solidification of silicon for Photovoltaics

Anjuli Appapillai, Doctor of Philosophy, MIT, June 2010.

Development of a Melting and Directional Solidification Process for Improving the Grain Structure and Electronic Properties of a Silicon Wafer

Allison Greenlee, Master of Science, May 2011.

Papers Published in Referred Journals

Nucleation Properties of Undercooled Silicon at Various Substrate J. Applied Physics, **109**, 084916 (2011), Anjuli T. Appapillai, Christoph Sachs, and Emanuel M. Sachs.

The effect of Substrate Material on Nucleation Behavior of Molten Silicon for Photovoltaics, J. Crystal Growth, **312** (2010) Issue 8, 1297-1300, Anjuli Appapillai, Emanuel Sachs.

A Method for Temperature Profile Measurement of Silicon Wafers in High-Temperature Environments, Journal of Applied Physics, **109**, 034902 (2011), Anjuli T. Appapillai and Emanuel M. Sachs.