Use of COTS Microelectronics in Radiation Environments

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Abstract

This paper addresses key issues for the cost-effective use of COTS microelectronics in radiation environments that enable circuit or system designers to manage risks and ensure mission success. COTS parts with low radiation tolerance should not be used when they degrade mission critical functions or lead to premature system failure. We review several factors and tradeoffs affecting the successful application of COTS parts including (1) hardness assurance and qualification issues, (2) system hardening techniques, and (3) life-cycle costs. The paper also describes several experimental studies that address trends in total-dose, transient, and single-event radiation hardness as COTS technology scales to smaller feature sizes. As an example, the level at which dose-rate upset occurs in Samsung SRAMs increases from 1.4x10⁸ rads(Si)/s for a 256K SRAM to 7.7x10⁹ rads(Si)/s for a 4M SRAM, indicating unintentional hardening improvements in the design or process of a commercial technology. Additional experiments were performed to quantify variations in radiation hardness for COTS parts. In one study, only small (10-15%) variations were found in the dose-rate upset and latchup thresholds for Samsung 4M SRAMS from three different date codes. In another study, irradiations of 4M SRAMS from Samsung, Hitachi, and Toshiba indicate large differences in total-dose radiation hardness. The paper attempts to carefully define terms and clear up misunderstandings about the definitions of "COTS" and "radiation-hardened" technology.

I. INTRODUCTION

Interest in COTS technology for military systems is part of the latest chapter in DoD Acquisition Reform dating back nearly fifteen years to the Grace and Packard Commissions. In April 1994, a Process Action Team (PAT) chartered by Coleen Preston, Deputy Undersecretary of Defense for Acquisition Reform, issued a series of recommendations for DoD acquisition reform in a document entitled "Blueprint for Change [1]." The document described a new way of doing business and this quote, taken from its Overview, makes the key point: "Defense acquisition reform is no longer a desirable goal; it is a national imperative. DoD's declining procurement budgets can no longer sustain a defense-unique industrial base to supply its needs. Without access to a broader national manufacturing and technology base, defense downsizing could jeopardize basic national security goals." On 29 June 1994, then Secretary of Defense (SECDEF) William Perry issued a memorandum [2] to the services and defense agencies that accepted the findings of the PAT, as well as an independent Industry Review Panel. The SECDEF memorandum, later termed the Perry COTS Initiative, largely dealt with specifications and standards, but in a press conference Perry summed up his thoughts on the use of COTS parts in military systems.

- Buy more commercial products
- Make greater use of commercial buying practices
- Use industrial specifications in place of military specifications
- Reduce cost

The Perry COTS Initiative is basically about acquisition reform. The main point was to get government (i.e., the customer) to set "performance-based" specifications that state requirements in terms of results with criteria for verifying compliance, but without stating the methods for achieving the required results. The government was to tell the contractor the "whats," but not the "hows." The aim was to have the government become a customer rather than a developer/producer. Make no mistake, a primary driver for the increased use of COTS parts was cost. Just switch the "T" and "S" in CO'TS" and you get CO'ST." Reductions in cost were correctly viewed as a natural outcome of acquisition reform.

The initial thinking on the use of COTS parts in radiation environments is illustrated on the left side of Fig. 1. COTS technology was viewed strictly as high volume, low cost technology with very low radiation tolerance. At the other extreme was "radiation-hardened" (RH) technology, with its low volume, high cost, and relative immunity to the detrimental effects of radiation. Radiation-tolerant (RT) technology sought the middle ground between COTS and RH technology. Historically, COTS technology was defined as susceptible to latchup (LU) with total-ionizing-dose (TID) failure levels less than 50 krads(Si) and single-event upset (SEU) error rates >10⁵ errors/bit-day. RH technology was LU immune with TID failure levels in excess of 200 krads(Si) and SEU error rates <10⁵ errors/bit-day. But these levels are
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A. What is radiation-hardened technology?

Although the concept of RT technology is intuitively appealing, the authors believe it can be potentially confusing and difficult to quantify.

Since COTS was associated with a hardness level, the proposal to heavily rely on COTS in military systems caused a great deal of alarm in the radiation-effects community. The primary concerns were that use of COTS would lead to premature system failure and greatly increase mission risk. In addition, the abandonment of military specifications and quality systems (e.g., QPL, Qualified Parts List and MIL-STD-883, Group E tests [3]) was troubling, since these documents embodied much of our knowledge of radiation effects and its application to test techniques and hardness assurance approaches.

Despite these concerns, designers of military systems, which often must operate in radiation environments ranging from natural space to a hostile nuclear threat, will no doubt strive to use the latest semiconductor microelectronics technologies for enhanced processing capability, autonomous control, and low power operation. There is no escaping the fact that the commercial electronics market is driving the electronics industry. While defense electronics was once 60 to 70% of the electronics industry in the early 1960’s, it is now about 0.05% of a $150B market! Clearly, we need to use COTS when it will reduce cost and still get the job done. This paper addresses several key issues associated with the cost-effective use of COTS microelectronics in radiation environments. The results of several experimental studies are presented to provide a technical basis for hardness assurance approaches and techniques required for the successful implementation of COTS. The final sections of the paper discuss system hardening techniques and life-cycle costs.

II. DEFINITION OF TERMS

A. What is radiation–hardened technology?

From the designer’s perspective, the important and distinguishing feature of RH technology is that radiation hardness is qualified and guaranteed by the manufacturer. RH technology would include QML-qualified product from Lockheed Martin Federal Systems Manassas (LMFS), Honeywell Solid State Electronics Division (HSSED), or Harris Semiconductor (HS) capable of operation at 1 Mrad(Si), as well as product from UTMC/AMI or National capable of operation at 100 krad(Si). RH technology would even include product hard to only 20 krad(Si), if the manufacturer wants to guarantee radiation hardness for a given low-dose tactical application. Basically, we believe any technology is RH if the manufacturer assures its radiation hardness. (In addition, radiation hardness can be guaranteed by a third party which does not actually manufacture the integrated circuit die, but does qualify the product for a given hardness level.) RH technology is not defined as a level, but by process, design, and qualification controls necessary for radiation-hardness assured product. The key point is who accepts the risk. When purchasing parts from non-RH vendors for use in radiation environments, please note that the customer is responsible for assuring the level of radiation hardness. These definitions of risk are historically referred to as “Radiation Hardness Assured” and “User RHA.”

In addition to the manufacturer’s guarantee of radiation hardness, RH technology is often characterized as technology in which the manufacturer has taken specific steps (i.e., controls) in materials, process, and design to improve the radiation hardness of a commercial technology [4]. For improved TID hardness, changes in the “isolation” structure may be required, e.g., a heavily-doped region or “guardband” can be formed by ion implantation that effectively shuts off radiation-induced parasitic leakage paths. In addition, a low thermal budget and minimum hydrogen during processing has been found to improve TID hardness. High-resistance feedback resistors, switched capacitors, cross-coupled transistors, and oversized transistors are often implemented for improved single-event-upset (SEU) immunity. For improved LU and transient dose-rate (DR) immunity, the change can be as simple as use of an epitaxial substrate. Finally, SOI technology that employs an active device layer built on an insulating substrate can provide significant improvement in DR and SEU tolerance.

There are also several design approaches [4] that can be used to increase radiation hardness. One global design change is the conversion of dynamic circuitry to full static operation, thereby placing data in a more stable configuration that is less susceptible to the perturbing effects of radiation. The use of wide power busses, multiple $V_{DD}/V_{SS}$ pads, frequent well/substrate ties to power busses, fewer fan-in/out gates, and no DC current paths to ground help prevent rail-span collapse that results in DR upset. For TID, n-channel transistors can be designed in “closed” geometry that shut off parasitic leakage paths. For SEU, memory cells with additional transistors, oversized transistors, and oversized transistors are often implemented for improved single-event-upset (SEU) immunity. For improved LU and transient dose-rate (DR) immunity, the change can be as simple as use of an epitaxial substrate. Finally, SOI technology that employs an active device layer built on an insulating substrate can provide significant improvement in DR and SEU tolerance.
Logic, etc.) are not willing to make process and design changes to their manufacturing process that would improve radiation hardness and, consequently, the radiation hardness of COTS is often low and variable.

A few RH vendors exist that supply parts at strategic hardness levels of \( >1 \) Mrad(Si), \( 10^9 \) rads(Si)/s, no LU, and \( <10^{10} \) errors/bit-day. Other RH suppliers employ a strategy to make minimally non-invasive changes to the commercial process flow, improving the radiation hardness by an order of magnitude, while maintaining the high reliability and yield of the commercial flow. National’s 0.65-\( \mu \)m CMOS65 and UTMC/AMI’s process flows [5] are both examples of RH technologies subjected to a few key process steps to improve hardness. Typically, such technologies have guaranteed TID hardness levels approaching 100 krad(Si), LU immunity, and SEU error rates of \( \sim 10^{-10} \) errors/bit-day. (Previously, the National and UTMC technologies would have been referred to as RT technologies.)

B. What is our definition of COTS?

"COTS" means that the product is Commercially available Off The Shelf. It means that you are buying what the supplier offers as their standard product, which can be found in supplier databooks or Standard Military Drawings (SMDs). A diode from Radio Shack is COTS. A radiation-hardened R6000 microprocessor LMFS is also COTS, although it doesn’t meet the high volume and low cost associated with commercial offerings. In addition, ASICs with standard cell libraries and Gate Arrays (GAs) that allow for typical user specifications are still characterized as COTS. (Since ASICs or GAs are designed with the same rules and fabricated on the same process line, we regard them as high-volume, low-cost “standard” product.) We define product that is not commercially available in supplier databooks as “Custom.” Custom parts often involve a unique design for a specific application that has a very small market. Sometimes, they are “special order” from a COTS supplier. For example, a customer may require a change in layout or a different type of packaging. The customer must pay for these changes. Custom products are generally defined in a Source Control Drawing (SCD).

Once again, our definition of COTS differs from the idea that COTS parts are exclusively reserved for high volume, low cost technology. The definition uses a literal interpretation of the acronym COTS and the belief that product found in databooks is notionally a “standard” product. We define product that is not commercially available in supplier databooks as “Custom.” Custom parts often involve a unique design for a specific application that has a very small market. Sometimes, they are “special order” from a COTS supplier. For example, a customer may require a change in layout or a different type of packaging. The customer must pay for these changes. Custom products are generally defined in a Source Control Drawing (SCD).

Although suppliers of radiation-hardened (RH) technology like LMFS, HSSED, or HS carefully control and qualify their technology (through QML, Qualified Manufacturer’s List [6-8]) to meet high levels of radiation, most commercial parts suppliers do not identify or control technology parameters that affect radiation hardness. Consequently, radiation hardness of COTS microelectronics is often low and highly variable and, more importantly, the manufacturer will not guarantee radiation-hardness levels. For example, state-of-the-art CMOS microprocessors, e.g., an Intel Pentium II chip, will fail at total-dose levels as low as a few kilorads and suffer latchup if exposed to high-energy particles in space [9]. Consequently, the focus of this work is to address the challenges of using COTS parts in radiation environments from manufacturers that don’t guarantee RH levels.

The lack of availability of RH-COTS microelectronics dictates that most high-performance COTS parts will likely be susceptible to radiation-induced degradation. However, COTS parts may exhibit higher levels of radiation hardness that result from unintentional variations in processing. In such cases, “upscreening” by the customer is required to identify those fabrication lots or wafers that can meet system requirements. Upscreening can be expensive and time consuming, and there is still the concern that process variations across a fabrication lot (or even a wafer) create uncertainty in radiation hardness. In any case, the customer performs radiation testing and assumes all risk. For user qualified product, the higher the radiation requirements of the system, the greater is the testing expense to identify satisfactory standard commercial electronics, and the greater is the reward for using radiation-hardened parts with reduced testing requirements [10].

III. EXPERIMENTAL STUDIES

A. Projected Technology Trends

Table 1, provided by DTRA [11], summarizes the expected effects of increased integration density and reduced operating voltage on radiation sensitivity. The chart indicates that single-event upset, single-event latchup, dose-rate upset (transient), and total-ionizing dose hardness will degrade as MOS and bipolar technologies scale to smaller feature sizes and reduced operating voltages. We review each of the entries in the table.

SEU is expected to degrade due to a reduction in nodal capacitance and voltage (i.e., notionally a reduction in “critical charge”) [12]. Although the chart indicates that single-event latchup (SEL) is expected to degrade, reductions in operating voltage and increased doping densities argue otherwise. For MOS, SEL will become less significant as \( V_D\text{dd} \) approaches 1 V. For bipolar, SEL has only been reported for an Analog A/D Flash Converter [13], but the authors subsequently
characterized their findings as a “high-current anomaly” and not a latchup (i.e., parasitic thyristor) event [14]. In general, there have been few reports of SEU in bipolar technology, but single-event transients in linear microcircuits are becoming an increasing concern [15].

Dose-rate upset levels may degrade if there is an increase in the effective junction area on the chip in which photocurrents are generated. In addition, complex metal routing schemes may contribute to rail span collapse and failure in the transient environment. If an epi layer is incorporated in the technology, then improvements in dose-rate tolerance might be expected. Finally, design rules for improved noise immunity and speed require more frequent metal contacts that may once again lead to improvements. The results of several experiments are reported in this paper to examine this trend which is ambiguous at best.

The table suggests that TID will get worse, but this is hard to determine. TID levels will be governed by the hardness of isolation oxides because thin gate-oxides are relatively immune due to limited collection volumes and interfacial tunneling. Since the LOCOS isolation process scales down to 0.35-µm, one might believe that hardness levels would remain the same or improve slightly as isolation oxides get thinner and higher well dopings increase the threshold for the “turn-on” of parasitic leakage paths. However, many manufacturers are migrating to “shallow trench” and the impact on hardness is unclear [16]. The important point is that right now at 0.5-micron, some circuits fail from isolation-oxide leakage at doses as low as a few kilorads [17], so it is hard to imagine that TID could get worse as technologies scale.

Table 1. Expected effects of increased integration density and reduced operating voltage on radiation sensitivity.

<table>
<thead>
<tr>
<th>Technology</th>
<th>SEL*</th>
<th>SEU*</th>
<th>Total Ionizing Dose</th>
<th>Displacement Damage</th>
<th>Dose Rate Upset</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS</td>
<td>X</td>
<td>XX</td>
<td>X</td>
<td>O</td>
<td>XX</td>
</tr>
<tr>
<td>Bipolar</td>
<td>X</td>
<td>XX</td>
<td>X</td>
<td>✓</td>
<td>X</td>
</tr>
</tbody>
</table>

* SEL = Single Event Latchup  
SEU = Single Event Upset

There is a slight improvement in the hardness of bipolar technologies with respect to displacement damage as active device “base” regions are reduced in depth (i.e., higher ft) and doping levels increase. There is no change in MOS with respect to displacement damage because MOS is a majority carrier device that is not sensitive to bulk lattice or displacement damage.

The trends summarized in Table 1 suggest lower radiation hardness as MOS and bipolar technologies scale to smaller feature sizes. To be fair, it is very difficult to make predictions of technology trends using simple scaling rules, since changes in design, process, and technology can offset and alter the expected response. In some cases, the spacecraft designer may choose to raise the operating voltage, trading off low-power requirements and reliability (e.g., single-event gate rupture, [18]) for improved radiation hardness. Finally, it is worth noting that new physics and failure modes occur as technologies scale - some examples are multi-bit upset, micro-dose, and micro-latchup. The only way to realistically assess these trends is to gain actual knowledge of advanced COTS technologies through experimentation and test.

B. Experiments that address trends in total-dose, transient, and single-event radiation hardness of COTS

In this section, we report the results of several experiments to quantify the impact of technology trends on the radiation susceptibility of CMOS technologies. The results of these experiments will be compared to the predictions of Table 1. In the first experiment, we examine the effect of scaling on dose-rate susceptibility of CMOS SRAMs. Figure 2 shows photocurrents for 256K, 1M, and 4Mbit SRAMs from Samsung irradiated at room temperature and 4.5 V with -20-ns FWHM pulses of 40-MeV electrons at the NSWC.
gigaohm pull-up resistors, and LOCOS isolation. Pre-irradiation currents for the 256K, 1M, and 4M were <1 μA, 2.2 mA, and 5.5 mA, respectively. DPA also revealed (1) memory array areas for the 4M:1M:256K are in the ratio of 5.7:2.8:1, (2) total common drain areas for the 4M:1M:256K are in the ratio 8.2:2.8:1, (3) the 256K and 4M have a 7-μm epi layer while the 1M is bulk, and (4) the spacing between $V_{DD}$ contacts (to second-level polysilicon) for distribution to the memory cells) for the 4M, 1M, and 256K is 33, 51, and 38 μm, respectively. Based on the DPA findings, it is difficult to explain why photocurrents are independent of the level of integration. However, equivalent photocurrents suggest that radiation-induced current densities and associated rail-span collapse [19] will be lower at higher levels of integration. Consequently, we expect higher upset levels as the level of integration increases from 256K to 4M. Although the 256K and 4M were built on an epitaxial substrate, its 7-μm thickness probably provided little advantage over bulk in terms reduced photocurrent collection. In addition, higher dose rate immunity of the 4M may result from design rules for improved noise immunity and speed or from metal routing that reduces rail-span collapse. Unfortunately, bitmaps were not available to determine if rail-span collapse was the likely failure mode. A final thought is that upset levels may be determined at the local cell as opposed to distributed rail-span collapse. The common drain area of an individual memory cell is reduced as we scale from 256K to 4M, thus supporting the higher upset levels reported here for the 4M. This study clearly disagrees with the technology trend of Table 1 and further suggests that up screening may be a viable approach to identify SRAMs with improved performance in dose-rate environments.

In a second experiment, SEU tests of the Samsung SRAMs were performed at the BNL Tandem Van de Graaff accelerator using 141-MeV F, 210-MeV Cl, 265-MeV Ni, and 312-MeV Au ions. All parts were tested with a logical checkerboard pattern while exposing the parts at a bias of 4.5 V. No difference was observed using a pattern of all ones or all zeros. Three parts each of the 256K and 1M SRAM and one 4M SRAM are plotted in Fig. 3. Comparing the error cross section curves in Fig. 3, we observed no significant difference in upset threshold for these three designs. The upset threshold for all three designs was approximately 3-5 MeV-cm$^2$/mg and clearly indicates that state-of-the-art COTS is highly susceptible to SEU [20,21].

The saturation cross section of the 1M is 7-8 higher than the cross section of the 256K, while the cross section for the 4M is lower than that of the 256K. DPA of these parts suggest that the total sensitive drain areas of the memories steadily increase with integration level and that the effective gate lengths decrease, i.e., 0.5 μm for the 4M, 0.65 μm for the 1M, and 0.75 μm for the 256K. Based on the DPA results, we would expect an increase in the saturation cross section as these memories scale to smaller feature sizes. The DPA results offer no explanation of the unexpectedly low saturation cross section for the 4M. However, it is interesting to note that Poivey et al. [21] report a saturation cross section of $4 \times 10^3$ MeV-cm$^2$/mg for a 4M Samsung SRAM with the same die revision, which is even lower than what is shown in Fig. 3. We also note that the saturation cross section of 4M SRAMs was surprisingly variable. The saturation cross section varied by three orders of magnitude for a sample of seven 4M SRAMs from three different date codes; the curve in Fig. 3 is for the part with the highest measured cross section. These parts would readily upset in proton environments. Testing showed no SEL to an LET of 120 MeV-cm$^2$/mg, which is typical of many COTS SRAMs [17,20,21]. However, these tests were at nominal conditions, with bias at 4.5 V and room temperature i.e., not at a worst case bias of 5.5 V and elevated temperature. For these SRAMs, the memory array is built in a large p-well and is latchup immune since parasitic thyristor structures do not exist. In summary, the data suggest that state-of-the-art SRAMs are highly susceptible to proton-induced SEU and may be difficult to use in low-earth-orbit communications systems without EDAC or redundancy.

In a third experiment, Samsung SRAMs were irradiated in a Co-60 cell at a dose rate of 55 rad(Si)/s and 5 V. A checkerboard pattern was written to the memory prior to irradiation, and this pattern and its complement verified following irradiation. Surprisingly, the checkerboard (and not its complement) resulted in failing bits at the lowest doses [22,23]. For the 256K, the first failing bits occurred at 14 krad(Si), while for the 1M and 4M, the first failing bits occurred at 18 and 25 krad(Si), respectively. Additional irradiations of 4M Samsung SRAMs at a dose rate of 9.3 rad(Si)/s and 5 V increased the failure dose to >30 krad(Si). This slight increase was most likely due to in situ annealing of radiation damage. DPA revealed that all parts have LOCOS isolation, but provided no insight into the increase in TID hardness as the technology scaled from 256k to 4M. The LOCOS isolation thickness was 410 nm for the 256K, 670 nm for the 1M, and 480 nm for the 4M.
except for RH-COTS vendors, technology parameters that determine radiation hardness are not intentionally controlled during the manufacture of COTS parts. Consequently, one expects a wide variability in the radiation hardness of COTS parts. This claim is supported by several studies that have appeared in the literature in recent years [22,24-26]. In one study [22], the failure level for commercial SEEQ Floating Gate 256K E\textsuperscript{2}PROM\textsuperscript{s} measured across thirteen wafers from the same diffusion lot varied between 5 and 25 krad(Si). In addition, there was a factor of 3 variation for a single wafer! In an investigation of the effects of packaging and burn-in on the radiation response of National Semiconductor 54AC02 Quad 2-input NOR gates [24], leakage currents varied from $10^{-7}$ to $10^{-2}$ A following a 50 krad(Si) irradiation. Clearly, variability in the total-dose response of COTS is the most serious hardness assurance challenge for upscreening. The challenge to upscreen applies equally well to bipolar devices that exhibit an enhanced low-dose rate sensitivity to TID, i.e., ELDRS [27].

In Fig. 5, 4M Samsung SR\textsuperscript{AM}s from three different manufacturers were irradiated at a dose rate of 55 rad(Si)/s and 3.3 V. The Hitachi SR\textsuperscript{AM}s failed functionally at 14 krad(Si), the Samsung SR\textsuperscript{AM}s at 32 krad(Si), and the Toshiba SR\textsuperscript{AM}s at >100 krad(Si). Functional failure was defined as the dose at which the first stuck memory cell occurred. Several parts from each manufacturer were irradiated and the variations from part to part were small (<20\%) for the Hitachi and Samsung parts, but more than a factor of two variation was observed for the Toshiba parts. From DPA, we were unable to identify any differences in isolation structures and cell design that would explain the improved TID tolerance of the Toshiba parts.

As mentioned above, TID hardness of COTS technologies is often quite variable. In MOS devices, charge transport and trapping in the amorphous SiO\textsubscript{2} gate insulator and isolation structures determine TID hardness. These properties depend on the detailed thermal cycles and ambients (e.g., hydrogen) that the device is exposed to during processing. It is not uncommon for a COTS vendor to make "minor" changes in processing that have a more significant, and often adverse, impact on TID hardness. Since TID hardness can vary significantly from lot to lot (or even from wafer to wafer within a lot), diffusion lot traceability may be important for ensuring radiation hardness of ICS. The implied assumption is that all material from a single date code is also from a single diffusion lot. In a study [28] of fourteen COTS vendors, it was found that date codes do not necessarily relate to the assembly date, but to the test date. This is because parts can only be binned and marked for performance after test, and full AC tests are not usually performed until after assembly. Also, there can be delays between assembly-and-test and test-to-mark depending on workload, priorities, and the location of facilities. In some cases, this delay can be as long as a month due to priorities and loads. In addition, COTS vendors use contract assemblers depending on the volume of their fabrication and assembly. Where contract assembly houses are used it is nearly impossible to get diffusion lot traceability, because all traceability is lost at the assembly level. In a study of the TID and SEU response of memories [29], a post-test destructive analysis revealed that in some cases supposedly identical parts contained a different die revision in the package, and indeed had different radiation characteristics! The bottom line is that we need to be careful in qualification of COTS components by acknowledging that parts from a given date code don't represent a single diffusion lot. This is very important if the radiation parameter of interest is sensitive to minor changes in processing.

In another experiment, the dependence of dose rate upset and latchup as a function of lot date code was examined for parts from three different date codes of Samsung 4M-bit SR\textsuperscript{AM}s exposed to 40-MeV electrons at 5 V at the NSWC Crane LINAC. An "upset" was defined as a change in the data pattern written into the memory prior to exposure. The data shown in Table 2 indicate <10\% variation in the average minimum dose-rate upset threshold. Four parts from each date code were tested. This small variation is a good indication...
that these memories have similar design, layout, and doping profiles in the silicon. Similarly, the variation in latchup sensitivity was <15% for these parts over these date codes, indicating that the parasitic bipolar transistors that control latchup are not varying from lot-to-lot. Unlike total-dose, dose-rate upset and latchup threshold may be somewhat independent of date code as long as basic technology/design parameters remain constant.

Table 2. Dose rate upset and latchup threshold for SRAMS irradiated at 5 V.

<table>
<thead>
<tr>
<th>Date Code</th>
<th>Average upset threshold [rad(Si)/s]</th>
<th>Average latchup threshold [rad(Si)/s]</th>
</tr>
</thead>
<tbody>
<tr>
<td>749</td>
<td>5.78E9</td>
<td>4.21E10</td>
</tr>
<tr>
<td>817</td>
<td>5.86E9</td>
<td>4.87E10</td>
</tr>
<tr>
<td>743</td>
<td>6.19E9</td>
<td>4.02E10</td>
</tr>
</tbody>
</table>

IV. SYSTEM HARDENING TECHNIQUES

Past systems found RH-COTS parts readily available and cost was seldom an issue. Since parts were quite robust in radiation environments, margins were often high, and subsystem and system hardening techniques were not overly emphasized. Today, with government demand to upgrade military forces using sophisticated defense and monitoring space systems and with NASA’s [30] need to support space exploration at lower cost, the use of high performance COTS is steadily growing. Although COTS parts can be upscreened for use in radiation environments, margins will be lower, and system-hardening techniques will be required to enhance design margins. In addition, upscreening to meet a complete set of radiation requirements is unlikely. For example, it might be possible to screen for improved TID hardness for a given space application, but it is unlikely that the same part will have the required SEU tolerance.

COTS parts must be considered high risk in radiation applications until proven or shown otherwise. This is a sobering thought, since with the increasing functionality built into a single microcircuit, there is an increased risk of massive mission failure due to the loss of a single device. The use of COTS presents many challenges and concerns for the system engineer. These concerns include:

- Possible increased sensitivity to radiation as technologies advance
- Variability in radiation hardness from lot to lot
- Changes in processes and designs without notification leading to degraded radiation hardness
- Absence of traceability to production lot
- Rapid obsolescence of a component
- Hardness assurance becoming the customer’s responsibility
- Manufacturers being unfamiliar with radiation-hardening techniques and approaches
- Radiation data unavailable or limited

- Minimal DC and AC parametric tests

These concerns dictate emphasis on system hardening techniques. There are a number of techniques at the system level for mitigating the radiation degradation of COTS components. Several of these techniques are described below. In addition to applying these techniques, it is important that these techniques be integrated into a design during the early stages of a new development program. Many projects have faltered from designing a board or a package without considering radiation effects until the design was near completion. This has resulted in slippage of schedules, costly redesigns, and overruns in budget and limited flexibility in subsequent hardening techniques. Once the board design is completed, one is generally limited to shielding, software control, or possibly pin-for-pin part replacement. For complex integrated circuits, such as a microprocessor or an ASIC, pin-for-pin replacements are difficult and costly.

In designing a cost-effective system, COTS should be used whenever possible. However, where a design is considered mission critical, an assessment for the use of RH-COTS parts must be made. For example, if a processor were required to control attitude, vectoring, location, or event sequencing for an entire system, it may be necessary to use a RH processor, such as the RH32 (from HSSED) or RAD6000 (from LMFS). In addition, in most military systems some type of RH memory is needed to protect operating states or modes of the system, possibly target codes, directional data, or other mission critical data. Hardened non-volatile memory elements for critical data in the past were usually magnet media of some sort, such as plated wire, ferrite cores or magnetic bubbles. Today semiconductor devices, such as nitride layered MOS devices or magnetoresistive devices are considered. These memory devices are used to store the critical data. After the radiation threat has passed, circumvention is needed to initiate the recovery of clean data from this memory.

System hardening methods associated with the use of COTS are listed below and a select few are discussed.

- Parts selection through upscreening
- Process technology selection, i.e., CMOS, bipolar
- Design using radiation-degraded parameters
- Dose rate characterization at high and very low rates
- Current limiting
- Shielding or localized shielding
- Conformal coating of boards
- Software and hardware error detection and correction
- Terminal protection devices at entry ports (TPDs)
- Circumvention or power strobe
- Watchdog timers
- Redundancy or triple voting logic
- Passive filters
- Minimize the number of selected suppliers and part count
- Minimize the number of active components
- Constant refreshing
• Use hardened parts in critical circuits of a system
• Use hardened nonvolatile memory, energy storage backup or ROM for storing critical data.

Shielding provides significant protection for energetic electrons in the Earth's radiation belts. However, shielding will not provide complete protection to the energetic galactic cosmic particles or protons from a solar flare or from the South Atlantic Anomaly region (SAA). If COTS parts sensitive to single-event upset are selected (such as a DRAM, SRAM, or microprocessor), software or hardware error detection and correction (EDAC) must be implemented. EDAC is necessary to constantly refresh data stored in DRAMs or SRAMs. The refresh cycle should cover the highest upset rate anticipated from the largest solar flare events. For a microprocessor, a watchdog timer that monitors the processor's health at specific time intervals is needed. If the microprocessor were to upset and not respond properly, the watchdog timer may initiate power circuitry, switch the system to a redundant unit or refresh the memory registers. Voting logic or triple redundant logic designs are also methods of mitigating soft error upsets. Low pass filters can be used for transient single-event upsets from linear devices [14]. For high speed electro-optical devices, voting logic or read verifications are possible solutions.

In the absence of guaranteed hardness and traceability, protection is important against catastrophic failure originating from single event burnout and latchup. Careful radiation lot sample testing of flight hardware may be required to assure that latchup does not exist [17,20]. Current limiting and circumvention of power may be required to provide extra protection. Other solutions include selecting a latchup immune technology, such as SOI (silicon-on-insulator), GaAs, or thin (< 2-μm) epitaxial CMOS silicon. In the case of spacecraft discharges, terminal protection devices are placed at the inputs, outputs, and supply lines of circuit boards. Conformal coatings over the boards add reliability and added charge protection.

Redundancy is a common design practice in satellite applications to increase reliability and survivability of a system. By detecting the malfunctioning of a component or a package, the questionable elements are switched out of the operational portion of the system and replaced with a redundant component. This, of course, assumes that the redundant component hasn't also degraded in the radiation field. This is mainly a concern for total-dose charging which may be significant even if all the pins of a device are shorted [27,31]. Reliability of the detector and the switching components are critical to this type of approach. The replacement mechanism is very important for the proper functioning of the system; an electrical or possibly a mechanical replacement may be used. Also, multiple paths for signals may be used in this type of radiation hardening. The difficulty with multiple paths lies in determining the correct output to use for the system. Voting logic has been successful in the past and data flags of various types have been used. Care is required not to degrade the performance of the unirradiated system. Given the weight and power constraints of space applications, elimination of potential failures at the lowest level (i.e., microcircuit reliability and hardness assurance) is often more cost effective than high-level redundancy or sparing schemes. In addition, redundancy carries with it a power penalty which may be unacceptable to the system engineer.

System designers must account for the degradation of DC and AC parameters, as well as gain degradation in linear devices and in the CTR (charge transfer ratio) of electro-optical devices. This derating is complicated by variability in the radiation hardness of COTS. To mitigate this problem (for example, in total dose hardness), extra design margins should be considered. For some applications, shielding is an excellent way to provide added margin and can be implemented at the component or box level, but the added weight is always unwelcome.

Hardness assurance procedures, such as lot sample testing, will be required to qualify parts that will be used as flight hardware. If one were to reduce the number of suppliers to a few and to utilize common parts among several programs, one can reduce the cost of testing and screening [32]. Minimization of the parts count is always good engineering, including the corollary of minimizing the number of suppliers. Both reductions in part sources and counts will simplify procurement and the monitoring of part suppliers, which are an obvious cost savings for a radiation-hardened system. Based on radiation test results presented in Section III, we suggest it is possible to screen COTS parts to meet mission requirements, but the cost may be significant for applications with serious radiation requirements. It has been suggested [33] that a commercial part needs to be 30 times less expensive than its RH counterpart to overcome “upscreening” costs, but this is very application dependent. In addition, it is worth noting that some semiconductor producers are adamantly opposed to upscreening because they insist it compromises the reliability of the end product. The company will only assume the liability for replacement of a faulty component, not for a system failure, and then only if the component was used as specified. The advent of upscreened COTS clearly undercuts our traditional comfort level derived from using parts deemed to be reliable for the intended environment.

IV. LIFE-CYCLE COSTS

From both a radiation and reliability perspective, the issue of life-cycle costs is an important one. Clearly, COTS components are initially less expensive than RH-COTS. However, common sense tells us that a component that leads to premature system failure is expensive by any metric. For many radiation applications like space, a component cannot be replaced like it can in an automobile or tank. Traditional approaches like Fail and Replace are not valid concepts for a
satellite on orbit or a tank on a nuclear battlefield. For many space and military systems, the issue of life-cycle costs revolves around what is acceptable risk. Making a decision between having more knowledge and working with limited knowledge is what the parts engineer must evaluate in a high-risk environment. The bottom line is that using COTS in space applications without risk requires having extensive knowledge and experience with a part, and that costs money. For the International Space Station and the NASA Space Shuttle, the electronic components represent less than 1 percent of total costs. For missiles and spacecraft, that share rises to 10 percent, but the integrated circuits represent 30 to 40 percent of the systems capability as measured by such functions as sensors, navigation, and information processing. At the far end of the spectrum are the U.S. Army hand-held tactical radios where you can’t afford to pay $500 for a $5 part. One simply needs to perform a life-cycle trade study for hardness assurance that weighs acceptable risk versus cost [32].

Logic Families (AC, ACT, ACTQ) 6 years
Memory Families (SRAMs, DRAMs, E2s) 9 months
Microprocessors (286, 386, 486, Pentium) 2 years
Digital Signal Processors 3 years
PLD 1 year
Linear Interfaces 8 years
Gate Arrays 2 years

Figure 6. Average introduction rate for new generations of commercial integrated circuits. Low-voltage digital technologies are projected to last an average of 12 to 15 years. This includes all 3V, 2V and 1V or less devices [34].

Another key issue associated with life-cycle costs is part obsolescence. Since COTS suppliers constantly introduce new products into the marketplace, devices chosen for a system become obsolete in a very short time. This may force certain decision about the up-front procurement of parts. Figure 6 shows the length of time typical integrated circuits are introduced into the commercial market before another advanced product is introduced [34]. Gate arrays for example, from Xilinx and Actel are introduced for about two years before another product family is introduced. Since military systems often take longer to develop, they generally are required to last between 15 to 30 years. Considering the component life cycle, Fig. 7 shows the number of upgrades that are projected if COTS parts are used in military systems. For a program beginning in 1998, it would require possibly seven upgrades to maintain a 30-year system.

Several alternatives that address obsolescence are: (1) Consider a lifetime buy. This is perhaps the least expensive option. If funding and defense procurement were not issues, a customer would simply order enough product to support the lifetime requirement of a program. (2) Develop a modular system design such that insertions of redesigned packages or boards can be cost effective. Use “open” architectures that provide for vendor and technology independence, as well as backward compatibility with enhanced performance. (3) Procure obsolete parts from third-party aftermarket manufacturers. (4) Procure SMD products from QML suppliers. Hopefully, the resulting demands for these parts will enhance their lifetimes. (5) Team with semiconductor suppliers to select components that have anticipated long lifetimes. (6) Identify critical components as part of the customer’s high priority list of procurements when funds are available. (7) Obtain fabrication support from a government national laboratory or contingency fabrication facility.

### 30 year military system lifecycle

<table>
<thead>
<tr>
<th>Year</th>
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<th>1998</th>
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<tbody>
<tr>
<td>In</td>
<td>15 years</td>
<td>12 years</td>
</tr>
<tr>
<td>Devices</td>
<td>15 years</td>
<td>12 years</td>
</tr>
<tr>
<td>Military</td>
<td>30 years</td>
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</tbody>
</table>

Figure 7. Projected number of modernizations based on component life cycles between military versus commercial devices [34].

**CONCLUSIONS**

The use of COTS parts in radiation environments presents a significant challenge to system designers. Since most COTS parts are susceptible to radiation damage, the designer must make wise choices to carefully manage risk and ensure mission success. "COTS" means that the product is Commercially available Off The Shelf, i.e., you are buying what the supplier offers as their standard product, which can found in supplier databooks or SMDs. We define product that is not commercially available in supplier databooks as “Custom.” From the designer’s perspective, the important and distinguishing feature of radiation-hardened technology is that radiation hardness is qualified and guaranteed by the manufacturer, as opposed to the user.

This paper evaluates several of the factors and tradeoffs affecting the successful application of COTS parts including hardness assurance issues arising from variability and date codes. Given the weight and power constraints of space applications, elimination of potential failures at the lowest level (i.e., microcircuit reliability and hardness assurance) is often more cost effective than high-level redundancy or sparing schemes. In some cases, the designer may be able to “upscrean” parts (perhaps for dose-rate) or employ shielding (for total-ionizing dose) or use system hardening techniques like EDAC and redundancy. COTS parts must be considered high risk in radiation applications until proven or shown otherwise. This is a sobering thought, since with the increasing functionality built into a single microcircuit, there is an increased risk of massive mission failure due to the loss of a
We owe a major debt of gratitude to Harvey Eisen, who helped us take our first steps toward defining a useable and working definition of COTS. We thank Dan Fleetwood, Paul Dodd, Rich Flores, and Dave Beutler for many stimulating discussions.

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REFERENCES


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