LS-159
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September 23, 1990

PULSED POWER SUPPLY FOR PAR INJECTION/EXTRACTION SEPTUM MAGNET

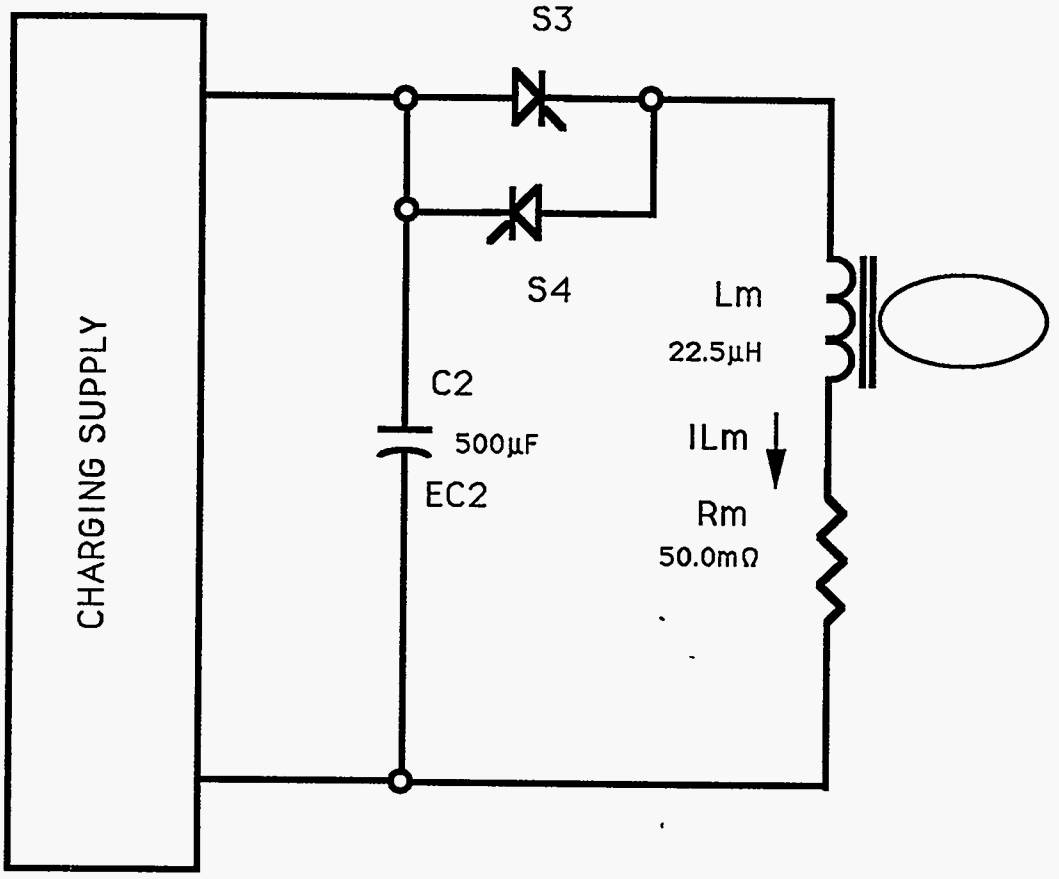
ABSTRACT

A 22.5 μH, 22.5 mΩ transformer septum magnet must be pulsed at a 60 Hz rate to inject beam from a 450 MeV positron linac into a positron accumulator ring (PAR) and to extract beam from it. Of the 60 pulses per second the first 24 are used for injection and the 30^{th} for extraction. The 25^{th} through the 29^{th} are not used. This pattern is repeated continuously. A design study was performed of the power supply proposed in the APS Title I design. This supply produces a pulse that is approximately a half-sine-wave with a base width of approximately 1/3 ms; its peak current is adjustable from 3.5kA to 4.7kA and is repeatable within ±0.05%. The septum steel is reset by a half-sine pulse of reverse polarity a few milliseconds after the forward current pulse. No beam is present during reset. The use of the transformer design minimizes the cost of the capacitors used for energy storage.

INTRODUCTION

During the injection of the 450 MeV positron beam from the linac into PAR and extraction from PAR, the septum magnet must be pulsed. The combined rise and fall time of the pulse should be ≤ 1/3 ms and the flattop time >1 μs. These requirements can be met with a capacitor discharge circuit that is resonant with the septum magnet at a frequency of approximately 1500 Hz. The peak current should be 4018 A in the transformer primary and 12054 A in the secondary. These requirements can be met with a half sine-wave pulse. This is accomplished by discharging the energy stored in capacitor bank (C_2) into the magnet as illustrated by Fig. 1. On triggering the forward thyristor S_3, the energy stored in C_2 between pulses is discharged into the magnet circuit. S_3 turns off at the end of the first half cycle of the damped oscillation. C_2 is then left

DISCLAIMER



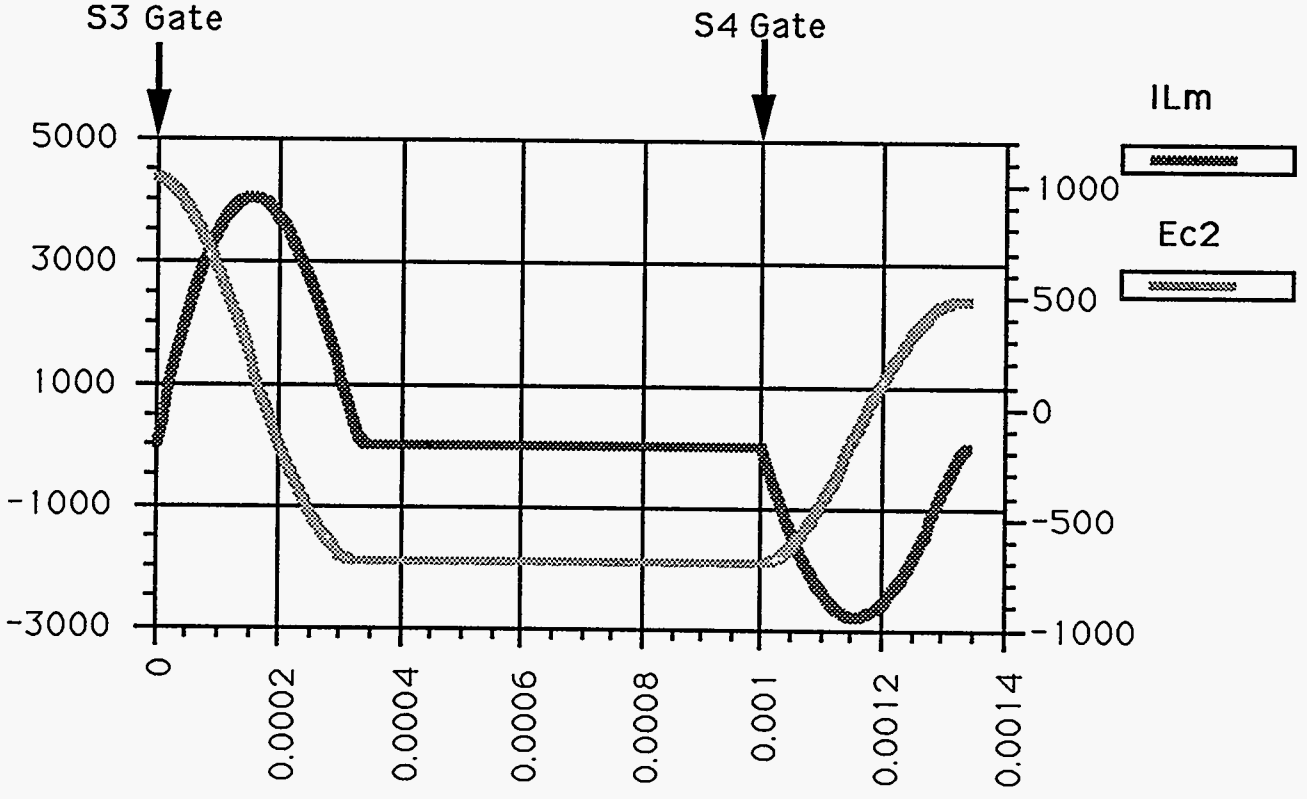


Fig. 1

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with a smaller charge of opposite polarity until the reverse thyristor S_4 is triggered and the second half cycle takes place with current flowing in the opposite direction. The difference between the original and the final charge is furnished by the charging supply between septum pulses.

Switching Circuits

Circuit Equations

When the capacitor C_2 of Fig. 1 is discharged into the load, an oscillatory current will result provided the total resistance in the circuit is sufficiently low.

The resonant frequency of the circuit is:

$$fr = \beta/2\pi \qquad [s^{-1}] \qquad (1)$$

where $\beta = ((1/L_m C_2)-(R_m^2/4L_m^2))^{0.5}$ $[s^{-1}]$

C_2 = capacitor bank [F]
L_m = total circuit inductance [H]
R_m = total circuit resistance [Ω]

The current at any time is:

$$i = (E/\beta L_m)\, e^{-\alpha t} \sin \beta t \qquad [A] \qquad (2)$$

where t = time after discharge starts [s]

$$\alpha = R_m/2\, L_m \qquad [s^{-1}]$$

The time where the current reaches its first peak is:

$$tp = 1/\beta \tan^{-1} \beta/\alpha \qquad [s] \qquad (3)$$

The first current peak does not occur at precisely the first quarter period of the discharge cycle, but at a point in time before. This is shown by the circuit simulation graphed in Fig. 2. The term $\tan^{-1}\beta/\alpha$

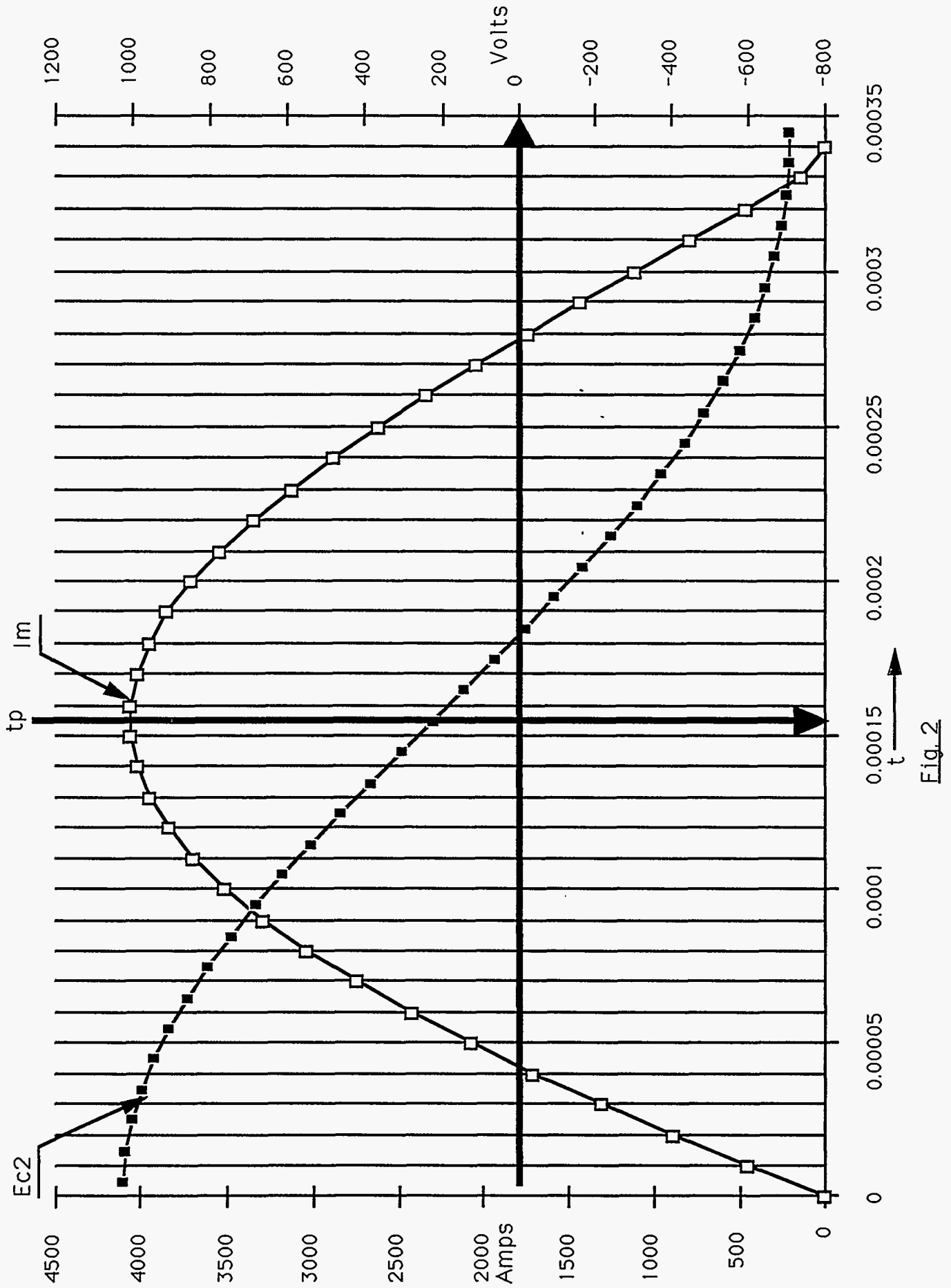

Ec2
Im
tp
Amps
Volts
t
4500
4000
3500
3000
2500
2000
1500
1000
500
0
1200
1000
800
600
400
200
0
-200
-400
-600
-800
0
0.00005
0.0001
0.00015
0.0002
0.00025
0.0003
0.00035

Fig. 2

describes the phase angle at which the peak current occurs.

In this application, R_m is made appreciably less than the value for critical damping. With $1/L_m C_2 > R_m^2 / 4L_m^2$ we can write $\beta \approx 1/(L_m C_2)^{0.5}$ and the above equations can be simplified to:

$$fr \approx 1/(2\pi(L_m C_2)^{0.5}) \qquad [s^{-1}] \qquad (1')$$

$$i \approx E_{c2} (C_2/L_m)^{0.5} e^{-\alpha t} \sin t/(L_m C_2)^{0.5} \qquad [A] \qquad (2')$$

The peak current is then

$$I_p \approx E_{c2}(C_2/L_m)^{0.5} e^{-((\pi R_m/4)(C_2/L_m)^{0.5})} [A] \qquad (2'')$$

and the voltage on the first reversal becomes

$$E_{c2} \approx - E_{c2} e^{-((\pi R_m/2)(C_2/L_m)^{0.5})} \qquad [V] \qquad (4)$$

Critical damping occurs at a resistance:

$$R_m = 2(L_m/C_2)^{0.5} \qquad [\Omega] \qquad (5)$$

Controlled Charging-Choke Circuit

Fig. 3 shows the controlled charging-choke circuit and the capacitor discharge circuit of Fig. 1 combined. The discharge capacitor C_2 is charged and recharged to make up the circuit losses incurred pulsing the magnet. These losses are made up from the unregulated dc power supply comprised of a circuit breaker, contactor, main transformer, diode rectifier assembly and low pass filter. The controlled charging circuit is comprised of L_2, C_2, S_1 and S_2. Gating on of S_1 is used to start the charging of C_2 from the dc power supply. At time t_0 the supply voltage E begins to drive an essentially sinusoidal current through the charging circuit.

$$E = iR_2 + L_2(di/dt) + (1/C_2) \int_0^{t_1} i_{c2}\, dt \qquad (8)$$

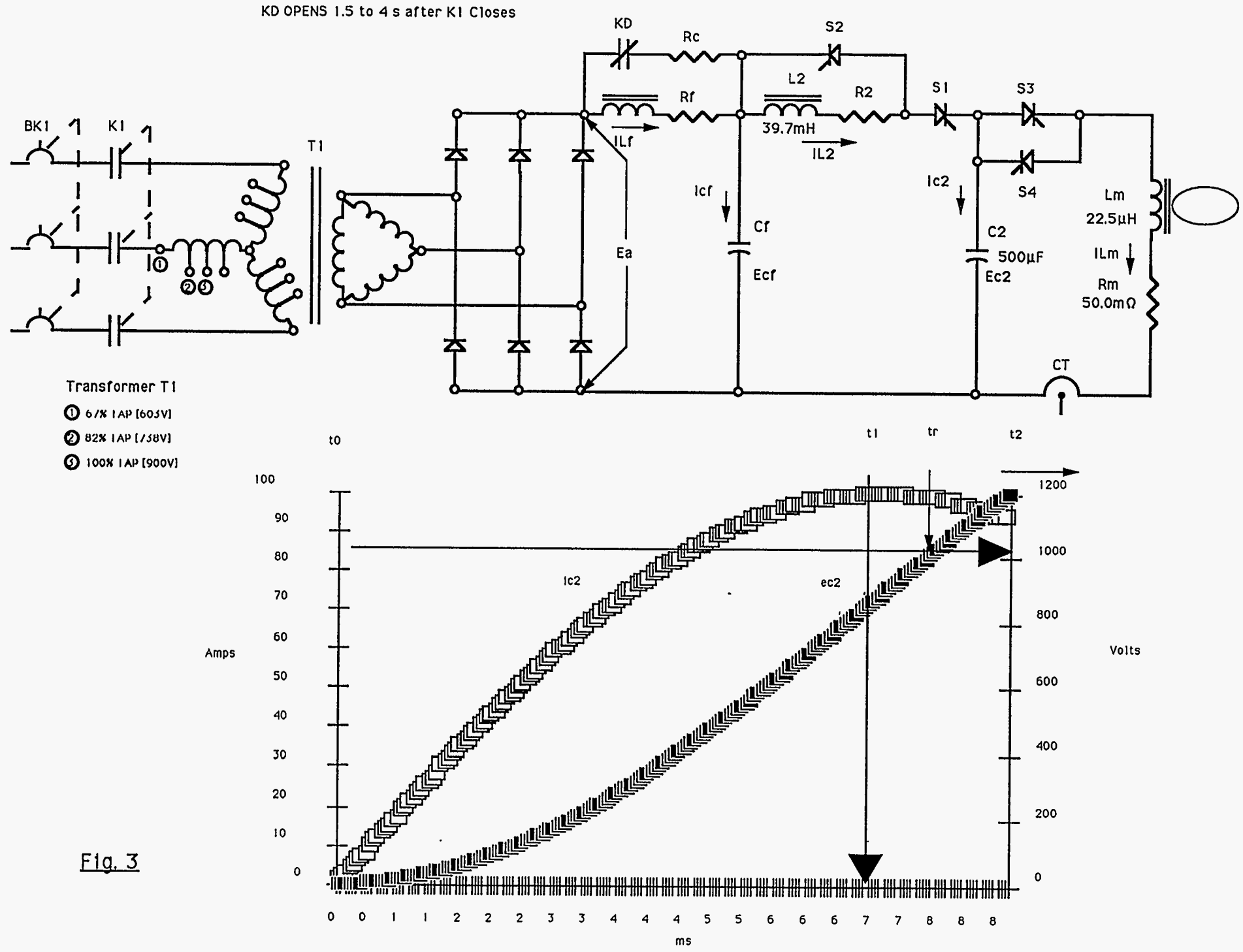

KD OPENS 1.5 to 4 s after K1 Closes
KD
Rc
S2
L2
Rf
R2
S1
S3
BK1
K1
T1
39.7mH
ILf
IL2
Ic2
S4
Icf
Cf
Ea
Ecf
C2
500µF
Ec2
Lm
22.5µH
ILm
Rm
50.0mΩ
CT
Transformer T1
① 67% IAP [603V]
② 82% IAP [738V]
⑤ 100% IAP [900V]
t0
t1
tr
t2
Ic2
ec2
Amps
Volts
ms
100
90
80
70
60
50
40
30
20
10
0
1200
1000
800
600
400
200
0
0 0 1 1 2 2 2 3 3 4 4 4 5 5 6 6 6 7 7 8 8 8

Fig. 3

At time t_1 the current is at its peak and

$$L_2 \, di/dt = 0, \tag{9}$$

$$E = iR_2 + (1/C_2) \, {}_0\int^{t_1} i_{C2} \, dt. \tag{10}$$

Between t_1 and t_2 the decaying charging current generates a voltage L_2 (di/dt) which aids the supply voltage to charge the capacitor C_2 to a voltage larger than E. In the case where $R \Rightarrow 0$, this voltage will be, at time t_2,

$$e_{C2} = E + L \, (di/dt) = 2E.$$

By providing a thyristor across the charging choke as shown in Fig. 3 the charging cycle can be terminated at any instant between times t_1 and t_2. A fraction of the capacitor voltage e_{C2} is compared with a reference voltage. At time t_r when the capacitor voltage is $\geq$ the supply voltage , a pulse can be generated which turns on S_2. With S_2 conducting, the driving voltage L_2 (di/dt) is removed from the circuit and the capacitor voltage e_{C2} is larger than the power supply voltage E, thyristor S_1 is back-biased and the charging current i_{C2} stops. The current i_{L2} flowing in choke L_2 at time t_r will decay with a time constant L_2/R, where R is the resistance of the choke and thyristor, S_2, circuit. Thyristor S_2 remains on until the time S_1 is gated on starting the charge cycle again or the choke current decays to 0. The current i_{L2} flowing in the choke when S_2 is turned off will aid in charging capacitor C_2 (the energy $0.5 \, L_2 \, i_{L2}^2$ is returned to the circuit). This makes the circuit very efficient.

Warning

It should be noted that the Q of the discharge circuit in Fig. 1 should be <5 for this charging circuit to operate properly. As the Q increases the current flowing in the choke L_2 will decrease. This in turn decreases the operating range of the charging circuit. The Q of the circuit was decreased from 9.4 to 4.2. This allowed for

operation with a normal line voltagefrom 3.5kA to 4.7kA or operation with the normal line fluctuation of ± 5% at 4kA. The circuit was simulated using the logic diagram in Fig. 4, the results are shown in Fig. 5, 6, 7 and 8. Fig. 8 shows the change in time for the first six charge cycles of capacitor C2. It should be noted the first charge cycle is the longest the second is the shortest and the sixth is approaching steady-state.

Pulsing the Magnet Without Resetting the Core

Heat losses in the magnet can be cut approximately 1/3 by not gating S_4 but the magnet core would not be reset. This mode of operation would allow the dc power supply and filter to operate at a lower voltage. Also the circuit Q could be increased increasing the operating efficiency. Fig. 9 shows the change in time for the first nine charge cycles of capacitor C2. It should be noted the first charge cycle is the longest, the second is next longest and the ninth is approaching steady-state.

Control

Control is accomplished with 2 external pulses and a pulse-train, as shown in Fig. 10. One pulse starts the charge cycle for C2 by gating S1 and the second starts the magnet current pulse by gating S2. The pulse train counts the DAC up or down setting the reference voltage that is compared with the capacitor voltage Ec2. If Ec2 is ≥ the reference voltage and Ec2 > Ecf the charge cycle is terminated by gating S2. The magnet reset current pulse is started by gating S4 after a fix delay from the start of the magnet current pulse.

Monitoring and Interlocks

Computer monitoring includes the power supply interlocks, magnet interlocks and two 14 bit analog-to-digital converters (ADC) as listed in attachment 1. One ADC reads the peak capacitor voltage and the other reads the peak magnet current.

In order to operate the power supply the interlocks listed in attachment 1 must be made-up. If they are not made-up or open during operation the contactor, K1, shown in Fig. 3 will open and the gating of the thyristors will be inhibited.

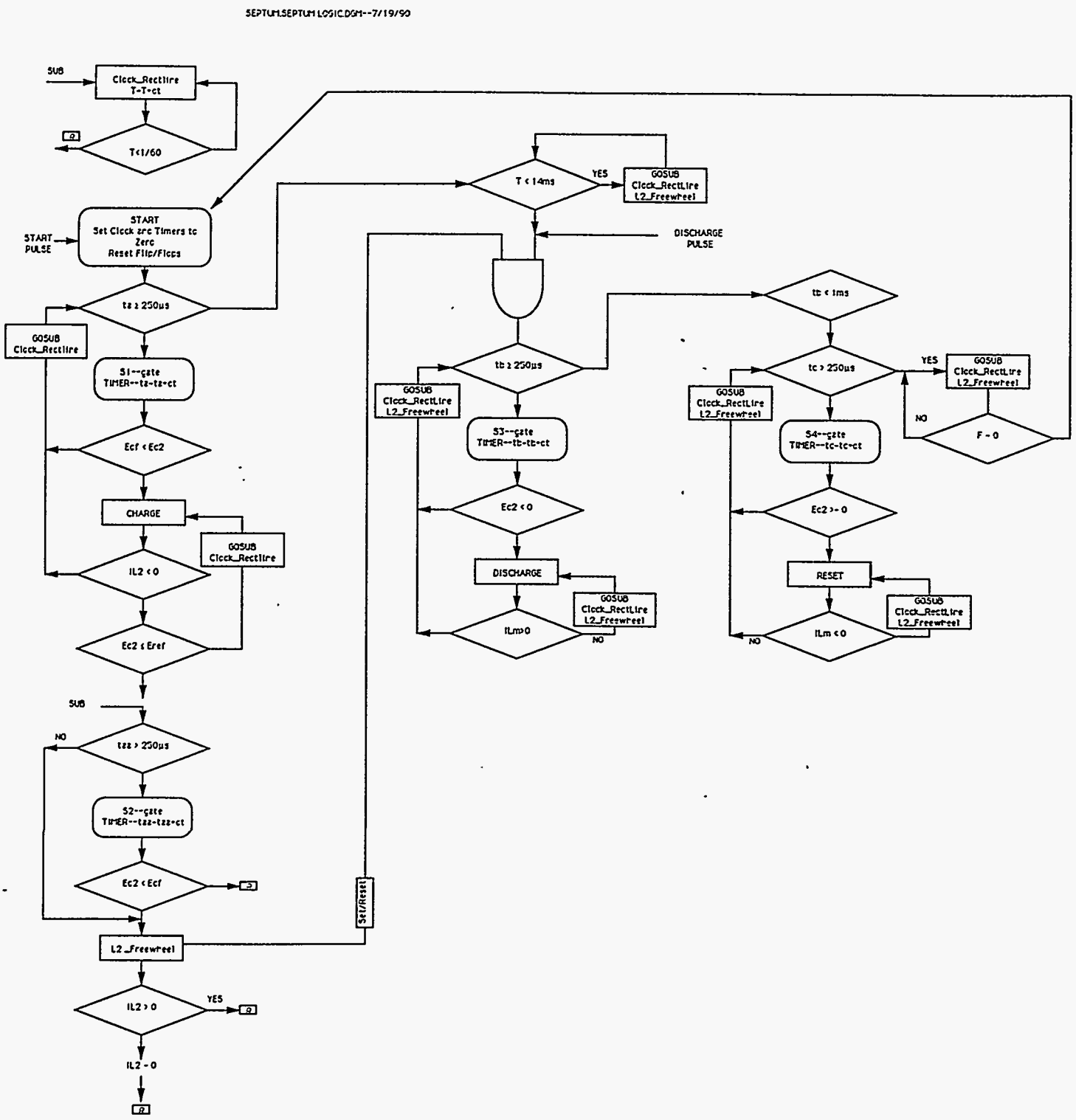
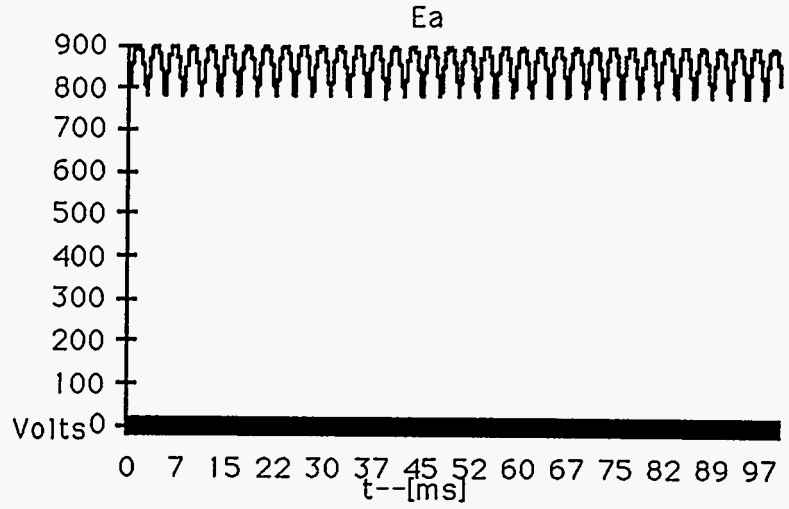
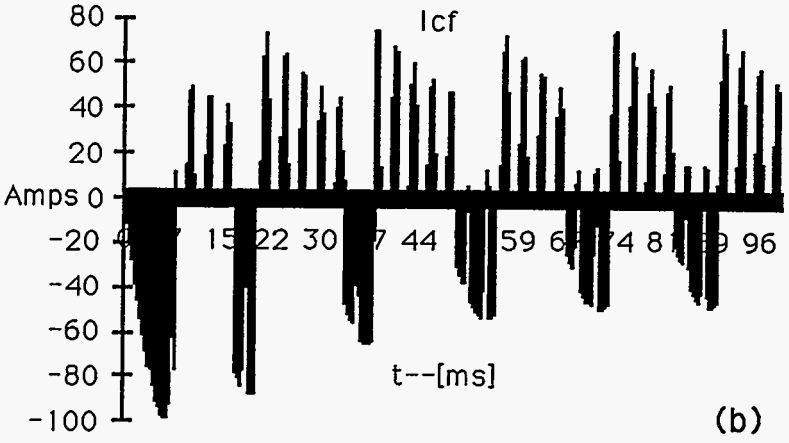

SEPTUM:SEPTUM LOGIC.DGM--7/19/90
SUB
Clock_Rectlire
T=T+ct
T<1/60
START
Set Clock and Timers to Zero
Reset Flip/Flops
START PULSE
ta ≥ 250µs
GOSUB Clock_Rectlire
S1--gate TIMER--ta-ta+ct
Ecf < Ec2
CHARGE
GOSUB Clock_Rectlire
IL2 < 0
Ec2 ≤ Eref
SUB
NO
tzz > 250µs
S2--gate TIMER--tzz-tzz+ct
Ec2 < Ecf
L2_Freewheel
IL2 > 0
YES
IL2 = 0
Set/Reset
T < 14ms
YES
GOSUB Clock_Rectlire L2_Freewheel
DISCHARGE PULSE
tb ≥ 250µs
GOSUB Clock_Rectlire L2_Freewheel
S3--gate TIMER--tb-tb+ct
Ec2 < 0
DISCHARGE
GOSUB Clock_Rectlire L2_Freewheel
ILm>0
NO
tb < 1ms
tc > 250µs
GOSUB Clock_Rectlire L2_Freewheel
S4--gate TIMER--tc-tc+ct
Ec2 > 0
RESET
GOSUB Clock_Rectlire L2_Freewheel
ILm < 0
NO
YES
GOSUB Clock_Rectlire L2_Freewheel
NO
F = 0

Fig. 4



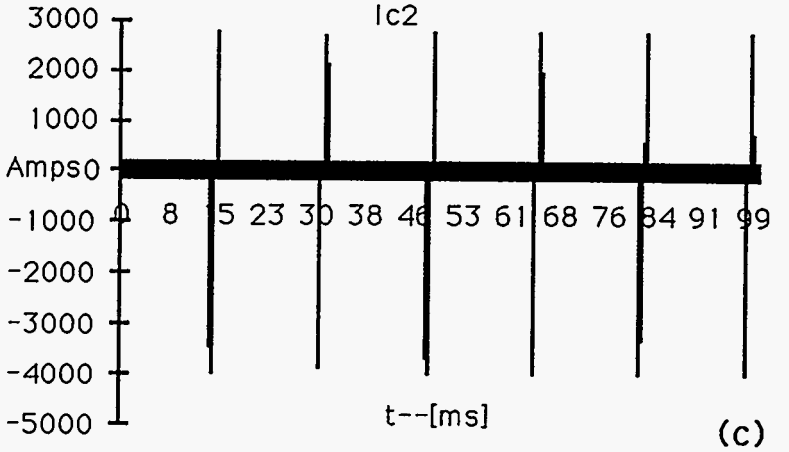
Ea (rms) = 860V

(a)



Tap	Icf +pk	Icf -pk	Icf rms
Max--100%	80	-100	33.5
Mon--100%	76	-100	35.9
Min--100%	68	-130	42.4
Max--82%	62	-82	27.4
Min--82%	56	-101	34.2
Max--67%	51	-68	22.5
Min--67%	46	-84	28.1

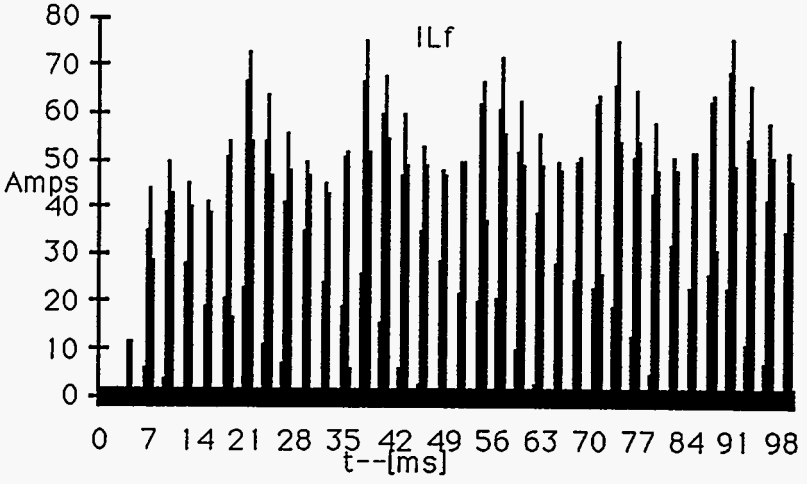
(b)



Tap	Ic2 +pk	Ic2 -pk	Ic2 rms
Max--100%	3275	-4761	564.2
Mon--100%	2793	-4061	481.7
Min--100%	2466	-3586	426.3
Max--82%	2591	-3767	446.5
Min--82%	2030	-2952	350.7
Max--67%	2139	-3111	368.7
Min--67%	1661	-2416	287.0

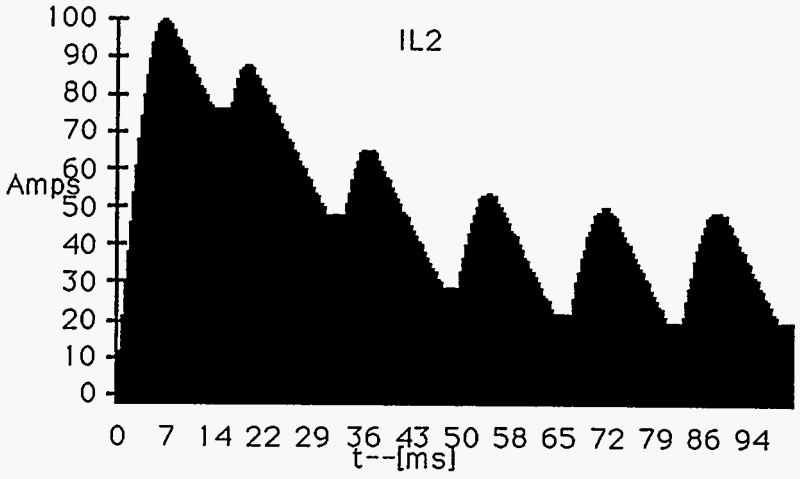
(c)

Fig. 5



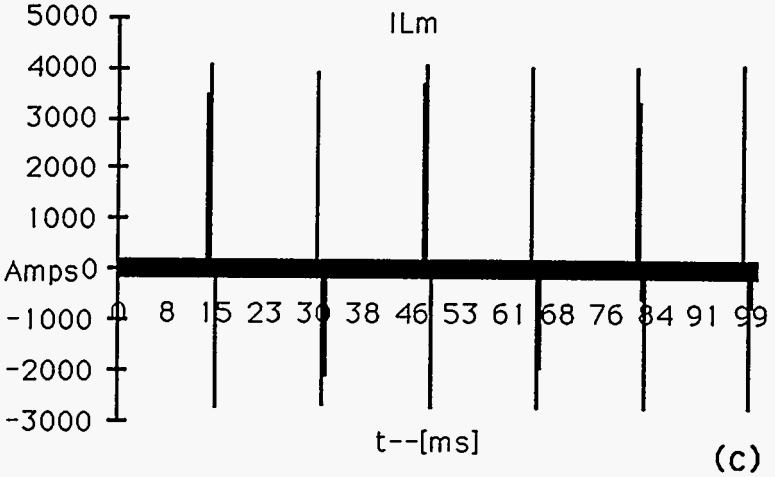
Tap	ILf +pk	ILf -pk	ILf rms
Max--100%	80	0	29.9
Mon--100%	76	0	26.2
Min--100%	68	0	23.5
Max--82%	65	0	23.7
Min--82%	56	0	19.3
Max--67%	53	0	19.5
Min--67%	46	0	15.7

(a)



Tap	IL2 +pk	IL2 -pk	IL2 rms
Max--100%	100	-1	33.5
Mon--100%	100	1	48.7
Min--100%	132	1	114.3
Max--82%	82	-1	28.9
Min--82%	102	0	90.4
Max--67%	67	-1	23.3
Min--67%	84	0	74.3

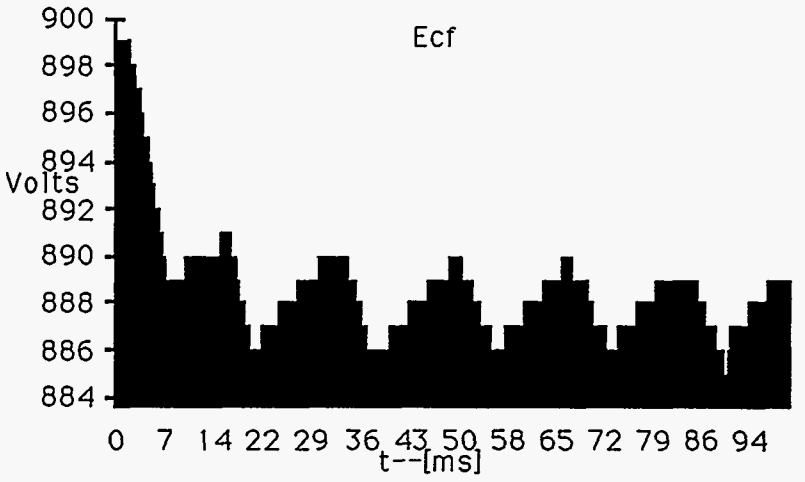
(b)



Tap	ILm +pk	ILm -pk	ILm rms
Max--100%	4760	-3276	563.4
Mon--100%	4060	-2794	480.7
Min--100%	3585	-2467	424.2
Max--82%	3766	-2592	445.8
Min--82%	2951	-2031	349.1
Max--67%	3110	-2140	368.2
Min--67%	2415	-1662	285.6

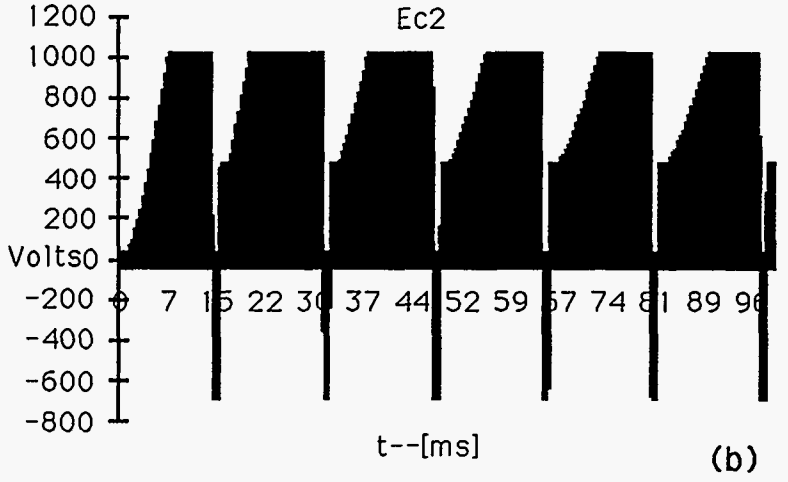
(c)

Fig. 6



(a)

Tap	Ecf +pk	Ecf -pk	Ecf rms
Max--100%	899	885	887.1
Mon--100%	899	885	888.2
Min--100%	899	886	888.8
Max--82%	737	726	727.6
Min--82%	737	726	728.9
Max--67%	604	595	596.4
Min--67%	604	595	597.4



(b)

Tap	Ec2 +pk	Ec2 -pk	Ec2 rms
Max--100%	1200	-823	892.8
Mon--100%	1025	-702	859.7
Min--100%	906	-619	810.2
Max--82%	950	-651	725.2
Min--82%	745	-509	666.1
Max--67%	785	-537	595.6
Min--67%	610	-417	545.4

Fig. 7

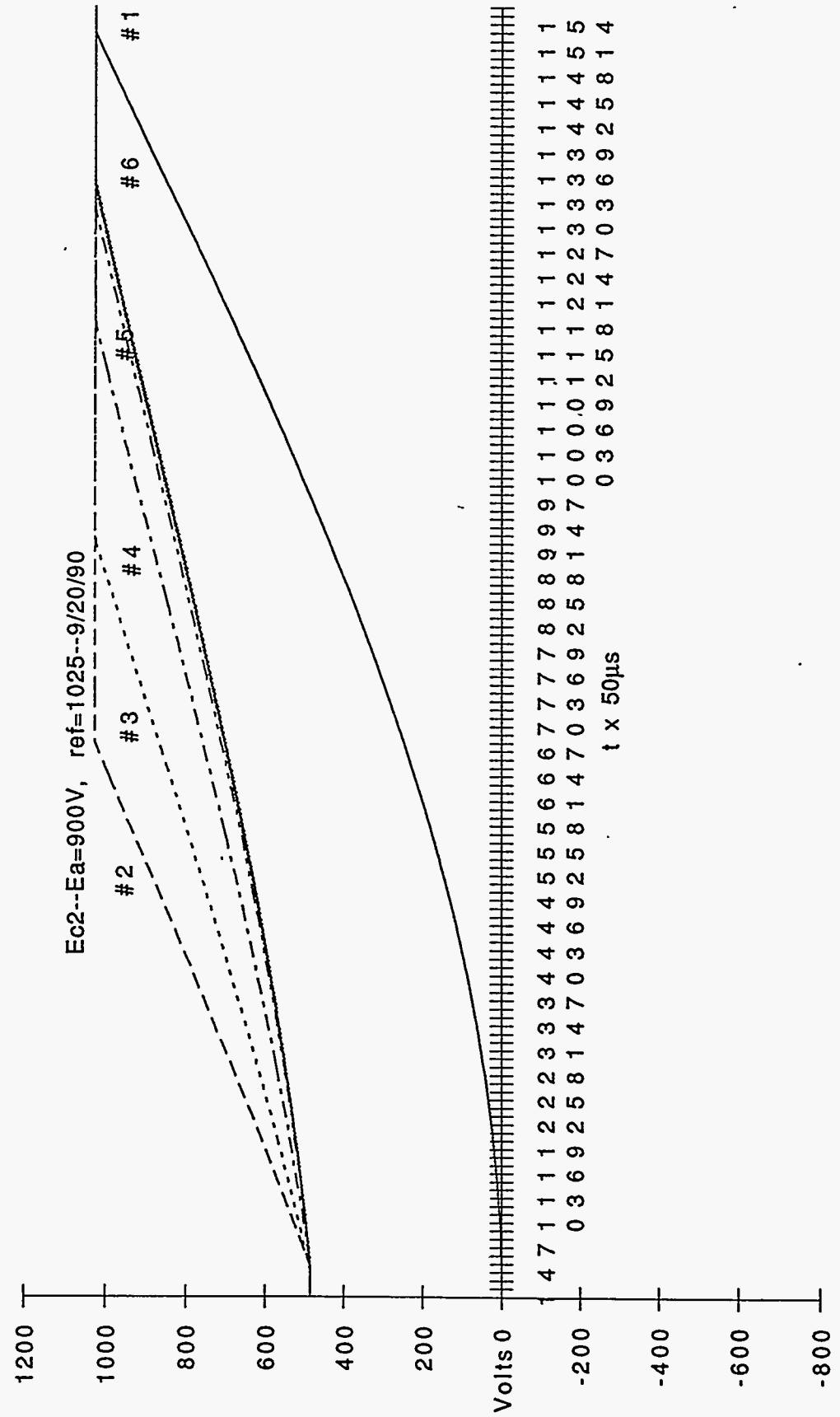

Ec2
Ec2--Ea=900V, ref=1025--9/20/90
#1
#2
#3
#4
#5
#6
1200
1000
800
600
400
200
Volts 0
-200
-400
-600
-800
t x 50µs

Fig.8

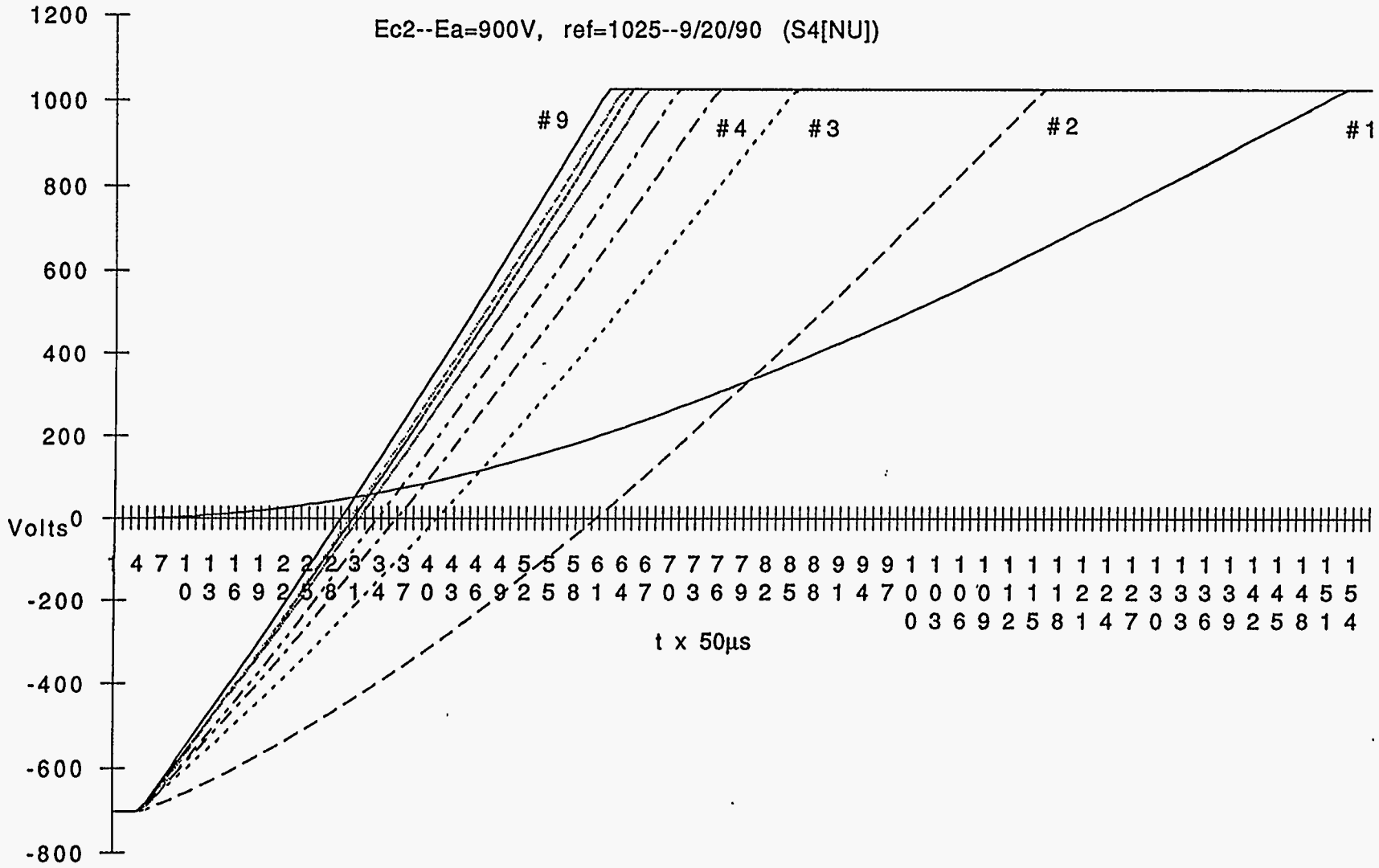

Ec2--Ea=900V, ref=1025--9/20/90 (S4[NU])
1200
1000
800
600
400
200
Volts 0
-200
-400
-600
-800
#9
#4
#3
#2
#1
t x 50µs

Fig. 9

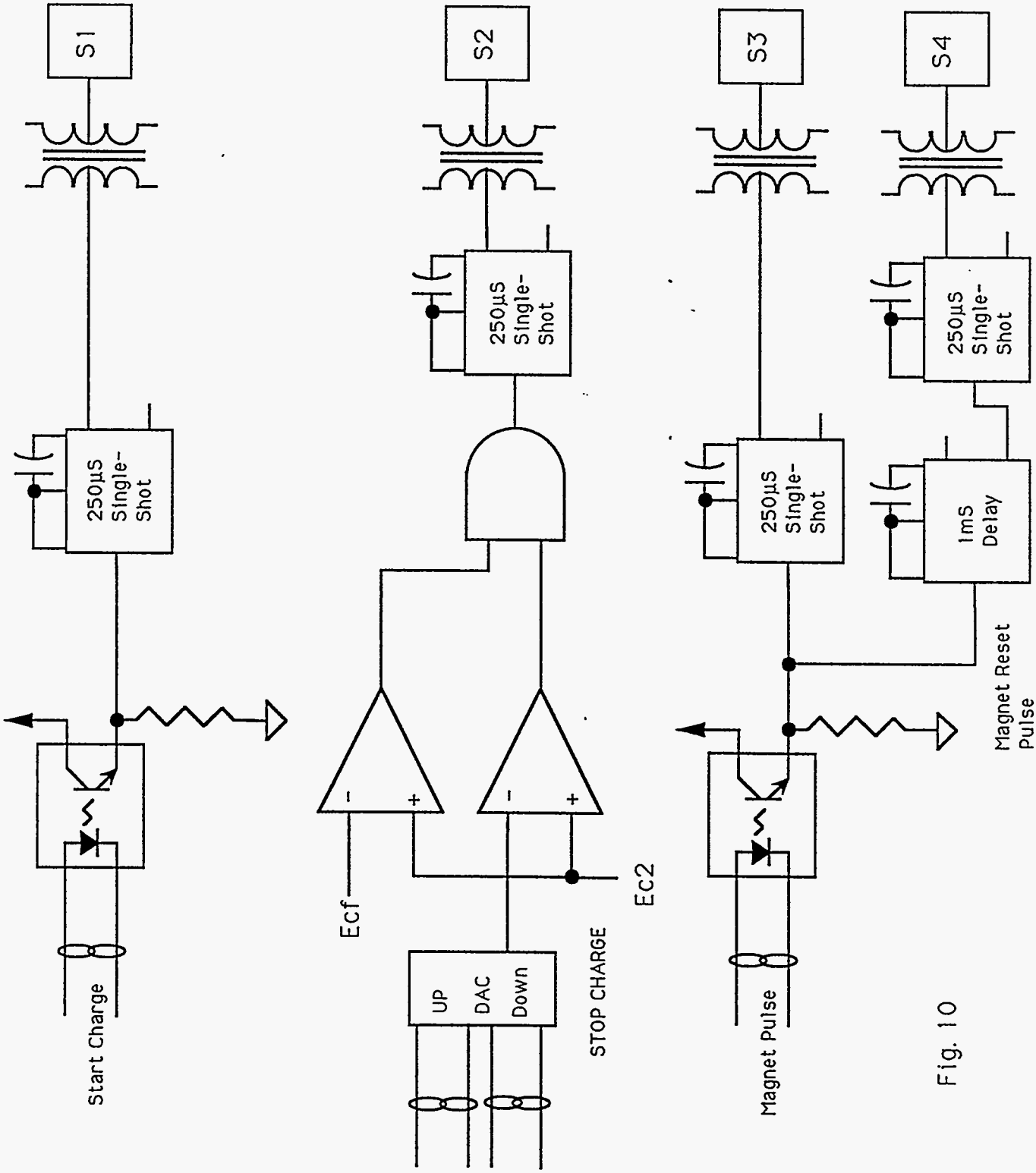

S1
S2
S3
S4
250µS Single-Shot
250µS Single-Shot
250µS Single-Shot
250µS Single-Shot
1mS Delay
Start Charge
Magnet Pulse
Magnet Reset Pulse
Ecf
Ec2
STOP CHARGE
UP
DAC
Down

Fig. 10

ATTACHMENT 1

CONTROL INTERLOCK AND MONITORING OF PAR's AC SEPTUM POWER SUPPLY

DGM WBS 1.2.5.2.6 6/7/90--REV. 10/25/90

COMPUTERR CONTROL SIGNALS:

1. "RESET"--OPTICALLY COUPLED PULSE

2. "ON/OFF"--OPTICALLY COUPLED STATE--(HIGH--ON>>>>LOW--OFF)

3. "CHARGE"--OPTICALLY COUPLED PULSE

4. "DISCHARGE"--OPTICALLY COUPLED PULSE

5. "DAC--COUNT-UP"-- OPTICALLY COUPLED PULSE

COMPUTER MONITORING SIGNALS:

1. "ADC--CAPACITOR-VOLTAGE"--OPTICALLY COUPLED

2. "ADC--PULSE MAGNET CURRENT--PEAK"--OPTICALLY COUPLED

3. "SYSTEM NORMAL/ABNORMAL"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--NORMAL)

    3.1 "WATER FLOW"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

    3.2 'WINDOW--PEAK MAGNET CURRENT ≤ DAC REFERENCE - FIXED"--(HIGH--NORMAL>>>>LOW--ABNORMAL)

    3.3 "WINDOW--PEAK MAGNET CURRENT ≥ DAC REFERENCE + FIXED"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

    3.4 "CAPACITOR C2 OVERVOLTAGE"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

    3.5 "AIR OVERTEMPERATURE"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

    3.6 "AC PHASE UNBALANCE"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

3.7 "DOOR SWITCHES"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

3.8 "EMERGENCY TRIP SWITCH IS MADE UP" (IN THE TUNNEL)--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

3.9 "MAGNET INTERLOCKS COMPLETE"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

3.9.1 "WATER FLOW--SUPPLY SIDE"--OPTICALLY COUPLED STATE--(HIGH--NORMAL>>>>LOW--ABNORMAL)

3.9.2 "SUPPLY WATER PRESSURE"--ANALOG SIGNAL

3.9.3 "RETURRN WATER PRESSURE"--ANALOG SIGNAL

NOTES FOR ITEMS 3.9.1 THROUGH 3.9.4:

- COMPARE THE SUPPLY AND RETURN WATER FLOW IF NOT THE SAME TRIP THE DC POWER SUPPLY.

- COMPARE THE DIFFERENTIAL PRESSURE WITH FLOW, IF INCORRECT ALARM.