A MONOLITHIC CONSTANT-FRACTION DISCRIMINATOR USING DISTRIBUTED R-C DELAY-LINE SHAPING*

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A Monolithic, Constant-Fraction Discriminator Using Distributed R-C Delay-Line Shaping

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A monolithic, CMOS, constant-fraction discriminator (CFD) was fabricated in the Orbit Semiconductor, 1.2 μ , N-well process. This circuit uses an on-chip, distributed, R-C delay-line to realize the constant-fraction shaping. The delay-line is constructed from a narrow, 500- μ serpentine layer of polysilicon above a wide, grounded, second layer of polysilicon. This R-C delay-line generates about 1.1 ns of delay for 5 ns risetime signals with a slope degradation of only $\approx 15\%$ and an amplitude reduction of about 6.1%. The CFD also features an automatic walk adjustment. The entire circuit, including the delay line, has a 200 μ pitch and is 950 μ long. The walk for a 5 ns risetime signal was measured as ± 100 ps over the 100:1 dynamic range from -15 mV to -1.5 V. The CFD consumes 15 mW.

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There has been much recent interest in monolithic, CMOS CFDs. Binkley, Simpson and Rochelle [1] reported an early version of a CMOS CFD that used an external delay-line as a shaping element. Nowlin [2,3], Turko and Smith [4] and Binkley [5] have reported CFD shaping methods that can be integrated on a chip. Binkley [5] and Simpson et al. [6], have reported fully integrated, CMOS CFDs that use the lumped-element shaping methods referred to above. The topic of this paper is a fully integrated, CMOS CFD which uses an on-chip, distributed, R-C delay-line for the CFD shaping. This CFD is intended for use in the $\approx 20,000$ channel, lead-scintillator calorimeter of the PHENIX detector at the Relativistic Heavy Ion Collider (RHIC)

The R-C delay-line consists of a $4.8\text{-}\mu$ wide, serpentine strip of polysilicon above a grounded, polysilicon plate. The delay-line was analyzed using the lumped-element, U model function available in the HSPICE circuit simulator [7]. Figure 1 shows delay time Vs line length as calculated with HSPICE. Shown in figure 2 is slope degradation as a percentage of input slope for a 5 ns risetime signal. For the 5 ns risetime signals generated by the PMTs used in this application, a $500\text{-}\mu$ line length was chosen.

The zero-crossing discriminator is composed of cascaded stages of differential input--differential output amplifiers and is similar to those discussed by Binkley [5] and Simpson et al. [6]. The offset of this discriminator is canceled by a dc feedback loop, thus eliminating the need for a walk adjustment. The threshold setting of the arming discriminator is the only required user adjustment. A channel of the CFD is contained in a $200\text{ }\mu$ wide X $950\text{ }\mu$ long strip which allows compact arraying for multi-channel systems. One channel of this CFD consumes about 15 mW. Figure 3 shows the measured time walk for the CFD over the 100:1 dynamic range from -15 mV to -1.5 V for 5 ns risetime signal.

Figure 1
Delay vs Delay Line Length

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Figure 3 Walk Vs Amplitude of Input Signal

Figure 2 Slope Degradation Vs Delay Line Length