Temperature-Independent Switching Rates for a Random Telegraph Signal in a Silicon Metal-
Oxide-Semiconductor Field-Effect Transistor at Low Temperatures

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Abstract

We have observed discrete random telegraph signals (RTS's) in the drain voltages of three, nominally $1.25\ \mu\text{m} \times 1.25\ \mu\text{m}$, enhancement-mode *p* channel metal-oxide-semiconductor (MOS) transistors operated in strong inversion in their linear regimes with constant drain-current and gate-voltage bias, for temperatures ranging from 4.2 K to 300 K. The switching rates for all the RTS's observed above 30 K were thermally activated. The switching rate for the only RTS observed below 30 K was thermally activated above 30 K but temperature-independent below 10 K. To our knowledge, this cross-over from thermal activation to tunneling behavior has not been previously observed for RTS's in MOS transistors.

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Metal-oxide-semiconductor field-effect transistors (MOSFETs) often exhibit relatively large levels of low-frequency ($1/f$) noise [1,2]. Much evidence suggests that this noise is related to the capture and emission of charge carriers by localized defects at or near the Si/SiO₂ interface [2-6]. Under constant current bias, the drain voltages of small gate-area devices, especially at low temperatures, often show random switching between two discrete levels, apparently from the capture and emission of individual charge carriers [2,7-11]. Such random telegraph signals (RTS) [12], observed in small gate-area devices, superpose to give $1/f$ noise in larger devices [2,7]. Thus, information gained from the study of RTS's in MOSFETs is helpful in understanding the origins of $1/f$ noise in these devices.

There have been many observations of random telegraph signals in small MOSFETs [2,7-11]. In all cases, switching rates have been thermally activated, often with different activation energies for capture and emission. Ralls et al. [7] first recognized that these phenomena cannot be due to simple capture and emission of charge carriers from a single trap of fixed energy. The data suggest that the capture and/or emission is accompanied by lattice relaxation. Though thermally activated behavior has always been observed, one might expect to see temperature-independent tunneling behavior at sufficiently low temperatures [7,9]. While not observed in MOSFETs, cross-over from thermal activation to configurational tunneling has been observed for RTS's in tunnel junctions [13].

We have investigated the noise in three $\sim 1.25 \mu\text{m} \times 1.25 \mu\text{m}$, p channel, enhancement mode MOSFETs at temperatures down to 4.2 K. Devices have a gate-oxide thickness of 18 nm and were fabricated using radiation-hardened technology [6,14]. Temporal fluctuations δV_d in the source-drain voltage V_d were observed with devices operated in their linear regimes with fixed gate-source voltage V_g and drain current I_d . The measurement circuit is similar to that used to characterize $1/f$ noise in larger devices [5]. The measurement bandwidth was 0.03 Hz to 30 kHz. For these devices, the statistical properties of the RTS's were very reproducible, even after many days and temperature cycles.

For each device it was possible to find a range of temperatures and gate voltages for which the drain voltage was observed to randomly switch between two discrete levels, designated as V_{up} and V_{dn} , similar to RTS's reported by others [2,7-11]. We have characterized six RTS's for temperatures above 30 K where thermally activated switching rates are observed. The properties of five of these have been

described in a prior study [15]. Here we describe the single RTS that was observable for temperatures T both below and above 30K. The RTS was characterized by its voltage change, $\Delta V \equiv V_{up} - V_{dn}$, and the mean times, τ_{up} and τ_{dn} , spent in the "up" and "down" voltage states. We found the data to be consistent with the idea that the high resistance state V_{dn} was associated with the trapping of a single charge carrier. Thus, we identify the mean time in the high resistance state (τ_{dn} in state V_{dn}) as the emission time τ_e for the trap, i.e., the mean time a captured charge carrier spends in the trap before it is emitted. Similarly, we identify the mean time in the low resistance state (τ_{up} in state V_{up}) as the capture time τ_c .

Figure 1 shows a typical time trace of the drain-voltage fluctuation $\delta V_d(t) \equiv V_d(t) - \langle V_d \rangle$. This particular measurement was recorded for $T = 20$ K, $I_d = -5$ μ A, and $V_g = -3.00$ V. The measured (average) drain voltage was $\langle V_d \rangle = -30.14$ mV. As indicated in the figure, the RTS is more often in the "up" state than in the "down" state. For this RTS we find $\Delta V = (8 \pm 1)$ μ V, $\tau_e = (0.44 \pm 0.09)$ s, $\tau_c = (1.56 \pm 0.36)$ s, and the duty-cycle $\eta \equiv \tau_c / (\tau_c + \tau_e) = 0.78$.

To determine the temperature dependence of the switching rates the device was biased at constant drain current (-15 μ A), and gate voltage (-3.00 V) and measurements were performed at temperatures ranging from 4.2 K to 35 K. Figure 2 shows Arrhenius plots of τ_c and τ_e for the higher temperature measurements, i.e., for $T = 25$ K to 35 K. Both capture and emission times vary by more than an order of magnitude in this narrow range of temperature, in a manner consistent with thermal activation. Linear least square fits yield activation energies $E_c = (23 \pm 2)$ meV and $E_e = (26 \pm 1)$ meV.

Switching times for the full range of temperature are shown in Figure 3. Data represented by open triangles were measured with $I_d = -15$ μ A and $V_g = -3.00$ V. The solid curves represent a theoretical fit to the triangle data with three adjustable parameters (see below). Figures 3(a) and 3(b) indicate that both the mean capture and emission times become independent of T at low temperatures and increase rapidly with T at high temperatures. To model this behavior, we assume that each switching rate (both capture and emission) may be represented by the sum of two rates, one being thermally activated and the other being temperature independent. Specifically, we write:

$$\frac{1}{\tau_{\alpha}} = \frac{1}{\tau_{\alpha,1}} + \frac{1}{\tau_{\alpha,2}}, \quad (1)$$

where α = capture or emission, $\tau_{\alpha,1}$ is temperature independent, $\tau_{\alpha,2}$ is thermally activated, i.e.,

$$\tau_{\alpha,2} = \tau_{\alpha,2}(T) = \tau_{\alpha,0} \exp(E_{\alpha} / k_b T), \quad (2)$$

k_b is the Boltzmann constant, and $\tau_{\alpha,0}$ and E_{α} are the temperature-independent attempt time and activation energy respectively. Thus,

$$\tau_{\alpha}(T) = \frac{\tau_{\alpha,1} \tau_{\alpha,0} \exp(E_{\alpha} / k_b T)}{\tau_{\alpha,1} + \tau_{\alpha,0} \exp(E_{\alpha} / k_b T)}. \quad (3)$$

The solid curve in Figure 3(a) (mean capture time) was obtained using a weighted nonlinear least-squares fit of Eq. (1) to the triangle data, with weighting inversely proportional to the square of the uncertainty in the measured times. A minimum in the Chi-square per degree of freedom of 2.3 was obtained for $\tau_{c,1} = (2.3 \pm 0.4)$ s, $\tau_{c,0} = (5 \pm 3)$ μ s, and $E_c = (18 \pm 2)$ meV. For Figure 3(b) (mean emission time) the solid curve was obtained similarly, also yielding a value of the Chi-square per degree of freedom of 2.4 for $\tau_{e,1} = (3.1 \pm 0.6)$ s, $\tau_{e,0} = (9 \pm 4)$ μ s, and $E_e = (19 \pm 2)$ meV.

One possible explanation for the observed temperature-independent switching rates is that the charge carriers are not in thermal equilibrium with the lattice, i.e., that while the lattice is being cooled from 20 K to 4.2 K, the holes remain "hot" due to the high drain current. We reject this explanation due to the following argument. If this were indeed the case we would expect the measured capture and emission rates to depend strongly upon the power dissipated in the channel. To test this we performed additional measurements for $I_d = -5$ μ A and $V_g = -2.85$ V, plotted as the solid squares in Figure 3 above. As the channel resistance does not depend strongly on gate voltage, these conditions correspond to roughly a factor of 9 lower power dissipation than for the earlier measurements. Within experimental error, the two sets of data agree. It therefore seems unlikely that the temperature-independent rates are an experimental artifact associated with carrier heating.

Instead, we believe that the transition from thermally activated to temperature-independent switching rates is associated with a lattice relaxation mechanism similar to that observed in metal-

insulator-metal tunnel junctions [13]. Capture and emission of carriers are mediated by lattice relaxation, which proceeds via a thermally activated process at higher temperatures and a configurational tunneling process at lower temperatures. Such mechanisms have been anticipated in Si MOSFETs but, to our knowledge, not previously observed [7,9,16]. We also note that this result appears to contrast with a recent report of temperature-independent hysteresis attributed to the tunnel exchange of electrons with near-interfacial oxide (border) traps in MOS capacitors reported by Bhat and Saraswat [17] over a temperature range of 293 K to 473 K, but is consistent with the activated nature of the channel-to-trap charge exchange observed in all other RTS studies in MOSFETs at higher temperatures [2,7-11].

The relative importance of lattice versus carrier temperature, mentioned earlier, is interesting to consider further. Jackel et al. have performed experiments to separate the effects of electron and lattice temperature on switching rates of a RTS in a narrow n-channel MOSFET [18]. They found that the electron capture rate depended on both lattice and electron temperatures while the emission rate depended only upon lattice temperature. This experiment is frequently quoted in support of trapping models, but we are unaware of any attempts to duplicate it with other samples. In the future, it would be interesting to separate out the effects associated with lattice and carrier temperatures for other RTS's in MOSFETs or other physical systems.

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Figure Captions

Figure 1. Time-trace of the fluctuation in the drain voltage at a lattice temperature of 20 K. For this *pMOS* device, a more negative voltage corresponds to a higher resistance state.

Figure 2. Arrhenius plot showing the thermally-activated behavior of both the mean capture (triangle) and emission (square) times of the RTS for temperatures above 20 K.

Figure 3. Arrhenius plot showing the temperature dependence of the mean capture time (a) and emission time (b) for a RTS for 4.2–30 K. The open triangles represent data measured with $V_g = -3.00$ V and $I_d = -15$ μ A, while the solid squares represent data measured with $V_g = -2.85$ V and $I_d = -5$ μ A. The line represents the theory with three adjustable parameters obtained using a weighted nonlinear least squares fit to the triangle data.

Fig. 1, Scofield, Appl. Phys. Lett.

Fig. 2, Scofield, Appl. Phys. Lett.

(a)

(b)

Fig. 3, Scofield, Appl. Phys. Lett.