Identification of Yield-Limiting Defects in a 0.5 Micron, Shallow Trench Isolation Technology

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Abstract

During the development and qualification of a radiation-hardened, 0.5 μm shallow trench isolation technology, several yield-limiting defects were observed. The 256K (32K x 8) static-random access memories (SRAMs) used as a technology characterization vehicle had elevated power supply current during wafer probe testing. Many of the die sites were functional, but exhibited quiescent power supply current (I_{DDQ}) in excess of 100 μA , the present limit for this particular SRAM. Initial electrical analysis indicated that many of the die sites exhibited unstable I_{DDQ} that fluctuated rapidly. We refer to this condition as "jitter." The I_{DDQ} jitter appeared to be independent of temperature and predominately associated with the larger 256K SRAMs and not as prevalent in the 16K SRAMs (on the same reticle set). The root cause of failure was found to be two major processing problems: silicide bridging and stress-induced dislocations in the silicon islands.

Introduction

Shallow Trench Isolation (STI) technology is becoming widely used throughout the semiconductor industry. STI processing enables reduced transistor spacing, improves latchup immunity, and provides better planarity for subsequent processing [1]. Sandia National Laboratories began developing a radiation-hardened STI process several years ago to manufacture more complex integrated circuits (ICs) for Department of Energy Defense Program needs. In the course of this development process, both 16K and 256K SRAMs were designed and fabricated for use as characterization vehicles. The two designs are also used for yield monitoring and improvement.

Sandia's STI process is shown in: Fig. 1. The active devices are fabricated in twin wells in lightly-doped p -type epitaxial silicon. The substrate is heavily doped p^+ silicon. Transistor sources, drains, and polysilicon gate regions are covered with self-aligned titanium silicide for higher conductivity and lower contact resistance. The fabrication backend process is multi-layer metal, with chemical-mechanical polishing (CMP) used to planarize the interlevel dielectrics and tungsten via plugs. All contact and via openings are lined with Ti/TiN, and the metal layers are a sandwich of Ti, AlCu, and TiN.

Fig. 1 Diagram showing Sandia National Laboratories 0.5 micron, radiation-hardened CMOS technology.

The SRAM memory cell and schematic for this technology is shown in Fig. 2. The cell is a 6-transistor cell. The inputs are cross coupled using a lightly doped polysilicon layer to create a high value feedback resistor (approximately 250 $k\Omega$). The bit line and word line drive the drain and gate, respectively, of the access transistors.

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Fig. 2 SRAM cell layout and schematic.

Initial Analysis Activities

Wafer probe testing of both 16K and 256K SRAMs using an Advantest T3340 indicated excessive I_{DDQ} on numerous die locations. The 256K SRAMs had higher I_{DDQ} and a higher percentage of defective die locations than the 16K SRAMs. Testing using a probe station and an HP-4155 Semiconductor Parameter Analyzer reproduced the problem. Current-voltage measurements were performed for a number of different die locations. Fig. 3 is an example of typical SRAM I_{DDQ} values.

Fig. 3 I - V curves of typical 256K SRAM die sites with both low ($<1\mu A$ @ 5V) and high ($>1\mu A$ @ 5V) I_{DDQ} .

The I - V curve indicates a non-linear conduction mechanism, and close to exponential. It shows a mechanism that starts at ~ 1.2 V. Low current devices do not exhibit this conduction mechanism but rather appear to be dominated by the inherent junction leakage of the technology. The conduction mechanism is believed to be associated with the salicide (to be discussed later). The current associated with the stress-induced dislocations (also to be discussed later) appears to be masked by the salicide conduction mechanism or very similar in nature to it.

Next, the I - V characteristics of SRAMs were examined with respect to time. A rapid fluctuation in current was observed on a large percentage of the samples. The fluctuations occurred typically at a rate faster than could be resolved with the Hewlett Packard 4155 Semiconductor Parameter Analyzer used for these measurements. A slight decrease in the magnitude of the current was observed immediately after power was applied. This change was fairly small and is most likely attributable to resistance changes associated with the salicide conduction mechanism. Several samples were examined at $85^{\circ}C$ to see if there was any change in overall magnitude or frequency of the fluctuations. None were observed on the samples (see Fig.4).

Fig. 4 I_{DDQ} versus time plot for a high current 256K SRAM. Note rapid fluctuation in current.

Photon Emission Microscopy was performed on a number of 16K and 256K SRAM die locations. Most of the 16K SRAM die locations had only a few light emission sites (see Fig. 5).

Fig. 5 Light emission photograph showing emission sites on a 16K SRAM die.

However, a number of the 256K SRAM locations had numerous light emission sites. The emission sites were correlated to n-channel access transistors in the memory array (see Fig. 6). There was some indication that the light emission might be coming from the edge of the transistor region rather than uniformly from the entire channel. However, the optics on the light emission system were insufficient to determine this for sure. The only significant difference between the 16K SRAM and the 256K SRAM is the SRAM cell size. In the 256K SRAM, the cell is approximately 40% smaller because of a layout shrink of the cell.

Fig. 6 Light emission images at increasing magnification showing numerous emission sites on a 256K SRAM die.

Fig. 7 Scanning electron microscope images of the SRAM cell region (a) after removal of poly-2 metal-1 interlevel dielectric (b) after removal of poly-1 and (c) after a decoration etch – arrow indicates missing silicon.

Initial deprocessing work was performed to determine if any defects or anomalies could be seen and to provide clues for the failure mechanism. Several samples were stripped down first to the polysilicon layer, then to the gate oxide layer. The samples were then etched to

delineate possible defects in the silicon. The samples were then imaged using a scanning electron microscope (see Fig. 7). Although some silicon removal was noted near the gate edges in some instances, this did not provide enough evidence to determine the failure mechanism.

Next, individual emission sites were identified and examined in cross section using transmission electron microscopy (TEM). TEM analysis showed two problems with the memory array. (1) Because of an intermittent processing problem, titanium silicide covered the source and drain regions (as desired) and sometimes also oppositely-doped regions along the trench sidewall (not desired). This conducting bridge created an unwanted conducting path (see Fig. 8). (2) Dislocations were observed bridging the source to drain regions on several samples (see Fig. 9). These dislocations provided an intermittent path for leakage current, resulting in the observed I_{DDQ} jitter.

Fig. 8 TEM image showing titanium silicide in the active region. The Ti silicide provided a leakage path between the drain and oppositely-doped regions along the trench sidewall.

We also examined the SRAM cells using plan view TEM imaging. Plan view TEM imaging involves thinning the sample such that imaging can be performed perpendicular to the surface of the silicon substrate. To prepare a plan view TEM sample, the die is first delayered to the gate oxide level. Next, the sample is thinned from the backside to the point where it is transparent to high energy electrons. This is approximately 0.5 μm in thickness. The plan view TEM imaging indicated a high density of dislocation defects along the edge of the trench associated with the n-channel access transistors (see Fig.

10). The defects appeared to be most common along one sidewall as opposed to the other sidewall.

Fig. 9 Transmission Electron Microscope image of a dislocation present in the channel of a suspect transistor.

Fig. 10 Plan view TEM sample showing dislocations near the trench edge in the n-channel access transistor.

Further investigation, including literature searches and discussions with experts in the field, into the dislocation problem revealed that stress at the edge of the trench caused the dislocations [2, 3]. This stress was the result of the thermal coefficient of expansion mismatch between the silicon and the dielectric in the trench, and was aggravated by the arsenic implants (to create the n+

regions for the n-channel transistors) that create defects in the lattice. Based on publications about DRAM dislocations, we believe that numerous dislocations in the 256K SRAMs were intermittently conducting, resulting in current jitter.

Discussion on Dislocation Leakage

Reverse biased *pn* diodes have a leakage current across the metallurgical junction, which is typically due to the presence of midgap energy states arising from impurities. These states enable band to impurity to band tunneling, which constitutes the current. This generation-recombination current (Schockly-Read-Hall) is temperature dependent and approximately constant for a given reverse bias. Some small fluctuations do occur in the current magnitude, however, and these variations are characterized as thermal or white noise. The general name applied to this leakage current is "junction leakage" and this type of leakage current dominates I_{DDQ} measurements in nominal SRAMs. The Arrhenius activation energy for this current can usually be measured as close to 0.6 eV or half the bandgap of silicon.

In some small electronic devices, other types of current fluctuations occur. These fluctuations are due to discrete switching of the conductivity of the device. In the case of the reverse biased diode, this switching can be attributed to the capture and emission of carriers at individual defect sites within or close to the depletion region. The presence or absence of the carriers at these sites act in a similar manner to applied voltage on the gate of an FET which modulates the conductivity of the transistor. In fact, in small area FETs, the same type of drain current fluctuations are observed and have been attributed to the emission and capture of carriers at individual traps in the gate oxide[4]. In this case, the carriers electrostatically modify the channel region underneath the gate oxide and thus influence the drain current. Because of the form these fluctuations assume, they are referred to as Random Telegraph Signals (RTS).

Fig. 11 Leakage currents in a CCD diode (Hopkins [8])

Figure 11 shows three typical current versus time recordings where the fluctuations in the current magnitudes are RTS fluctuations for the upper two traces. In these two cases there are two discrete conductivities of the device as evidenced by the two distinct current levels.

RTS currents arise in electronic devices where crystal defects occur. As noted, this has been observed at Si-SiO₂ interfaces and in bulk silicon in depletion regions of *pn* junctions. Today's submicron technologies accomplish device isolation with Shallow Trench Isolation (STI) in place of LOCOS oxide. In addition, some DRAM technologies use deep trench capacitors for memory cells. Both of these trench technologies create mechanical stress in the single crystal silicon, which can give rise to defects and dislocations. Layers of materials that cross the STI and single crystal silicon also can produce mechanical stress in the single crystal. Dislocations associated with both of these trench technologies have been shown to cause anomalous leakage currents, some which exhibit RTS characteristics. [5, 6, 7]

One model of dual state conduction along dislocations relies on impurity decoration of the dislocation. The impurities act as a filament of doped material. The conduction channel formed by the filament can be "pinched off" electrostatically by the presence of trapped charge carriers adjacent to the filament. This model holds that the decoration occurs during the dislocation formation. A dislocation that nucleates in a highly doped region will "drag" dopants along with it as it grows and propagates through the lattice. An example is a dislocation which begins at an STI edge in a *n*-doped drain region and propagates through the single crystal silicon to the drain-body junction and into the p-type p-well. This dislocation could drag arsenic or phosphorus atoms along the dislocation and thus form an n-type filament into the p-well. A trap state adjacent to the filament could cutoff the current in the filament by trapping a negative charge carrier.

These descriptions of RTS distinguish the conduction mechanism from normal junction leakage. The presence of the dislocations in the SRAMs fabricated in the Sandia STI process thus allows the exploration of differences in the two types of conduction. Here, 16K SRAMs were used to study the response of the I_{DDQ} as a function of temperature. Figs. 12 and 13 show I_{DDQ} for two 16K SRAMs vs. supply voltage magnitude at varying temperatures. Fig. 12 shows I_{DDQ} for an SRAM without dislocations. As a consequence, the magnitudes of I_{DDQ} at low temperatures are small ($\sim 2\text{E-}10$ for 3 V). The log of the current for any given voltage increases linearly with temperature in a well behaved fashion as seen in the family of curves in Fig. 12. The activation energy calculated for these curves is approximately 0.6 eV, which is an indication that only junction leakage is occurring in this SRAM.

Figure 13 shows the temperature dependence for a 16K SRAM with dislocations. Several differences stand out when compared to Fig. 12. The first is the amount of noise, which is obvious from the *I-V* curves, most prominently at low temperatures. The magnitude of the currents at low temperatures is almost 2 orders of magnitude larger at voltages around 3 volts and above. The differences are much smaller at lower values of V_{DD} . Another difference is the lack of increase of current with temperature for temperatures $< \sim 70^\circ\text{C}$. Above 70°C , the junction leakage current is comparable to or larger than the dislocation conduction current so the *I-V* curves begin to show temperature dependence. The shape of the *I-V* curves also differ remarkably from the curves in Fig. 12. Note that in both sets of curves, the perturbations at just below 1 V are due to the settling of the CMOS latches into stable on/off states. This same difference is also seen in Fig. 2.

Fig. 12 Temperature dependence of 16K SRAM I_{DDQ} in SRAM without dislocations from 22°C to 120°C

Fig. 13 Temperature dependence of 16K SRAM I_{DDQ} in SRAM with dislocations from 25°C to 120°C .

For low temperatures where the dislocation conduction current is greater than the junction leakage, the current magnitude responds weakly to temperature increase. Using the carrier emission and capture model of the discrete switching of the conductivity, some temperature effect is expected in the capture and emission rate. Figure 14 shows I_{DDQ} vs. time for a 16K SRAM with dislocations. The three graphs correspond to temperatures of 27°C, 50°C, and 120°C. Note that the number of transitions in each trace increases with temperature, which corresponds to an increase in the capture and emission rate of trap sites. In general, it is not expected that the average lifetime in the low and high conductivity states should be equal [9]. It also should be noted that the difference in magnitude of the low and high current states increases with temperature. This is most likely due to the dislocation providing a better conduction path at higher temperatures.

Fig. 14 Time dependence of 16K SRAM I_{DDQ} Current in SRAM with dislocations.

Figure 15 I_{DDQ} distributions of 256K SRAMs before and after process changes.

Corrective Action

Process changes were made to correct the leakage mechanisms. Most importantly, the silicon nitride sidewall spacer etch process was modified to avoid attacking and exposing the corners of the shallow trench isolation adjacent to the transistor drains. This change prevented silicide from shorting the n+ drain to the p-type trench sidewall implant. This modification alone dramatically improved the I_{DDQ} distributions (see Fig. 15). Investigations are also underway to reduce the dislocation density by modifying the thermal budget of the trench-fill dielectric and by reducing the source/drain implant doses.

Conclusions

The major mechanism responsible for the low yielding wafer lots appears to be the silicide bridging problem. A secondary mechanism, stress-induced dislocations, is the second-order mechanism responsible for low yield. Advancements in technology have necessitated the use of higher performance imaging tools such as the transmission electron microscope. These tools are increasingly necessary to localize and characterize defects on ICs. However, this work also points out the importance of interpreting and understanding I - V signatures on ICs. Electrical data is a powerful tool for understanding failure mechanisms. It will become increasingly important as technologies continue to shrink, precluding extensive physical analysis.

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References

1. L. Peters, "Choices and Challenges for Shallow Trench Isolation," *Semiconductor International*, April 1999, pp. 69-76.
2. D. Ha, C. Cho, D. Shin, G. Koh, T. Chung, and K. Kim, "Anomalous Junction Leakage Current Induced by STI Dislocations and Its Impact on Dynamic Random Access Memory Devices," *IEEE Trans. Elec. Dev.*, Vol. 46, No. 5, May 1999, pp. 940-946.
3. P. J. Restle, J. W. Park, B. F. Lloyd, "DRAM Variable Retention Time," *Proc. Int. Elec. Dev. Meeting*, April 1992, pp. 807-810.

4. P. J. Restle, A. Gnudi "Internal Probing of Submicron FETs and Photoemission using Individual Oxide Traps" *IBM J. Res. Develop.*, Vol. 34, No. 2/3 March/May 1990.
5. P. J. Restle, J. W. Park, B. F. Lloyd, "DRAM Variable Retention Time," *Proc. Int. Elec. Dev. Meeting*, April 1992, pp. 807-810.
6. D. Ha, C. Cho, D. Shin, G. Koh, T. Chung, and K. Kim, "Anomalous Junction Leakage Current Induced by STI Dislocations and Its Impact on Dynamic Random Access Memory Devices," *IEEE Trans. Elec. Dev.*, Vol. 46, No. 5, May 1999, pp. 940-946.
7. P. Schani, S. Subramanian, V. Soorholtz, P. Liston, J. Moss, E. Widener, A. Chu "Analysis of FSRAM Single Bit Failures Due to Unique Dislocations" *Int. Symp. Test. Fail. Anal.*, Nov. 1998, pp. 373-376.
8. Hopkins "Further Measurements of Random Telegraph Signals in Proton Irradiated CCDs" *IEEE Transactions on Nuclear Science*, Vol. 42, No. 6, Dec 1995.
9. M. Kirton, M. Uren "Noise in Solid-State Microstructures: A new Perspective on Individual Defects, interface States and Low-Frequency (1/f) Noise" *Advances in Physics*, Vol. 38, No. 4, 1989, pp 367-468