LA-UR- 95-2171

CONF-9508122-4

Title:

Contributions from the SuperKamiokande Collaboration

Author(s):

Y. Fukuda, K. Inoue, Y. Ito, T. Kajita, M. Miura, M. Nakahata, K. Nakamura, M. Shiozawa, Y. Suzuki, Y. Takeuchi, Y. Totsuka, K. Nishikawa, J. Kanzaki, Y. Oyama, O. Sasaki, S. Tasaka, A. T. Suzuki, T. Suda, M. Mori, K. Miyano, H. Miyata, Y. Nagashima, M. Takita, A. Suzuki, T. Hasegawa, F. Suekane, M. Koshihara, K. Nishijima, K. Kaneyuki, T. Tanimori, Y. Watanabe, S. Dye, J. T. Hong, E. Kearns, M. Masuzawa, J. Stone, L. Sulak, M. Goldhaber, T. Barszczak, J. Breault, W. Gajewski, P. Halverson, J. Hsu, W. Kropp, L. Price, F. Reines, H. Sobel, K. Ganezer, B. Keig, B. Bratton, J. Flanagan, J. Learned, S. Matsuno, V. Stenger, T. J. Haines, M. Cherry, R. Svoboda, M. Vagins, M-L. Chen, Z. Conner, J. Goodman, R. Ellsworth, C. K. Jung, C. Mauger, C. McGrew, B. Viren, C. Yanagisawa, D. Kielczewska, A. Stachyra, V. Chaloupka, R. J. Wilkes, and K. K. Young

Submitted to:

XXIV International Cosmic Ray Conference
Rome, Italy, August 28-September 8, 1995

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ST 2629 10/91

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SuperKamiokande Outer DAQ System

R. Jeffrey Wilkes¹, for the SuperKamiokande Collaboration²

¹ Univ. of Washington, Seattle, USA

Abstract

SuperKamiokande is a 50 kT ring-imaging water Cerenkov detector approaching completion at 2700 MWE depth in the Kamioka-Mozumi mine in Japan. The inner detector (32 kT mass) is instrumented with 11,200 PMTs of 50cm diameter, while the outer volume, separated by a light-proof barrier, is instrumented by 1850 PMTs of diameter 20 cm. The outer (anti-coincidence) detector has an independent data acquisition system, with the capability of triggering independently as well as in coincidence with the inner detector. We will describe the outer detector front end DAQ electronics, data-handling scheme, and associated equipment.

1 Introduction

The SuperKamiokande water Cerenkov detector, now approaching completion, will occupy a cylindrical stainless steel tank filled with ultra-purified water. The tank has dimensions approximately 39m D x 41m H at depth 2700 MWE, with a sensitive volume of approximately 50 kT. The inner detector (ID) is lined with 11,200 Hamamatsu 50cm photomultiplier tubes facing inward, while the outer 2.5m shell of water volume will be viewed by 1,850 outward-facing Hamamatsu R-1408 PMTs, with 20 cm diameter hemispherical photocathodes, previously used in the IMB experiment. In this paper, we will describe the outer detector (OD) data acquisition system, whose output will be integrated into the separate data system being constructed for the ID.

²Y. Fukuda, K. Inoue, Y. Ito, T. Kajita, M. Miura, M. Nakahata, K. Nakamura, M. Shiozawa, Y. Suzuki, Y. Takeuchi, Y. Totsuka (ICRR), K. Nishikawa (INS), J. Kanzaki, Y. Oyama, O. Sasaki (KEK), S. Tasaka (Gifu U.), A.T. Suzuki, T. Suda (Kobe U.), M. Mori (Miyagi Education U.), K. Miyano, H. Miyata (Niigata U.), Y. Nagashima, M. Takita (Osaka U.), A. Suzuki, T. Hasegawa, F. Suekane (Tohoku U.), M. Koshihara, K. Nishijima (Tokai U.), K. Kaneyuki, T. Tanimori, Y. Watanabe (Tokyo Inst. Tech.), S. Dye, J.T. Hong, E. Kearns, M. Masuzawa, J. Stone, L. Sulak (Boston U.), M. Goldhaber (BNL), T. Barszczak, J. Breault, W. Gajewski, P. Halverson, J. Hsu, W. Kropp, L. Price, F. Reines, H. Sobel (UC/Irvine), K. Ganezer, B. Keig (CSU/Dominguez Hills), B. Bratton (Cleveland State U.), J. Flanagan, J. Learned, S. Matsuno, V. Stenger (U. Hawaii), T. Haines (LANL), M. Cherry, R. Svoboda, M. Vagins (LSU), M-L. Chen, Z. Conner, J. Goodman (U. Maryland), R. Ellsworth (George Mason U.), C.K. Jung, C. Mauger, C. McGrew, B. Viren, C. Yanagisawa (SUNY/SB), D. Kielczewska (Warsaw U.), A. Stachyra, V. Chaloupka, R. J. Wilkes, K. K. Young (U. Washington).

A single coaxial cable supplies HV and carries signals out from each OD PMT, which will be mounted on the outer surface of an internal stainless steel framework that also supports the ID PMTs. There will be two OD PMTs mounted on the back of each modular patch of 12 ID PMTs. Light collection by the OD PMTs is aided by wavelength-shifter plates; these are attached to each tube just above its midplane to collect photons over an area of $60 \times 60 \text{ cm}^2$ and channel them into the photocathode. In addition, the outer walls of the SuperK tank are lined with Tyvek, a material made of bonded white polyethylene fibers with diffuse reflectance approximately 90% in the appropriate wavelength range. The ID and OD PMTs are separated by a light-proof barrier comprising a black polyethylene inside layer bonded to a white Tyvek outer layer.

Five counting houses will be established on a platform above the SuperK detector. There will be one counting house for each quadrant of the detector, containing fast front-end electronics and HV supplies for both ID and OD PMTs. The central counting house will contain second-level electronics, host computers and auxiliary data systems.

The purpose of the Outer Detector DAQ system is to record the arrival times and net charge of PMT pulses associated with events in the Super-K detector. In its simplest application, the OD will function as a veto counter to reject events with associated entering charged particles. However, it will be possible to use the OD to provide more detailed supplementary information to the ID system. The OD DAQ system will operate independently of the DAQ system being constructed by the Japanese side of the collaboration for the inner detector. It must identify a very wide variety of possible event types from the recorded data, so the system must be very flexible. A simplified overall block diagram is shown in the figure.

2 PMT Data Handling

The light collection system for the OD consists of the PMT, wave-length-shifter (WLS) plates, and diffuse reflector material (Tyvek) lining the Outer Detector. The WLS plates increase the effective net photocollection area of each tube. The Tyvek allows collection of reflected light from outward-moving tracks, increases the total amount of light collected, and also increases the exponential fall-off time for the tail of the PMT pulse due to multipaths. The time response of the WLS plates increases the overall PMT time slewing to about 12 nsec.

Raw PMT signals are picked off the HV lines and fed to specially designed discriminator modules set to a threshold corresponding to $1/4 \text{ pe}$. They produce two pulses of standardized height: a Time Over Threshold (TOT) pulse,

which is just the discriminator output, and after a fixed delay, a "Q" pulse whose length is proportional to the integrated charge of the input signal. In addition, an analog sum of the stretched discriminator outputs (HITSUM) for the 16 channels on an individual front-end card is produced. The HITSUM signal can be used to form an independent OD trigger if desired.

Discriminator outputs will be fed to Lecroy 1877 multihit TDCs. These are 96-channel, FASTBUS TDCs with 32 μ sec total window duration, allowing detection of up to 16 edges (upward or downward transitions in the signal) per channel. Edges must be separated by a minimum of 20 nsec to be resolved. An 8 event circular buffer allows readout without interrupting DAQ, and ensures handling of bursts such as would be expected during a supernova event. The ID trigger (TRG) module will transmit a trigger pulse to the OD TDCs. The fact that the TDC is in effect a FIFO pipeline of length 32 μ sec is very useful, since one wants to identify processes such as muon decay with time scales of several μ sec.

The TDC deadtime while digitizing hits is on the order of 1 μ sec, depending on the number of hits per module. A front-panel busy output will be logged to monitor deadtime, using an auxiliary data latch to insert the busy bit transition times into the data stream.

The FASTBUS modules (TDCs, aux data latch) will be housed in crates controlled by FSCC (Fastbus Smart Crate Controller) modules developed at Fermilab. One crate and FSCC will be required per quadrant counting house. The FSCCs are data-driven, and deliver output via an RS-485 port, with rates up to 10 MHz for 4-byte words. The four quadrant FSCCs funnel FASTBUS data to a single VME crate located in the central counting house. The VME crate will contain four ping-pong dual-port memory (DPM) sets, one per quadrant. The DPMs allow uninterrupted buffering of data from the FSCCs via the VME bus into the OD host computer. In each DPM, two identical banks of 32 MB memory are accessible from both a VSB bus and a VME bus, with access mediated by a local controller. The ping-pong mode of operation allows one bank to collect FASTBUS data from its VSB port while the other bank is being read out via its VME bus, with roles switched when a sufficient block of data has been accumulated or if the bank becomes filled. This will occur at intervals of about 5 sec. The memory bank which has been toggled for output will be read through the VME bus into the SUN-20 host computer, which functions as the VME crate controller via an SBus-to-VME interface.

The Sun-20 OD-host CPU has sufficient memory to allow it to handle a full DPM bank of data without delays. It is interfaced to the ID host computer (another Sun-20) via an FDDI (fiber-distributed data interface) network.

3 Merging Data Streams

In addition to the PMT data stream, we will have auxiliary information that will be required for event building and data analysis. These data must be synchronized with the fast data from the PMTs.

The absolute time (UTC, Universal Time - Coordinated) of each event or event component will be recorded using a GPS (Global Positioning System) receiver at the surface laboratory, which provides absolute UTC data accurate to 100 nsec. The GPS clock system consists of an antenna, satellite receiver, and a UTC clock which is disciplined by the realtime satellite data. The surface unit outputs a standard time code (IRIG-B, DC-level shift) which is interfaced by a fiber-optic link with a clock board located in the OD VME crate in the central counting house. The underground VME module contains a local clock board which is disciplined by the IRIG-B signal with 1 μ sec accuracy, sufficient for our purposes.

Each time a trigger is received, the current UTC will be logged as an auxiliary event data block with the current event number using a VME data latch module. The same module will be used as a deadtime monitor to record the times when the TDC and ADC modules have their busy-bits on, allowing us to properly correct and interpret observed event rates. To simplify association of the current ID event number and UTC with the contents of the FAST-BUS datastream, we will also install an auxiliary data latch module in each quadrant's FASTBUS crate.

The 11,200 PMTs of the ID will be digitized by specially-designed ATM modules designed at KEK, and will be buffered by VME ping pong dual port memories systems similar to those described here. It is planned that the toggling will occur at the same time for the ID and OD DAQ. In this way the complete events can be assembled by the main host event builder by picking data associated with the proper event number from the OD host's buffers. The events will be identified by event numbers which have been commonly generated in the TRG module.