

Integrated X-ray and charged particle active pixel CMOS sensor arrays using an epitaxial silicon sensitive region

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ABSTRACT

Integrated CMOS Active Pixel Sensor (APS) arrays have been fabricated and tested using X-ray and electron sources. The 128 by 128 pixel arrays, designed in a standard 0.25 micron process, use a ~10 micron epitaxial silicon layer as a deep detection region. The epitaxial layer has a much greater thickness than the surface features used by standard CMOS APS, leading to stronger signals and potentially better signal-to-noise ratio (SNR). On the other hand, minority carriers confined within the epitaxial region may diffuse to neighboring pixels, blur images and reduce peak signal intensity. But for low-rate, sparse-event images, centroid analysis of this diffusion may be used to increase position resolution. Careful trade-offs involving pixel size and sense-node area verses capacitance must be made to optimize overall performance. The prototype sensor arrays, therefore, include a range of different pixel designs, including different APS circuits and a range of different epitaxial layer contact structures. The fabricated arrays were tested with 1.5 GeV electrons and Fe-55 X-ray sources, yielding a measured noise of 13 electrons RMS and an SNR for single Fe-55 X-rays of greater than 38.

Keywords: CMOS, Epitaxial, Active Pixel, Radiation, Sensor

1. INTRODUCTION

A standard CMOS active pixel sensor [1], particularly one fabricated in a modern and highly scaled standard digital CMOS technology, will not function as an efficient sensor for minimum ionizing particles or X-rays. This is due to the very shallow junction depth inherent in these processes [2], which limit the depth of the sensitive region, hence the amount of collected charge. The resulting signal to noise ratio would be too poor for it to detect single photons or individual minimum ionizing particles efficiently, if at all. Some means of increasing the cross-section of the sensitive region is, therefore, desirable. Previously, this has been accomplished by using a separate sensor plane, for example of high-resistivity silicon or germanium [3]. Liberated from the constraints of what is available in a standard CMOS process, this permits almost any sensor technology or configuration. Specialized sensor arrays, however, are expensive, and one must attach the sensor plane to the readout plane by some electrical and mechanical means, such as bump-bonding. The latter is a complex and costly process that has certain limitations, for example, in the pitch of the bumps, which limits pixel size, hence ultimate spatial resolution. Finding a way to integrate the sensor on the electronics plane, just as in common digital cameras, will result in dramatically reduced costs and other improvements.

Recently, the use of an integrated epitaxial silicon layer has been explored as a sensor region [4, 5, 6]. The use of epitaxial silicon — particularly pure silicon that is grown on top of a standard silicon wafer — is now commonly used in many CMOS processes. In CMOS circuits, it provides better isolation among transistors. Epitaxial layer thicknesses of up to 12 microns are specified in CMOS processes, though they can be grown up to 100 microns thick, if desired. Figure 1 shows a cross-section of a silicon wafer region with epitaxial layer as used for particle and X-ray detection. The p + bulk layer is the standard silicon starting wafer, that is, in this case, doped to be p -type silicon. Above it is the p -epitaxial layer, a purer silicon layer of higher resistance. At the top is an n + diffusion layer that is selectively implanted as part of the normal CMOS processing. Below it is a depletion region that forms at the n + / p - diode junction.

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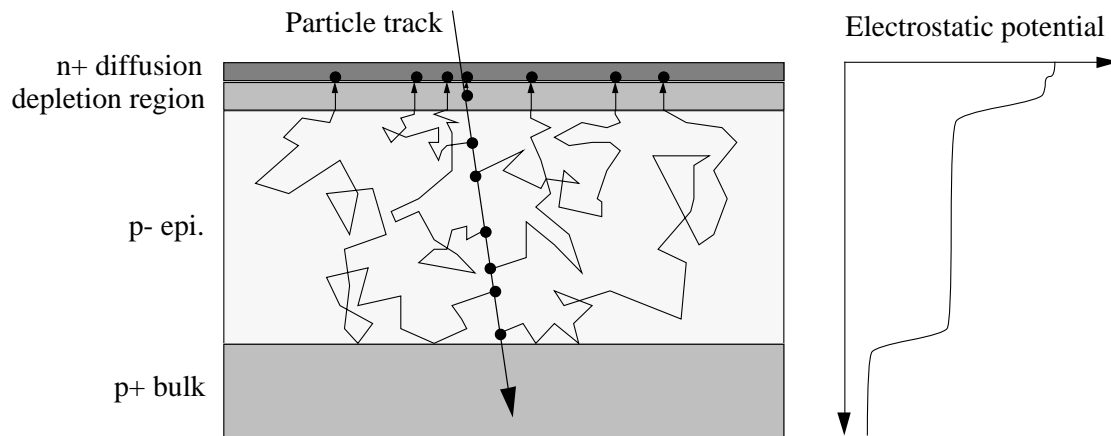


Figure 1: Cross-section of a silicon wafer designed with an epitaxial region and surface diode that is sensitive to ionizing radiation.

On the right is a representation of the electrostatic potential versus depth into the wafer. Clearly, it decreases monotonically into the wafer. So, for example, at the p -epitaxial silicon / p + bulk silicon junction, there is a heightened barrier that would tend to reflect electrons, confining them to the epitaxial region. The depletion region does not extend fully into the epitaxial region. Hence, there is no electric field in the epitaxial region and liberated electrons diffuse rather than drift in it. Provided that the epitaxial region is very pure, the lifetime of liberated electrons is sufficiently long that there is a high probability that they will eventually diffuse into the depletion region. This is shown as the random-walk pathways in the p -epitaxial region. Once they do encounter the depletion region, they drift toward the n + diffusion region and are trapped in its deep potential well.

2. CMOS CIRCUIT AND EPITAXIAL SENSOR COMBINATIONS

The above concept can be extended to incorporate CMOS readout circuitry. Figure 2 shows a similar cross section, but one that includes n -channel transistors in a p -well structure. The same bulk silicon and epitaxial regions are shown, but now at the surface we include additional CMOS processing steps and layers. In the top-center area, we see the same n + diffusion and a lightly doped n -well region. It is a physically smaller version of the continuous n + diffusion region shown in Figure 1. The addition of an n -well is commonly required in digital CMOS technology design rules. A depletion region is not shown, but it would exist at the n -well / p -epitaxial silicon interface. Hence, we now have a small area diode located in the epi region. On the right, we again see plots of the electrostatic potential. Curve (B) depicts the potential at position (B) in the wafer; this is essentially the same as the curve in Figure 1.

The center n + diffusion / n -well region is shown flanked by p -well regions in which n -channel transistors can be fabricated. The heavy black lines are metal contacts and wires traces can connect the diode to the n -channel transistors. The p -well regions reflect and confine the diffusing electrons in the more lightly doped epitaxial silicon region just as the interface to the bulk p -type silicon does. Potential curve (A) in the figure, found at position (A) in the wafer, depicts this additional barrier. Only at the diode junction can the electrons be collected. Since n -channel transistors are constructed in a p -well, they are shielded from diffusing electrons. Since p -channel transistors must be made in an n -well, the well would form an additional diode which would absorb electrons; additional n -wells cannot be used in the sensor array without additional insulation. Fortunately, only n -channel transistors (in p -wells) are needed to make standard active pixel sensor arrays.

As discussed above, the use of n -channel readout electronics is compatible with a p -epitaxial silicon process. Three varieties of CMOS pixel readout circuits are shown in Figure 3. On the left is a passive pixel sensor (PPS) including one access transistor that multiplexes the integrated charge onto an output bus. This circuit is compact, but has the disadvantage of being unbuffered and thus slower and more noise prone. In the middle is a standard APS circuit, which includes three transistors for reset, buffering, and multiplexing. It is larger but faster and of lower noise; it is the most

popular CMOS circuit for higher-quality digital cameras. On the right is an enhanced version that includes an additional transistor and a capacitor that together act as a sample and hold or shutter. The inclusion of a sample and hold is particularly valuable in high speed imaging [7], where it can be used as a fast shutter and also insures that the entire focal plane is sampled at once, rather than in a raster-scan fashion. This can eliminate a type of distortion when imaging moving subjects. Because of the added capacitance, it has lower gain and correspondingly higher well capacity i.e, the amount of charge that can be integrated before the pixel overflows or saturates.

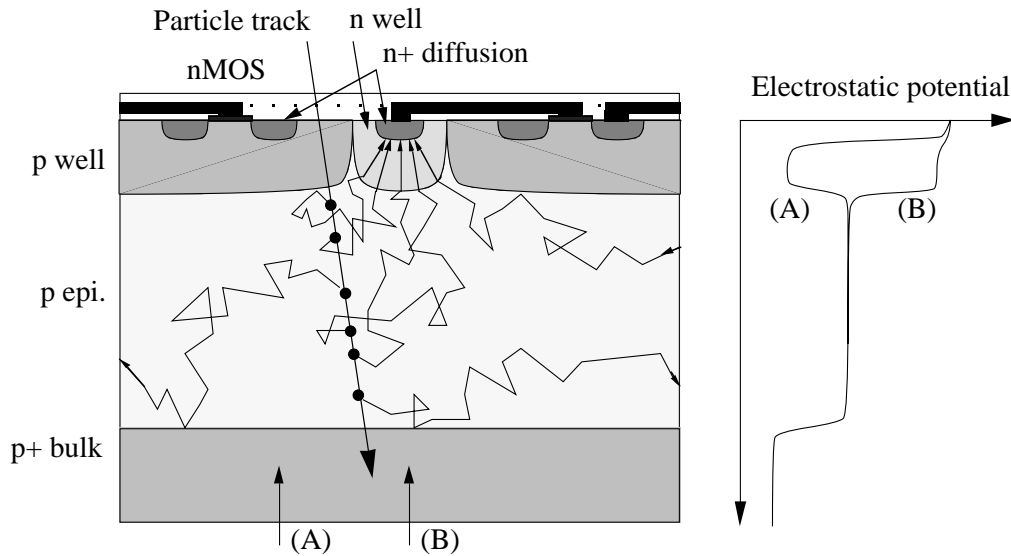


Figure 2: Cross section showing small collection diode flanked by n-channel transistors formed in p-wells.

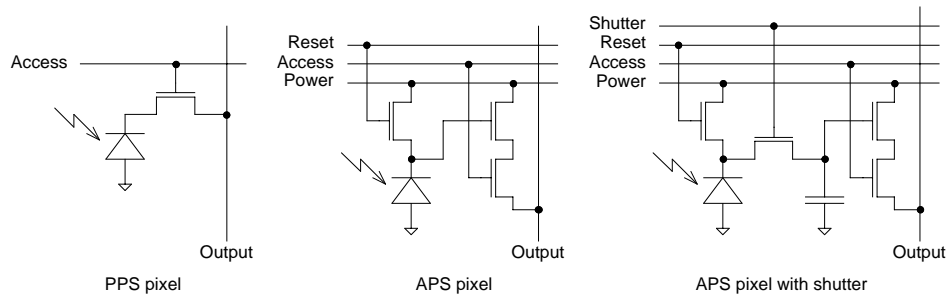


Figure 3: Three common CMOS pixel readout circuits.

The shutter circuit can optionally be used as a common-gate amplifier. When used this way, it shields the readout circuit from the capacitance of the collection diode. The collection diode can then be made large to collect more locally generated charge, yet the charge to voltage conversion gain can still be high.

Vastly more complex CMOS pixel readout electronics can be devised. For example, CMOS image sensors with an analog-to-digital converter and digital memory per pixel [8, 9, 10] have been demonstrated. With massively parallel analog-to-digital conversion and fast digital readout, these are capable of very fast frame rates. Unfortunately, these more elaborate circuits require complementary transistors incompatible with an epitaxial sensor, perhaps unless additional insulation such as provided by silicon-on-insulator technology is available.

3. PROTOTYPE CMOS RADIATION SENSOR

A prototype CMOS radiation sensor camera chip has been designed, fabricated and tested. A plot of the chip is shown in Figure 4. The prototype sensor array includes 128 by 128 pixels, broken into 4 quadrants of 64 by 64 pixels. Each quadrant uses a different sensor structure and/or readout circuit. Each pixel is 20 by 20 μm in size, and the entire array is about 2.5 mm on a side. The chip was designed in a standard digital 0.25 μm CMOS process that includes an 8-10 μm epitaxial layer.

The four quadrants of the prototype are designed to test different pixel sensor and readout structures. The circuit diagrams for the four quadrants are shown in Figure 5. Four different sizes and configurations of sensor diodes are shown, and two different readout structures are used. Quadrants 1 and 2 have a standard APS readout structure. These consist of three transistors: a reset transistor, a readout transistor, and a row-select transistor. In order to preserve maximum flexibility, the reset potential is supplied by a separate, arbitrary voltage supply, as opposed to being tied to Vdd as common in APS readout circuits. Quadrants 3 and 4 differ in that they use common-gate amplifiers, as discussed above, that are designed to shield higher capacitance diodes from the output gates, preserving higher conversion gain.

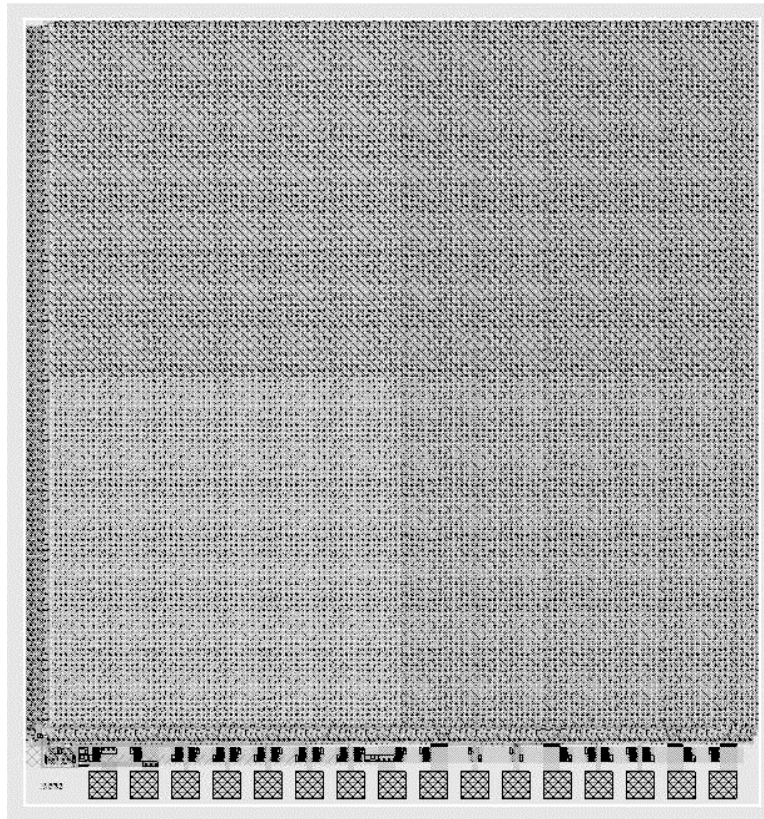


Figure 4: Prototype CMOS radiation image sensor layout containing 128 by 128 pixels in four differing quadrants. Total size is about 2.5 by 2.5 mm.

Each quadrant has a different collection diode topology. In APS1 pixels, there is one minimum-size collection diode. It is designed to have the highest charge to voltage conversion gain due to its lowest possible sensor capacitance. However, its very small area means that less of the charge that is liberated locally will be picked up by the diode, and more diffusion to neighboring pixels will occur. In APS2 pixels, there are 4 minimum-sized collection diodes. The dispersing of multiple small diodes about the pixel is intended to increase the collection of locally-liberated charge without resorting to large area diodes. APS3 and APS4 pixels have two slight variations on a large-area collection diode. The large-area diodes collect more of the charge liberated in the location of a given pixel. Here the use of the

common-gate amplifiers may permit the use of these larger diodes while maintaining adequate gain. A plot of the four different pixel topologies is shown in Figure 6.

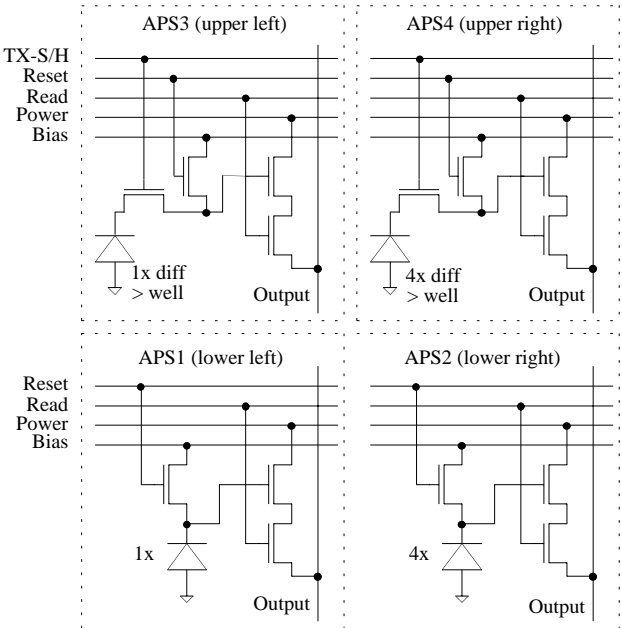


Figure 5: Four quadrants in the prototype radiation sensor array.

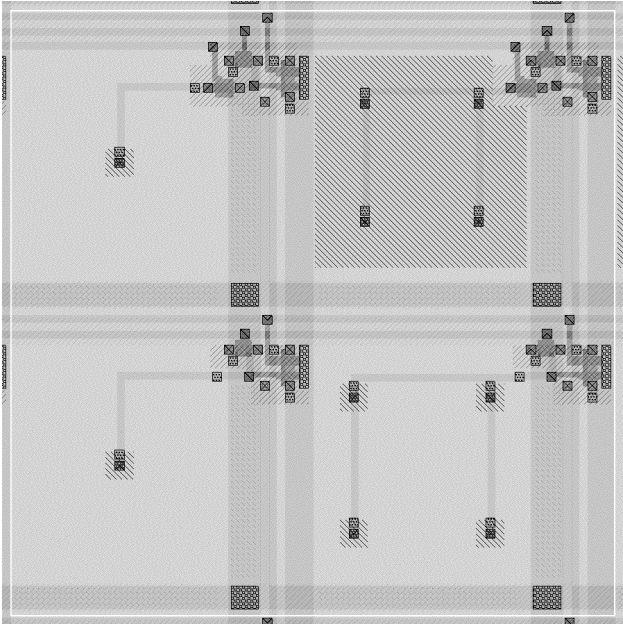


Figure 6: Four pixels from four 64 x 64 pixel quadrants in the proof-of-principle test chip. They differ in their collection diode and circuit topologies.

The test prototype contains pixels of 20 by 20 microns; relatively large compared to what is actually possible in the 0.25 micron process. In fact, pixels of about 5 by 5 microns would be practical. Hence, a million pixels could fit in a die of

under 6 by 6 mm. Yet the fill-factor — the ratio of the area of each pixel that is actually sensitive to radiation to the total area of the pixel — would be 100 percent, since the epitaxial region under the readout circuit area is fully sensitive. This is a substantial advantage over normal visual CMOS digital cameras, where a small pixel size usually leads to a poor fill-factor, hence reduced sensitivity.

4. SENSOR ARRAY TEST RESULTS

The prototype array was tested with Sr-90 and Fe-55 sources and also in an electron beam at the Advanced Light Source at Lawrence Berkeley National Laboratory. Figure 7 shows two quadrants of 64 by 64 pixels from the APS1 quadrant of the prototype as a 3-D plot. The diagram on the left shows an individual frame with an Sr-90 (0.232 MeV X-ray) source applied. Five interactions can be seen to be individually resolved. The diagram on the right is of an individual frame without the source, showing the noise floor of the device.

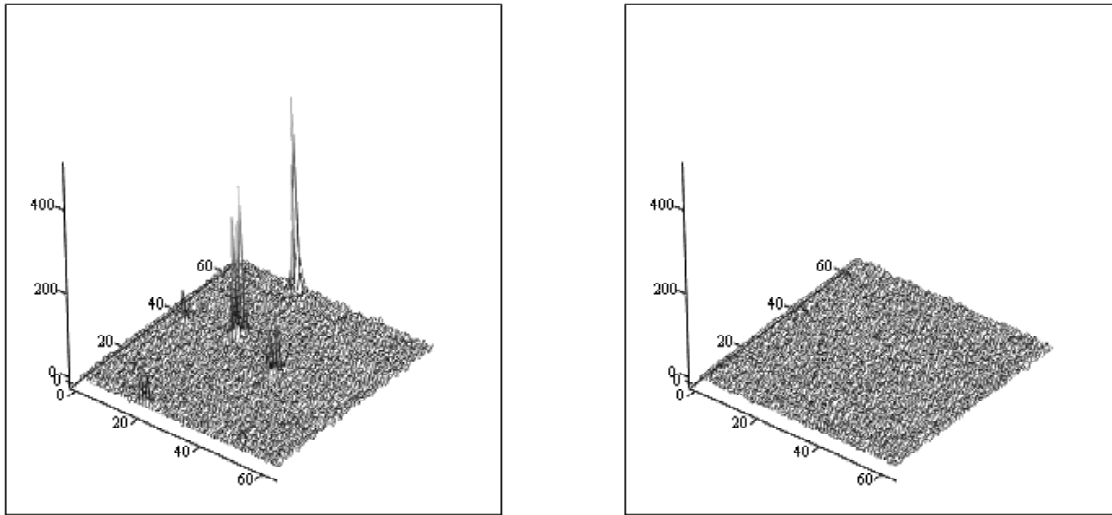
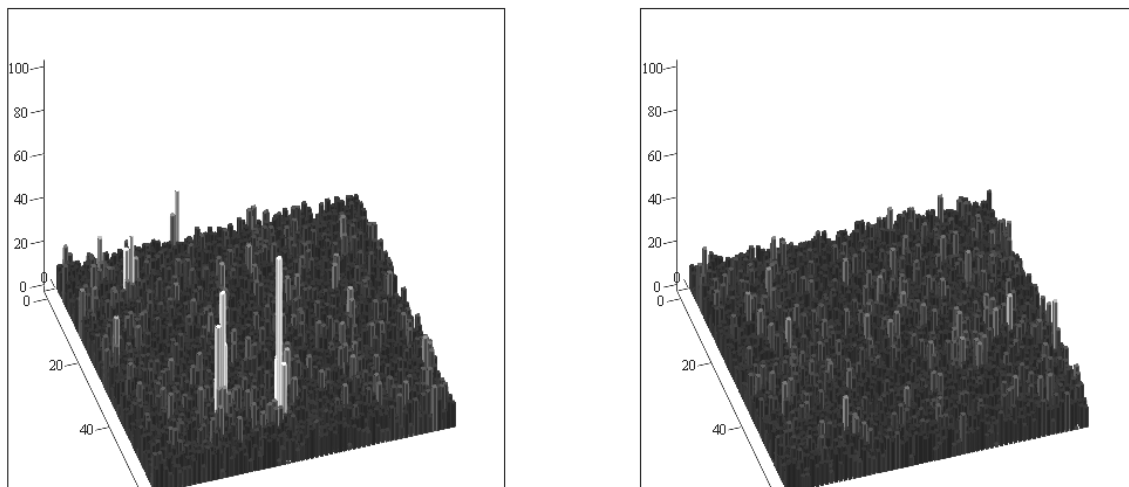


Figure 7: Test quadrants with Sr-90 source applied (left), showing five interactions, and without the source (right), showing only the noise-floor of the sensor array.



SE + 10

NE + 10

Figure 8: Test frames with 1.5 GeV electron beam from the Advanced Light Source. On the left is a frame with several electron hits, and on the right is a frame without beam.

The device was placed in a 1.5 GeV electron beam at the Advanced Light Source. Figure 8 shows two individual frames with and without the beam applied to the sensor chip. On the left is a frame with the beam applied, with several hits visible. On the right is the chip without the beam on, where all that is visible is the noise floor. Figure 9 shows the measured energy spectrum with a calculated energy spectrum superimposed. The plot displays excellent agreement with the expected results.

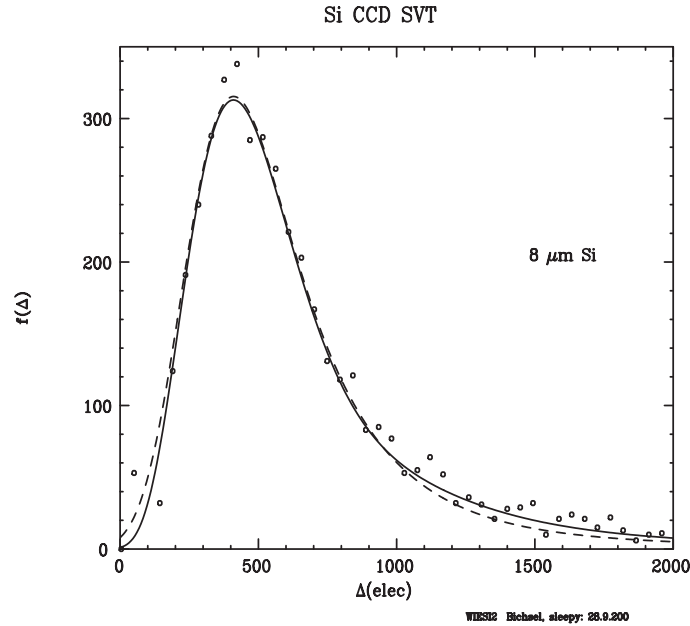


Figure 9: Energy spectrum of 1.5 GeV electrons. The circles are measured data while the solid line is a calculated energy spectrum assuming an 8 μm epitaxial layer.

Diffusion causes liberated electrons to be dispersed and collected over a radius including a number of pixels, and strategies for obtaining optimum position resolution are dependent on the analysis of this diffusion profile versus collection diode topologies. Measurements were made that sum the total charge collected over a range of pixels, from individual pixels up to a radius that includes 81 pixels. As the summation radius increases, the total charge collected per interaction increases. In addition, since the charge collected per pixel is very small for a single X-ray or particle interaction, pixel leakage can reduce signal levels and decrease signal to noise ratios. Figure 10 shows the total charge collected by APS1 pixels versus number of pixels summed for two integration times; 2 ms and 32 ms. We can see that the total charge collected per interaction increases as the number of summed pixels is increased. In fact, at least some charge is lost until a summation radius of between 25 and 81 pixels is used. We can also see that as much as 12 percent more charge is read out in the reduced integration time case.

Even though the total signal increases as a larger summation radius is used, the signal to noise may decrease. Figure 11 compares the signal to noise ratio of APS1 pixels in response to the Fe-55 signal source (~ 1639 electrons liberated in Si). Both 2 ms and 32 ms integration times are plotted. One can see that the signal to noise decreases beyond a very small radius of about 2-4 pixels. Note that the theoretical signal to noise of $\sim 1639/13 \approx 126$ is not obtained due to the diffusion of electrons over several pixels.

As expected, decreasing the integration time also increases signal to noise ratio. Indeed, the peak SNR was improved by almost 50 percent when the integration time was reduced from 32 ms to 2 ms. In many applications, such as collider-physics experiments, the exposure time for one frame can be extremely short. For these applications, the total integration time can be limited by the readout rate, and efforts to increase readout speed will result in improved SNR.

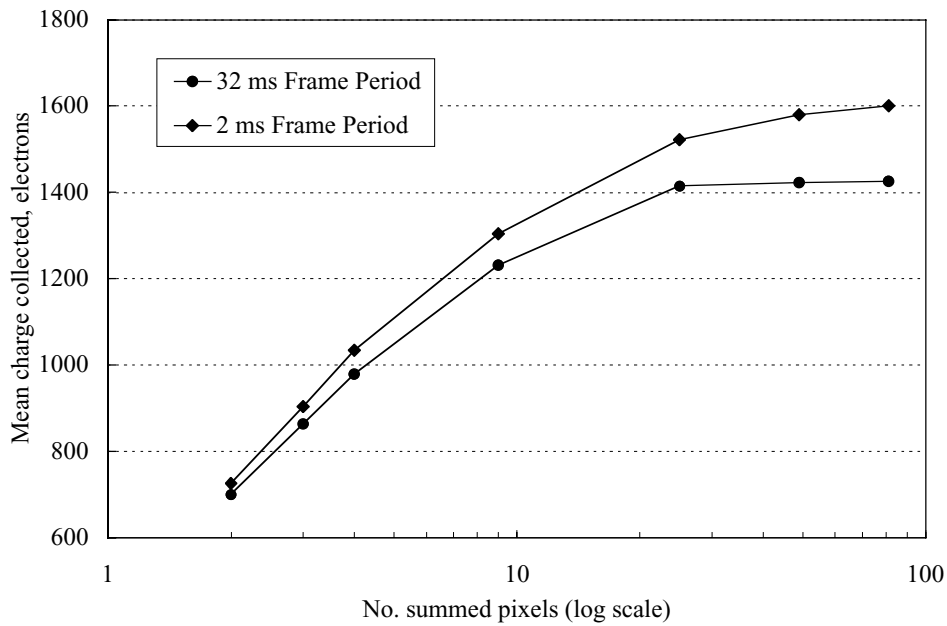


Figure 10: Total charge collected verses number of pixels summed and integration time.

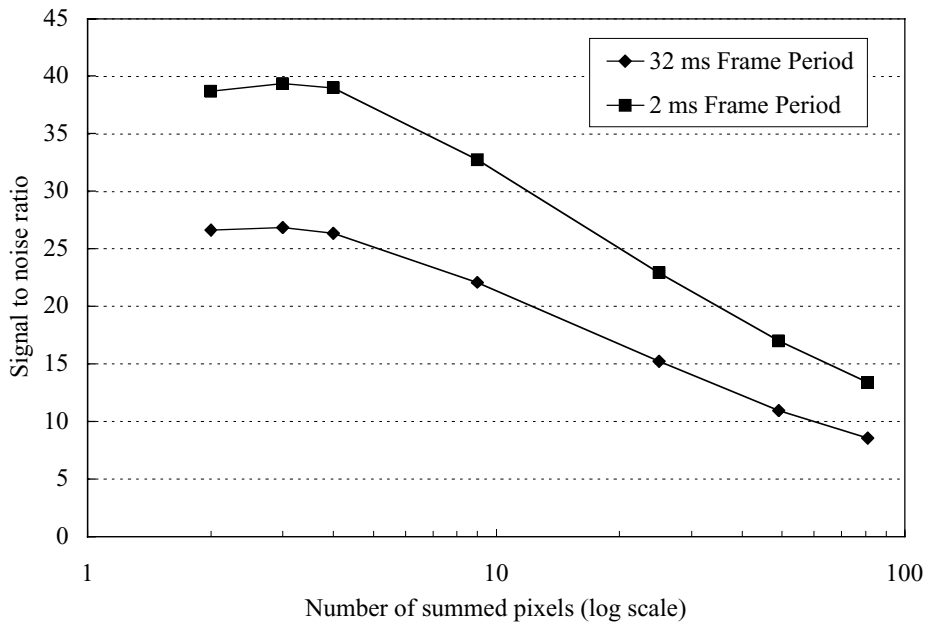


Figure 11: Signal to noise (RMS) verses number of pixels summed and integration time.

The radius of electron diffusion is also heavily dependent on the pixel collection diode size and topology. Increasing the size of the collection diode on each pixel increases the number of electrons collected, but reduces the conversion gain of the pixel due to concomitantly increased capacitance. A compromise strategy is to disperse small collection diodes about the pixel in an attempt to increase local collection with less reduction in the pixels conversion gain. A second iteration test chip was fabricated to permit more detailed tests of this and other strategies. Figure 12 depicts four pixels from this

test chip that use between 1 and 4 minimum-sized diodes that are physically dispersed about the pixel area. Figure 13 plots the relative charge collection of the four pixel variations verses number of summed pixels. One can see that for smaller summation cases, the percent of the total charge collected increases as the number of diodes per pixel increases. About 65 percent more charge is collected per pixel in the 4-diode case, and essentially all charge is collected with a summation radius including 4 pixels. Although more charge is collected per pixel in the multiple-diode cases, both the conversion gain and leakage is expected to be worse and so there are some disadvantageous tradeoffs involved. Indeed, Figure 14, which plots the SNR of the four pixel topologies as a function of summed pixels, confirms this. In general, the SNR becomes worse as the number of per-pixel diodes are increased. There may, however, be a small advantage to multiple diodes when no summation is performed (1 pixel sum), as three of those four data points tend to show. In this case, the increase in locally collected charge may slightly improve over-all performance. Other data from the same test chip, including data from pixels with single large area diodes and/or common-gate amplifiers, confirmed that the simplest, highest-gain, pixel topologies tend to provide superior performance in sparse-event applications. With more continuous illumination, similar to conditions of standard digital photography, the design trade-offs will likely also become similar to those of standard APS, and larger diodes may then provide a more clear advantage.

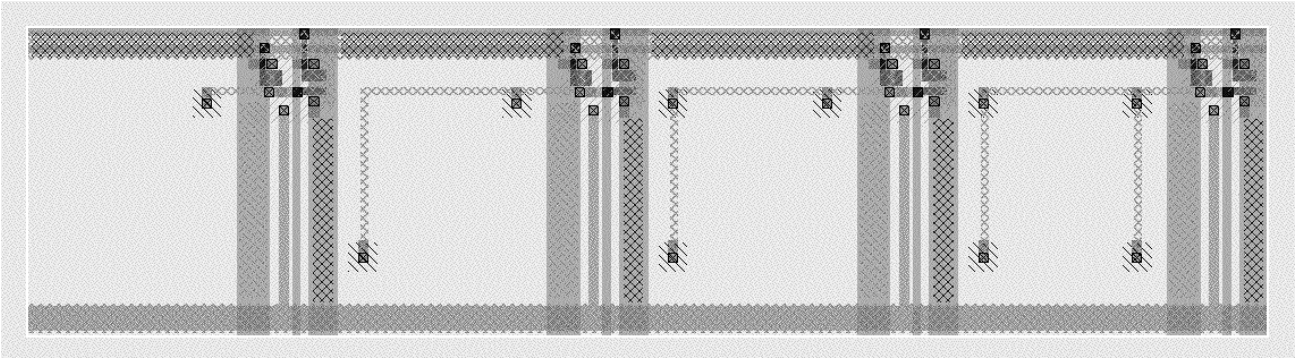


Figure 12: Four different pixels with one to four minimum-sized charge collection diodes.

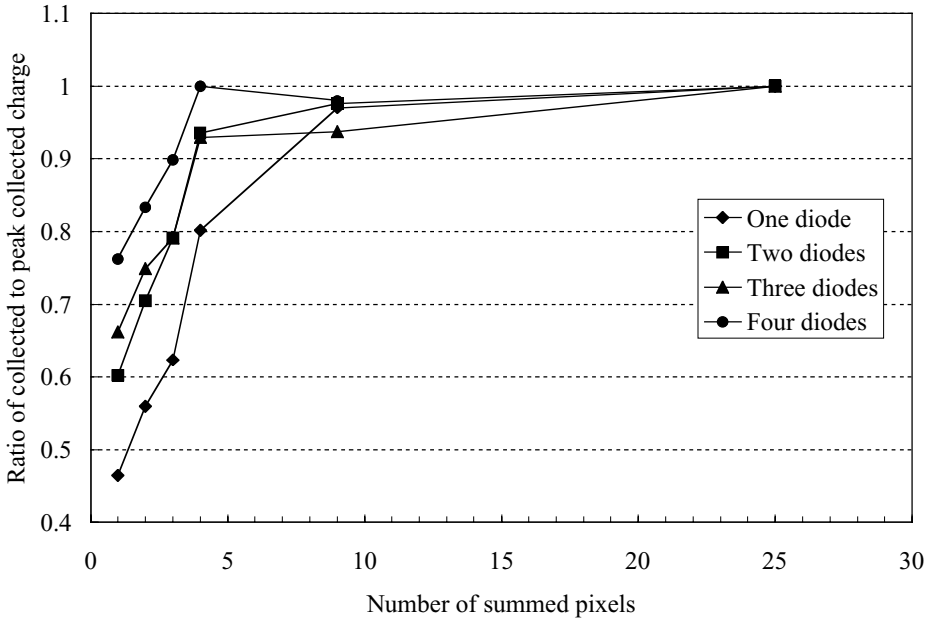


Figure 13: Comparison of diode topology verses collected charge.

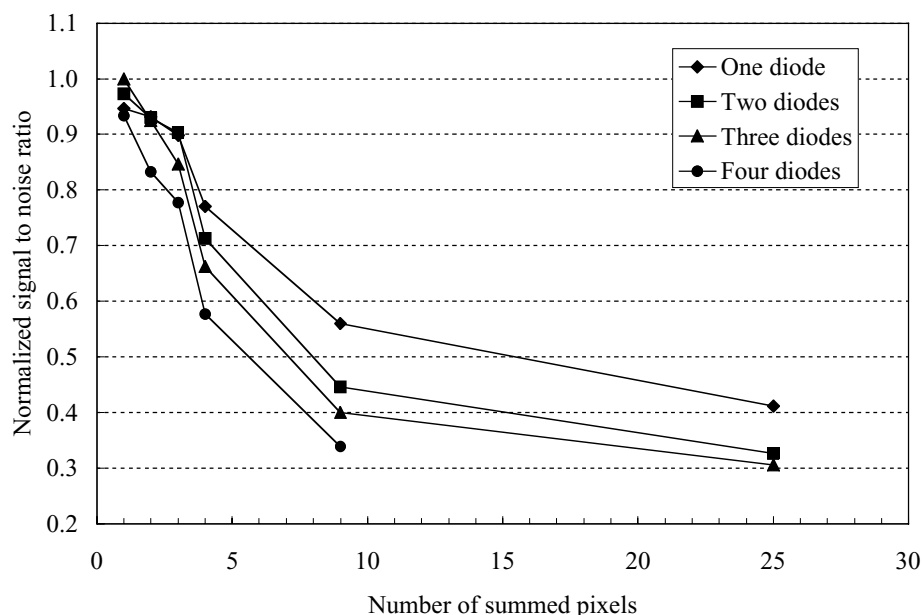


Figure 14: Comparison of pixel diode topology verses signal to noise ratio.

5. CONCLUSIONS

A CMOS active pixel sensor array using an epitaxial silicon sensor medium has been designed and successfully tested. The 128 by 128 pixel arrays, designed in a standard digital 0.25 micron process, use an 8-10 micron epitaxial silicon layer as a detection region. A variety of pixel topologies and circuits were included in order to empirically examine tradeoffs in technology and design choices, particularly those centered on maximizing the local collection of charge and minimizing lateral diffusion to neighboring pixels. In general, optimum performance in a sparse-event environment was obtained by the simplest and highest-gain pixel designs. The fabricated arrays were tested with 1.5 GeV electrons and Fe-55 X-ray sources, yielding a measured noise of 13 electrons RMS and an SNR for single Fe-55 X-rays (5.9 keV) of greater than 38. Due to the small signal levels (~400 electrons per pixel for Fe-55), leakage and other time-dependent sources of noise were found to significantly impact SNR. The use of short integration times (from 32 ms down to 2 ms) improved SNR by about 50 percent. The work demonstrated that standard digital CMOS can be used to make radiation sensors that can efficiently resolve individual gamma rays and minimum-ionizing charged particles.

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